SEGA MARK III

To VDP (315-5124) To
PSG (SN76489)

To SK-1100 (keyboard) To
FM-70 (FM sound source unit)

Return to HPD200 (paddle controller) MK III Reader,
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SEGA MARK III specs

CPU	D780C-1 (Z80A) 3.579MHz
VDP	315-5124
PSG	SN76489 (compatible and built into VDP)
ROM	Supplied by slot
RAM	8KB (expandable)
V-RAM	16KB

High-end model of SG-1000 / II
From general-purpose VDP to dedicated chip, hardware scrolling
Everything you need for a real-time game, such as a screen mask
Hardware scrolling is a pretty interesting feature while fixing a particular screen
An extended I / O port is available, but unfortunately it is not fully decoded and not very expandable.
Also, it is good that the sprite does not have a reversing function, but instead the function of the BG screen is high.
The more you look up, the more it seems to be a prototype of the master system (although it doesn't mean that you're in trouble)

CPU: µPD780-1

Uses NEC PD780-1
The clock divides 10.7386MHz by 3 and is about 3.579MHz.
Interruption is in mode 1 and NMI is triggered by pressing the PAUSE button.
INT is assigned to VDP (V-SYNC and H-SYNC).

VDP: 315-5124

315-5124 is made by Yamaha, and this chip is in charge of address decoding, PSG, etc.
Hardware scroll, screen mask, BG 64 color 32 palette, sprite 64 color 32 palette
The TMS-9918 used in the previous model is greatly expanded in screen mode.
It has almost the same function as TMS-9918, but the color development is slightly different.

Built-in PSG: 315-5124

Compatible with the SN76489 used in the SG-1000 series and built into the VDP chip
Clock is 3.579MHz

ROM

ROM is not built in the main body,
It will be supplied by cartridge or card
Because the mega ROM is controlled by the chip of the cartridge
The main unit alone does not have functions such as bank switching.
Bank switching methods are basically unified (excluding non-licensed software)

RAM

RAM has 8KB built in the main body,
You can disable the RAM built into the main unit from the cartridge (set B3 to 1).
It is newly designed so that S-RAM can be used as a substitute for the internal RAM.
Also, / EXT1 becomes / CS of 08000H.
The address is located from 0C000H to 0DFFFH.

In game gear, switching between SMS / GG mode
Switch with the jumper in the cartridge
At that time, the communication port and usage are switched and it cannot be used in SMS mode.
You will not be able to retain the data on the communication port.
Using that, in Game Gear's IPL
Determines SMS mode or GG mode

interrupt

MARK III has two interrupts in mode 1.
1: Generated from VDP / INT
2: Generated when the PAUSE button is pressed / NMI

/ INT is a combination of EI0 and EI1 of VDP R # 00 and R # 01
There are 4 types, V-SYNC and H-SYNC, both that do not generate interrupts.
Since it is / INT, it will fly to 00388H when it occurs.
Therefore, I judge whether it is V-SYNC or H-SYNC and jump to each interrupt routine.
To determine, you need to look at d7 in the VDP status register.
  If 1, V-SYNC (VBLANK) interrupt
  If 0, H-SYNC (H-LINE) interrupt

/ NMI flies to 00066H.

weight

MARK III is no weight in normal use
If you write the PSG port, it will take about 32 clocks of wait (unconfirmed).

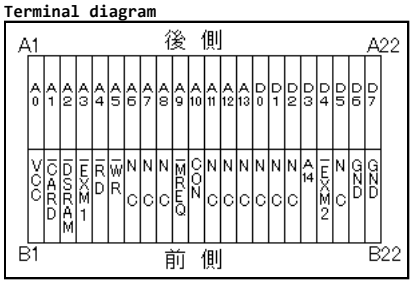
Difference from master system

MARK III switches between the cartridge, card, and main unit RAM using only the circuit.
The master system is to switch with the port at IC 315-5297.
Control ports 03EH and 03FH of 315-5297 have been added.
It also controls the JOY terminal, etc.
Along with that, ports 0DCH to 0DFH have also been slightly changed.

For 3D system control, MARK III has the B2 terminal open.
Make it possible to activate the card terminal of the 3D adapter
The master system is controlled by 315-5297

VDP takes a little time to start
In MARK III, wait (wait for 2 seconds) first and then access (initialize) VDP.
If you access VDP without weighting, nothing will be displayed on the screen.
After IPL is started and weight is applied to the master system
It is not necessary because external software will start

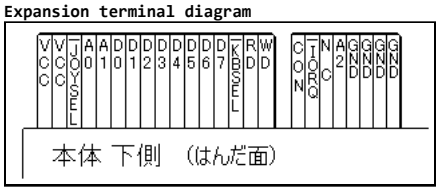
Terminal diagram



A0-A14: Address bus
D0 to D7: Data bus
/ CARD: Use of CARD slot 1 = not available, 0 = available
/ DSNA: Use of RAM in the main unit 1 = unusable, 0 = usable
/ EXM1: 08000H CS (negative ethics)
/ EXM2: 00000H CS (negative ethics)
CON: Directly connected to pin 18 of the expansion connector

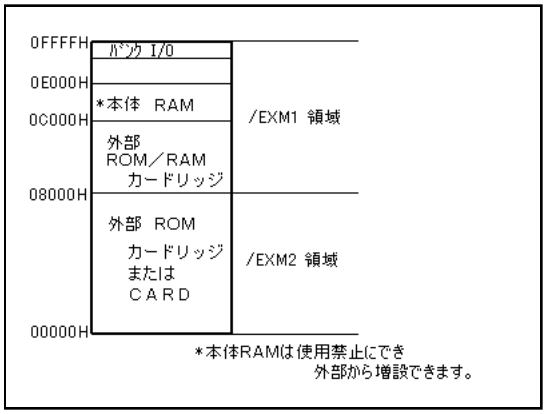
B2 (/ CARD) is for normal games
It is short-circuited with VCS and can use 3D glass. C. It has become
Therefore, while stabbing 3D glass compatible games and card games
There is a risk of bus competition
/ CARD is a terminal dedicated to MARK III (there are differences depending on the model)

Expansion terminal diagram



It is a connection terminal of FM sound source unit and keyboard SK-1100.
/ JOYSEL is linked with the joystick area
If / JOYSEL, / KBSEL, / RD are 0, the JOY terminal can be used.
B11 is connected to PB4 if it is SK-1100, and to B11 of the cassette terminal if it is the main body.
You can see the status at d4 of 0DDH of the port.

Memory map



The capacity of the ROM area varies depending on the card and cartridge.
RAM and ROM can be mounted on 08000H.
The RAM in the main body can be prohibited by setting the B3 terminal to 1 (the master system can be switched by software).
Memory can be placed in the master system with three slots (cartridge, card, expansion terminal).
Port 03EH is used for slot switching, but in MARK III, it becomes 0FFH even if you look into the port.
In the master system, the contents of port 03EH used for IPL startup, slot check, and switching are
Output to 0C000H and use (master system only)

Mega ROM has a memory mapper in the cartridge and there is no bank switching function in the main body
There are also some memory mappers, but the control method is almost the same for all cartridges.
It is a bank switching method and is controlled by memory-mapped I / O.
The address is used from 0FFFCH to 0FFFFH, and it switches every 16KB.

The 3D adapter is in the range of 0FFF8H to 0FFFBH.
The software uses 0FFFBH (other addresses are mirrors)
Since it is not fully decoded, 0DFFCH to 0DFFFH of the work RAM in the main body is
Cannot be used (it is a mirror of Mappa)

  0FFF8H to 0FFFBH: Used in 3D system Normally, only 0FFFBH is used (switch between left and right at d0?)
  0FFFCH: Mainly backup RAM switching
  0FFFDH: Select a bank for 00000H to 03FFFH of the main body
  0FFFEH: Select a bank for 04000H to 07FFFH of the main body
  0FFFFH: Select a bank for 08000H to 0BFFFH of the main body

I / O port

Port control is performed within the VDP
The address bus used is only connected to A15, A14, A7, A6, A0.
A15 and A14 are for / EXM1 and 2, and A7, A6 and A0 are for ports.
Therefore, the ports are separated by 040H.
Since there are / KBSEL and A0 to A2 in the expansion connector
Ports after port 0C0H can control the lower 4 bits from 0 to 7.
  000H-03FH: Control (unused)
  040H-07FH: PSG / VDP
  080H-0BFH: VDP
  0C0H to 0FFH: JOY terminal / expansion connector (FM-70, SK-1100)

03EH: Not used in MARK III
  In MARK III, use the cartridge and card together, and use the internal RAM and expansion RAM (0C000H or later).
  The circuit has decided to prohibit it, but after the master system, this port is used.
  Switch cartridges and RAM in the main unit, etc.
  Port 03EH and Port 03FH make a big difference between MARK III and Master System
  It can be said that the master system uses MARK III for hardware and port 03EH and port 03FH for software.
  Since it is unused in MARK III, the data is not retained, but the data changes every time it is read.
  Although it is used in the master system, it will be 0FFH when read because it is a write port.
  Therefore, port 03EH becomes the contents of work 0C000H by slot check at the start of the master system.
  When using an FM sound source, read this 0C000H and set it to port 03EH (JOY terminal prohibited).
  Will be accessed

03FH: Not used in MARK III
         The master system controls the memory and JOY terminal / FM unit.

07EH: Current V counter (input)
07FH: Current H counter (input) / PSG (output)

0BEH-0BFH: VDP

Ports 0C0H to 0C1H: JOY terminal (mirror)
  Since it is not decoded, it becomes a mirror of ports 0DCH to 0DDH (when nothing is connected to the expansion terminal).
  Ports 0C0H to 0C1H are used in the mysterious castle pit pot.
  However, if the FM unit is attached, the operation will be strange, so it is better not to use it.

0DCH: JOY terminal (input)
  d7: JOY2 pin 2 (DOWN) 1 = off, 0 = on
  d6: JOY2 1 pin (UP) 1 = off, 0 = on
  d5: JOY19 pin 9 (2 buttons) 1 = off, 0 = on
  d4: JOY1 6-pin (1 button) 1 = off, 0 = on
  d3: JOY1 4-pin (RIGHT) 1 = off, 0 = on
  d2: JOY1 pin 3 (LEFT) 1 = off, 0 = on
  d1: JOY1 pin 2 (DOWN) 1 = off, 0 = on

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  d0: JOY1 pin 1 (UP) 1 = off, 0 = on

0DDH: JOY terminal + CON terminal (input)
  d7: Fixed with pin 1 of IC9 74LS257 (unused)
  d6: Fixed with pin 1 of IC9 74LS257 (unused)
  d5: Fixed with 6-pin 1 of IC9 74LS257 (unused)
  d4: CON terminal 1 = off, 0 = on
  d3: JOY2 9-pin (2 buttons) 1 = off, 0 = on
  d2: JOY2 6-pin (1 button) 1 = off, 0 = on
  d1: JOY2 4-pin (RIGHT) 1 = off, 0 = on
  d0: JOY2 pin 3 (LEFT) 1 = off, 0 = on

  * You can judge Japanese hardware or overseas hardware by looking at port 0DDH.
    Output 0F5H to port 03FH to see port 0DDH
    It can be judged by outputting 055H to port 03FH and looking at port 0DDH.
      For MARK III
        Port 03FH is not used
        Port 0DDH d7-6 is fixed at 11

      In the case of Japanese master system
        Since the content of d3-1 of port 03FH is 0
        Port 0DDH d7-6 is 00 both times

      For overseas master system
        Since the value of the 7-pin setting of the JOY terminal is entered
        Port 0DDH d7-6 is 11 and 00

      11 to 11 is MARK III
      From 00 to 00, the Japanese master system
      If it changes from 11 to 00, it will be an overseas master system.

0DCH to 0DFH: SK-1100 (optional keyboard)
  8255 is used, and 0DCH to 0DFH is the range of use.
  Since the I / O port is not full-day coded, it overlaps with the JOY terminal.
  Therefore, when accessing SK-1100 normally
  The JOY terminal inside the main body is prohibited.
  When key select number 07 is selected
  The keyboard will be prohibited and the JOY terminal will be used.

  Since MARK III alone does not retain (latch) port data.
  First, write 092H to port 0DFH (8255CW) and set the input / output.
  Write 000H to 0DEH (8255PC) and read port 0DEH
    For 0FFH, only MARK III,
    If it is 000H, it will be MARK III + SK-1100.

  If it is only the main body, the data will not be retained, so even if you write 000H, it will be 0FFH.
  In the SK-1100 connection, it is judged by using the fact that 000H is written normally by 8255.

0F0H to 0F2H: FM-70 (using the optional FM sound source unit YM2143)
  It overlaps with the JOY terminal and SK-1100 (cannot be shared with SK-1100).
  Ports 0F0H and 0F1H overlap with the JOY terminal.
  The JOY terminal is an input only, and the FM unit is a basic output.
  Since 0F2H is the input, it overlaps with 0DCH, but the JOY terminal is prohibited in the FM unit circuit.
  In the Japanese master system, d2 of port 03EH is set to 1 and the JOY terminal is prohibited.
  Check the connection (two types of connection check are required)
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Model judgment

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The judgment method between MARK III and the previous model (so-called all models) is judged by using the difference in the mirror of the memory.
  SG-1000 1KB model 0C000H-0C3FFH (hereinafter mirror)
  SC-3000 etc. 2KB model 0C000H-0C7FFH (hereinafter mirror)
  MARK III etc. 8KB model 0C000H-0DFFFH (hereinafter mirror)

Write 000H to both 0C000H and 0D000H.
Write data (for example, 055H) to 0C000H and read the data of 0D000H.
All models are mirrors for multi-vision, so 0C000H and 0D000H have the same value.
The data will be different if it is MARK III or later.
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Memory mapper 315-5208

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It is the oldest memory mapper, but this mapper is the standard
The board TYPE-N used for the ROM with built-in mapper has the same access.
The port used is a memory-mapped I / O.
The range is 0FFFDH to 0FFFFH and the bank is from 0 to 7 (maximum 1MBit).
Please note that the built-in RAM of the main unit is 0C000H to 0DFFFH.
0E000H-0FFFFH is a mirror
Therefore, if the stack pointer is specified as 0DFFFH, the stack data will be displayed from 0DFFFH.
At the same time as entering, data is also entered in the 0FFFFH mapper, causing a malfunction.
Therefore, it is necessary to specify the stack pointer around 0DFF0H to prevent malfunction.
Furthermore, in the master system, the light of 07FF0H-07FFFH is also prohibited.

  0FFFDH: Bank designation of area 0 (0000H to 03FFFH)
    d7: 0
    d6: 0
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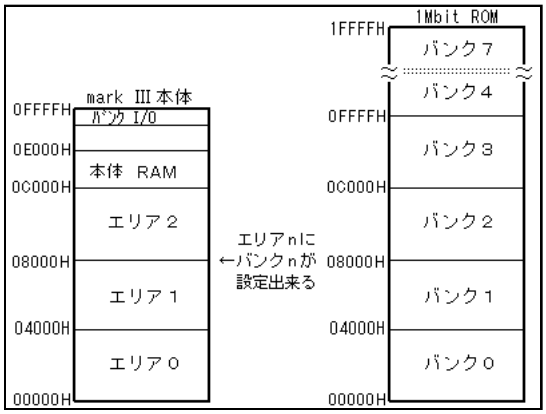
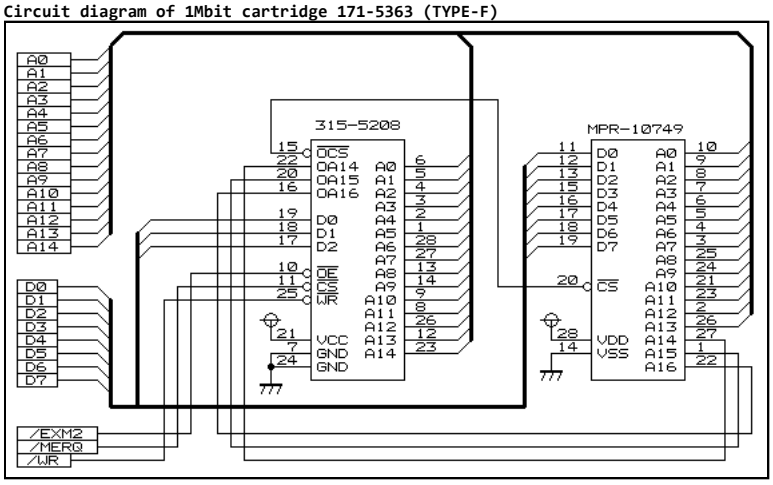
d5: 0
d4: 0
d3: 0
d2: Bank D2
d1: Bank D1
d0: Bank D0

0FFFEH: Bank designation of area 1 (04000H to 07FFFH)
d7: 0
d6: 0
d5: 0
d4: 0
d3: 0
d2: Bank D2
d1: Bank D1
d0: Bank D0

0FFFFH: Bank designation of area 2 (08000H to 0BFFFH)
d7: 0
d6: 0
d5: 0
d4: 0
d3: 0
d2: Bank D2
d1: Bank D1
d0: Bank D0



Circuit diagram of 1Mbit cartridge 171-5363 (TYPE-F)



Memory mapper 315-5235

It is a mapper with an expanded backup RAM and an expanded number of banks by expanding 315-5208.
The output port adopts memory-mapped I / O
The range of use is 0FFFCH to 0FFFFH, and the bank is from 0 to 31 (maximum 4MBit?).
You can also control the backup RAM
Pay attention to the specification of the stack pointer as in the old mapper (315-5208).

0FFFCH: Memory control
d7: Write protect (for development) 1 = read / write, 0 = read only
d6: 0
d5: 0
d4: Selection of area 4 (0C000H to 0DFFFH) 1 = external RAMnn, 0 = main unit RAM
d3: Selection of area 2 (08000H to 0BFFFH) 1 = external RAMnn, 0 = ROM
d2: Bank of external RAM 1 = external RAM02, 0 = external RAM01
d1: Bank shift (usually 0)
d0: Bank shift (usually 0)

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    * Bank shift is the bank No. that divides the total capacity of the mega ROM itself by 16K. The specification of is shifted.
      Bank shift 00 000H, 001H, 002H. .. ..
      Bank shift 01 018H, 019H, 01AH. .. ..
      Bank shift 10 010H, 011H, 012H. .. ..
      Bank shift 11 008H, 009H, 00AH. .. ..
        Bank No. If it shifts from 000H to 01FH due to bank shift, it will be 000H after 1FH.

    External RAM (backup RAM) can be installed up to 32KB
    Is it possible to switch this to two banks? (unconfirmed)

0FFFDH: Bank designation of area 0 (0000H to 03FFFH)
  d7: 0
  d6: 0
  d5: 0
  d4: Bank D4
  d3: Bank D3
  d2: Bank D2
  d1: Bank D1
  d0: Bank D0
(Note) Area 0 00000H to 03FFFH is fixed to bank # 00:00H to 03FFFH.
     No matter which bank you specify, 00000H to 03FFFH will not change.
     It is unknown when the bank shift is other than 00.

0FFFEH: Bank designation of area 1 (04000H to 07FFFH)
  d7: 0
  d6: 0
  d5: 0
  d4: Bank D4
  d3: Bank D3
  d2: Bank D2
  d1: Bank D1
  d0: Bank D0

0FFFFH: Bank designation of area 2 (08000H to 0BFFFH)
  d7: 0
  d6: 0
  d5: 0
  d4: Bank D4
  d3: Bank D3
  d2: Bank D2
  d1: Bank D1
  d0: Bank D0
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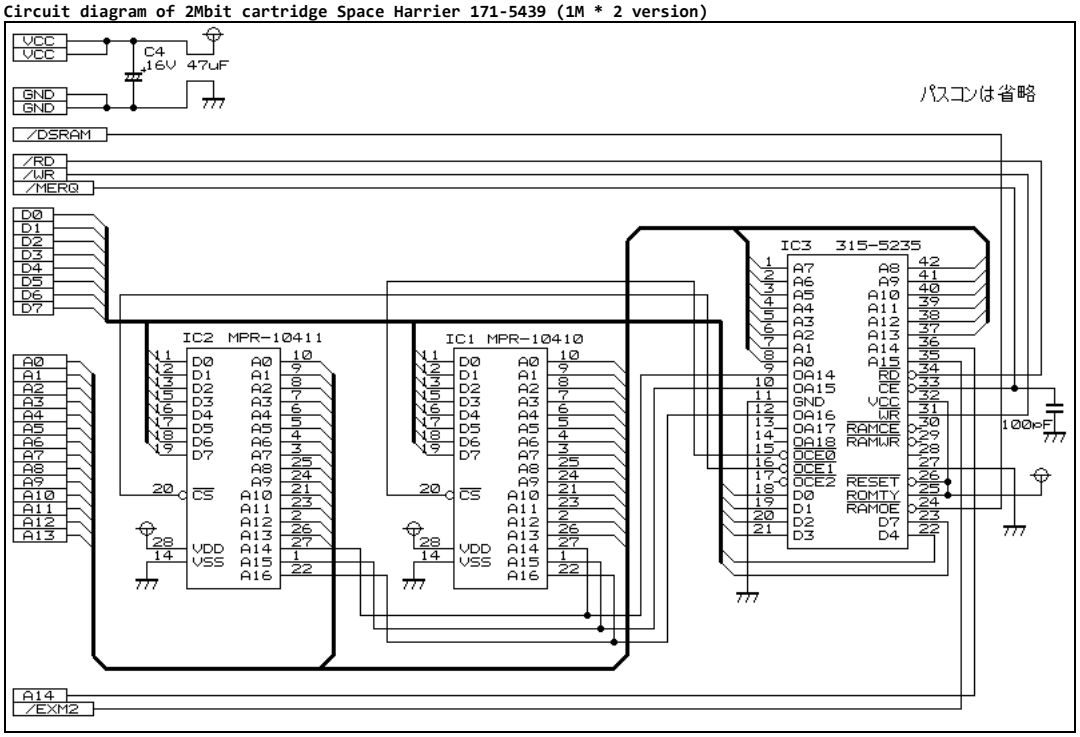
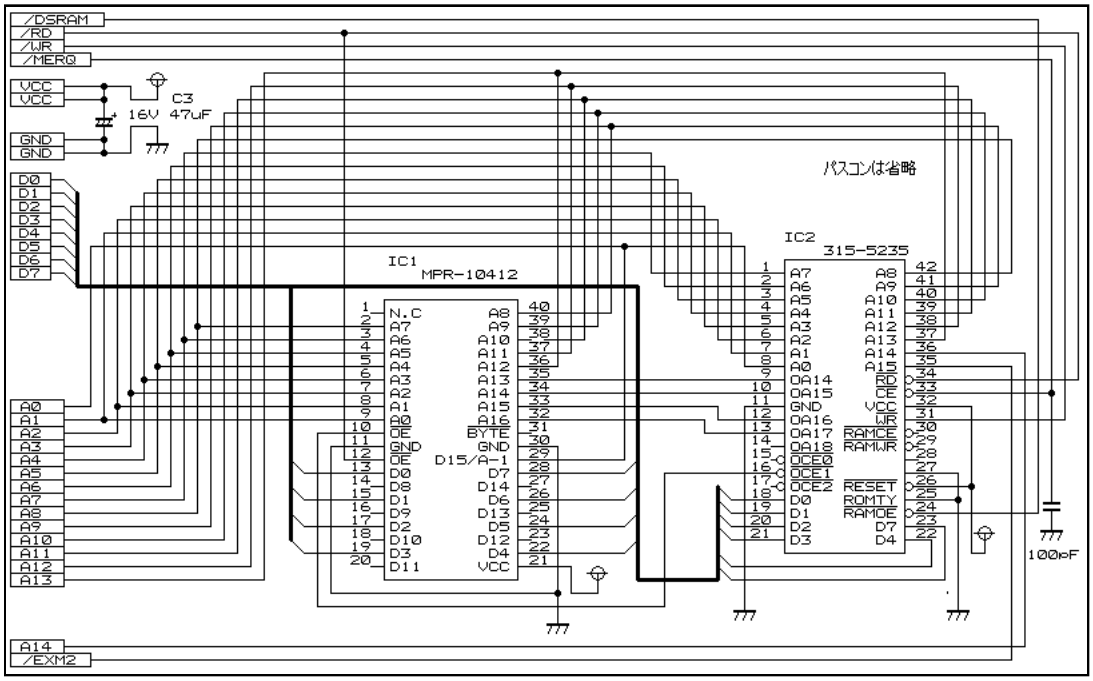
Circuit diagram of 2Mbit cartridge Space Harrier 171-5439 (1M * 2 version)



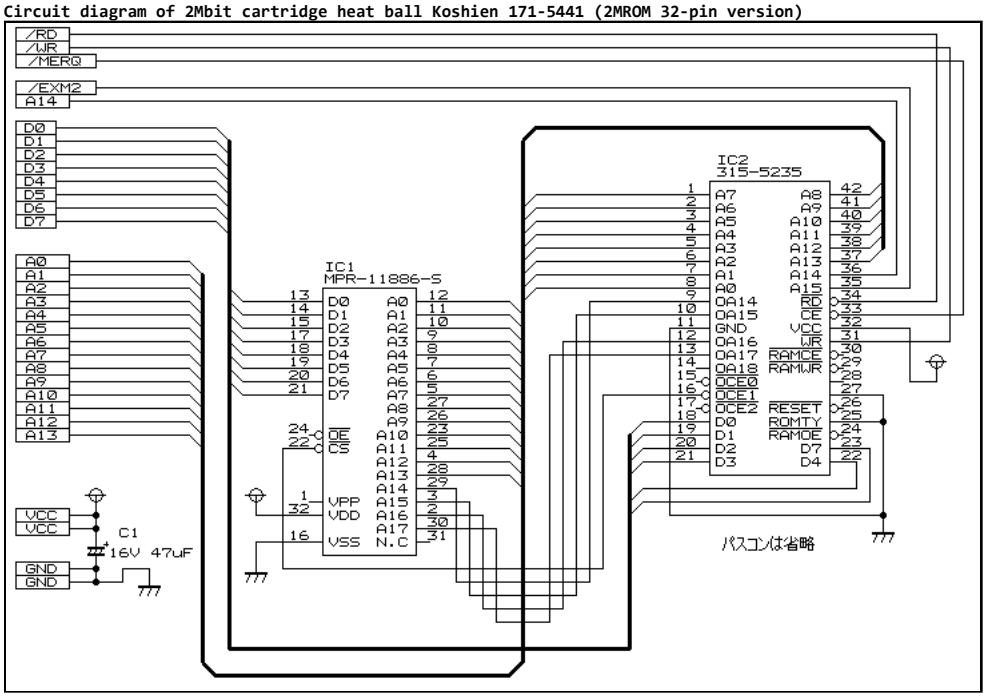
Used in Space Harriers and Outrun.
In addition, it is now possible to support large-capacity ROMs, and the access of the mapper has been expanded a little.
However, the basic access method is the same, due to the convenience of checking the ROM of the overseas master system.
It seems that it can not be checked unless it is the same method.

Circuit diagram of 2Mbit cartridge Space Harrier 171-5440 (2M * 1 version)



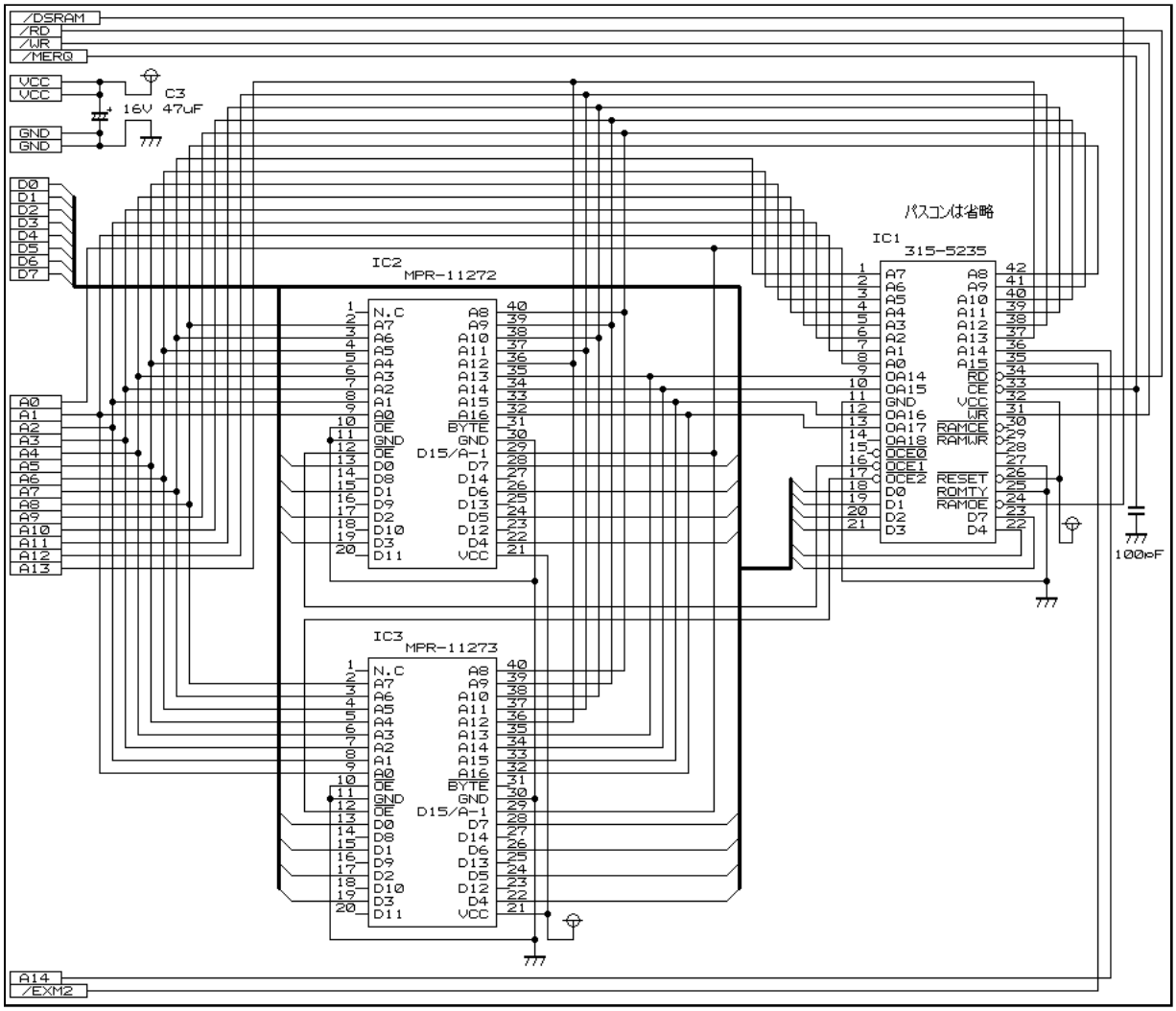
It is also a 2M BitROM * 1 version of Space Harrier. (Late version?)
It seems that they are using the same memory mapper, but the wiring is slightly different.
The difference here is the input of pin 25 of 315-5325 of the mapper and the output of / CE0 and / CE1.
The remaining blank space is probably used for bank switching / CE and selection of its output type.
ROM name MPR-1041 refers to Space Haria, and the remaining 1 digit is the type of ROM?
Since the data buses connected to the mapper are d7 and d4 to 0, d7 enables RAM.
It seems that d4 to 0 will be the bank nn (000H to 01FH).
Also, the memory that can be installed is 1MBit, 2MBit, 4MBit, and the maximum memory seems to be 4MBit.

Circuit diagram of 2Mbit cartridge heat ball Koshien 171-5441 (2MROM 32-pin version)



It uses a 32-pin mask ROM.

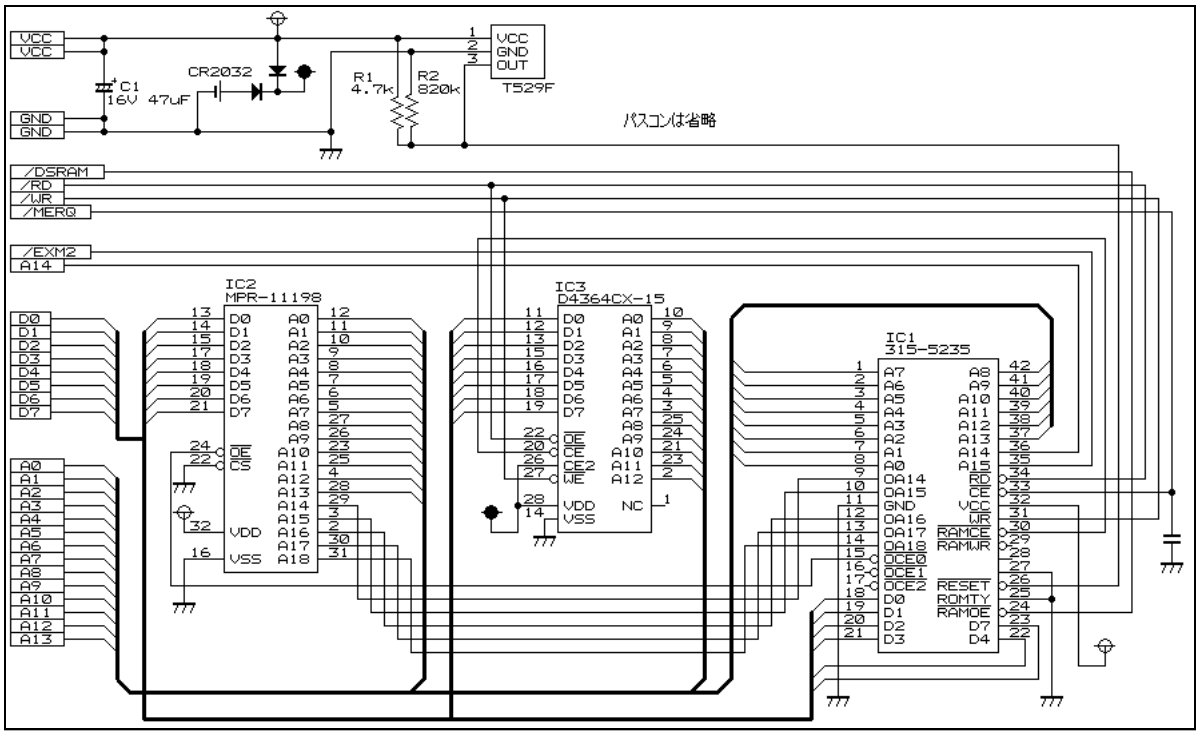
Circuit diagram of 4Mbit cartridge afterburner 171-5589D (2M * 2)



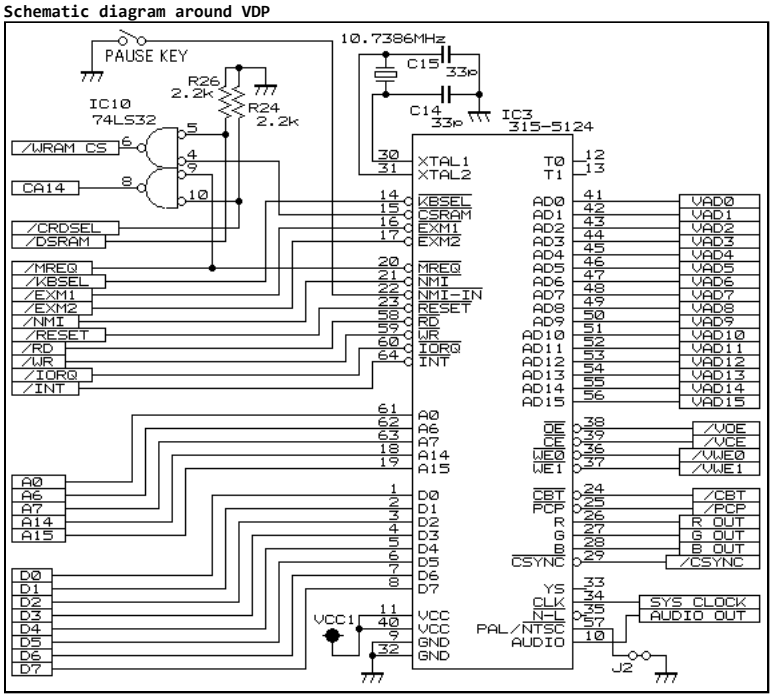
Circuit diagram of 4Mbit cartridge Phantasy Star 171-5583 (4M + 64KBitS-RAM)

Types of boards in the cartridge

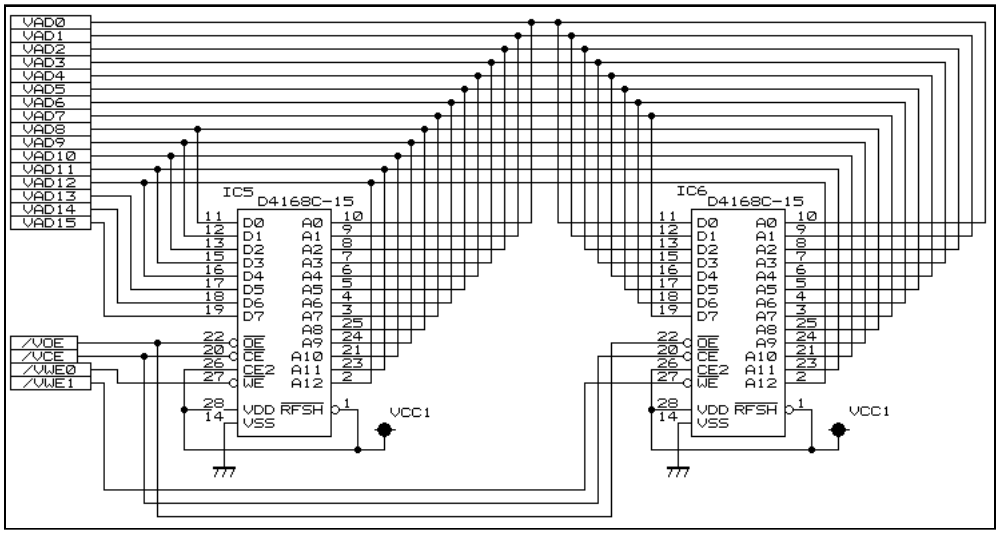
171-5362: 1MBit ROM with built-in TYPE-N mapper
171-5363-01: TYPE-F 315-5208 + 1MBit ROM
171-5439: 315-5235 + 1MBit ROM * 2
171-5440: 315-5235 + 2MBit ROM
171-5500: 315-5235 + 1MBit ROM + 64KSRAM + MB3771
171-5506: 2MBit ROM with built-in mapper
171-5518: 1MBit ROM with built-in mapper
171-5177: A board for SG-1000 made similar to TYPE-N using jumper wires.
171-5564: 2MBit ROM with built-in mapper
171-5589D: 315-5235 + 2MBit ROM * 2
171-5583: 315-5235 + 4MBit ROM + 64KSRAM + T529F



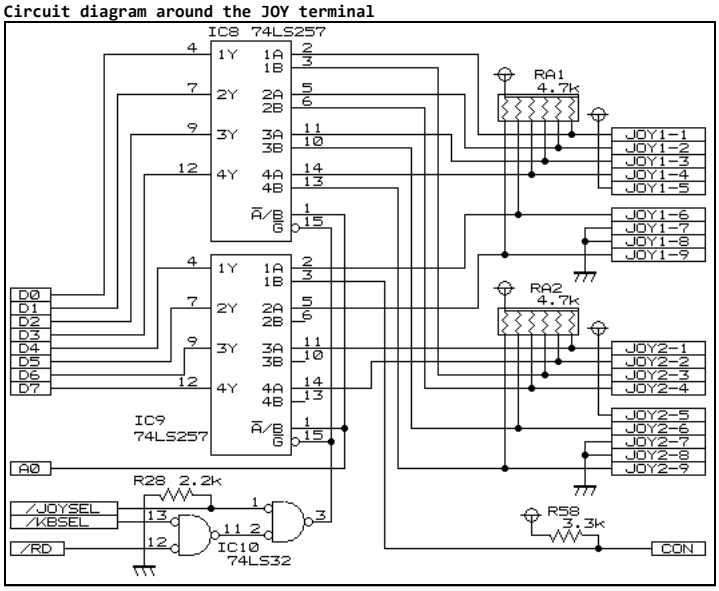
Schematic diagram around VDP



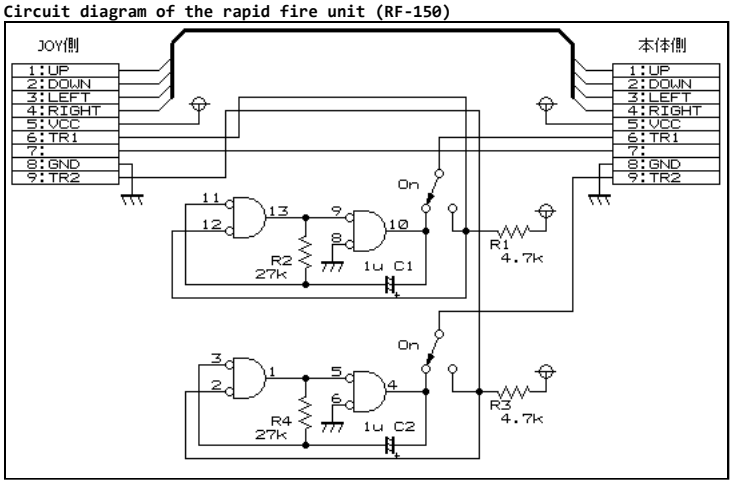
Circuit diagram around V-RAM



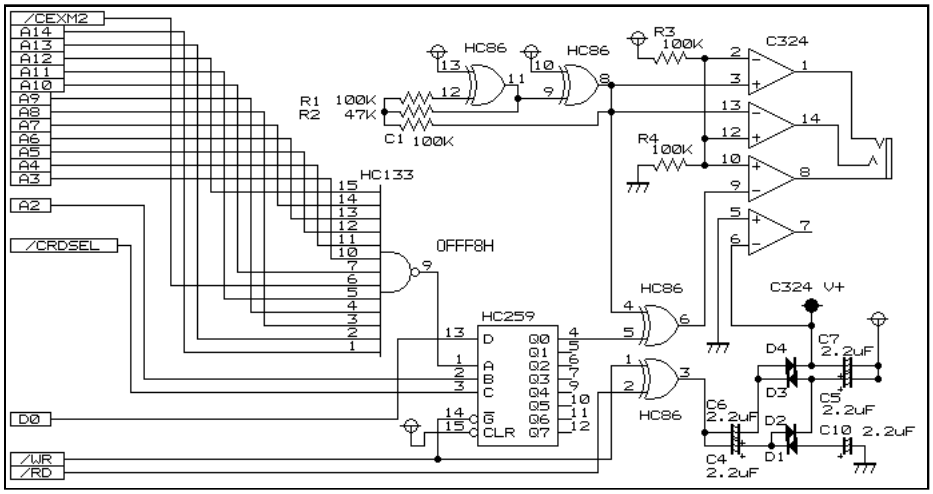
Circuit diagram around the JOY terminal



Circuit diagram of the rapid fire unit (RF-150)



Circuit diagram of 3D adapter



Sample download
All programs are free and the source can be created with "The Macroassembler AS".
And it is just for reference.

- Main circuit diagram of sports pad for great ice hockey
- BG TEST program (can be operated by MARKIII, master system, emulator)
- I / O port Peping program (can be operated by MARKIII, master system, emulator)
- VDP R # 03 test program (can be operated by MARKIII, master system, emulator) MARKIII, can be operated on the master system, cannot be operated on the e

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