

fifo_pipe.v

AUTHORS

JAY CONVERTINO

DATES

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INFORMATION

Brief

Pipe fifo signals to help with timing issues, if they arise.

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fifo_pipe

```
module fifo_pipe #(
    parameter RD_SYNC_DEPTH = 0,
    parameter WR_SYNC_DEPTH = 0,
    parameter DC_SYNC_DEPTH = 0,
    parameter
```

```

BYTE_WIDTH
=
1,
parameter
DATA_ZERO
=
0,
parameter
COUNT_WIDTH
=
1
)
(
input
rd_clk,
input
rd_rstn,
input
rd_en,
input
rd_valid,
input
[(BYTE_WIDTH*8)-1:0]
rd_data,
input
rd_empty,
output
r_rd_en,
output
r_rd_valid,
output
[(BYTE_WIDTH*8)-1:0]
r_rd_data,
output
r_rd_empty,
input
wr_clk,
input
wr_rstn,
input
wr_en,
input
wr_ack,
input
[(BYTE_WIDTH*8)-1:0]
wr_data,
input
wr_full,
output
r_wr_en,
output
r_wr_ack,
output
[(BYTE_WIDTH*8)-1:0]
r_wr_data,
output
r_wr_full,
input
data_count_clk,
input
data_count_rstn,
input
[COUNT_WIDTH:0]
data_count,
output
[COUNT_WIDTH:0]

```

```

    r_data_count
)

```

Pipe fifo signals to help with timing issues, if they arise.

Parameters

BYTE_WIDTH <small>parameter</small>	How many bytes wide the data in/out will be.
COUNT_WIDTH <small>parameter</small>	Data count output width in bits. Should be the same power of two as fifo depth(256 for fifo depth... this should be 8).
RD_SYNC_DEPTH <small>parameter</small>	Add in pipelining to read path. Defaults to 0.
WR_SYNC_DEPTH <small>parameter</small>	Add in pipelining to write path. Defaults to 0.
DC_SYNC_DEPTH <small>parameter</small>	Add in pipelining to data count path. Defaults to 0.
DATA_ZERO <small>parameter</small>	Zero out data output when enabled.

Ports

rd_clk <small>input</small>	Clock for read data
rd_rstn <small>input</small>	Negative edge reset for read.
rd_en <small>input</small>	Active high enable input of read interface.
rd_valid <small>input</small>	Active high output input that the data is valid.
rd_data <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Output data input
rd_empty <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Registered Active high output when read is empty.
r_rd_en <small>output [(BYTE_WIDTH* 8)- 1:0]</small>	Registered Active high enable of read interface.
r_rd_valid <small>output [(BYTE_WIDTH* 8)- 1:0]</small>	Registered Active high output that the data is valid.
r_rd_data <small>output [(BYTE_WIDTH* 8)- 1:0]</small>	Registered Output data
r_rd_empty <small>output [(BYTE_WIDTH* 8)- 1:0]</small>	Active high output when read is empty.
wr_clk <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Clock for write data
wr_rstn <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Negative edge reset for write
wr_en <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Active high enable of write interface, feed into register.
wr_ack <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Active high when enabled, that data write has been done, feed into register.
wr_data <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Input data, feed into register.
wr_full <small>input [(BYTE_WIDTH* 8)- 1:0]</small>	Active high output that the FIFO is full, feed into register.
r_wr_en	Register Active high enable of write interface.

```
output [(BYTE_WIDTH* 8)- 1:0]  
r_wr_ack  
output [(BYTE_WIDTH* 8)- 1:0]  
r_wr_data  
output [(BYTE_WIDTH* 8)- 1:0]  
r_wr_full  
output [(BYTE_WIDTH* 8)- 1:0]  
data_count_clk  
input [(BYTE_WIDTH* 8)- 1:0]  
data_count_rstn  
input [(BYTE_WIDTH* 8)- 1:0]  
data_count  
input [COUNT_WIDTH:@]
```

Register Active high when enabled, that data write has been done.

Register Input data

Register Active high output that the FIFO is full.

Clock for data count

Negative edge reset for data count.

Output that indicates the amount of data in the FIFO.