Sunday ,Oct 3rd, 2021

meet with the team [20min]

we talked briefly over the overall concept of the project

and decided we will commit to the mem to mem processor. We decided to learn more about the concept and meet tomorrow.

Monday, Oct 4th, 2021

meet with the team[1hr]

we worked the design documents. we wrote draft version of relPrime.

And make the memory allocation, assembly language fragment, and

My job was wrting a j-type instruction (but it as dele

ted)and writing part of the machine language translation for relPrime.

my job for the milestone 2 is to write RTL for i-type instruction.

Thurs, Oct 7th, 2021

meeting with the team[20min]

We talked about the RTL and how we are going to write it. And we divided our work.

My work for M2 is to come up with the components we will use in the datapath.

Sunday, Oct 10t, 2021

working alone[50min]

I did the part that is assigned to me, which is writing components needed.

Mon, Oct 11th, 2021

meeting with the team[20min]

We brefly overview the work we did over the weekend. And we reviewed each other’s work.

I re-wrote the teammate's description on component to make it clearer.

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M3

I worked on the integration plan and worked on the control signal.

M4

Oct 20, 2021

Meeting with the team[10min]

We breifly talked about what we should fix in our design of the datapath. We decided to make the control unit a demux, since it takes 1 input and multiple output.

Oct 25, 2021

Meeting with the team in class worktime[50min]

I worked on the contol unit and continue making a muxes and ALU operator verilog and their testbench.

M5

Meeting with the team [20 min]

Oct 30,2021 Saturday

We talked about our component and we ask each other a question about what they did and how is the progress on the work.

Working alone in class/ outside of the class [3hr]

Nov 2, 2021 Tuesday

I worked on the control unit. I used the if statement for the input opcode. For instance if 1 < opcode < 3, output control signal src = 2 and if 4 < opcode < 6, output different control signal. And I also wrote a test bench for the mux.

Working alone in class [2hr]

Nov 3, 2021 Wednesday

I realized that I need to include the fech/decode/execute…. Cycle on the control unit. If I continude with the simple if statement, it only suits for single cycle. Since we are doing multi-cycle, I changed more.

Nov 4, 2021 Thurs [3hr]

I added steps in the control unit so it can produce different output in each stage. But it needs to be worked on the opcode, because for instance, for m-type instruction, it needs different op inputs to perform the task but everything else is the same. So I left it 0000 first. It needs to be fixed.

Nov 6, 20201 [2hr]

I did the additional feature part of the project, which is writing the Mips form of relprime and gcd to phython and see if each components and instructions are outputting the correct data

Nov 10 2021 [2hr] in class

I updated the design document by editing the data path and fixing some error we made previously