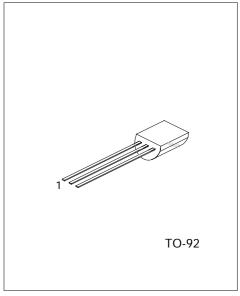


XL/ML1225 **SCR**

MEDIUM POWER LOW **VOLTAGE TRANSISTOR**

DESCRIPTION

The XL1225/ML1225 silicon controlled rectifiers are high performance planner diffused PNPN devices. These parts are intended for low cost high volume applications.



*Pb-free plating product number: XL1225L/ML1225L

PIN CONFIGURATION

PIN NO.	PIN NAME
1	CATHODE
2	GATE
3	ANODE

ORDERING INFORMATION

Order Number		Package	Packing	
Normal	Lead free	Fackage	racking	
XL1225-T92-B	XL1225L-T92-B	TO-92	Tape Box	
XL1225-T92-K	XL1225L-T92-K	TO-92	Bulk	
ML1225-T92-B	ML1225L-T92-B	TO-92	Tape Box	
ML1225-T92-K	ML1225L-T92-K	TO-92	Bulk	

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XL/ML1225 scr

■ ABSOLUATE MAXIUM RATINGS (Ta= 25 , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITION	RATINGS	UNIT
Repetitive Peak	XL1225	V_{DRM}	T _J =40 ~ 125°C	400	\/
Off-State Voltage	ML1225	V DRM	$R_{GK} = 1k\Omega$	300	V
On-State Current		I _{T(RMS)}	Tc=40°C	0.8	Α
Average On-State Current		I _{T(AV)}	Half Cycle=180,Tc=40°C 0.5		Α
Peak Reverse Gate Voltage		V_{GRM}	IGR=10uA	1	V
Peak Gate Current		I_{GM}	10us Max.	0.1	Α
Gate Dissipation		$P_{G(AV)}$	20ms Max.	150	mW
Operating Temperature		TJ		+125	°C
Storage Temperature		T _{STG}		-40 ~ +150	°C

- Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 - 2. The device is guaranteed to meet performance specification within 0 \sim 70 operating temperature range and assured by design from -20 \sim 85 .

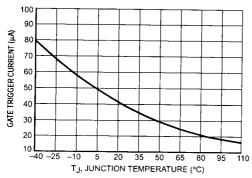
■ ELECTRICAL CHARACTERISTICS (Ta= 25 , unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Off State Leakage Current	I _{DRM}	@V _{DRM} (R _{GK} =1KΩ), T _J =125°C			0.1	mA	
Off State Leakage Current	I _{DRM}	$@V_{DRM}(R_{GK}=1K\Omega), T_J=25^{\circ}C$			1.0	μΑ	
On State Voltage	V _T	AT I _T =0.4A			1.4	V	
On State voltage	۷T	AT I _T =0.8A			2.2		
On State Threshold Voltage	$V_{T(TO)}$	T _J =125°C			0.95	V	
On State Slops Resistance	Rt	T _J =125°C			600	m	
Gate Trigger Current	I _{GT}	V _D =7V			200	μΑ	
Gate Trigger Voltage	V_{GT}	V _D =7V			8.0	V	
Holding Current	I _H	$R_{GK}=1K\Omega$			5	mA	
Latching Current	IL	$R_{GK}=1K\Omega$			6	mA	
Critical Rate of Voltage Rise	DV/DT	$V_D = 0.67^*V_{DRM}(R_{GK} = 1K\Omega), T_J = 125$				V/μs	
Critical Rate of Current Rise	DV/DT	$I_G=10\text{mA}, dI_G/dt=0.1A/\mu s, T_J=125$				A/μs	
Gate Controlled Delay Time	T_{GD}	l _G =10mA, dl _G /dt=0.1A/μs			2.2	μS	
Commutated Turn-off Time	TG	$T_J = 85^{\circ}C, V_D = 0.67^*V_{DRM}$ $V_R = 35V, I_T = I_{T(AV)}$			200	μS	

CLASSIFICATION OF I_{GT}

RANK	В	С	AA	AB	AC	AD
RANGE	50-100uA	100-200µA	8-15uA	15-20µA	20-25uA	25-50uA

TYPICAL CHARACTERICS



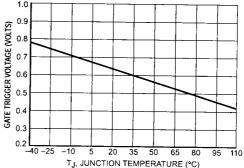


Figure 1. Typical Gate Trigger Current versus Junction Temperature

Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

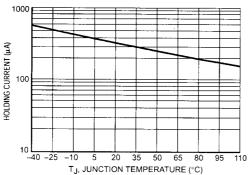


Figure 3. Typical Holding Current versus Junction Temperature

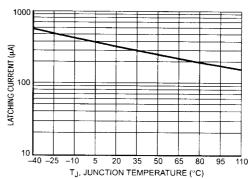


Figure 4. Typical Latching Current versus Junction Temperature

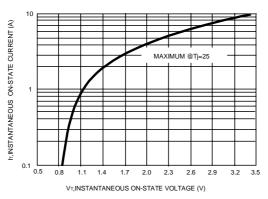


Figure 5. Typical On-State Characteristics

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