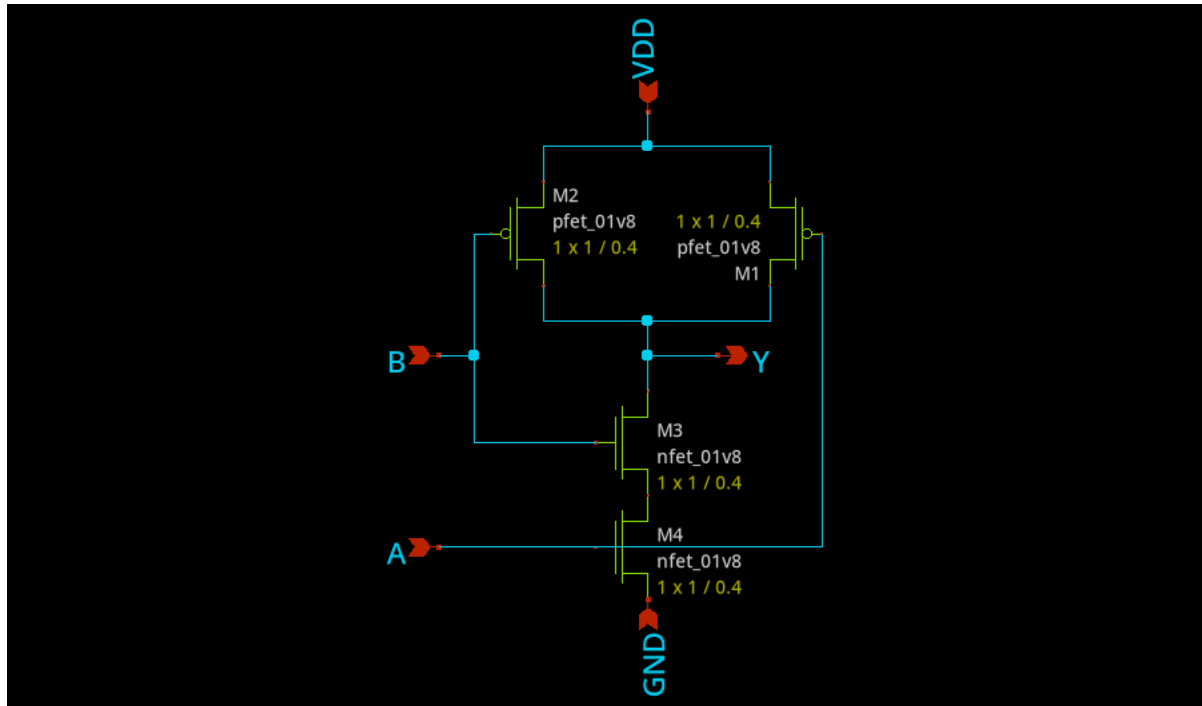# ENGR3426 MAD-VLSI: Miniproject 1
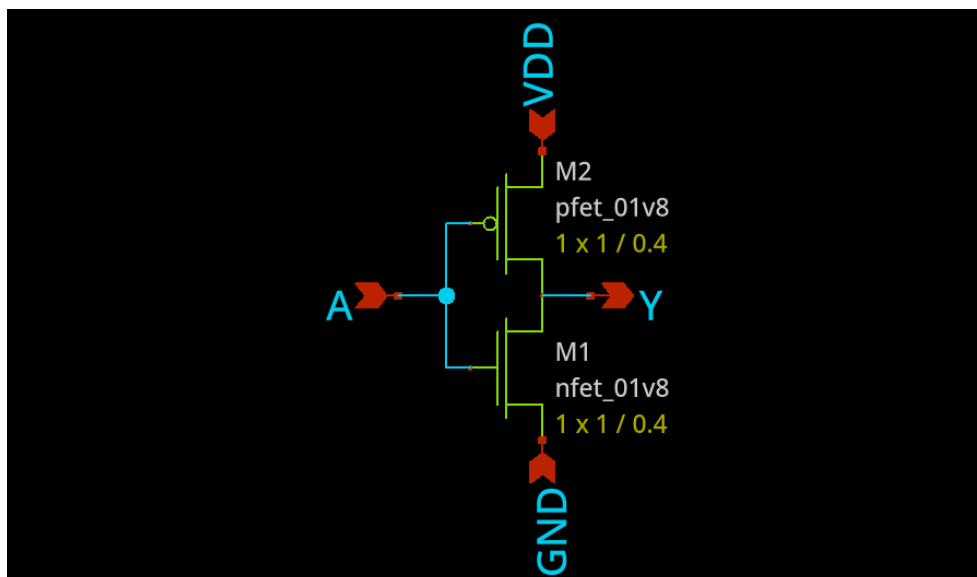
Sparsh Gupta

Xschem
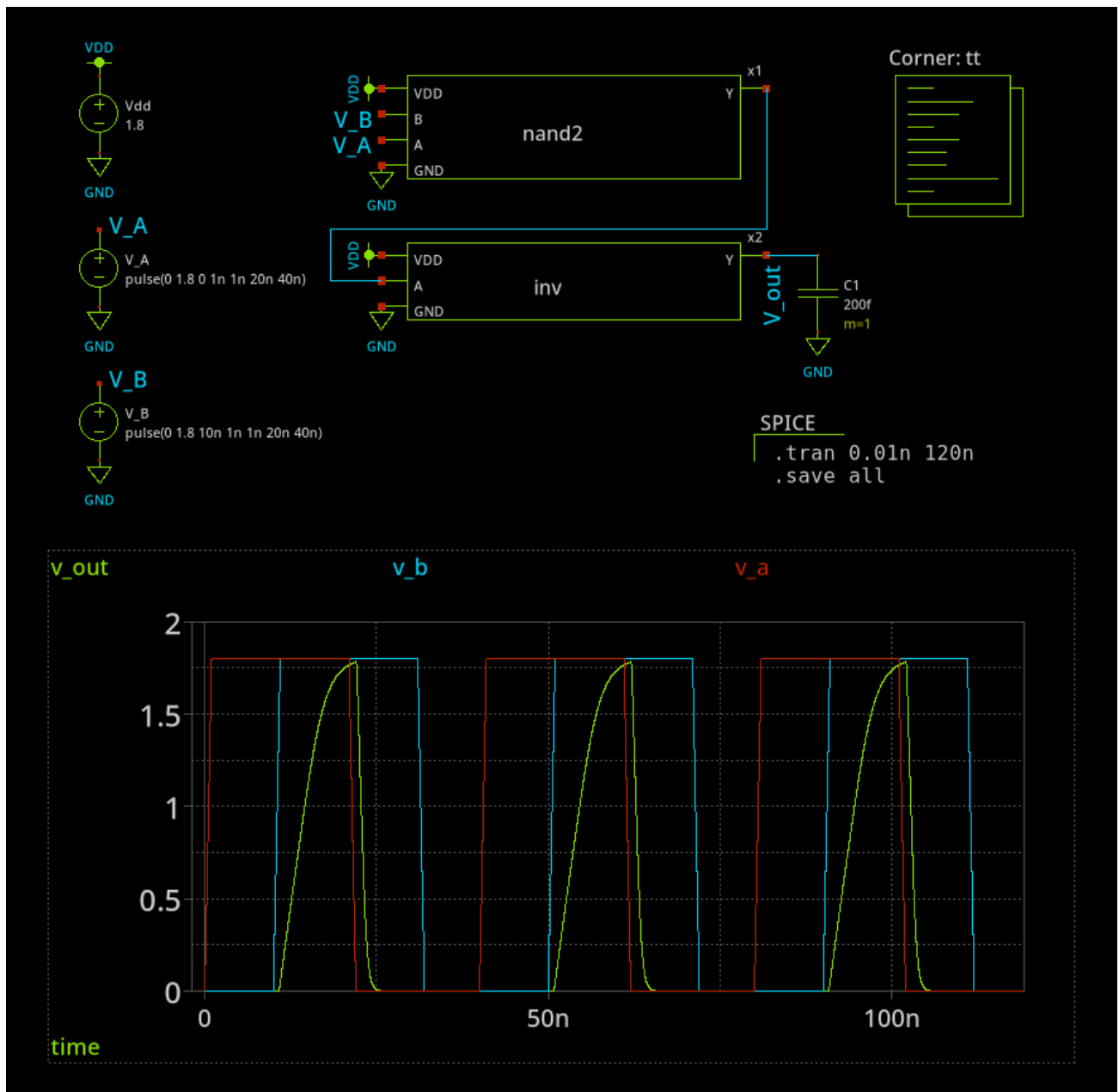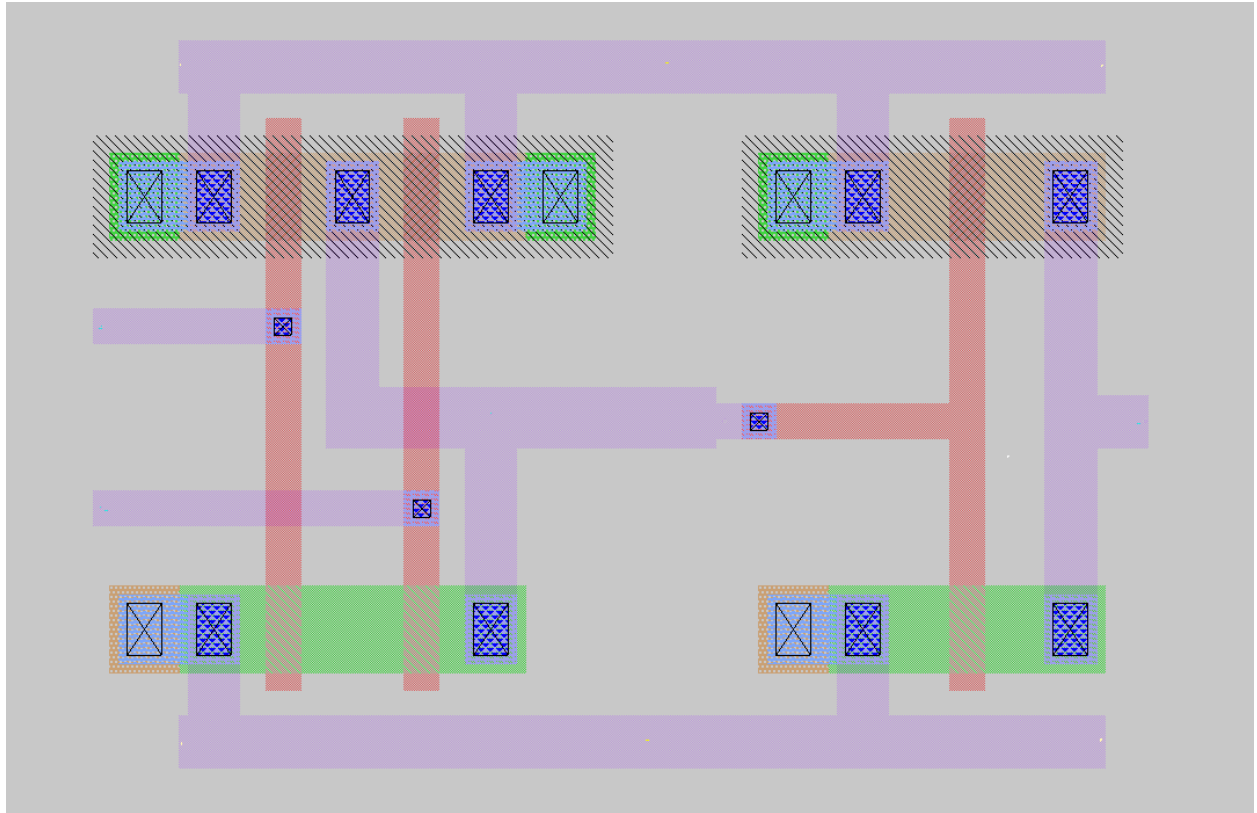
NAND

Inverter

AND gate + Transient Simulation

VDD

Vdd
1.8

GND

V_A
pulse(0 1.8 0 1n 1n 20n 40n)

GND

V_B
pulse(0 1.8 10n 1n 1n 20n 40n)

GND

nand2

x1
VDD
B
A
GND
Y

inv

x2
VDD
A
GND
Y

V_out

C1
200f
m=1

GND

Corner: tt

SPICE
.tran 0.01n 120n
.save all

v_out   v_b   v_a

time

Magic VLSI layout AND

LVS Output

Circuit 1 cell sky130_fd_pr__nfet_01v8 and Circuit 2 cell sky130_fd_pr__nfet_01v8 are black boxes. Warning: Equate pins: cell sky130_fd_pr__nfet_01v8 is a placeholder, treated as a black box. Warning: Equate pins: cell sky130_fd_pr__nfet_01v8 is a placeholder, treated as a black box.

Subcircuit pins:

Circuit 1: sky130_fd_pr__nfet_01v8	Circuit 2: sky130_fd_pr__nfet_01v8
1	1
2	2
3	3
4	4

Cell pin lists are equivalent. Device classes sky130_fd_pr__nfet_01v8 and sky130_fd_pr__nfet_01v8 are equivalent.

Circuit 1 cell sky130_fd_pr__pfet_01v8 and Circuit 2 cell sky130_fd_pr__pfet_01v8 are black boxes. Warning: Equate pins: cell sky130_fd_pr__pfet_01v8 is a placeholder, treated as a black box. Warning: Equate pins: cell sky130_fd_pr__pfet_01v8 is a placeholder, treated as a black box.

Subcircuit pins:

Circuit 1: sky130_fd_pr__pfet_01v8	Circuit 2: sky130_fd_pr__pfet_01v8
1	1
2	2
3	3
4	4

Cell pin lists are equivalent. Device classes sky130_fd_pr__pfet_01v8 and sky130_fd_pr__pfet_01v8 are equivalent.

Subcircuit summary:

Circuit 1: inv	Circuit 2: inv
sky130_fd_pr__nfet_01v8 (1)	sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)	sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2	Number of devices: 2
Number of nets: 4	Number of nets: 4

Netlists match uniquely.

Subcircuit pins:

Circuit 1: inv	Circuit 2: inv
Y	Y
A	A
GND	GND
VDD	VDD

Cell pin lists are equivalent. Device classes inv and inv are equivalent.

Subcircuit summary:

Circuit 1: nand2	Circuit 2: nand2
sky130_fd_pr__pfet_01v8 (2)	sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)	sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4	Number of devices: 4
Number of nets: 6	Number of nets: 6

Netlists match uniquely.

Subcircuit pins:

Circuit 1: nand2	Circuit 2: nand2
GND	GND
Y	Y
B	B
A	A
VDD	VDD

Cell pin lists are equivalent. Device classes nand2 and nand2 are equivalent.
Flattening instances of nand2 in cell ./xschem/simulation/and.spice (0) makes a better match Flattening instances of inv in cell ./xschem/simulation/and.spice (0) makes a better match Making another compare attempt.

Final result:
Cells have no pins; pin matching not needed.
Device classes ./xschem/simulation/and.spice and ./magic/and.spice are equivalent.
Verify: cell ./magic/and.spice has no elements and/or nodes. Not checked.