0306_ESE_MCQ_MCA_Sem 4

ECC 402- Microcontrollers

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1. Which of the following parts of the microprocessor is closely related to register?

- Processor
- ALU
- CPU
- Memory

Clear selection

2. During the execution of a program, which register is initialized first?

- Instruction registers
- Program Counter
- Stack pointer
- Program status word

Clear selection

3. A microprocessor is clocked at a rate of 3 GHz. How long is a clock cycle?

- 0.2ns
- 0.3ns
- 1.5ns
- 1ns

4. How can we change the speed of a DC motor using PWM in PIC 16F886 microcontroller?

- ○ By changing amplitude of Pulse
- ○ By keeping fixed duty cycle
- ◉ By changing duty cycle
- ○ By increasing power of Pulse

Clear selection

5. A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB), which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

- ○ 11 bits
- ○ 13 bits
- ◉ 15 bits
- ○ 20 bits

Clear selection

6. The high speed memory between the CPU and main memory is called as-------

- ◉ Cache Memory
- ○ Virtual memory
- ○ Secondary memory
- ○ Storage memory

Clear selection

7.	The register that can be used as a scratch pad in 8051 is

- ○ Accumulator
- ○ Stack Pointer
- ○ Program Counter
- ◉ B register

Clear selection

8.	The registers that provide control and status information about Timer/Counters in 8051 is

- ○ IP, IE
- ◉ TMOD, TCON
- ○ SCON,SBUF
- ○ Flag register, Accumulator

Clear selection

9.	The higher and lower bytes of a 16-bit register DPTR in 8051 are represented respectively as

- ○ LDPTR and HDPTR
- ○ DPTRL and DPTRH
- ◉ DPH and DPL
- ○ HDP and LDP

Clear selection

10. The pin that is grounded for interfacing external program memory in 8051 is

- (●) EA(active low)
- ( ) PSEN(active low)
- ( ) OE(active low)
- ( ) ALE

Clear selection

11. The 8051 instruction that is used to complement or invert the bit of a bit addressable SFR is

- ( ) CLR C
- ( ) CPL C
- (●) CPL Bit
- ( ) ANL Bit

Clear selection

12. The first byte of an absolute jump instruction in 8051 consists of

- ( ) 3 LSBs of opcode and 5 MSBs of 11-bit address
- (●) 5 LSBs of opcode and 3 MSBs of 11-bit address
- ( ) 5 MSBs of opcode and 3 LSBs of 11-bit address
- ( ) 6 MSBs of opcode and 1 LSB of 11-bit address

Clear selection

13.	What is the function of a watchdog timer (WDT)?

- ○ It resets the system if applied voltage increased above threshold value
- ○ It resets the system if applied voltage decreases below threshold value
- ◉ It resets the system if the software fails to operate properly.
- ○ It resets the system if Power failure is detected.

Clear selection

14.	The instructions that change the sequence of execution are

- ○ conditional instructions
- ○ logical instructions
- ◉ control transfer instructions
- ○ data transfer instructions

Clear selection

15.	In the instruction "MOV TH1, #-3", what is the value that is being loaded in the TH1 register?

- ○ 0xFCH
- ○ 0xFBH
- ◉ 0xFDH
- ○ 0xFEH

Clear selection

16.	How many registers are there in ARM7?

- ○ 35 register(28 GPR and 7 SPR)
- ○ 37 registers(28 GPR and 9 SPR)
- ◉ 37 registers(31 GPR and 6 SPR)
- ○ 35 register(30 GPR and 5 SPR)

Clear selection

17.	How much flash memory does the Atmega328 have?

- ○ 13K bytes
- ◉ 32K bytes
- ○ 256K bytes
- ○ 16K bytes

Clear selection

18.	What is the capability of ARM7 instruction for a second?

- ○ 110 MIPS
- ◉ 130 MIPS
- ○ 150 MIPS
- ○ 125 MIPS

Clear selection

19. Which of the following are pipelining stages of ARM7?

- ○ Fetch, Decode, Write
- ○ Fetch, Decode, Execute, Write
- ○ Fetch, Execute, Write
- ◉ Fetch, Decode, Execute

Clear selection

20. In ARM 7, program counter is implemented using _____

- ○ Caches
- ○ Heaps
- ◉ General purpose register
- ○ Stack

Clear selection

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