Technical Writing in Electrical Engineering

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Abstract— Technical communication is everywhere, from simple emails to presentations to immense publications. In this paper, technical communication in electrical engineering is analyzed through interviews with a professional and an upperclassman, three sample electrical engineering documents, and three articles detailing guidelines for technical communication. The results of this analysis show that writing is a substantial portion of the day to day activities for electrical engineers. Secondary results include some general guidelines for effective communication in electrical engineering. Understanding the importance of technical communication is a must for anyone entering the field of electrical engineering.

Keywords— Electrical engineering, technical communication, technical writing, interview, IEEE

I. INTRODUCTION

Conveying information is important in any engineering discipline. Up to this point, a substantial amount of English instruction has been focused on writing papers emphasizing grammar, spelling, and format while excluding how to convey information effectively in different scenarios. Through the study of technical communication, this necessity can be directly addressed. In this project, technical communication in real world electrical engineering applications is examined through interviews, research, and analysis of example documents.

II. INTERVIEWS

a senior at New Mexico Tech, provided some insight into technical writing further along in the electrical engineering program. The majority of the writing involved in Chris's coursework involves technical reports based on both experimentation and research. As a residential assistant (RA) here at Tech, a substantial part of his job is writing emails to other RAs and work orders for the maintenance crew. These documents, while not being highly technical, need to be formal, clear, and concise so as to be understood by all parties involved. In the future, Chris

expects to work in research and development, where he plans to write complex reports and convincing grant proposals.

h, an electrical engineering PhD. working for Motorola, also had some interesting information to share. When initially asked about writing, John replied, "I became an engineer so I didn't have to write." Despite his best efforts, he estimates that he spends one to two hours writing every day – most of which is email. While his writing is not limited by budget, it certainly is by time; most of the people in John's group work on many different projects simultaneously.

In addition to email, John participates in writing monthly reports and substantial white papers. Monthly reports, he notes, are normally only about one page and are designed to be read by a wide variety of readers. On the other hand, white papers can reach more than a hundred pages in length and usually go through seven or more revisions before being published. These white papers are usually aimed at obtaining funding for a project and are persuasive in nature. John actually uses a version control system to manage his formal documents, similar to source code. All of his formal writing conforms to IEEE standards.

John gives a substantial amount of presentations, both inside and outside Motorola. Internally, he presents about current projects and new proposals to both small and large audiences. Externally, such as at conferences, he presents public domain research results for examination by his peers.

Throughout his career, John has gained some valuable insight into applying for a job in electrical engineering. He believes that the most important things to emphasize when writing a resume are interest, skills, and passion. He suggests that considering the current economic situation may also be important when searching for a job.

III. LIBRARY RESEARCH

A. IEEE Citation Guidelines

Proper citations are a necessity in any formal research document; without them, readers would be unable to verify the author's claims quickly. Electrical engineering follows the IEEE citation style, which is described in detail in [1]. In short, this document provides a useful quick reference for using in-text citations and for formatting references at the end of a document. Of the useful information in this manual, possibly the most interesting is the way that in-text citations differ between MLA and IEEE formats. In MLA format, citations are not directly a part of the text, occurring at the end of sentences. In IEEE format, references like [1] are used directly as nouns. IEEE format also lists references in order of first use, rather than in alphabetical order.

B. Sample IEEE Paper

Formatting is especially important in electrical engineering; most conferences simply will not publish papers that do not adhere to a strict formatting guideline. Electrical engineering follows the IEEE publication format for formal documents, which is detailed in [2]. This document itself follows the IEEE format while describing guidelines and providing examples of how to write a paper for publication. Every single detail of writing a publication worthy paper is detailed in [2], from font style and size to indentation and graphics. One of the most interesting details provided in this paper is that all images must be of decent resolution – low resolution images are unacceptable.

C. Rhetorical Analysis of Introductions

Giving presentations is an inevitable and important part of working in electrical engineering. In [3], the authors examined 40 presentations about engineering in an attempt to understand the different introductory methods used by professionals.

In the results of this research, [3] identifies three basic rhetorical strategies used – attentum, benevolum, and docilem. An appeal to attentum is an attempt to capture the audience's attention; this can be done through saying something witty or simply by addressing the audience directly. The second strategy, benevolum, is an appeal to the audience's goodwill towards the speaker. An example of this strategy would be to pretend to improvise, making the speaker more personable to the audience. The third

strategy, docilem, is to directly introduce the topic of the presentation.

For each of these rhetorical strategies, the authors of this article identify several unique techniques in which the speaker delivers the appeal. After performing this research, the authors show that introducing the subject material, docilem, is by far the most popular appeal used. For future presentations, the author suggests using a combination of the three different rhetorical strategies to produce the most memorable and productive introduction.

IV. EXAMPLE DOCUMENTS

Three sample documents, a whitepaper in [4], a datasheet, and a memo, are analyzed in Table 1. This table examines how each respective author chooses language, format, and graphics to achieve a specific purpose in appealing to a target audience.

V. CONCLUSION

In this project, technical writing in electrical engineering is studied through analysis of real world documents, library research, and interviews with professionals. Through this process, it is clear that audience and purpose have great impacts on the language and format of any communication, from emails to presentations. Technical writing is clearly an integral part of this profession, and strong writing skills may trump engineering ability in the ultimate search for employment.

ACKNOWLEDGEMENT

The author would like to thank and and helpful information. Also, thanks to for substantial peer review advice.

REFERENCES

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- 3] D. V. D. Mieroop, J. D. Jong, and B. Andeweg, "I Want to Talk About...: A Rhetorical Analysis of the Introductions of 40 Speeches About Engineering," *Journal of Business and Technical Communication*, vol. 22, no. 2, p. 186, p. 195-200, Apr. 2008. [Abstract]. Available: http://jbt.sagepub.com/content/22/2/186. [Accessed Sep. 7, 2010]
- [4] Z. Ye and J. Grosspietsch, "An All Digital QAM Modulator with Radio Frequency Output," presented at SDR 05 Technical Conference and Product Exposition, 2005.

TABLE I
COMPARISON OF SAMPLE DOCUMENTS

Title	Document Type	Purpose	Audience	Language / Tone	Format / Design	Graphics
"An all Digital QAM Modulator with Radio Frequency Output"	Whitepaper	Describe research findings on digital signal modulation for review by other professionals. Showcase the benefits of using such a system over existing systems.	Other highly skilled engineers interested in new signal modulation research. Engineers working on improving existing systems.	Highly technical information and research findings. Tone is objective, informational and highly formal. Good English understanding required.	Conforms to IEEE format. Abstract and subsections are very modular so that they can be read independently. Significant in text references to existing material.	Small tables and mathematics are laid out within the text and labeled. Larger figures, graphs, etc. are located at the end of the document and have descriptive captions.
"ATD_10B8C Block User Guide"	Datasheet	Details the operations of the analog to digital subsystem of the Motorola MC9S12 microcontroller. Serves as a programming reference for MC9S12 users.	Designers who need to use the analog to digital subsystem, or those who are considering using it. Highly technical audience.	Detailed descriptions of functionality. Tone is formal and informative, all third person. Moderate to Good English understanding required.	Designed such that sections are independent and can be used as a quick reference. Comprehensive table of contents at the beginning of the document.	Technical depictions of components. Many graphics depicting layout of registers embedded in text for easy readability and quick reference.
"Micro- controller Power Management"	Memo	Describe how TinyOS 2.x mechanisms manage microcontroller power effectively. Describes basics of microcontroller subsystem power management.	Developers within the TinyOS community. Microcontroller users looking for an operating system. The TinyOS community in general – author requests discussion and feedback.	Language semitechnical so as to be read by professionals and general users alike. Tone informative and moderately formal with no use of first or second person. Moderate English understanding required	Sequential, author builds up all necessary information to understand document. Written to loosely conform to IEEE format	No formal graphics in this text. Limited tables and code are used with no headers Two tables embedded within the text Microcontroller code embedded within the text.

APPENDIX

- Presentation Handout
- [1] Citation Reference
- [2] Sample IEEE Paper[3] Rhetorical Analysis of Introductions
- [4] All Digital QAM Modulator
- Analog to Digital Converter Datasheet
- Microcontroller Power Management

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Abstract

Conveying information is important in any engineering discipline. Up to this point, a substantial amount of English instruction has been focused on writing papers emphasizing grammar, spelling, and format while excluding how to convey information effectively in different scenarios. Through the study of technical communication, this necessity can be directly addressed. In this project, technical communication in real world electrical engineering applications is examined through interviews, research, and analysis of example documents.

INTERVIEW

- EE Senior, New Mexico Tech

- Writes technical reports based on research and experimentation
- Expects to create proposals and patent documentation in his work in research and development

– EE PhD., Motorola

- "I became an engineer so I didn't have to write"
- 1-2 hours of writing every day, mostly email
- Participates in creating monthly reports, whitepapers, and patent documents

LIBRARY RESEARCH

IEEE Citation Guidelines

Details how to formulate complete IEEE compliant citations

Sample IEEE Paper

Provides a formatting example for creating an IEEE compliant paper

Rhetorical Analysis of Introductions

- Analyses 40 presentations for techniques employed in the introduction
- Three types of introductory components:
 - Attentum Grab listeners attention
 - Benevolum Improve audience's goodwill towards speaker
 - o Docilem Describe content of the presentation

EXAMPLE DOCUMENTS

An All Digital QAM Modulator with Radio Frequency Output

- Whitepaper Highly technical and complex
- Describes research findings to other highly skilled engineers in IEEE format

ATD 10B8C Block User Guide

- Datasheet Highly technical, simple to use
- Describes in detail how to use an analog to digital converter as a quick reference

Microcontroller Power Management

- Memo Somewhat technical, easy to read
- Describes the benefits of using TinyOS to microcontroller designers



Library

How To Cite References - IEEE Style

The Institute of Electrical and Electronics Engineers (IEEE) Style is used primarily for publications in engineering, electronics, telecommunications, computer science and information technology.

When using EndNote bibliographic software, please use the following output style - IEEE.

Please remember to check with your unit co-ordinator or tutor before submitting your assignments, as their style preference may vary from the guidelines presented here.

Updated February 2008

Contents

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 Print Documents
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- Internet Documents

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- Other Formats Podcasts
- O A reference list: what should it look like?
 - O Abbreviations
- O Other sources of information

These guidelines follow the principles given in the Information for Authors: IEEE Transactions, Journals and Letters published by the Institute of Electrical and Electronics Engineers (IEEE) in 2003 and the Reference Guide: IEEE Style, University of Illinois at Urbania Champaign, College of Engineering, 1998. An additional source of information on the citation of electronic resources was Numeric Referencing, University of Wales, Swansea, 2004.

document. In its simplest form, a ditation is given consisting of a number enclosed by square brackets. The full details of IEEE Style uses a notational method of referencing when referring to a source of information within the text of a the source are given in a numerical reference list at the end of the document.

Citation Within The Text

Indicating the relevant reference in the text

essay or assignment. Once a source has been cited, the same number is used in all subsequent references. No distinction A number enclosed in square brackets, eg. [1] or [26], placed in the text of the essay, indicates the relevant reference. reference containing publication information about the source cited in the reference list at the end of the publication, Citations are numbered in the order in which they appear in the text and each citation corresponds to a numbered is made between print and electronic references when citing within the text.

Each reference number should be enclosed in square brackets on the same line as the text, before any punctuation, with a

space before the bracket.

Here are some examples of this kind of referencing:

```
"The theory was first put forward in 1987 [1]."
"...end of the line for my research [13]."
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"Several recent studies [3, 4, 15, 16] have suggested that..." "Scholtz [2] has argued that.....

"For example, see [7]."

It is not necessary to mention either the author(s) or the the date of the reference unless it is relevant to your text. It is not necessary to say " in reference [26] ..." "In [26] ..." is sufficient.

Citing more than one reference at a time

When citing more than one source at a time, the preferred method is to list each reference number separately with a comma or dash between each reference:

[1], [3], [5]

Although the following method is also acceptable:

Acceptable

[1, 3, 5]

[Contents]

Personal Communications

IEEE style states that you cite only published works, forthcoming published works, and unpublished materials available to Personal comunications indude conversations, letters, interviews, e-mails and telephone conversations.

For interviews or other "non-recoverable" information, no citation number is necessary. This does not mean that an attempt to identify the author is unnecessary, but that it needs to be done in the text itself. scholars in a library, a depository, or an archive.

"In a personal interview with Bill Gates, he suggested that he would soon rule the world."

"In a letter to the author, professor Mueller detailed his expereinnces with using this data collection software."

Creating a reference list or bibliography

citation in the text of the assignment or essay, not in alphabetical order. List only one reference per reference number Footnotes or other information that are not part of the referencing format should not be included in the reference list. A numbered list of references must be provided at the end of the paper. The list should be arranged in the order of

The following examples demonstrate the format for a variety of types of references. Induded are some examples of citing electronic documents. Such items come in many forms, so only some examples have been listed here.

Print Documents

Books

Note: Every (important) word in the title of a book or conference must be capitalised. Only the first word of a subtitle should be capitalised. Capitalise the "v" in Volume for a book title. Punctuation goes inside the quotation marks.

Standard format

[#1 A. A. Author/editor, Title: Subtitle (in italics), Edition(if not the first), Vol.(if a multivolume work).

Place of publication: Publisher, Year, page number(s) (if appropriate).

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- [1] W.-K. Chen, Linear Networks and Systems. Belmont, CA: Wadsworth, 1993, pp. 123-135.
- [2] S. M. Hemmington, Soft Science. Saskatoon: University of Saskatchewan Press, 1997.

Edited work

[3] D. Sarunyagate, Ed., Lasers. New York: McGraw-Hill, 1996.

Later edition

- [4] K. Schwalbe, Information Technology Project Management, 3rd ed. Boston: Course Technology, 2004.
- [5] M. N. DeMers, Fundamentals of Geographic Information Systems, 3rd ed. New York : John Wiley, 2005.

More than one author

- [6] T. Jordan and P. A. Taylor, Hacktivism and Cyberwars: Rebels with a cause? London: Routledge, 2004
- [7] U. J. Gelinas, Jr., S. G. Sutton, and J. Fedorowicz, Business processes and information technology. Cincinnati: South-Western/Thomson Learning, 2004.

Three or more authors

Note: The names of all authors should be given in the references unless the number of authors is greater than six. If there are more than six authors, you may use et al. after the name of the first author. [8] R. Hayes, G. Pisano, D. Upton, and S. Wheelwright, Operations, Strategy, and Technology: Pursuing the competitive edge. Hoboken, NJ: Wiley, 2005.

[9] M. Bell, et al., Universities Online: A survey of online education and services in Australia, Occasional Paper Series 02-A. Canberra: Department of Education, Science and Training, 2002.

Corporate author (ie: a company or organisation)

[10] World Bank, Information and Communication Technologies: A World Bank group strategy. Washington, DC: World

Conference (complete conference proceedings)

[11] T. J. van Weert and R. K. Munro, Eds., Informatics and the Digital Society: Social, ethical and cognitive issues: IFIP TC3/WG3.183.2 Open Conference on Social, Ethical and Cognitive Issues of Informatics and ICT, July 22-26, 2002, Dortmund, Germany. Boston: Kluwer Academic, 2003.

Government publication

[12] Australia. Attomey-Generals Department. *Digital Agenda Review, 4* Vols. Canberra: Attomey- General's Department,

Manual

[13] Bell Telephone Laboratories Technical Staff, *Transmission System for Communications*, Bell Telephone Laboratories,

Catalogue

[14] Catalog No. MWM-1, Microwave Components, M. W. Microwave Corp., Brooklyn, NY.

Application notes

[15] Hewlett-Packard, Appl. Note 935, pp. 25-29.

Note: Titles of unpublished works are not italiased or capitalised. Capitalise only the first word of a paper or thesis.

Fechnical report

[16] K. E. Elliott and C.M. Greene, "A local adaptive protocol," Argonne National Laboratory, Argonne, France, Tech. Rep. 916-1010-BB, 1997.

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Papers presented at conferences (unpublished)

[18] H. A. Nimr, "Defuzzification of the outputs of fuzzy controllers," presented at 5th International Conference on Fuzzy Systems, Cairo, Egypt, 1996.

[19] H. Zhang, "Delay-insensitive networks," M.S. thesis, University of Waterloo, Waterloo, ON, Canada, 1997.

Thesis or dissertation

[20] M. W. Dixon, "Application of neural networks to solve the routing problem in communication networks," Ph.D. dissertation, Murdoch University, Murdoch, WA, Australia, 1999.

Parts of a Book

Note: These examples are for chapters or parts of edited works in which the chapters or parts have individual title and author/s, but are included in collections or textbooks edited by others. If the editors of a work are also the authors of all of the included chapters then it should be cited as a whole book using the examples given above (Books). Capitalise only the first word of a paper or book chapter.

[#] A. A. Author of Part, "Title of chapter or part," in *Title: Subtitle of book*, Edition, Vol., A. Editor Ed. Place of publication: Publisher, Year, pp. inclusive page numbers.

Single chapter from an edited work

- [1] A. Rezi and M. Allam, "Techniques in array processing by means of transformations, " in Control and Dynamic Systems, Vol. 69, Multidemsional Systems, C. T. Leondes, Ed. San Diego: Academic Press, 1995, pp. 133-180.
- [2] G. O. Young, "Synthetic structure of industrial plastics," in Plastics, 2nd ed., vol. 3, J. Peters, Ed. New York: McGraw-Hill, 1964, pp. 15-64.

Conference or seminar paper (one paper from a published conference proceedings)

- European and former Soviet Union (CEE/FSU) countries," in Second International Telecommunications Energy Special [3] N. Osifchin and G. Vau, "Power considerations for the modernization of telecommunications in Central and Eastern Conference, 1997, pp. 9-16.
- [4] S. Al Kuran, "The prospects for GaAs MESFET technology in dc-ac voltage conversion," in Proceedings of the Fourth Annual Portable Design Conference, 1997, pp. 137-142.

Article in an encyclopaedia, signed

[5] O. B. R. Strimpel, "Computer graphics," in McGraw-Hill Encyclopedia of Science and Technology, 8th ed., Vol. 4. New York: McGraw-Hill, 1997, pp. 279-283.

Study Guides and Unit Readers

Note: You should not cite from Unit Readers, Study Guides, or lecture notes, but where possible you should go to the original source of the information. If you do need to die articles from the Unit Reader, treat the Reader articles as if they were book or journal articles. In the reference list or bibliography use the bibliographical details as quoted in the Reader and refer to the page numbers from the Reader, not the original page numbers (unless you have independently consulted

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[6] L. Vertelney, M. Arent, and H. Lieberman, "Two disciplines in search of an interface: Reflections on a design problem," in The Art of Human-Computer Interface Design, B. Laurel, Ed. Reading, MA: Addison-Wesley, 1990. Reprinted in Human-Computer Interaction (ICT 235) Readings and Lecture Notes, Vol. 1. Murdoch: Murdoch University, 2005, pp.

Journal Articles

You may spell out words such as volume or December, but you must either spell out all such occurrences or abbreviate all. Note: Capitalise only the first word of an article title, except for proper nouns or acronyms. Every (important) word in the You must either spell out the entire name of each journal that you reference or use accepted abbreviations. You must consistently do one or the other. Staff at the Reference Desk can suggest sources of accepted journal abbreviations. title of a journal must be capitalised. Do not capitalise the "v" in volume for a journal article. You do not need to abbreviate March, April, May, June or July.

Standard format

To indicate a page range use pp. 111-222. If you refer to only one page, use only p. 111.

[#] A. A. Author of article. "Title of article," *Title of Journal*, vol. #, no. #, pp. page number/s, Month

Journal articles

- [1] E. P. Wigner, "Theory of traveling wave optical laser," Phys. Rev., vol. 134, pp. A635-A646, Dec. 1965.
- [2] J. U. Duncombe, "Infrared navigation Part I: An assessment of feasability," IEEE Trans. Electron. Devices, vol. ED-11, pp. 34-39, Jan. 1959.
- [3] G. Liu, K. Y. Lee, and H. F. Jordan, "TDM and TWDM de Bruijn networks and shufflenets for optical communications," IEEE Trans. Comp., vol. 46, pp. 695-701, June 1997.

OR

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- [5] I. S. Qamber, "Flow graph development method," Microelectronics Reliability, vol. 33, no. 9, pp. 1387-1395, Dec. 1993.
- [6] E. H. Miller, "A note on reflector arrays," IEEE Transactions on Antennas and Propagation, to be published.

Electronic documents

If only the first page number is given, a plus sign indicates following pages, eg. 26+. If page numbers are not given, use Note: When you cite an electronic source try to describe it in the same way you would describe a similar printed publication. If possible, give sufficient information for your readers to retrieve the source themselves. paragraph or other section numbers if you need to be specific.

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the date of access is included since an electronic source may change between the time you cite it and the time it is

accessed by a reader.

E-Books

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Standard format

[#] A. Author. *Title of E-book*. Place: Publisher, Date of original publication. [Format] Available: Source.

- [1] L. Bass, P. Clements, and R. Kazman. Software Architecture in Practice, 2nd ed. Reading, MA: Addison Wesley, 2003. [E-book] Available: Safari e-book.
- [2] T. Eckes, The Developmental Social Psychology of Gender. Mahwah NJ: Lawrence Erlbaum, 2000. [E-book] Available: netLibrary e-book.

Article in online encyclopaedia

- [3] D. Ince, "Acoustic coupler," in A Dictionary of the Internet. Oxford: Oxford University Press, 2001. [Online]. Available: Oxford Reference Online, http://www.oxfordreference.com. [Accessed: May 24, 2005].
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[Contents]

E-Journals

Standard format

[#] A. Author, "Title of Article," Title of Journal, vol., no., p. page numbers, month year. [Format]. Available: Database Name (if appropriate), internet address. [Accessed date of access].

Journal article abstract accessed from online database

[1] M. T. Kimour and D. Meslati, "Deriving objects from use cases in real-time embedded systems," Information and Software Technology, vol. 47, no. 8, p. 533, June 2005. [Abstract]. Available: ProQuest, http://www.umi.com /proquest/. [Accessed May 12, 2005]. Note: Abstract citations are only included in a reference list if the abstract is substantial or if the full-text of the article could not be accessed.

Journal article from online full-text database

Note: When including the internet address of articles retrieved from searches in full-text databases, please use the Recommended URLs for Full-text Databases, which are the URLs for the main entrance to the service and are easier to

- [2] H. K. Edwards and V. Sridhar, "Analysis of software requirements engineering exercises in a global virtual team setup," Journal of Global Information Management, vol. 13, no. 2, p. 21+, April-June 2005. [Online]. Available: Academic OneFile, http://find.galegroup.com. [Accessed May 31, 2005].
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Newspaper article from the Internet

[7] C. Wilson-Clark, "Computers ranked as key literacy," The West Australian, para. 3, March 29, 2004. [Online]. Available: http://www.thewest.com.au. [Accessed Sept. 18, 2004].

Internet Documents

Standard format

[#] A. Author, "Document title," Webpage name, Source/production information, Date of internet publication. [Format]. Available: internet address. [Accessed: Date of access].

Professional Internet site

[1] European Telecommunications Standards Institute, "Digital Video Broadcasting (DVB): Implementation guidelines for DVB terrestrial services; transmission aspects," European Telecommunications Standards Institute, ETSI TR-101-190, 1997. [Online]. Available: http://www.etsi.org. [Accessed: Aug. 17, 1998].

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General Internet site

[3] J. Geralds, "Sega Ends Production of Dreamcast," vnunet.com, para. 2, Jan. 31, 2001. [Online]. Available: http://nll.vnunet.com/news/1116995. [Accessed: Sept. 12, 2004].

Internet document, no author given

[4] "A 'layman's' explanation of Ultra Narrow Band technology," Oct. 3, 2003. [Online]. Available: http://www.vmsk.org /Layman.pdf. [Accessed: Dec. 3, 2003].

Contents

Non-Book Formats

[#] A. A. Person, Responsibility (if appropriate), Title: Subtitle. [Format]. Special credits (if appropriate). Place of publication: Publisher, Year.

Podcasts

- [1] W. Brown and K. Brodie, Presenters, and P. George, Producer, "From Lake Baikal to the Halfway Mark, Yekaterinburg", Peking to Paris: Episode 3, Jun. 4, 2007. [Podcast television programme]. Sydney: ABC Television. Available: http://www.abc.net.au/tv/pekingtoparis/podcast/pekingtoparis.xml. [Accessed Feb. 4, 2008].
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Other Formats

[3] W. D. Scott & Co, Information Technology in Australia: Capacities and opportunities: A report to the Department of

Science and Technology. [Microform]. W. D. Scott & Company Pty. Ltd. in association with Arthur D. Little Inc. Canberra: Department of Science and Technology, 1984.

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Software

Video recording

[5] Thomson ISI, EndNote 7. [CD-ROM]. Berkeley, Ca.: ISI ResearchSoft, 2003

[6] C. Rogers, Writer and Director, Grils in IT. [Videorecording]. Bendigo, Vic. : Video Education Australasia, 1999.

[Contents]

A reference list: what should it look like?

The reference list should appear at the end of your paper. Begin the list on a new page. The title References should be either left justified or centered on the page. The entries should appear as one numerical sequence in the order that the material is cited in the text of your assignment.

Note: The hanging indent for each reference makes the numerical sequence more obvious.

- [1] A. Rezi and M. Allam, "Techniques in array processing by means of transformations, " in Control and Dynamic Systems, Vol. 69, Multidemsional Systems, C. T. Leondes, Ed. San Diego: Academic Press, 1995, pp. 133-180.
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[Contents]

Abbreviations

Standard abbreviations may be used in your citations. A list of appropriate abbreviations can be found below:

Ed./Eds.	editor/editors
ed.	edition
et al.	and others
no.	number
p./pp.	page/pages
para.	paragraph
pt.	part

rev.	revised
suppl.	supplement
Vol.	Volume (book)
vol.	volume (joumal)

[Contents]

Other sources of information

Note: This list of examples is in no way exhaustive. Only the most often-used types of references are listed here. Refer to the following publications for more information on citing references:

Institute of Electrical and Electronics Engineers, Inc., IEEE Transactions, Journals and Letters: Information for authors. Piscataway NJ: IEEE, 2003. Available: http://www.ieee.org/portal/cms_docs/pubs/transactions/auinfo03.pdf. [Accessed May 20, 2005]

University of Illinois, College of Engineering, *Reference Guide: IEEE style*. Urbana-Champaign IL: University of Illinois, 1998. Available: http://www.ece.uiuc.edu.edu/pubs/ref_guides/leee.html. [Accessed May 20, 2005].

University of Wales, Library and Information Services, *Numeric referencing: Examples of reference types*. Swansea: University of Wales, 2004. Available: http://www.swan.ac.uk/lis/help_and_training/htmdocs /bibliographic_referencing/numeric_referencing_examples.asp. [Accessed May 24, 2005]. University of Wales, Library and Information Services, Numeric referencing: Overview. Swansea: University of Wales, 2004. Available: http://www.swan.ac.uk/lis/help_and_training/htmdocs/bibliographic_referencing /numeric_referencing_overview.asp. [Accessed May 24, 2005].

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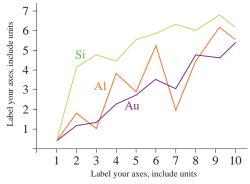


Fig. 1 A sample line graph using colors which contrast well both on screen and on a black-and-white hardcopy

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Fig. 2 Example of an unacceptable low-resolution image



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- example of a patent in [5]
- example of a website in [6]
- example of a web page in [7]
- example of a databook as a manual in [8]
- example of a datasheet in [9]
- example of a master's thesis in [10]
- example of a technical report in [11]
- example of a standard in [12]

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I Want to Talk About

Introductions of 40 Speeches A Rhetorical Analysis of the About Engineering

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rhetorical perspective to address the problems audiences seem to have with derived from classical manuals on rhetoric. This model enumerates and groups with an evaluation of the exordial model and a discussion of the study's This article investigates the introductions of 40 professional speeches from a presentations about engineering. The authors use an exordial model that they rhetorical exordial techniques into 3 main functions: attentum, benevolum, and docilem. The study shows that rhetorically complete introductions are rare. Most of the speakers seemed to prefer a content-oriented, direct approach (docilem) in their introductions and seldom used techniques to garner the audience's attention (attentum) or sympathy (benevolum). The article concludes pedagogical implications. Keywords: rhetorical analysis; oral presentations; engineers; introductions; exordial model

Lesteem because of their specialized skills and technical knowledge, but they are not considered to be articulate communicators. This unflattering In Belgium and the Netherlands, engineers are generally regarded with view of engineers has been pervasive for decades. In 1961, Weller and Stuiveling noted that many engineers lacked linguistic proficiency and the Authors' Note: Please address correspondence to Dorien Van De Mieroop, Department of Applied Language Studies, Lessius University College, Sint-Andriesstraat 2, B-2000 Antwerp, Belgium; e-mail: dorien.vandemieroop@lessius.eu.

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ability to express their thoughts effectively (p. 207). More recently, Simon De Bree (1998), the chairman of the board of directors of DSM (a large European conglomerate in the food and pharmaceutical industry), stated that although engineers have dedication, technical skill, and integrity, they do not have sufficient communication and marketing skills. But such claims have been supported only by anecdotal evidence and lack a solid empirical foundation. Communicating effectively, however, is a major part of an engineer's job (Paradis, Dobrin, & Miller, 1985). Research into how engineers actually communicate, both in speaking and in writing, is essential in helping them perform their tasks more effectively.

Speakers (including engineers) make their first impression on an audience in the first few minutes of their speech (Harms, 1961). Getting and retaining the audience's attention in these first few minutes is crucial because people listen selectively. If audience members initially find the speaker, the subject, or the treatment of the subject uninteresting or the oral presentation unprofessional, they are less receptive to both the messenger and the message. Does the alarming opinion of Weller and Stuiveling (1961) and of De Bree (1998)—that engineers are poor communicators—in any way stem from the rhetorical techniques that engineers use in the beginning of their speeches? An investigation of engineers' exordial techniques is necessary to find out whether teachers of oral communication skills need to emphasize in their rhetorical training the basic techniques involved in making effective speech introductions.

Furthermore, we limit ourselves to speech introductions because they are essential components of oral presentations (Locker, 2003, p. 468). In effective introductions, speakers accomplish a lot: not only arousing the audience's interest in the topic but also "establishing [their] credibility, and preparing the audience for what will follow" (Bovée & Thill, 2000, p. 570). If speakers fail to accomplish these tasks in their introductions, then their speech most likely will not be successful. As Goethe (1973) once stated, "When with buttoning up the first button goes wrong, the remaining ones cannot make In this article, we focus exclusively on oral presentations or speeches. up for it" (p. 546).

Our purpose in this study is to describe the exordial behavior of Dutchspeaking professionals (most of whom are engineers). More specifically, we aim to answer this question: How do these professionals begin their oral presentations? To determine the introductory practices of these speakers, literature on this subject (Andeweg & De Jong, 2004a). First we summarize this analyzing tool. Next we review previous research on the oral presentations we developed an exordial model based on both classical and modern advisory

of engineers, including survey results that we compare with the results of our analysis here. Then we describe our corpus of 40 speeches and the method of our study. Then we explain the results of our exordial analysis. Finally, we evaluate the exordial model as a descriptive tool and discuss the pedagogical implications of this study.

The Exordial Model

classical manuals on rhetoric, including Rhetorica ad Alexandrum (author ductions. In our critical review and analysis of these manuals, we focused on sections concerning speech introductions. Listing all the recommendations on introductions we could find, we compiled an overview of numerous introduction, the exordium, should fulfill three functions: It needs to make Greek and Roman rhetoricians have masterfully theorized how orators should approach their subject and reach their intended audience. The unknown, c. 336 B.C.), Aristotle's Rhetorica (c. 336 B.C.), Cicero's De Inventione (c. 89 B.C.), and Quintilian's Institutio Oratoria (95 A.D.), This overview formed the classical basis for an exordial model. The common the audience (a) attentive (attentum), (b) sympathetic (benevolum) and (c) understanding (docilem) for the whole speech to be received as favorably as possible. To investigate whether the classical recommendations survived the ages, we documented all the relevant literature of the 20th century that was written in Dutch (including translations from English and German books). We made an overview of works on oral communication (N = 136) and, with the aid of a panel of 10 experts, selected 42 books from the overview. We then analyzed the contemporary recommendations from these books and placed them within provide a useful foundation for developing analytical tools for speech introintroductory techniques, categorizing them by their three rhetorical functions. the classical model, which resulted in the extended version of the exordial model that is shown in Table 1 (Andeweg & De Jong, 2004a).

attentum, benevolum, and docilem. The function of attentum techniques is to attract the audience's attention and includes techniques such as using humor, anecdotes, or quotations. The aim of benevolum techniques is to make the audience favorably disposed, or sympathetic, toward the speech The exordial model presented in Table 1 lists the three different categories of introductory techniques, depending on their rhetorical functions: and the speaker, such as by stressing solidarity or flattering the audience. Finally, the purpose of docilem techniques is to enable the audience to follow, or understand, the main line of the presentation by introducing the

The Exordial Model Table 1

Attentum techniques	Benevolum techniques	Docilem techniques
	Classical recommendations	
A1. Stressing the importance of the subject A2. Demanding attention A3. Promising to give a brief speech A4. Saying something witty A5. Addressing others A6. Presenting an imaginary person A7. Giving a historic example A8. Drawing comparisons or using metaphors A9. Using a wordplay A10. Using a wordplay	Ab nostra persona [Regarding ourselves] B1. Enhancing credibility B1a. Enhancing your own credibility B1b. Enhancing your own and your company's credibility B1c. Enhancing your company's credibility B1c. Enhancing your company's credibility B2. Praising yourself and those you represent as Pretending to improvise B3. Pretending to improvise B4. Countering prejudices against yourself B5. Choosing the underdog position Ab adversariorum persona [Regarding our adversaries] B6. Blackening the opponent's reputation B7. Praising suspicious qualities Ab indicum persona [Regarding the addience Judge] B8. Flattering and praising B9. Stressing collectivity B10. Scaring/reassuring the case] B11. Underlining the bright spots B12. Shirking your own responsibility Other classical benevolum techniques B13. Asking for understanding for the flaws in the presentation	D1. Presenting the core of the speech (thesis or opinion) D2. Listing the main points (partitio) D3. Giving a brief previous history (narration)
	Modern recommendations	

(continued)

D7. Starting from a general issue and

B17. Introducing participants to each B16. Stressing what you will not be

A14. Asking a question A13. Quoting someone challenging

talking about (praeteritio)

D6. Announcing practicalities

D4. Naming the subject D5. Giving a definition

B15. Thanking the person who

A11. Telling an anecdote A12. Saying something

introduced you

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Table 1 (continued)

Attentum techniques	Docilem techniques
A15. Presenting the	narrowing down the
subject from a present-	subject (funnel
day point of view	opening)
A16. Addressing the	D8. Dealing with the
audience	equipment
A17. Referring to time,	D9. Marking the
place, circumstances	transition to the core
A18. Presenting a riddle	of the presentation
A19. Using visuals or	
audioeffects	
A20. Giving an example	
A21. Role-playing	
A22. Giving the title of the	
presentation	
A23. Using a proverb	

Note: This model was derived from data in De Eerste Minuten: Attentum, Benevolum en Docilem Parare in de Inleiding van Toespraken [The First Minutes: Attentum, Benevolum and Docilem Parare in the Introductions of Speeches], by B. A. Andeweg & J. C. De Jong, 2004a, doctoral dissertation, Radboud University Nijmegen.

vious history of the subject. Although some techniques can fulfill more than one function, we classified them in the category to which most of our source authors assigned them. For instance, although telling an anecdote in the introduction—which we assigned to the attentum category—serves to enhance the credibility of the speaker and to shed light on the topics to be changed advisory context. The classical writers prepared their readers discussed, it most of all serves to attract the attention of listeners (Andeweg & De Jong, 2006). Some of the techniques in the model—especially some benevolum techniques (e.g. blackening an opponent's reputation)—are seldom recommended in our contemporary sources, probably because of the mainly, but not only, for court presentations whereas the modern Dutch major points of the speech, for example, or by giving an insight into the prewriters never applied their recommendations to judicial contexts (the Dutch judicial system does not use trial by jury).

Our original exordial model consisted of techniques, strategic rhetorical means, that we found in the classical and modern advisory (prescriptive) literature. But when we analyzed concrete introductions, we found that

To strengthen the descriptive power of the model, then, we added extra techniques such as introducing participants to each other and dealing with the equipment. Our characterization of an exordial utterance as a technique in the model does not imply that we value the utterance as an effective technique. Our aim here is to use this model as a descriptive tool to enhance the level of detail in our analysis. After developing this extended model, we made our original research question (i.e., How do speaking professionals such as techniques do these speakers use in the introductions of their presentations, and which of the three rhetorical functions (attentum, benevolum, and docilem) some of the exordial utterances were hard to analyze in terms of the model. engineers begin their oral presentations?) more specific: What rhetorical do the speakers carry out in the introductions?

Previous Research

What does previous research tell us about the oral presentations of professionals such as engineers? Much of our knowledge about such presentations is derived from limited surveys conducted by Scheiber and Hager (1994) and Andeweg, De Jong, Van Oyen, and Wehrman (2000). In Scheiber and Hager's survey, technical professionals (N = 210, response 50%, 10 questions) reported that the primary objective of their presentations was to inform and instruct; only 18% indicated that they had a persuasive goal. The most important problems in designing and delivering presentations, according to Scheiber and Hager, included "1) attempting to cram too much information into a chosen presentation format within a limited time frame, 2) devoting or allowing insufficient time for preparation and 3) selecting an appropriate organization and structure" (p. 179). Their survey did not cover the rhetorical strategies of American engineers in the introduction or in the rest of their speeches.

response 25%, 130 questions) of Dutch engineers that probed their frequency of and attitude toward speeches. In this research, an oral presentation was defined as a monologue of at least 10 minutes that was directed toward at least three listeners. The results showed not only that engineers quite regularly speak in public within their professional contexts (17 times a year on average) but that their attitudes toward public speaking were quite positive: 86% of the respondents considered public speaking to be an important part of their jobs, and 70% even reported that they enjoyed giving presentations. But the Andeweg et al.'s (2000) study presented a large-scale survey (N = 4,000,

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survey also revealed that most Dutch engineers have little training in giving neers in Scheiber and Hager's (1994) study. The Dutch survey also queried pare those Dutch engineers' responses to the survey questions relating to their introductory style with the results from our analysis. In particular, we compare our results to their responses concerning (a) their attitudes about the introductions to speeches and (b) their own practices during the first minutes of their two last presentations. The results of that survey were grouped on the basis of the exordial model (see Table 1). The engineers from the survey considered designing and presenting an introduction to be vant content), but at the same time, they considered it to be the most the least important task from a list of 12 presentational tasks (e.g., determining the goal of the presentation, structuring the content, choosing releoral presentations, especially in comparison with that of the American engithe engineers about their introductory style. In our present study, we comdifficult task on the list.

(p < .01) less important than *docilem* techniques (4.2). Yet, they did not use attention techniques in only 15.6% of the introductions of their last two presentations. And the most frequent of these attentum techniques—stressing getting techniques in an introduction as significantly more important (3.7 on a 5-point scale; p < .01) than benevolum techniques (3.0) and significantly attention-getting techniques frequently: They reported using one or more The engineers responding to Andeweg et al.'s (2000) survey rated attentionthe importance of the subject—they reported using in only 5% of their last two presentations.

Only one third of the respondents considered benevolum techniques to tions, much more often than they reported using attentum techniques. The most common benevolum techniques they reported using are enhancing be necessary in the introductions of professional presentations. But they reported using benevolum techniques in 35.7% of their last two presentatheir own credibility, enhancing their company's credibility, and introducing participants to each other.

of the three categories of techniques. More than two thirds of the respondents The most frequent kind of docilem technique that they used is narration, in The respondents considered docilem techniques to be the most important (77.4%) reported using a docilem technique in their last two presentations. which the speaker gives a brief history of the subject of the speech. They also used other docilem techniques such as listing the main points and presenting the core of the speech.

In short, the respondents seemed to attach great importance to ensuring that the audience is able to follow the main thrust of the presentation and to situate the subject within its context. They attached less importance to enhancing their own credibility and their company's credibility and rarely used catchy openings to get the audience's attention. They preferred a direct, subject-oriented approach in the introductions of their presentations. In the following section, we describe our corpus and our method of analysis.

The Corpus and Method of Analysis

The communicative techniques that people report using are often quite different from those that they actually use. Van De Mieroop (2005a), for instance, demonstrated this variation by triangulating findings from speakers' general self-evaluations with findings from a perception survey completed by the audience and from discourse analyses. The results of such a triangulation revealed many discrepancies between these three perspectives, which seems fairly logical because "triangulating different perspectives . . . gives access to different versions of the phenomenon that is studied" (Flick, 1992, p. 194). Likewise Veltman, Andeweg, and de Jong (2003) concluded from their research on Dutch government speakers and their speechwriters that the analysis of rhetorical strategies cannot be based only on what speakers say they plan to do or say they have done but should also take into consideration the prepared text and the actual spoken text. Andeweg and De Jong (2004a) showed that obtaining fully written presentations from engineers is difficult (even after repeated e-mail requests). One of the main reasons for this difficulty is that today many professionals use printouts of their slides, which "eliminate the need for additional notes" (Locker & Kaczmarek, 2001, p. 382; see also Farkas, 2006; Yates & Orlikowski, 2007). One rather laborious way to obtain a useful corpus of engineers' speeches is to attend the presentations and record them on tape.

Van De Mieroop (2005a) collected a corpus of 40 speeches given by and 2002. The speeches were given at seminars organized by two Belgian professional associations. The first association was run by and targeted at engineers and was highly active in informing and training its members on new technical issues. The second—in many aspects similar to the first—was targeted at people who work in the supply chain. The topics of these mainly informative speeches ranged from the handling of water sediment in riverbeds and the new liberated energy market in Belgium to newly emerging Dutch-speaking (or Flemish-speaking) Belgian professionals between 2001

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speakers from various external companies and organizations. Dorien Van pathogenetic organisms in the environment and soil sanitation. During each of these seminars, approximately seven speeches were presented by different De Mieroop recorded the 40 speeches during eight seminar days, retaining for analysis only the speeches given by native Dutch speakers.

an average length of 4,580 words. The transcriptions of the audiotape of the way in which a lexical item is pronounced versus the way in which it is (1983), "the data we shall quote from is spoken by co-operative adults who are not exploiting paralinguistic resources against the verbal meanings of The transcription of these 40 speeches resulted in a corpus of more than 180,000 words. This corpus is also the subject of previous discourse analyses Furthermore, the transcriber used modified orthography to "capture roughly written" (Ochs, 1979, p. 61) and added punctuation to facilitate a correct pp. 225-226). In using the transcriptions for this study, we did not take paralinguistic features into consideration because, as in Brown and Yule's study The length of the speeches ranged from 1,487 to 8,975 words, with the speeches incorporated details such as hesitations and reformulations. understanding of the text and the speech (Wetherell & Potter, 1992, their utterances but are, rather, using them to reinforce the meaning" (p. 4). (see Van De Mieroop 2003, 2004, 2005b, 2006a, 2006b, 2007).

from which we learned that their ages ranged from 24 to 58 years (M =most of the speakers prepared their presentations individually (78%). More already given a presentation on this issue). These figures suggest that most The 40 speakers who made these presentations filled out a questionnaire 40.3, Mdn = 38). The vast majority of the speakers were men (90%), and than half of the speakers did not give oral presentations very frequently (54% gave professional speeches less than five times a year), but they were used to speaking about the subject of their current presentation (70% had speakers were selected mainly because of their technical expertise rather than because of their experience with giving speeches.

on average, the introductions accounted for 6.5% of the presentation, with a sentation.1 This average is slightly less than the average recommended length In analyzing the introductions of these presentations, we determined that, minimum length of 0.8% and a maximum length of 25.8% of the entire preof introductions (10%) that we found in the advisory literature.

We labeled the techniques we found in these introductions in terms of For this test, we proceeded as follows: First, one of us divided the speeches into the exordial model (see Table 1). To verify that all three of us applied the exordial model similarly, we tested the interrater reliability for 10 speeches. segments. Second, the rest of us independently categorized the rhetorical

techniques that were used in these particular segments. Finally, we calculated the interrater reliability of the categorization of rhetorical techniques in this test set of 10 speeches. This reliability was acceptable (Cohen's kappa = 0.71; p < .001). We thus concluded that there was sufficient correspondence between our three analyses to safely proceed with categorizing the remaining 30 speech introductions in the corpus. Each of us then analyzed one third of the remaining corpus apiece.

To determine what engineers do in the first minutes of their presentations, we examined the rhetorical techniques in the 40 introductions in our corpus. We identified 261 instances of rhetorical techniques, an average of 6.5 techniques per introduction (range = 3-12). Within this group, we found 35 different kinds of techniques. Then we attributed these techniques to the three exordial functions. In the following subsections, we describe our quantitative results grouped by function and provide a qualitative analysis of the techniques most frequently used. Our intention is to give an overview of the extent to which the techniques are used and to illustrate the ways in which these techniques are inserted into the introductions and how they serve the rhetorical character of the introduction. Our triangulation of quantitative and qualitative analyses reinforces our interpretation of the results because "the flaws of one method are often the strengths of another, and by combining methods, observers can achieve the best of each, while overcoming their unique deficiencies" (Denzin, 1970, p. 309).

Attentum Techniques

stressing the importance of the subject, saying something witty, or asking a Getting the listeners' attention is one of the main goals of a speaker, and during the introduction is perhaps the most suitable time of the presentation to fulfill this task. Therefore, we expect this rhetorical function to be prevalent in the introductions, and our results point in this direction; we identified eight different attentum techniques that were used more than once in the corpus of 40 speeches (see Table 2). Addressing the audience directly proved to be by far the most common technique in the corpus: More than half (62.5%) of the speakers used it. None of the other techniques, such as question, is nearly as widespread in the corpus. Interestingly, we found no anecdotes in the introductions of these 40 speeches. This finding is remarkable because this technique is prevalent in Dutch advisory literature of the

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Percentages of the 40 Speech Introductions in Which Attentum Techniques Were Used Table 2

Attentum techniques	%
A16 Addressing the audience	62.5
A1 Stressing the importance of the subject	30.0
A4 Saying something witty	20.0
A14 Asking a question	20.0
A3 Promising to give a brief speech	12.5
A12 Saying something challenging	10.0
A8 Drawing comparisons or using metaphors	7.5
A13 Quoting someone	5.0

sented in the table. Also, sometimes a particular technique was used more than once in a speech (e.g., saying something witty). This multiple use of one technique was counted as one occurrence. Note: Some attentum techniques only occurred once in the entire corpus, namely, using wordplays, proverbs, riddles, visuals or audio effects, and irony and demanding attention. These are not pre20th century (see Andeweg & De Jong, 2006), which clearly illustrates the discrepancy between theory and practice.

frequently used attentum technique in this corpus, most speakers used this technique in a rather standardized way. The vast majority of the speakers Addressing the audience. Although addressing the audience is the most used stereotypical phrases such as "Goedemorgen dames en heren [Good morning, ladies and gentlemen]."

by less than one third of the speakers (30%). We found two main versions of this technique. In the first version, the speakers merely state that the subject of their speech is important. For example, "Binnen het kader van de ... leefmilieuproblematiek bij Defensie vormt bodemsanering een van de belangrijkste facetten [Within the framework of the ... environmental problems at (the ministry of) Defense, soil sanitation is one of the most important aspects]." In the second version, the speakers highlight the importance of the subject and support their argument. For example, "Toch is het belangrijk da we daar even over nadenken, euh, en voornamelijk omwille van de reden dat daar nogal wat aansprakelijkheidsproblemen mee te maken hebben [Still, it is important Stressing the importance of the subject. The second most common attentum technique in the corpus, stressing the importance of the subject, was used that we think about that, uh, and especially because of the reason that there are quite a lot of liability problems involved]." 198

Saying something witty. One fifth of the speakers (20%) said something witty in their introductions, making this technique the third most common one in the corpus. When using this technique, the speakers usually made one quite general, short, and perhaps improvised remark that seemed aimed at drawing the audience's attention and making them smile. For example, at one seminar, the last speaker of the day started his presentation as follows: "k Heb dus de eer gekregen om hier, euh, deze namiddag het slaapliedje te zingen, euh, al ga ik mij beperken tot spreken want mijn zangtalent is niet uh, but I am going to limit myself to speaking since it is said that my talent for music is not that big]." Although one speaker in the corpus created a relaxed atmosphere in his introduction by inserting seven humorous so groot, het schijnt [I have the honor to, uh, to sing the lullaby this afternoon, remarks, that was clearly an exception to the rule.

Benevolum Techniques

From the perspective of classical rhetoric, improving the audience's goodwill toward the speaker is one of the most elaborated and important functions of speech introductions. But this function receives far less attention in the contemporary advisory literature (Andeweg & De Jong, 2004a). Table 3 gives an overview of the benevolum techniques that we found in more than one speech in this corpus. The speakers used two techniques quite frequently: thanking the person who introduced them and enhancing credibility (i.e., their own, their company's, or both). Furthermore, we found that many speakers pretended to improvise and that they explicitly asked for the audience's understanding for the flaws in the presentation. Thanking the person who introduced you. Like the most frequent attentum technique, addressing the audience, this benevolum technique, thanking the person who introduced you, is also used stereotypically by the speakers. In the vast majority of cases, the speakers just added a polite expression of gratitude by saying, "Dank u, mijnheer de voorzitter [Thank you, Mr. Chairman]." Some speakers used a more informal variant of this phrase, addressing the chairman by his first name (e.g., "Dank u, Bert [Thank you, Bert]"), but half (50%) of all the speakers thanked the person who introduced them. Enhancing credibility. Almost half of the speakers (42.5%) inserted some sort of credibility enhancing technique in their introductions, but these techniques may be oriented quite differently. Some speakers highlighted their personal credibility whereas others focused on enhancing the credibility

Percentages of the 40 Speech Introductions in Which Benevolum Techniques Were Used Journal of Business and Technical Communication Table 3

Benevolum techniques ^a	%
B15 Thanking the person who introduced you	50.0
B1 Enhancing credibility	42.5 ^b
B1c Enhancing your company's credibility	22.5
B1b Enhancing your own and your company's credibility	12.5
B1a Enhancing your own credibility	12.5
B3 Pretending to improvize	27.5
B13 Asking for understanding for the flaws in the presentation	17.5
B16 Stressing what you will not be talking about (praeteritio)	12.5
B2 Praising yourself and those you represent	10.0
B8 Flattering and praising	10.0
B10 Scaring/reassuring the audience	5.0
B9 Stressing collectivity	5.0

because two speakers used two subtechniques separately. In figuring the percentage for B1, a. The technique choosing the underdog position was used only once, so it is not included here. b. The sum of the percentages for B1a, B1b, and B1c does not equal the percentage for B1 however, we counted the speeches in which more than one form of B1 technique was used as just one occurrence, thus reducing the overall percentage.

ibility. Many speakers in some way drew the audience's attention to their of their company or on enhancing both their own and their company's credcompany, as in the following example:

in ons land. Euth, wij hebben dus of baten uit een 8.000 kilometer luchtlijnencountry. Uh, so we have, or we manage about 8,000 kilometers of air cable wires, with 800 high-voltage posts, 20,000 power pylons, so a lot of material.]² bedrijf, is dus pas in juni, eind juni vorig jaar opgericht. Wij beheren het we zullen straks zien dat dat dus verschillend is met de bevoegdheidsverdeling [Maybe, just briefly, (I should) present us ourselves. Uh, X is still a young company, was established only in June, end of June last year. We manage the high voltage net of 380 kV, so 380,000 voltage to 20,000 voltage. Uh, we will see later that that is quite different from the division of jurisdiction in our Misschien even kort toch wel ons ons voorstellen. Euh, X is nog een jong hoogspanningsnet van 380 KV, dus 380.000 volt tot en met 20.000 volt. Euh, kabels, met 800 hoogspanningsposten, 20.000 pylonen, dus heel wat materiaal.

explicitly focusing on the large quantity of material it manages, ranging from In this example, the speaker stresses the importance of his company by

the amount of voltage to the length of wires. By emphasizing such numbers, the speaker positions his company as an important player in its field. Pretending to improvise. More than one fourth (27.5%) of the speakers pretended to improvise at some point in their speech introductions. In a classic rhetorical sense, this technique serves to help a well-prepared speaker to come across as more spontaneous and fluent. But when we studied the examples of this technique in the corpus, we suspected that, instead of pretending, the speakers actually were improvising—or perhaps had just added some because they usually referred to another speaker's words, as in this example: notes to their speech while they were listening to the previous speaker-

Euh, aansluitend op, euh, de uitleg van, euh, meneer X die meer heeft gesproken over de, euh, ex-situ behandeling van baggerspecie ...

[Uh, linking up, uh, to the explanation of, uh, Mister X, who spoke more about the, uh, ex situ treatment of dredgings]

fifth (17.5%) of the speakers asked for understanding for the flaws in their presentation. This technique is known now in the advisory literature as a vitium, or a technique that is explicitly advised against (Andeweg & De Jong, 2004b). The examples we found in this corpus are clumsy ways in which the speakers reacted to the situation. According to the advice literature, these remarks draw attention to the shortcomings of speakers and their presentations instead of the speaker explicitly apologizes for mistakes in his handouts, which he did Asking for understanding for the flaws in the presentation. Less than one divert audiences' attention away from these flaws. In the following example, not have time to correct. Then he further emphasizes his responsibility by repeating his apology:

het aantal foutjes dat er in de tekst zit dat u gekregen heeft want ik heb die niet kunnen contro ... kunnen controleren wegens afwezigheid, dus, euh, Ik zou me dus in de eerste plaats willen verontschuldigen dus voor dus, euh, mijn excuus daarvoor.

In the first place, I wish to apologize for, uh, the number of mistakes that are in the text that you received because I was not able to contr . . . able to control these because of absence, so, uh, my apologies for that.]

Docilem Techniques

duction is to clarify what the speech is about. According to their survey responses, the speakers seemed to agree with his view, ranking docilem According to Aristotle, the most important function of a speech's intro-

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Percentages of the 40 Speech Introductions in Which Docilem Techniques Were Used

Docilem techniques	%
D2 Listing the main points (partitio)	67.5
D4 Naming the subject	32.5
D8 Dealing with the equipment	32.5
D3 Giving a brief previous history (narration)	25.0
D1 Presenting the core of the speech	22.5
D9 Marking the transition to the core of the presentation	10.0
D6 Announcing practicalities	7.5

Note: The techniques starting from a general issue and narrowing down the subject and giving a definition occurred only once, so they are not included here.

Listing the main points, or the partitio, is used by two thirds (67.5%) of the speakers, making it the most frequently used introductory technique of this corpus. This technique exceeds the frequencies of the stereotypically used echniques as the most important of the three techniques. Table 4 gives an overview of the docilem techniques occurring more than once in the corpus. techniques of addressing the audience and thanking the person who introduced you. Other frequently used docilem techniques include naming the subject and dealing with the equipment.

to display the main points of the presentation. Whereas some speakers briefly dealt with these main points in their introduction, limiting themselves to merely reading out loud the words that were written on the overview slide Listing the main points (partitio). Many speakers used an overview slide (see example 1), others devoted considerable time to enumerating the points they would discuss in their presentation (see example 2):

Example 1: En ik heb, euh, de voordracht eigenlijk, euh, (...) ingedeeld, euh, op Europees niveau, Belgisch niveau en Vlaams niveau.

And I have, uh, actually, uh (. . .) divided the presentation in, uh, the European level, the Belgian level and the Flemish level.] Example 2: Mijn voordracht is, euh, ingedeeld in een 4-tal puntjes. Eerst wil parameters die de groei van Legionella beïnvloeden. Ten tweede dan het eigenlijke voorkomingsbeleid, hoe kunnen we die bacterie die van nature toch bijna overal aanwezig is, hoe kunnen we gaan voorkomen dat die uitgroeit tot een ik kort iets, euh, meer vertellen over Legionella, euh, algemeen en wat zijn de concentratie die potentieel gevaarlijk is

[My presentation is, uh, divided into four points. First, I briefly want to, uh, tell something more about Legionella, uh, in general and what the parameters are that influence the growth of Legionella. Second, the actual prevention policy, how can we, that bacteria that is present almost everywhere by nature, how can we prevent it from growing to a concentration that is potentially dangerous...]

Naming the subject. One third of the speakers (32.5%) explicitly mentioned the subject of their speeches, usually within the scope of one sentence. Here is a typical example of how they used this technique:

Nu, in elk geval, het onderwerp van vandaag handelt over de bereiding van proceswater, zoals reeds gezegd.

[Now, anyhow, the subject of today deals with the preparation of soil sanitation, as has been said before.]

Dealing with the equipment. Because speakers in earlier times did not have to contend with the practical challenges posed by modern technology, dealing with the equipment is a contemporary addition to the group of docilem techniques. It belongs in this group because it refers typically to speakers who explain to their audience what they will be showing with the screen equipment or who make sure what they are showing with the equipment is legible for the audience. We found that one third (32.5%) of the speakers in our study mentioned the equipment they were using for their speech. But they only seemed to refer to the equipment when something was wrong with it, thus drawing further attention to their own clumsiness, as in the following example:

Euh, ik ga, (...) excuseer, ik heb te rap geduwd. (...) Ja, sorry, ik ga proberen, sta ik zo uit de weg voor, euh, iedereen want 't is nogal moeilijk om hier te staan maar ik ga proberen....

[Uh, I am going, (...) excuse me, I pushed too quickly. (...) Yes, sorry, I am going to try, am I out of the way like this for, uh, everybody, because it is rather difficult to be standing here, but I am going to try

In this example, the speaker puts a lot of emphasis on his own technical shortcomings. Therefore, the effect of this technique seems quite similar to what the advice literature claims is the effect of the *benevolum* technique of asking for understanding for the flaws in the presentation—that is, to draw attention to the speaker's and the presentation's shortcomings. We could thus argue that such instances of this technique should be added to the list

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of vitia, or negative advice, especially because they underline the speaker's limited technical capacity rather than divert the audience's attention away from it.

Discussion and Conclusion

speaking professionals (most of them engineers): How do they begin their functions (attentum, benevolum, and docilem) do the speakers carry out in their introductions? Our analysis of the 40 presentations in our corpus shows nies more sympathetic (benevolum), and enable the listeners to understand their presentation (docilem). They use benevolum techniques somewhat less frequently than the other two types of techniques. In two thirds of the speech terms it. This finding is greater than what we expected to find on the basis of That survey showed that only 3% of the respondents performed all three rhetorical functions in their speech introductions. Therefore, the results of our presentations in terms of the exordial model that Andeweg and De Jong in their introductions of these presentations, and which of the three rhetorical that the speakers use many different techniques in their introductions and quite often serve the three rhetorical functions: They use techniques that garner the attention of the listeners (attentum), make themselves or their compamaking the introductions rhetorically complete, as the advisory literature analysis would seem to contradict the findings of Weller and Stuiveling The purpose of this study is to describe the exordial behavior of Dutch-(2004a) developed? Or more precisely, what rhetorical techniques do they use introductions in the corpus, the speakers executed all three exordial functions, the results of the earlier survey of Dutch engineers (Andeweg et al., 2000). (1961) and De Bree (1998), that Dutch-speaking engineers lack communication skills. But let us not jump to conclusions too quickly.

Self-Analysis Versus Rhetorical Analysis

Before we continue, we must reiterate the differences between the nature of the data from the survey and the nature of the data from our rhetorical analysis. On the one hand, we have data from a self-analysis conducted by speakers who are not linguistically trained, who seldom write out their presentations completely, and who had to fill out a long questionnaire. On the other hand, we have data from an analysis conducted by trained rhetoricians who exhaustively studied every sentence in the introductions of fully transcribed presentations. Therefore, the speakers were probably not able to

Compared With the Percentage of the Survey Respondents' Last Percentages of the 40 Speech Introductions That Included the Three Rhetorical Functions (Before and After Recalculation) Two Speech Introductions That Included These Functions Table 5

Rhetorical function	% Before recalculation	% After recalculation	Survey %
Attentum (getting attention)	93.0	67.5	15.6
Benevolum (engendering sympathy)	83.0	52.5	35.7
Docilem (enabling understanding)	0.06	87.5	77.4
Presentations that carry out all three functions	0.89	35.0	3.0

addressing the audience (e.g., "Good morning, ladies and gentlemen") and the benevolum technique of thanking the person who introduced you (e.g., "Thank you, Mr. Chairman"). Furthermore, they seldom referred to problemmanagement techniques: the benevolum techniques of asking for understanding or the flaws in the presentation and pretending to improvise, as well as the docilem technique of dealing with the equipment. In short, the speakers understandably did not see these utterances as premeditated rhetorical behavior or techniques. To account for these differences between the results of the survey and those of the rhetorical analysis, we recalculated the frequency of the techniques that we identified in our corpus after we excluded the aforementioned techniques. But the recalculated amount of techniques in the corpus still greatly exceeds the amount of techniques that the survey respondents reported using. Table 5 presents the results of this recalculation exhaustively describe everything they did; for instance, they rarely referred to simple and self-evident techniques such as the attentum technique of and compares them with the survey results from Andeweg et al.'s (2000) study.

As Table 5 shows, the percentage of presentations from the corpus with an introduction that carries out all three functions is reduced by about one third (from 68% to 35%) after recalculation. The docilem function now emerges in the dominant position, which corresponds with the results from the survey. The ratio between the attentum techniques and the benevolum techniques is different when we compare both groups of speakers. The 40 speakers from the corpus are relatively more inclined to try to grab the attention of their listeners than to gain their sympathy whereas the speakers who responded to the survey show a relatively greater inclination to use benevolum techniques than to use attentum ones. We cannot definitely conclude, however, that these

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respondents and those of the Belgian professionals whose speeches make up our corpus because even after our recalculation, the methods of the two are factual differences between the speaking practices of the Dutch survey studies still differ greatly.

A conclusion that we can draw from this study is that the speakers in this ical techniques that supported these functions. These other techniques were usually quite factual, such as the benevolum technique of enhancing the company's credibility, or rather straightforward, such as the attentum technique of stressing the importance of the subject. In short, although we tions, we seldom found introductions that the advisory literature would majority of the speakers focused immediately on the content of the speech driven approach is quite logical. Still, a significant amount of speakers used techniques that served an attentum or benevolum function. They used these techniques most frequently in stereotypical ways, such as by greeting the audience or thanking the chairman. In several cases, they used other rhetorcounted frequent occurrences of rhetorical techniques in these introduccorpus all used some form of rhetoric in their introductions. The greatest by listing the main points of the presentation or by clearly naming its subject. Given the informative nature of the presentations in this corpus, this subjectterm rhetorically elaborated.

Evaluation of the Exordial Model as a Descriptive Tool

classical and modern speech advisors. After conducting this study, we can now evaluate the use of this exordial model, which was developed from Our framework for analyzing these speeches was the exordial model, which enumerates rhetorical techniques that have been recommended by prescriptive advice, as a descriptive tool for analyzing the speaking practices. In evaluating this model, we made three important discoveries.

First, the exordial model sharpened our view of what happened in the first minutes of these presentations. We could reliably categorize the various utterances in those first minutes by using the model. Not only did it enable us to identify the different techniques that the speakers used, but it also helped us to assess the rhetorical function of the specific techniques so that we could draw a bigger picture of the ratio between the attentum, benevolum, and docilem functions.

modern advisors. The speakers used 24 exordial techniques in the speech Second, the model showed us that the speakers in our corpus did not make exhaustive use of the techniques that are recommended by the classical and introductions in our corpus, just under half of the total amount of techniques

that are enumerated in the model. Why they never used these other techniques is an interesting question to consider in further research. We can formulate several hypotheses that may answer this question: For example, some techniques may be out of date and thus no longer compatible with audiences' contemporary expectations, or some techniques may be linked to specific subgenres of speeches, particular settings, or certain sociocultural contexts. These hypotheses demand different research approaches, such as an experimental or an intercultural research design.

Third, when critically scrutinizing our setup, we detected a certain degree of friction between our initial inception of the model, which consisted of prescriptive techniques, and its use as a descriptive tool. In a way, this prescriptive nature implies that the model not only sharpens the focus of the observer but also carries some sort of qualitative, evaluative load. In short, implies that when speakers do not use the three basic exordial functions in the introductions of their presentations, they may not be starting their presentations in the best manner. Three problems arise here. First, the formulaic stressing the importance of the subject, thanking the person who introduced you) leads us to question their effectiveness. Second, the speakers' reasons for using some of the techniques we identified may not correspond to the reasons stated in the advisory literature. For instance, Quintilian, in Institutio Oratoria (IV, 1: 54), recommended the classical exordial technique of pretending to improvise so that speakers could hide their prepared persuasive "tricks." In our corpus, however, the speakers seemed not to be pretending to improvise as a conscious attempt to persuade the audience but instead seemed to be actually improvising last-minute attempts to cope with contextual contingencies, such as responding to an earlier remark made by the audience. Third, some categories of techniques in the model do not stem from recommendations that we found in the classical or modern advisory literature. The category dealing with the equipment, for example, is not so much a technique as it is a form of nonpremeditated behavior that seems common in these times of nonfunctioning laptops and disappearing screen cursors. By observing and labeling this "technique," we were obviously not making a qualitative judgment on whether the speaker was carrying out an the prescriptive basis of the model, which lies in the advisory literature, implementation of several of the techniques (e.g., addressing the audience, exordial function.

In summary, the exordial model helps us to describe speakers' introductory practices more concretely and precisely, but we may profit from further experimental research to determine whether a speaker's choice for a particular opening technique is a sensible one and, on a more fundamental level, whether it is a conscious one, on the basis of premeditated behavior. With this

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further research, we could again link the present descriptive study with the model's prescriptive origin in an attempt to reconcile the model's evaluative nature with its descriptive use.

Pedagogical Implications

functions in their speech introductions. Although a minority of speakers carried out all three functions in their introductions, we found a tendency that tionship. This tendency corresponds with the classical critique that engineers lack communicative skills. To this finding, we could add two other findings et al., 2000). In comparison, professional speakers, such as Dutch ministers dote, problem activating, or ethos enhancing) directly after the introduction Still, audiences listening only to the direct approach (i.e., docilem without to focus more on the docilem function than on the attentum and benevolum could be phrased as First give them the information, then establish a relafrom earlier research. First, engineers do not consider designing and presenting an introduction to be a very important task, and yet they consider it to be the most difficult task on a list of tasks concerning oral presentations (Andeweg (and their speechwriters), value the task of designing an introduction as very experiments suggest that adding exordial techniques (e.g., including an aneccan have effects that are noticeable. Listeners value these techniques differattentum or benevolum) remember less of the speech than they do of the same speech that incorporates the other two techniques as well (Andeweg, De This study shows that these speakers, most of whom are engineers, tended important and not very difficult (Andeweg & De Jong, 2004a). Second, ently, and the effects have largely disappeared at the end of the presentation. Jong, & Hoeken, 1998).

These findings about speakers' exordial practices provide food for thought for those who advise and teach about oral presentations. Here we name four possible pedagogical implications:

- We should teach students that not every beginning is an introduction. Introductions fulfill important functions and must be carefully designed rather than simply improvised by freshmen in the field. Without having a carefully planned introduction, speakers risk making a "cold start": They may hesitate, mumble, and use worn-out phrases in the first minutes of their speech, typically causing the audience to become inattentive, unsympathetic, and puzzled.
- 2. The exordial model may help students to design effective introductions because it reduces a chaos of exordial possibilities to two basic choices: (a) Which of the three functions is most important in a specific presentation (in classical rhetoric, the doxa doctrine [Andeweg & De Jong, 2004a]), and (b) which repertoire of techniques would best fulfill this function?

- 3. We could make engineers more aware of their preference for the *docilem* function and their relative neglect of the *attentum* and *benevolum* functions. Scheiber and Hager (1994) have shown engineers' preference for informative genres, and in our research, we found that engineers tend to see their presenting activities as informative, even when the contextual data clearly show that their activities are, in fact, persuasive (Andeweg & De Jong, 2004a).³ This preference for the *docilem* function may, on the one hand, have good communicative reasons. For example, in the contemporary sociocultural situation in Belgium and the Netherlands, audiences may perceive these *attentum* and *benevolum* techniques as being somewhat contrived for the plainspoken ethos of engineers, so using such techniques may lower the speakers' credibility instead of raising it. On the other hand, Andeweg et al. (1998) have shown the advantages of including the two other functions. This particular issue requires further research to draw well-documented conclusions.
- 4. Advisors need to develop more detailed strategies to change shallow exordial behaviors (e.g., conventional ways of addressing the audience, stereotypical ways of thanking the person who introduced you, and clumsy forms of dealing with the equipment) into more effective performances.

Finally, an introduction that is well designed and elegantly written according to the advisory literature still appears to be a rare commodity. Consequently, when engineers give speeches, they often hurry through the first minutes of the presentation. After straightforwardly addressing their audience, giving a short thanks to the introducing chairman, sometimes rummaging about with their presentational equipment, and perhaps making sober remarks about themselves or their company, they rush through listing the main points on a slide, thus ignoring the warning of the Dutch advisor and nationally well-known speaker Van der Meiden (1991):

There are speakers who hastily run through the introduction, to get to the formulation of the problem as quickly as possible and widely elaborate on that..... You should refrain from this practice. (p. 61)

Notes

1. Andeweg and De Jong (2004a) showed that defining the borders of speech introductions is difficult because speakers are rarely explicit about when they are moving from the introduction to the core of their presentation. To minimize subjectivity, we determined the borders as reliably and consistently as possible. Two of us analyzed each speech, and we each independently set the borders of the introductions according to criteria such as speechmarkers—purpose statements, content structure statements, or formal addresses (e.g., "Ladies and gentlemen")—and topic changes. The agreement between us was 82.5%, a satisfactory result in terms of reliability. We resolved our remaining differences by discussion.

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- We attempted to make this English translation as close as possible to the original Dutch transcript. Such a literal translation sometimes results in odd sentences and poor English.
- 3. Although some may argue that this misconception is a strategically smart one, we found, from our own experience with engineers in training, that engineers tended not to view their presenting activities as being potentially persuasive. This unawareness made them use few attentum and benevolum techniques.

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AN ALL DIGITAL QAM MODULATOR WITH RADIO FREQUENCY OUTPUT

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ABSTRACT

A software defined radio (SDR) terminal promotes programmable realizations of the physical layer functionalities. A lot of research work has been done in applying digital signal processors (DSP) and field programmable gate arrays (FPGA) to implement the baseband functionalities of the physical layer. In this paper, the programmable solutions are extended to the radio frequency (RF) band for the transmitter. Digital pulse width modulation (PWM) technique is used to generate binary signals at radio frequency. A QAM modulator, combined with PWM, is implemented using off the shelf FPGA. The output of this all digital transmitter has a center frequency of 800 MHz.

1. INTRODUCTION

A software defined radio (SDR) is defined as a radio in which the digitization is performed at some stage downstream from the antenna. Then the radio can use flexible and reconfigurable functional blocks for the implementation of digital signal processing algorithms. As technology advances, the digitization might be at, or very close to the antenna, such that almost all the radio functionalities are realized using software using high speed and reprogrammable digital signal processing engine [1].

The current radios consist of a mixture of analog and digital building blocks. The radio frequency (RF) functionalities are most likely being implemented using analog circuits, while the baseband functionalities are more suitable for DSP implementations. Digital front end (DFE) is often used to bridge between radio frequency and baseband processing [1]. The DFEs are normally capable of processing signals with frequencies at about tens of megahertz, often referred to as digital intermediate frequencies (IF). Therefore, there remain significant analog blocks between the RF and digital IF.

Digital RF transceivers are studied to extend the software defined functionalities into the radio frequencies [1]. The focus of this paper is about all digital transmitter technology. The advantages of all digital transmitters are:

- high efficiency power amplification ([2], [3])
- digital combining of signals from multiple channels
- software programmable, or reconfigurable

Using an all digital transmitter, the entire transmitter can be realized using DSP or FPGA, which can take advantage of the rapid performance increase of CMOS technology. Besides its compatibility with SDR's requirement, DSP based RF system can also be made to compensate for the impairments of the RF channel. Therefore digital generation of signals directly at radio frequency has drawn a lot of interests among researchers and engineers.

One of the more traditional methods is described in [3], which uses band-pass delta-sigma modulation to generate binary signals at radio frequency. Binary signaling can be used together with switch mode power amplifiers (PA) to achieve higher efficiency comparing to other types PA technology. This transmitter architecture is shown in Figure 1. The drawback of this architecture is that the band-pass delta-sigma (BPDS) modulator is running at 4 times of the center frequency, which can be several giga-hertz. In order to accommodate such high frequency of operations, custom integrated circuits have to be very carefully designed, which lacks re-programmability.

Another method uses pulse width modulation (PWM) [4] to synthesize binary RF signals digitally. PWM was introduced as an analog modulation long time ago, but has gained popularity recently, especially in the digital audio amplification applications. Class-D audio PA, driven by PWM modulated audio signals, can achieve efficiency above 90%. Delta-sigma type of modulation can also be used in digital PWM, but operates at much lower frequency compared with aforementioned BPDS method. However the delta-sigma loop tends to be more complicated than what is used in BPDS, because of the low over-sampling ratio and the non-linearity associated with PWM.

Both references [3] and [4] only presented simulation and non real-time test results. The test setup uses signal sources computed offline that are stored in pattern generator. In this paper, a real-time system was designed to demonstrate the capabilities of digital generation of RF signals using digital PWM. The rest of this paper will be organized as following. First, the method of generation of binary RF signals is discussed. Next, the different noise shaping behaviors between PWM and traditional DAC are described. This difference will lead to the discussion on our noise-shaping filter design method for the digital RFPWM system. Then the detailed implementation of an all digital transmitter based on digital RFPWM is presented. The final section summarizes the paper and presents conclusions.

2. DIGITAL RFPWM GENERATION

2.1. Digital PWM

Digital pulse width modulation (PWM) was motivated by the digital power amplification technique, by which a digital signal can be converted directly into high power analog signals without intermediate digital to analog converter (DAC) stages [5]. The digital power amplification has gained some popularity in the digital audio applications, due to the increasing interest to develop all digital audio system. In digital PWM, the pulse widths are quantized with respect to a high speed clock. Therefore a simple counter can be used to generate the digital PWM waveform based on the reference high speed clock. The general signal processing blocks consist of a digital PWM system are shown in Figure 2.

- Interpolator. The interpolator increases the sampling frequency of the PCM input to a frequency suitable for performing PWM modulation. In this paper, this frequency is referred to as pulse repetition frequency (PRF).
- Natural Sampler. The natural sampler calculates the naturally sampled signal values based on the uniformly sampled digital signal. It has been shown that naturally sampled signal experiences far less baseband distortion comparing to uniformly sampled signal, when PWM is performed [6].
- Quantization with noise shaping. The quantization is necessary to make the high speed reference clock running at reasonable frequencies implementation purpose. For example, if the original PCM input is 44.1 KHz, a 16 times interpolator will result in the PRF equals to 705.6 KHz. The high speed reference clock needs to have the frequency of 46 GHz if the pulse width is quantized to 16 bits. If only 8 bits are needed to quantize the pulse width, the frequency of the high speed reference clock can be reduced to 180 MHz, therefore makes it much easier to implement using moderate technology. Noise shaping technique, e.g., delta-sigma modulation, can be used to

suppress the baseband noise introduced by quantization.

One can also see that the processing intensive blocks, natural sampler and quantization with noise shaping, have the sampling frequency of PRF. This is the main motivation of this work: the main signal processing algorithms are executed at the lower PRF rather than the RF. In order to accommodate the bandwidth requirement in the QAM modulator in our demonstration, this difference is 100 MHz versus several GHz.

2.2. All Digital RFPWM

The method of an all digital radio frequency pulse width modulation RFPWM was introduced in [4], called quadrature integral noise shaping (INS). INS is an algorithm used in the quantization and noise shaping block. Its main goal is to suppress the noise power in the baseband introduced by the pulse width quantization process. It differs from other algorithm by introducing non-linear terms into the feedback loop. The details of INS are provided in [7]. Without considering the details of the INS algorithm, the quadrature INS can be viewed as two individual PWM modulators for inphase (I) and quadrature (Q) paths of complex signals respectively. These PWM modulations use the same architecture as described in subsection 2.1. The outputs from these PWM are baseband signals that need to be further mixed with digital local oscillator signals to form band-pass signal at RF. If both the baseband PWM signals and the digital local oscillator signals are binary, this mixing operation is nothing more than a simple logic XOR operation. Another method to simplify this mixing operation is to make the inphase LO take these ternary values of {0, +1, 0, -1}, while the quardrature LO taking the values of {-1, 0, +1, 0}, therefore the digital mixer only outputs these values {-Q, +I, +Q, -I} in sequence. When both I and Q are binary PWM signals, the mixer's output will be binary too. In order to make the LO signals have one of these two formats, the sampling frequency needs to be at 4 times of the LO frequency. The signals from two digital mixers are then combined to form the desired signal at the radio frequency, referred to as RFPWM signal in this paper.

For a signal modulated using PWM, the signal information is carried in the width of the pulse. Since pulse width is defined by the duration time from the rising edge to the falling edge, the transition edges should be preserved after the baseband PWM. However there exists 90 degree phase difference between the inphase LO signal and quadrature LO signal, extra attention needs to be paid to ensure that the baseband PWMs are synchronized with their LO signals respectively. Since the sampling rate is set at 4 times of the LO frequency, the 90 degree phase difference is equivalent to one quarter cycle time difference. The baseband PWM waveforms for inphase and quadrature are

constructed differently: there is an intentional quarter cycle difference being introduced to compensate for the phase difference between the inphase LO signal and the quadrature LO singal. The spectrum plots after each processing steps in the RFPWM are illustrated in [4]. Figure 3 shows the timing waveforms of baseband PWMs and RFPWMs. In this figure, the LO signals take the ternary format, and it can be seen that the combined output RFPWM signal is binary. Additionally, both baseband PWMs are synchronized to the rising edges of their LO signals respectively.

The QAM-PWM modulator presented in this paper uses the quadrature PWM architecture, while INS algorithm is not chosen due to its high computational requirement. A non-recursive noise shaping method is used instead [8].

3. NOISE SHAPING IN DIGITAL PWM

Noise shaping has been widely adopted in over-sampled data converters. The purpose of noise shaping is to generate coarsely quantized signals instead of finely quantized signals, while preserving the SNR performance within a limited bandwidth. In the digital PWM system, noise shaping is necessary since the reference clock would be have inhibitly high frequency had the pulse width been finely quantized, e.g., using 16 bits instead of 8 bits when PRF is 705.6 KHz.

The noise shaping filters used in traditional data converters have been well studied, and most methods can be used in the digital PWM as well. But the noise shaping behavior in digital PWM differs from traditional D-to-A converter, due to the non-linear effects introduced by PWM.

A simulation model was created to compare the noise shaping performance between PWM and traditional DAC as shown in Figure 4. The digital PWM and the traditional DAC use the same noise shaping filter and the same quantizer. The noise transfer functions (NTF) used in this simulation are specified by $H(z)=(1-z^{-1})^N$, where N ranges from 1 to 5. This type of noise shaping filter is not optimal as far as the inband noise suppression performance is considered, but it is sufficient to demonstrate the different behaviors between the PWM and traditional DAC. The effects of analog components in the DAC are not included in the simulation, only the all digital noise shaping loop is considered. The following parameters were selected for the simulation

- Frequency of the input single tone signal = 11 KHz
- Baseband bandwidth = 20 KHz
- Sampling frequency = 705.6 KHz
- Input signal level = -6 dBFS
- Ouantization levels = 64

For traditional DAC, the quantization levels indicate the number of bits used in the final DAC, while for PWM, this means the number of high speed clock edges in each pulse cycle. The inband SNR performance from PWM and traditional DAC is summarized in Table 1.

Table 1 Comparison of noise shaping between PWM and DAC

NTF order	PWM SNR (dB)	DAC SNR (dB)
1	63.35	64.03
2	81.03	80.51
3	84.41	92.98
4	73.33	94.51
5	61.34	94.55

It can be seen that the SNR measurements are almost identical between PWM and traditional DAC when the lower order NTFs are used, i.e., N=1 and N=2. When the order of NTF is increased, the SNR trend for PWM differs from traditional DAC:

- 1. The PWM SNR may not be improved as rapidly as traditional DAC when N is increased from 2 to 3
- 2. The PWM SNR deteriorates when N is further increased to 4 and 5

The 2nd observation was pointed out in [5] that the quantization noise might be folded back to the baseband if the gain of the NTF is high at the high frequency. We think the 1st observation can be explained by the non-linearity nature of the PWM modulation. However this non-linearity effect can be neglected if only moderate baseband SNR performance is required. Through this simulation model, we formulated our criteria to design a non-recursive NTF filter used for digital PWM system:

- 1. Minimize the ratio between baseband energy and total energy when the filter's input is white noise.
- The filter coefficients should satisfy minimum phase, 1-norm requirement, and its 1st coefficient should be unity. These conclusions are provided in [8] with details.
- 3. The filter gain at high frequency ($\omega = \pi$) should be limited. This requirement is derived from the above simulation results.

These criteria can then be formulated mathematically as follows. Assume an N-tap FIR filter with coefficients \mathbf{h} , where $\mathbf{h} = \{h_0, h_1, ..., h_{N-1}\}^T$, the baseband energy can be calculated by

$$E_b = \int_0^{\omega_b} \left| H(e^{j\omega}) \right|^2 d\omega = h^T R h \tag{1}$$

wherein \mathbf{R} is a matrix, and

$$r_{m.n} = \begin{cases} \omega_b, m = n \\ \frac{\sin(n-m)\omega_b}{n-m}, m \neq n \end{cases}$$
 (2)

The total energy can be calculated using Parseval's theorem, i.e.,

$$E_t = \sum_{i} \left| h_i \right|^2 \tag{3}$$

Therefore the optimized NTF should try to minimize

$$J = \frac{(E_b)^{\alpha}}{(E_t)^{\beta}} \tag{4}$$

The parameter α and β are used as weighting factors when performing the optimization. The object function should be minimized subject to these conditions:

 The 1-norm of h should be bounded, which is dependent on the number of levels in the quantizer, i.e.,

$$\sum_{i=0}^{N-1} \left| h_i \right| \le q \tag{5}$$

- The filter should be minimum phase, i.e., all the zeros of the filter should be within the unit circle
- The gain at high frequency should be bounded, i.e.

$$\sum_{i=0}^{N-1} (-1)^i h_i \le b \tag{6}$$

The all digital transmitter to be demonstrated is specified to have 10 MHz baseband bandwidth, and the PRF is chosen to be 100 MHz. The center frequency is 800 MHz; therefore the frequency of the high speed reference clock is 3.2 GHz. The prototype implementation uses an 8 tap finite impulse response (FIR) NTF designed using this method.

4. HARDWARE PROTOTYPING AND MEASUREMENTS

As described in section 2.1, the entire signal processing algorithms required by digital PWM is running at the frequency of PRF. The only high speed circuit required is the final PWM waveform generation. Therefore it is feasible to prototype an all digital QAM-PWM modulator on an off the shelf FPGA device.

The architecture of the digital QAM-PWM modulator is shown in Figure 5. Only the block diagram of the inphase path is shown in detail; however the quadrature path should consist of almost identical architectural blocks. The QAM modulator consists of one QAM symbols generator whose symbol rate is 5.057 MHz, one interpolation filter to upsample the sampling rate to 16 times of the symbol rate, and one sample rate converter that converts the sampling rate to the 100 MHz PRF. The details of this QAM modulator are provided in [9]. The digital PWM consists of one natural sampler, one quantization with noise shaping block, and one PWM waveform generator. The natural sampling algorithm [6] consists of only feed-forward datapaths; therefore it can be pipelined fairly easily. The quantization with noise shaping block has feed-back paths, therefore is more difficult to implement even though the PRF is merely 100 MHz. The FIR NTF filter is realized using the transposed struccture, combined with retiming technique and canonic signed digit (CSD) conversion of some coefficients. The mixing between LO signals and all the possible baseband PWM signals were pre-computed and stored in a ROM. This ROM is addressed by the quantization output, i.e., the quantized pulse width. The selected RF PWM waveforms from inphase path and quadrature path will be combined before the high speed serializer generates the 1 bit RF signal.

The FPGA device chosen for the prototype is Xilinx's Virtex2pro: XC2VPX20-FF896, speed grade -7. This FPGA has on chip multi-gigabit transceiver (MGT) which is used as the high speed parallel to serial converter to generate binary signal at 3.2 GHz. In Table 2, the logic resource allocation is broken down for the QAM-PWM modulator implemented on this device.

Table 2 Logic resource allocation for QAM-PWM modulator

Logic Elements	PWM	QAM
REGISTER	787(26.1%)	2221(73.5%)
LUT	2447(47.7%)	1833(35.7%)
MUXCY	2052(67.1%)	1008(32.9%)
XORCY	1958(66.8)	973(33.2%)

The logic elements allocation results are extracted from Synplcity synthesis results. The final place and route tool reports that the entire QAM-PWM design utilizes 18 multipliers (20%), 4 RAM16s (4%), and 3911 slices (39%). The percentage number in the parenthesis is the percentage with respect to the total available resources on this FPGA.

The spectrum and EVM measurements are shown in Figure 6. While the pass-band noise floor is about 45 dB down from the signal, more aggressive noise shaping technique can be used to achieve better pass-band noise performance. However the computation requirement for that case might prevent it being implemented, at least using the off the shelf FPGA device will be very difficult. The EVM measurement is less than 1%, which is almost identical to the EVM measured at the output of QAM [9].

5. SUMMARY

An all digital QAM-PWM modulator is presented in this paper. To the best of the authors' knowledge, this work is the first demonstration of real time digital RF PWM signal synthesis, especially using an off the shelf FPGA device. The fundamental operations for digital PWM are briefly discussed, including natural sampling and quantization with noise shaping. The noise shaping of digital PWM differs from traditional DAC converter based on simulation results; therefore the NTF for digital PWM needs to be designed using additional restrictions. A design method is formulated based on the observation from simulation, and one design example is presented based on our QAM-PWM modulator

requirements. This type of NTF is chosen mainly because of its less computation requirement. The QAM-PWM modulator's architecture and performance measurements are presented at the end.

6. ACKNLEDGEMENT

The authors would like to thank Curtis Williams in Motorola Labs for sharing his experience of using MGT on the Xilinx's FPGA devices.

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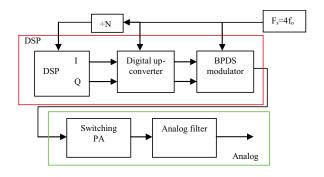


Figure 1 Digital transmitter using BPDS

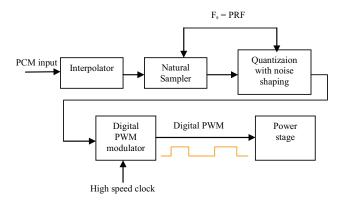


Figure 2 All digital transmitter using PWM

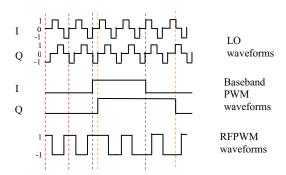


Figure 3 Digital RFPWM timing diagram

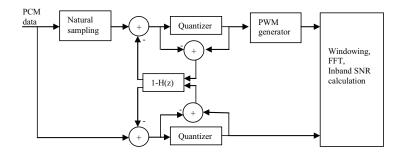


Figure 4 Simulation to compare noise shaping behaviors of PWM and traditional DAC

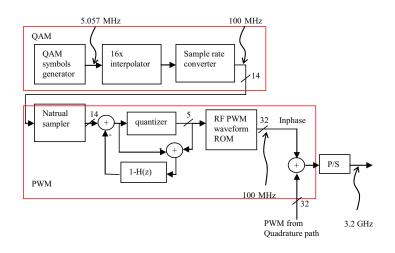


Figure 5 Architectural diagrams for all digital RFPWM prototype

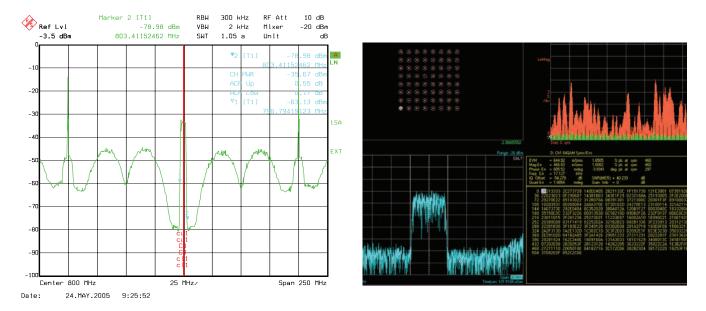


Figure 6 Measurements of RFPWM: wideband spectrum and EVM

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
00.00	27-10-2000			Initial SRS2 release.
01.00	06-06-2001	,		Updated the description of ATDDIEN and PORTAD1 register.
01.10	16-06-2001			Made SRS2 Compliant
V02.00	20 June 2001	20 June 2001		Reworked whole document to make it more user friendly
V02.01	26 July 2001			Added document names Variable definitions and names have been hidden
V02.02	5 Sept 2001	5 Sept 2001		Corrected sampling phase description, other minor corrections
V02.03	8 Nov 2001	8 Nov 2001		Corrected AWAI bit description
V02.04	16 Jan 2002	16 Jan 2002		Syntax corrections
V02.05	8 Mar 2002	8 Mar 2002		Removed document number from all pages except cover sheet
V02.06	11 Apr 2002	11 Apr 2002		Documented special channel conversion in ATDTEST1 register
V02.07	22 Apr 2002	22 Apr 2002		Corrected Table "Available Result Data Formats"
V02.08	16 Aug 2002	16 Aug 2002		FIFOR flag: corrected clearing mechanism B)
V02.09	23 Aug 2002	23 Aug 2002		Detailed AWAI Bit description. Fundional Description: Detailed and corrected Low power modes Table "Available Result Data Formats": Re-corrected
V02.10	21 Feb 2003	21 Feb 2003		Formal corrections on ATDTEST0/1 and ATDDRHx/ATDDRLx register descriptions
V02.11	24 Mar 2005	24 Mar 2005		Corrected PAD7-0 port description
V02.12	28 June 2005	28 June 2005 28 June 2005		Enhanced FIFO bit description

Table 0-1 Revision History

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Section 1 Introduction

1.1 Overview

The ATD_10B8C is an 8-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to device electrical specifications for ATD accuracy.

The block is designed to be upwards compatible with the 68HC11 standard 8-bit A/D converter. In addition, there are new operating modes that are unique to the HC12 design.

1.2 Features

- 8/10 Bit Resolution.
- 7 µsec, 10-Bit Single Conversion Time.
- Sample Buffer Amplifier.
- Programmable Sample Time.
- Left/Right Justified, Signed/Unsigned Result Data.
- External Trigger Control.
- Conversion Completion Interrupt Generation.
- Analog Input Multiplexer for 8 Analog Input Channels.
- Analog/Digital Input Pin Multiplexing.
- 1 to 8 Conversion Sequence Lengths.
- Continuous Conversion Mode. Multiple Channel Scans.

1.3 Modes of Operation

1.3.1 Conversion modes

There is software programmable selection between performing single or continuous conversion on a single channel or multiple channels.

1.3.2 MCU Operating Modes

Stop Mode

standby mode. This aborts any conversion sequence in progress. During recovery from Stop Mode, there must be a minimum delay for the Stop Recovery Time to the before initiating a new ATD Entering Stop Mode causes all clocks to halt and thus the system is placed in a minimum power conversion sequence.

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Wait Mode

Entering Wait Mode the ATD conversion either continues or aborts for low power depending on the logical value of the AWAIT bit.

Freeze Mode

In Freeze Mode the ATD 10B8C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

1.4 Block Diagram

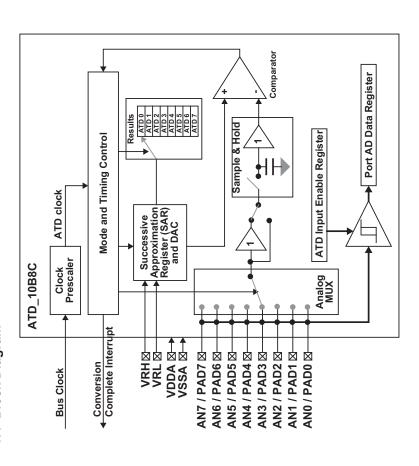


Figure 1-1 ATD_10B8C Block Diagram

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2.1 Overview

The ATD_10B8C has a total of 12 external pins.

2.2 Detailed Signal Descriptions

2.2.1 AN7 / ETRIG / PAD7

This pin serves as the analog input Channel 7. It can be configured to provide an external trigger for the ATD conversion. It can be configured as digital port pin.

2.2.2 AN6 / PAD6

This pin serves as the analog input Channel 6. It can be configured as digital port pin.

2.2.3 AN5 / PAD5

This pin serves as the analog input Channel 5. It can be configured as digital port pin.

2.2.4 AN4 / PAD4

This pin serves as the analog input Channel 4. It can be configured as digital port pin.

2.2.5 AN3 / PAD3

This pin serves as the analog input Channel 3. It can be configured as digital port pin.

2.2.6 AN2 / PAD2

This pin serves as the analog input Channel 2. It can be configured as digital port pin.

2.2.7 AN1 / PAD1

This pin serves as the analog input Channel 1. It can be configured as digital port pin.

2.2.8 AN0 / PAD0

This pin serves as the analog input Channel 0. It can be configured as digital port pin.

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2.2.9 VRH, VRL

VRH is the high reference voltage and VRL is the low reference voltage for ATD conversion.

2.2.10 VDDA, VSSA

These pins are the power supplies for the analog circuitry of the ATD_10B8C block.

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Section 3 Memory Map and Register Definition Freescale Semiconductor, Inc.

3.1 Overview

This section provides a detailed description of all registers accessible in the ATD_10B8C.

3.2 Module Memory Map

Table 3-1 gives an overview on all ATD_10B8C registers.

Table 3-1 Module Memory Map

Address Offset	Use	Access
\$_00	ATD Control Register 0 (ATDCTL0) ¹	ĸ
\$_01	ATD Control Register 1 (ATDCTL1) ²	œ
\$_02	ATD Control Register 2 (ATDCTL2)	R/W
\$_03	ATD Control Register 3 (ATDCTL3)	R/W
\$_04	ATD Control Register 4 (ATDCTL4)	R/W
\$_05	ATD Control Register 5 (ATDCTL5)	R/W
90_\$	ATD Status Register 0 (ATDSTAT0)	R/W
\$_07	Unimplemented	
\$_08	ATD Test Register 0 (ATDTEST0) ³	œ
60 \$	ATD Test Register 1 (ATDTEST1)	R/W
\$_0A	Unimplemented	
\$_0B	ATD Status Register 1 (ATDSTAT1)	ĸ
\$_0C	Unimplemented	
\$_0D	ATD Input Enable Register (ATDDIEN)	R/W
\$_0E	Unimplemented	
\$_0F	Port Data Register (PORTAD)	R
\$_10, \$_11	ATD Result Register 0 (ATDDR0H, ATDDR0L)	R/W
\$_12, \$_13	ATD Result Register 1 (ATDDR1H, ATDDR1L)	R/W
\$_14, \$_15	ATD Result Register 2 (ATDDR2H, ATDDR2L)	R/W
\$_16, \$_17	ATD Result Register 3 (ATDDR3H, ATDDR3L)	R/W
\$_18, \$_19	ATD Result Register 4 (ATDDR4H, ATDDR4L)	R/W
\$_1A, \$_1B	ATD Result Register 5 (ATDDR5H, ATDDR5L)	R/W
\$_1C, \$_1D	ATD Result Register 6 (ATDDR6H, ATDDR6L)	R/W
\$_1E, \$_1F	ATD Result Register 7 (ATDDR7H, ATDDR7L)	R/W

NOTES:

- ATDCTL0 is intended for factory test purposes only.
 ATDCTL1 is intended for factory test purposes only.
 ATDTEST0 is intended for factory test purposes only.

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level. NOTE:

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3.3 Register Descriptions

This section describes in address order all the ATD_10B8C registers and their individual bits.

3.3.1 Reserved Register (ATDCTL0)

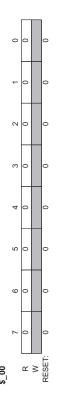


Figure 3-1 Reserved Register (ATDCTL0)

Unimplemented or Reserved

Read: always read \$00 in normal modes

Write: unimplemented in normal modes

3.3.2 Reserved Register (ATDCTL1)

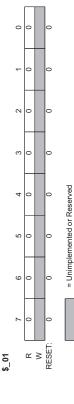


Figure 3-2 Reserved Register (ATDCTL1)

Read: always read \$00 in normal modes

Write: unimplemented in normal modes

NOTE: Writing to this registers when in special modes can alter functionality.

3.3.3 ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

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Figure 3-3 ATD Control Register 2 (ATDCTL2)

Read: anytime

Write: anytime

ADPU — ATD Power Up

consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled. This bit provides on/off control over the ATD_10B8C block allowing reduced MCU power

- 1 = Normal ATD functionality
 - 0 = Power down ATD
- AFFC ATD Fast Flag Clear All
- register will cause the associate CCF flag to clear automatically. 0 = ATD flag cleaning operates normally (read the status register ATDSTAT1 before reading the 1 = Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result
- result register to clear the associate CCF flag)

AWAI — ATD Power Down in Wait Mode

reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires When entering Wait Mode this bit provides on/off control over the ATD_10B8C block allowing a recovery time period after exit from Wait mode.

- 1 = Halt conversion and power down ATD during Wait mode
- After exiting Wait mode with an interrupt conversion will resume. But due to the recovery time the result of this conversion should be ignored.
 - 0 = ATD continues to run in Wait mode

ETRIGLE — External Trigger Level/Edge Control

This bit controls the sensitivity of the external trigger signal. See Table 3-2 for details

ETRIGP — External Trigger Polarity

This bit controls the polarity of the external trigger signal. See Table 3-2 for details.

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Table 3-2 External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	falling edge
0	1	nising edge
1	0	level wol
1	1	high level

ETRIGE — External Trigger Mode Enable

This bit enables the external trigger on ATD channel 7. The external trigger allows to synchronize sample and ATD conversions processes with external events.

- i = Enable external trigger
- 0 = Disable external trigger

The conversion results for the external trigger ATD channel 7 have no meaning while external trigger mode is enabled. NOTE:

ASCIE — ATD Sequence Complete Interrupt Enable

1 = ATD Interrupt will be requested whenever ASCIF=1 is set.

0 = ATD Sequence Complete interrupt requests are disabled.

ASCIF — ATD Sequence Complete Interrupt Flag

If ASCIE=1 the ASCIF flag equals the SCF flag (see 3.3.7), else ASCIF reads zero. Writes have no

- I = ATD sequence complete interrupt pending
 - 0 = No ATD interrupt occurred

3.3.4 ATD Control Register 3 (ATDCTL3)

This register controls the conversion sequence length, FIFO for results registers and behavior in Freeze Mode. Writes to this register will abort current conversion sequence but will not start a new sequence.

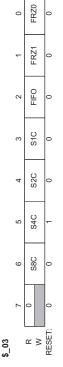


Figure 3-4 ATD Control Register 3 (ATDCTL3)

= Unimplemented or Reserved

Read: anytime

Write: anytime

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S8C, S4C, S2C, S1C — Conversion Sequence Length

These bits control the number of conversions per sequence. **Table 3-3** shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 family.

Table 3-3 Conversion Sequence Length Coding

Number of Conversions per Sequence	80	-	2	3	4	5	9	7	8
S1C	0	-	0	-	0	-	0	-	×
S2C	0	0	1	1	0	0	1	1	×
S4C	0	0	0	0	-	1	1	1	×
S8C	0	0	0	0	0	0	0	0	-

FIFO — Result Register FIFO Mode

If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register, the second result in the second result register, and so on.

If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC2-0 in ATDSTATO) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-0) clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1).

Which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data.

- 1 = Conversion results are placed in consecutive result registers (wrap around at end).
- 0 = Conversion results are placed in the corresponding result register up to the selected sequence length.

FRZ1, FRZ0 — Background Debug Freeze Enable

When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in **Table 3.4**. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

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Table 3-4 ATD Behavior in Freeze Mode (breakpoint)

Continue conversion	Reserved	Finish current conversion, then freeze	Freeze Immediately
0	1	0	-
0	0	1	1
	0 Continue conversion	0 0 Continue conversion 0 1 Reserved	0 Continue conversion 0 1 Reserved 1 0 Finish current conversion, then freeze

3.3.5 ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e.: 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.



1 0	S2 PRS1 PRS0	0
3	PRS3 PRS2	0
4	PRS4	0
2	SMP0	0
9	SMP1	0
7	SRES8	0
	∝ ≥	RESET:

Figure 3-5 ATD Control Register 4 (ATDCTL4)

= Unimplemented or Reserved

Read: anytime

Write: anytime

wine, any mile

SRES8 — A/D Resolution Select

This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits; however, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution.

1 = 8 bit resolution

0 = 10 bit resolution

SMP1, SMP0 — Sample Time Select

These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine's storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. **Table 3-5** lists the lengths available for the second sample phase.

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Table 3-5 Sample Time Select

Length of 2nd phase of sample time	2 A/D conversion clock periods	4 A/D conversion clock periods	8 A/D conversion clock periods	16 A/D conversion clock periods
SMP0	0	1	0	1
SMP1	0	0	1	-

PRS4, PRS3, PRS2, PRS1, PRS0 — ATD Clock Prescaler

These 5 bits are the binary value prescaler value PRS. The ATD conversion clock frequency is calculated as follows:

$$ATDclock = \frac{[BusClock]}{[PRS+1]} \times 0.5$$

Note that the maximum ATD conversion clock frequency is half the Bus Clock. The default (after reset) prescaler value is 5 which results in a default ATD conversion clock frequency that is Bus Clock divided by 12. **Table 3-6** illustrates the divide-by operation and the appropriate range of the Bus Clock.

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Table 3-6 Clock Prescaler Values

Min. Bus Clock ²	1 MHz	2 MHz	3 MHz	4 MHz	5 MHz	6 MHz	7 MHz	8 MHz	9 MHz	10 MHz	11 MHz	12 MHz	13 MHz	14 MHz	15 MHz	16 MHz	17 MHz	18 MHz	19 MHz	20 MHz	21 MHz	22 MHz	23 MHz	24 MHz	25 MHz	26 MHz	27 MHz	28 MHz	29 MHz	30 MHz	31 MHz	32 MHz
Max. Bus Clock ¹	4 MHz	8 MHz	12 MHz	16 MHz	20 MHz	24 MHz	28 MHz	32 MHz	36 MHz	40 MHz	44 MHz	48 MHz	52 MHz	56 MHz	60 MHz	64 MHz	68 MHz	72 MHz	76 MHz	80 MHz	84 MHz	88 MHz	92 MHz	96 MHz	100 MHz	104 MHz	108 MHz	112 MHz	116 MHz	120 MHz	124 MHz	128 MHz
Total Divisor Value	divide by 2	divide by 4	divide by 6	divide by 8	divide by 10	divide by 12	divide by 14	divide by 16	divide by 18	divide by 20	divide by 22	divide by 24	divide by 26	divide by 28	divide by 30	divide by 32	divide by 34	divide by 36	divide by 38	divide by 40	divide by 42	divide by 44	divide by 46	divide by 48	divide by 50	divide by 52	divide by 54	divide by 56	divide by 58	divide by 60	divide by 62	divide by 64
Prescale Value	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101	10110	10111	11000	11001	11010	11011	11100	11101	11110	11111

3.3.6 ATD Control Register 5 (ATDCTL5)

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will about current conversion sequence and start a new conversion sequence.

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^{1.} Maximum ATD conversion clock frequency is 2MHz. The maximum allowed Bus Clock frequency is shown in this column. 2. Minimum ATD conversion clock frequency is 500KHz. The minimum allowed Bus Clock frequency is shown in this column.

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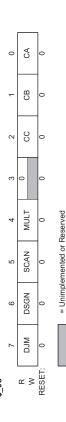


Figure 3-6 ATD Control Register 5 (ATDCTL5)

Read: anytime

Write: anytime

DJM — Result Register Data Justification

This bit controls justification of conversion data in the result registers. See 3.3.13 ATD Conversion Result Registers (ATDDRHx/ATDDRLx) for details.

- 1 = Right justified data in the result registers

0 = Left justified data in the result registers

DSGN — Result Register Data Signed or Unsigned Representation

Signed data is represented as 2's complement. Signed data is not available in right justification. See This bit selects between signed and unsigned conversion data representation in the result registers.

3.3.13 ATD Conversion Result Registers (ATDDRHx/ATDDRLx) for details.

- 1 = Signed data representation in the result registers
- 0 = Unsigned data representation in the result registers

Table 3-7 summarizes the result data formats available and how they are set up using the control bits.

Table 3-8 illustrates the difference between the signed and unsigned, left justified output codes for an input signal range between 0 and 5.12 Volts.

Table 3-7 Available Result Data Formats

MLO

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Table 3-8 Left Justified, Signed and Unsigned ATD Output Codes.

ts _	Signed 8-Bit Codes	Unsigned 8-Bit Codes	Signed 10-Bit Codes	Unsigned 10-Bit Codes
- 1	7F	#	7FC0	FFC0
	7F	出	7F00	FF00
	7E	FE	7E00	FE00
	10	81	0100	8100
	00	80	0000	8000
	£	7F	FF00	7F00
	81	01	8100	0100
	80	00	8000	0000

SCAN — Continuous Conversion Sequence Mode

This bit selects whether conversion sequences are performed continuously or only once.

- 1 = Continuous conversion sequences (scan mode)
 - 0 =Single conversion sequence

MULT — Multi-Channel Sample Mode

When MULT is 0, the ATD sequence controller samples only from the specified analog input channel S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CC, CB, for an entire conversion sequence. The analog channel is selected by channel selection code (control across channels. The number of channels sampled is determined by the sequence length value (S8C, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the bits CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples channel selection code.

- 1 = Sample across several channels
 - 0 =Sample only one channel

CC, CB, CA — Analog Input Channel Select Code

multi-channel scans (MULT=1), this selection code represents the first channel to be examined in the These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. conversion sequence. Subsequent channels are determined by incrementing channel selection code; Table 3-9 lists the coding used to select the various analog input channels. In the case of single channel scans (MULT=0), this selection code specified the channel examined. In the case of selection codes that reach the maximum value wrap around to the minimum value.

Table 3-9 Analog Input Channel Select Coding

Analog Input Channel	ANO	AN1	AN2	AN3	
CA	0	1	0	1	
CB	0	0	1	1	
္ပ	0	0	0	0	

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Freescale Semiconductor, Inc. Table 3-9 Analog Input Channel Select Coding

Analog Input Channel	AN4	AN5	9NP	AN7
CA	0	-	0	-
CB	0	0	1	-
သ	1	1	1	1

3.3.7 ATD Status Register 0 (ATDSTAT0)

This read-only register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

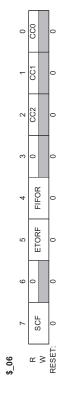


Figure 3-7 ATD Status Register 0 (ATDSTAT0)

= Unimplemented or Reserved

Read: anytime

Write: anytime (No effect on (CC2, CC1, CC0))

SCF — Sequence Complete Flag

This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN=1), the flag is set after each one is completed. This flag is cleared when one of the

following occurs:
A) Write "1" to SCF

B) Write to ATDCTL5 (a new conversion sequence is started)

C) If AFFC=1 and read of a result register

1 = Conversion sequence has completed 0 = Conversion sequence not completed

ETORF — External Trigger Overrun Flag

While in edge trigger mode (ETRIGLE=0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: A) Write "1" to ETORF

B) Write to ATDCTL2, ATDCTL3 or ATDCTL4 (a conversion sequence is aborted)

C) Write to ATDCTL5 (a new conversion sequence is started)

1 = External trigger over run error has occurred

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0 = No External trigger over run error has occurred

FIFOR - FIFO Over Run Flag.

This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been over written before it has been read (i.e. the old data has been lost). This flag is cleared when one of the following occurs:

A) Write "1" to FIFOR

B) Start a new conversion sequence (write to ATDCTL5 or external trigger)

= An over run condition exists

0 = No over run has occurred

CC2, CC1, CC0 — Conversion Counter

These 3 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. E.g. CC2=1, CC1=1, CC0=0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO=0) the conversion counter is initialized to zero at the begin and end of the conversion sequence. If in FIFO mode (FIFO=1) the register counter is not initialized. The conversion counters wraps around when its maximum value is reached.

Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-0) clears the conversion counter even if FIFO=1.

3.3.8 Reserved Register (ATDTEST0)

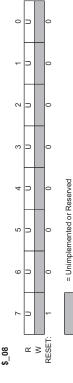


Figure 3-8 Reserved Register (ATDTEST0)

Read: anytime, returns unpredictable values

Write: anytime in special modes, unimplemented in normal modes

OTE: Writing to this registers when in special modes can alter functionality.

3.3.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

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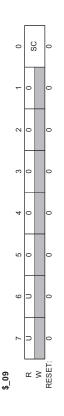


Figure 3-9 ATD Test Register 1 (ATDTEST1)

Unimplemented or Reserved

Read: anytime, returns unpredictable values for Bit7 and Bit6

Write: anytime

SC - Special Channel Conversion Bit

If this bit is set, then special channel conversion can be selected using CC, CB and CA of ATDCTL5

Table 3-10 lists the coding.

1 = Special channel conversions enabled 0 = Special channel conversions disabled Always write remaining bits of ATDTESTI (Bit7 to Bit1) zero when writing SC bit. Not doing so might result in unpredictable ATD behavior. NOTE:

Table 3-10 Special Channel Select Coding

					Г
Analog Input Channel	Reserved	V _{RH}	VRL	(V _{RH} +V _{RL}) / 2	Reserved
CA	×	0	-	0	1
СВ	×	0	0	1	-
သ	0	-	-	1	-
၁ၭ	1	1	-	1	1

3.3.10 ATD Status Register 1 (ATDSTAT1)

This read-only register contains the Conversion Complete Flags.

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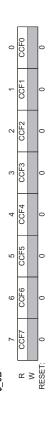


Figure 3-10 ATD Status Register 1 (ATDSTAT1)

= Unimplemented or Reserved

Read: anytime

Write: anytime, no effect

CCFx — Conversion Complete Flag x (x=7,6,5,4,3,2,1,0)

A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags

in result register ATDDR0; CCF1 is set when the second conversion in a sequence is complete and the Therefore, CCF0 is set when the first conversion in a sequence is complete and the result is available result is available in ATDDR1, and so forth. A flag CCFx (x=7,6,5,4,3,2,1,0) is cleared when one of are associated with the conversion position in a sequence (and also the result register number). the following occurs:

A) Write to ATDCTL5 (a new conversion sequence is started)

B) If AFFC=0 and read of ATDSTAT1 followed by read of result register ATDDRx

C) If AFFC=1 and read of result register ATDDRx

 $1 = \text{Conversion number x has completed, result ready in ATDDR}_{x}$

0 =Conversion number x not completed

3.3.11 ATD Input Enable Register (ATDDIEN)

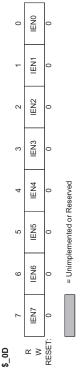


Figure 3-11 ATD Input Enable Register (ATDDIEN)

Read: anytime

IENx — ATD Digital Input Enable on channel x (x=7, 6, 5, 4, 3, 2, 1, 0)

This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register.

1 = Enable digital input buffer to PTADx

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0 = Disable digital input buffer to PTADx

NOTE: Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

3.3.12 Port Data Register (PORTAD)

The digital port pins are shared with the analog A/D inputs AN7-0.

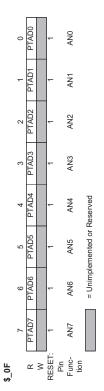


Figure 3-12 Port Data Register (PORTAD)

Read: anytime

Write: anytime, no effect

PTADx — A/D Channel x (ANx) Digital Input (x= 7,6,5,4,3,2,1,0)

If the digital input buffer on the ANx pin is enabled (IENx=1) read returns the logic level on ANx pin (signal potentials not meeting VIL or VIH specifications will have an indeterminate value)).

If the digital input buffers are disabled (IENx=0), read returns a "1".

Reset sets all PORTAD bits to "1".

3.3.13 ATD Conversion Result Registers (ATDDRHx/ATDDRLx)

The A/D conversion results are stored in 8 read-only result registers ATDDRHx/ATDDRLx. The result data is formatted in the result registers based on two criteria. First there is left and right justification; this selection is made using the DJM control bit in ATDCTL5. Second there is signed and unsigned data; this selection is made using the DSGN control bit in ATDCTL5. Signed data is stored in 2's complement format and only exists in left justified format. Signed data selected for right justified format is ignored.

Read: anytime

Write: anytime, no effect in normal modes

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Freescale Semiconductor, Inc. 3.3.13.1 Left Justified Result Data

\$_10 = ATDDR0H, \$_12 = ATDDR1H, \$_14 = ATDDR2H, \$_16 = ATDDR3H \$_18 = ATDDR4H, \$_1A = ATDDR5H, \$_1C = ATDDR6H, \$_1E = ATDDR7H

	10-bit data	8-bit data	
0	BIT 2	BIT 0	0
-	BIT 3	BIT 1	0
2	BIT 4	BIT 2	0
3	BIT 5	BIT 3	0
4	BIT 6	BIT 4	0
2	BIT 7	BIT 5	0
9	BIT 8	BIT 6	0
7	BIT 9 MSB	BIT 7 MSB	0
	œ	>	RESET:

= Unimplemented or Reserved

Figure 3-13 Left Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

\$_11 = ATDDR0L, \$_13 = ATDDR1L, \$_15 = ATDDR2L, \$_17 = ATDDR3L \$_19 = ATDDR4L, \$_18 = ATDDR5L, \$_10 = ATDDR6L, \$_1F = ATDDR7L

	0	0	0	0
	_	0	0	0
	7	0	0	0
, ¢	က	0	0	0
	4	0	0	0
, ,	2	0	0	0
1	9	BIT 0	⊃	0
יייייייייייייייייייייייייייייייייייייי	7	BIT 1	_	0
1		œ	>	RESET

10-bit data

8-bit data

Figure 3-14 Left Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

= Unimplemented or Reserved

3.3.13.2 Right Justified Result Data

\$_10 = ATDDR0H, \$_12 = ATDDR1H, \$_14 = ATDDR2H, \$_16 = ATDDR3H \$_18 = ATDDR4H, \$_1A = ATDDR5H, \$_1C = ATDDR6H, \$_1E = ATDDR7H

	10-bit data	8-bit data	
0	BIT 8	0	0
_	BIT 9 MSB	0	0
2	0	0	0
3	0	0	0
4	0	0	0
2	0	0	0
9	0	0	0
7	0	0	0
	œ	>	RESET:

= Unimplemented or Reserved

Figure 3-15 Right Justified, ATD Conversion Result Register, High Byte (ATDDRxH)

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= Unimplemented or Reserved

Figure 3-16 Right Justified, ATD Conversion Result Register, Low Byte (ATDDRxL)

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Freescale Semiconductor, Inc. Section 4 Functional Description

4.1 General

The ATD_10B8C is structured in an analog and a digital sub-block.

4.2 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies VDDA and VSSA allow to isolate noise of other MCU circuitry from the analog sub-block.

4.2.1 Sample and Hold Machine

The Sample and Hold (S/H) Machine accepts analog signals from the external surroundings and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node. The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics still draw their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of VSSA to VDDA.

4.2.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 8 external analog input channels to the sample and hold

4.2.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

4.2.4 Analog-to-Digital (A/D) Machine

The A/D Machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled notential

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When not converting the A/D machine disables its own clocks. The analog electronics still draws quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.

4.3 Digital Sub-block

This subsection explains some of the digital features in more detail. See register descriptions for all details.

4.3.1 External Trigger Input (ETRIG)

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The input signal (ATD channel 7) is programmable to be edge or level sensitive with polarity control. **Table 4-1** gives a brief description of the different combinations of control bits and their affect on the external trigger function.

Table 4-1 External Trigger Control Bits

			,	
ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
×	×	0	0	Ignores external trigger. Performs one conversion sequence and stops.
×	×	0	-	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	×	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	×	Rising edge triggered. Performs one conversion sequence per trigger.
-	0	1	×	Trigger active low. Performs continuous conversions while trigger is active.
-	1	1	×	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one Bus Clock cycle plus any skew or delay introduced by the trigger circuitry.

NOTE: The conversion results for the external trigger ATD channel 7 have no meaning

while external trigger mode is enabled.

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Once ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

sequence, this does not constitute an overrun; therefore, the flag is not set. If the trigger is left asserted in If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion level mode while a sequence is completing, another sequence will be triggered immediately.

4.3.2 General Purpose Digital Input Port Operation

multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply external input data that can be accessed through the digital port register PORTAD (input-only). The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are

The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog inputs of the ATD_10B8C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

4.3.3 Low Power Modes

The ATD_10B8C can be configured for lower MCU power consumption in 3 different ways:

- Stop Mode: This halts A/D conversion. Exit from Stop mode will resume A/D conversion, But due to the recovery time the result of this conversion should be ignored.
- Wait Mode with AWAI=1: This halts A/D conversion. Exit from Wait mode will resume A/D conversion, but due to the recovery time the result of this conversion should be ignored.
- Writing ADPU=0 (Note that all ATD registers remain accessible.): This aborts any A/D conversion in progress.

Note that the reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

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Section 5 Resets

5.1 General

At reset the ATD_10B8C is in a power down state. The reset state of each individual bit is listed within the Register Description section (see **Section 3 Memory Map and Register Definition**) which details the registers and their bit-field.

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6.1 General

The interrupt requested by the ATD_10B8C is listed in **Table 6-1**. Refer to MCU specification for related vector address and priority.

Table 6-1 ATD_10B8C Interrupt Vectors

Local Enable	ASCIE in ATDCTL2
CCR Mask	l bit
Interrupt Source	Sequence Complete Interrupt

See register descriptions for further details.

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Microcontroller Power Management

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Note

and suggestions for improvements. Distribution of this memo is unlimited. This memo is in full This memo documents a part of TinyOS for the TinyOS Community, and requests discussion compliance with TEP 1.

Abstract

This memo documents how TinyOS manages the lower power state of a microcontroller.

1. Introduction

Microcontrollers often have several power states, with varying power draws, wakeup latencies, and peripheral support. The microcontroller should always be in the lowest possible power state that can satisfy application requirements. Determining this state accurately requires knowing a great deal about the power state of many handles an interrupt, it moves from a low power state to an active state, and whenever the TinyOS scheduler mechanisms to decide what low power state it puts a microcontroller into: status and control registers, a dirty bit, and a power state override. This memo documents these mechanisms and how they work, as well as the subsystems and their peripherals. Additionally, state transitions are common. Every time a microcontroller finds the task queue empty it returns the microcontroller to a low power state. TinyOS 2.x uses three basics of subsystem power management.

2. Background

CPU and main system clock, to LPM4, which disables the CPU, all clocks, and the oscillator, expecting to be woken by an external interrupt source. The power draws of these low power modes can differ by a factor of instructions) and five low-power modes. The low power modes range from LPM0, which disables only the 550 or more (75 uA for LPM0 at 3V, 0.2 uA for LPM4). Correctly choosing the right microcontroller low The TinyOS scheduler[2] puts a processor into a sleep state when the task queue is empty. However, processors can have a spectrum of power states. For example, the MSP430 has one active mode (issuing power state can greatly increase system lifetime.

approaches. The mica platforms, for example, have a component named HPLPowerManagement, which has a compute the low power state based on the configuration of its various control and status registers, storing the the control register to decide exactly which power state to go into. In contrast, MSP430 based platforms such result in the Atmega128's MCU control register. When TinyOS tells the microcontroller to go to sleep, it uses commands for enabling and disabling low power modes, as well as a command (adjustPower()) to tell it to TinyOS 1.x platforms manage MCU power in several different ways, but there are commonalities in the as Telos and eyes compute the low power state every time the scheduler tells the system to go to sleep.

simpler, in that the system will always enter the right power state without any external prompting. However, it is correspondingly costly, introducing 40-60 cycles of overhead to every interrupt that wakes the system up, calculates the low power state when told to. However, this leaves the decision of when to calculate the low Each of the two approaches has benefits and drawbacks. The 1.x mica approach is efficient, in that it only hardware abstraction architecture in 1.x exacerbates this problem. In contrast, the MSP430 approach is power state to other components, which is an easy way to introduce bugs. The lack of a well-defined which can be a bottleneck on the rate at which the system can handle interrupts.

control and status registers. For example, the MSP430 defaults to low power mode 3 (LPM3) unless it detects perspective of what peripherals and subsystems might wake the node up or must continue operating while the way to give the TinyOS microcontroller power manager information on their requirements, which it considers (the basis of platforms such as the imote2) can have power states with wakeup latencies as large as 5ms. For that Timer A, the USARTs, or the ADC is active, in which case it uses low power mode 1 (LPM1). From the microcontrollers, such as the Atmega128 and MSP430, more powerful processors, such as the Xscale family some application domains, this latency could be a serious issue. Higher level components therefore need a MCU sleeps, this is true. However, power modes introduce wakeup latency, a factor which could be of Both of these approaches assume that TinyOS can determine the correct low power state by examining interest to higher-level components. While wakeup latency is not a significant issue on very low power when calculating the right low power state.

3. Microcontroller Power Management

TinyOS 2.x uses three basic mechanisms to manage and control microcontroller power states: a dirty bit, a chip-specific low power state calculation function, and a power state override function. The dirty bit tells TinyOS when it needs to calculate a new low power state, the function performs the calculation, and the override allows higher level components to introduce additional requirements, if needed.

and Tasks[2]. This loop is called from the boot sequence, which is described in TEP 107: Boot Sequence[3]. These three mechanisms all operate in the TinyOS core scheduling loop, described in TEP 106: Schedulers The command in question is Scheduler .taskLoop (), when microcontroller sleeping is enabled.

If this command is called when the task queue is empty, the TinyOS scheduler puts the microcontroller to sleep. It does so through the McuSleep interface:

```
async command void sleep();
interface McuSleep {
```

This command deprecates the __nesc_atomic_sleep() call of TinyOS 1.x. Note that, as the 1.x call suggests, putting the microcontroller to sleep MUST have certain atomicity properties. The command is called the system handles an interrupt after it re-enables interrupts but before it sleeps: the interrupt may post a task, from within an atomic section, and MUST atomically re-enable interrupts and go to sleep. An issue arises if MGUSleep.sleep() puts the microcontroller into a low power sleep state, to be woken by an interrupt but the task will not be run until the microcontroller wakes up from sleep.

Microcontrollers generally have hardware mechanisms to support this requirement. For example, on the Atmega128, the sei instruction does not re-enable interrupts until two cycles after it is issued (so the sequence sei sleep runs atomically).

automatically wire it to the scheduler implementation. McuSleepC is a chip- or platform-specific component, A component named McuSleepC provides the McuSleep interface, and TinySchedulerC MUST whose signature MUST include the following interfaces:

```
async command mcu_power_t lowestState();
                                                             provides interface PowerState;
                                                                                          uses interface PowerOverride;
                                provides interface McuSleep;
                                                                                                                                                                                                                async command void update();
                                                                                                                                                                                                                                                                                                             interface McuPowerOverride
                                                                                                                                                                                     interface McuPowerState {
component McuSleepC {
```

McuSleepC MAY have additional interfaces.

3.1 The Dirty Bit

the microcontroller, it MUST call McuPowerState.update(). This is the first power management mechanism, a dirty bit. If McuPowerState.update() is called, then McuSleepC MUST recompute the low power state before component changes an aspect of hardware configuration that might change the possible low power state of Whenever a Hardware Presentation Layer (HPL, see TEP 2: Hardware Abstraction Architecture[1]) the next time it goes to sleep as a result of McuSleep.sleep() being called.

3.2 Low Power State Calculation

McuSleepC is responsible for calculating the lowest power state that it can safely put the microcontroller into perform this calculation: it is an inherently atomic calculation, and so if performed very often (e.g., on every without disrupting the operation of TinyOS subsystems. McuSleepC SHOULD minimize how often it must interrupt) can introduce significant overhead and jitter.

MCU power states MUST be represented as an enum in the standard chip implementation header file. This file MUST also define a type mou_power_t and a combine function that given two power state values returns one that provides the union of their functionality.

For example, consider a hypothetical microcontroller with three low power states, (LPM0, LPM1, LPM2) and two hardware resources such as clocks (HR0, HR1). In LPM0, both HR0 and HR1 are active. In LPM1, HR0 is inactive but HR1 is active. In LPM2, both HR0 and HR1 are inactive. The following table describes the results of a proper combine function (essentially a MAX):

	LPM0	LPM1	LPM2	
LPM0	LPM0	LPM0	LPM0	
LPM1	LPM0	LPM1	LPM1	
LPM2	LPM0	LPM1	LPM2	

In contrast, if in LPM2, HR0 is active but HR1 is inactive, the combine function would look like this:

LP	LPM0	LPM1	LPM2
LPM0 LP	LPM0	LPM0	LPM0
LPM1 LP	LPM0	LPM1	LPM0
LPM2 LPM0	M0	LPM0	LPM2

3.3 Power State Override

When McuSleepC computes the best low power state, it MUST call PowerOverride.lowestState(). McuSleepC SHOULD have a default implementation of this command, which returns the lowest power state the MCU is capable of. The return value of this command is a mcu_power_t. McuSleepC MUST respect the requirements of the return of this call and combine it properly with the low power state it computes

longer than twenty or thirty cycles; implementations SHOULD be a simple return of a cached variable. Wiring SHOULD be used sparingly, if at all. Because it is called in an atomic section during the core scheduling loop, implementations of PowerOverride.lowestState() SHOULD be an efficient function, and SHOULD NOT be arbitrarily to this command is an easy way to cause TinyOS to behave badly. The presence of a combine function for mcu_power_t means that this command can have fan-out calls. requirements that cannot be captured in hardware status and configuration registers, such as a maximum tolerable wakeup latency. Because it can overrides all of the MCU power conservation mechanisms, it The PowerOverride functionality exists in case higher-level components have some knowledge or

Section 5 describes one example use of McuPowerOverride, in the timer stack for the Atmega128 microcontroller family.

4. Peripherals and Subsystems

AsyncStdControl. These interfaces are imperative in that when any component calls stop on another At the HIL level, TinyOS subsystems generally have a simple, imperative power management interface. component, it causes the subsystem that component represents to enter an inactive, low-power state. Depending on the latencies involved, this interface is either StdControl, SplitControl, or

subsystem will be notified of a significant change and act appropriately when the system next goes to sleep. TEP 115[5] describes the power management of non-virtualized devices in greater detail, and TEP 108[4] From the perspective of MCU power management, this transition causes a change in status and control registers (e.g., a clock is disabled). Following the requirements in 3.1, the MCU power management

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describes how TinyOS can automatically include power management into shared non-virtualized devices.

5. Implementation

Microcontroller Power Management

An implementation of McuSleepC can be found in tinyos-2.x/tos/chips/atm128, tinyos-2.x/tos/chips/msp430, and tinyos-2.x/tos/chips/px27ax.

tinyos-2.x/tos/chips/atml28/timer/HplAtml28TimerOAsyncP.nc, and tinyos-2.x/tos/chips/atml28/timer/HplAtml28TimerOAsyncC.nc automatically wires it to McuSleepC if it is included. An example of a use of McuPowerOverride can be found in the atmega 128 timer system. Because some low-power states have much longer wakeup latencies than others, the timer system does not allow long latencies if it has a timer that is going to fire soon. The implementation can be found in

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6. Citations

- TEP 2: Hardware Abstraction Architecture Ξ
- TEP 106: Schedulers and Tasks. [2]
- TEP 107: TinyOS 2.x Boot Sequence. [3]
- TEP 108: Resource Arbitration 4
- TEP 115: Power Management of Non-Virtualised Devices [5]

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