IIIT BANGALORE

VLS 502

Analog CMOS VLSI Design

Project Report

Submitted By:-

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Submitted To:-

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1. Specifications

In this project, we have developed an LDO designed to operate under various conditions. The design includes both externally compensated and internally compensated configurations. We have explored multiple technology nodes for this purpose. Specifically, the figure below showcases the design using the 45nm technology node, with the corresponding technology node file attached. Our objective is to optimize the LDO to handle both maximum and minimum load conditions effectively.

For externally Compensated we have the following specifications:-

Table 1: Specifications Table

Parameter	**Value**	**Comments**
V_{in}	1.4 V	-
V_{out}	1 V	Relaxed
PSRR	60 dB	Aggressive
$I_{load,\ max}$	2 mA	Moderate
C_{load}	1 F	Aggressive
$I_{quiescent}$	50 A	Moderate

For internally compensated we have the following specifications:-

Table 2: Specifications Table

Parameter	**Value**	**Units**	**Comments**
Vin	1.4	V	-
Vout	1	V	Relaxed
PSRR	50	dB	Aggressive
Iload—min	2	mA	-
Iload—max	10	mA	Moderate
Cload	2	nF	Aggressive
Load Slew Rate	50	mA/s	Aggressive
Transient Spread	15	% of Vout peak-to-peak	Relaxed
Iquiescent	50	A	Moderate
Transient Duration	1	s	Moderate

2. Purpose of an LDO

An LDO is a type of linear regulator, which can regulate output voltages to values very close to the supplied input voltage. The input to output differential voltage, at which the LDO fails to regulate the output is defined as the dropout voltage. The structure of a generic LDO is provided in the block diagram shown in Figure 1. An LDO consists of an error amplifier (EA), an NMOS or PMOS pass transistor (PT) and a resistor divider forming a negative feedback loop. The EA is fed with a constant reference voltage (Vref) by a bandgap circuit and in turn controls the PT through the feedback loop and the resistor divider circuit. The EA tracks the error between the output and Vref and accordingly regulates the gate voltage of PT. The PT acts as a variable resistor and adjusts the output current to further control the output voltage at the desired level.

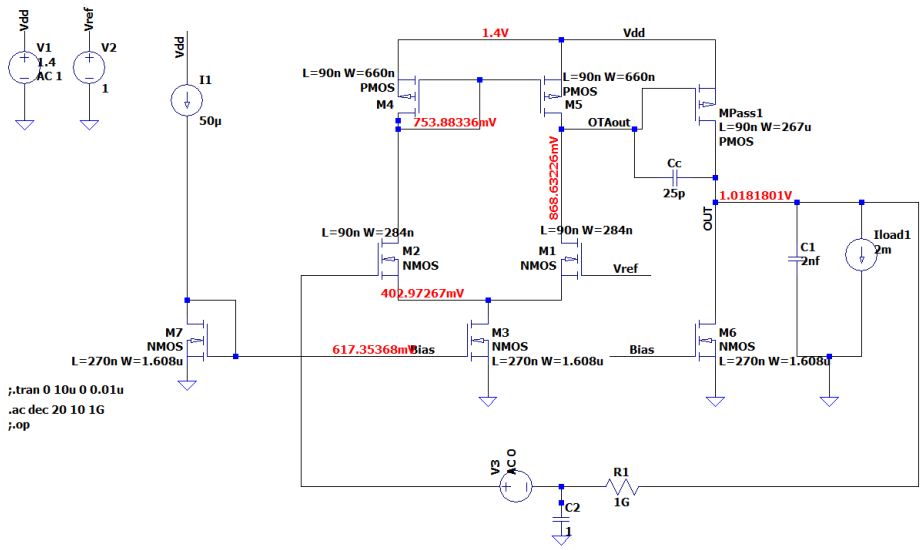

Figure 1: Our LDO schematic

3. Relevance of Techplots

We Include all techplots generated after Python postprocessing, there are 5 takeaways, and we share a schematic of how these techplots were obtained.

- **Github Link**: https://github.com/spcjjp

  Technology node : 45 nm

- f_T improves with shorter channel lengths, making circuits faster with scaling.
- Comparison of different FOMs at different lengths

Length (nm)	gmro	Id/w	ft (GHz)
45	7	170	180
67.5	30	120	100
225	135	40	10

Table 3: Comparison of different FOM at different lengths for NMOS

- We chose the Vds to be 0.4 mV, and we expect that to result in some error because the Vds across every MOSFET might not be the same after sizing the circuit under a particular load. It is very possible that the Vds across the MOSFETs can change under different values of load current. The above phenomenon can be understood from the output log files mentioned below.

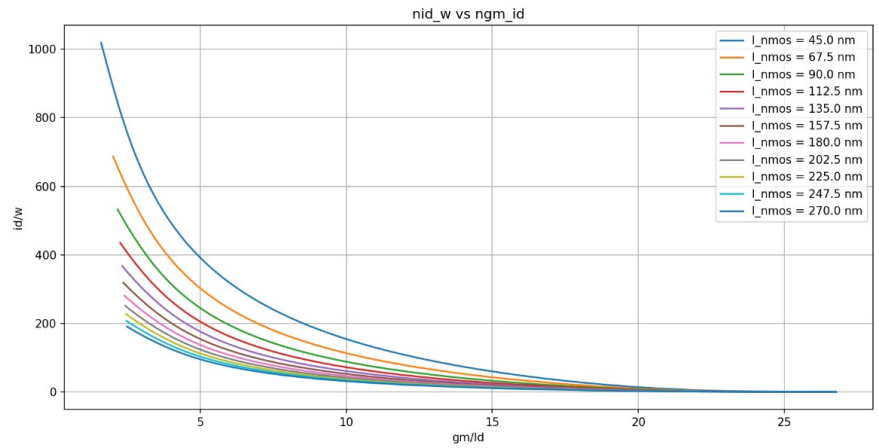

Figure 2: NMOS Techplots after Python postprocessing - Id/W

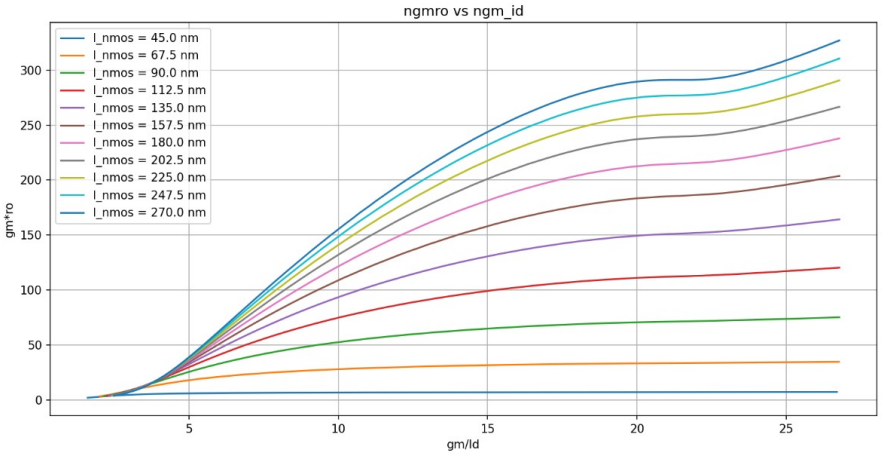

Figure 3: NMOS Techplots after Python postprocessing - gmro

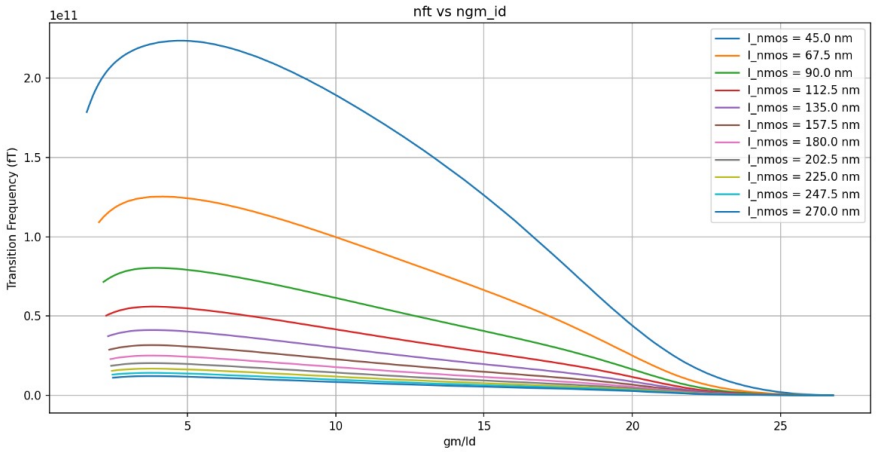

Figure 4: NMOS Techplots after Python postprocessing - fT

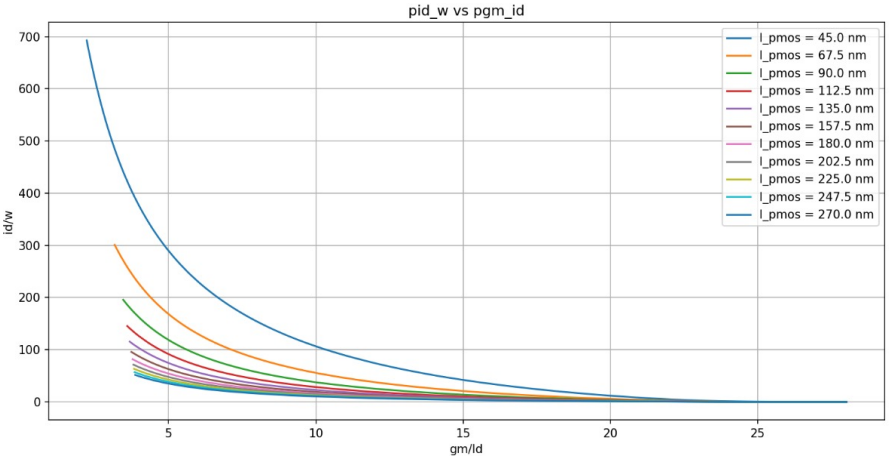

Figure 5: PMOS Techplots after Python postprocessing - Id/W

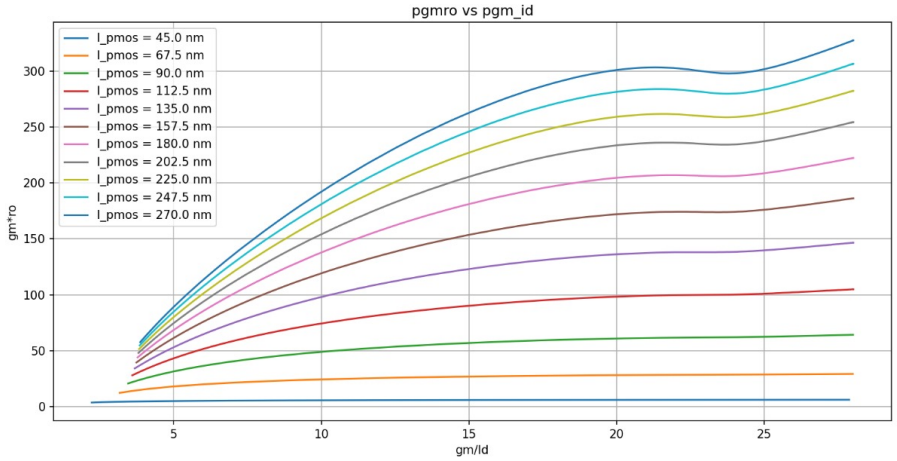

Figure 6: PMOS Techplots after Python postprocessing - gmro

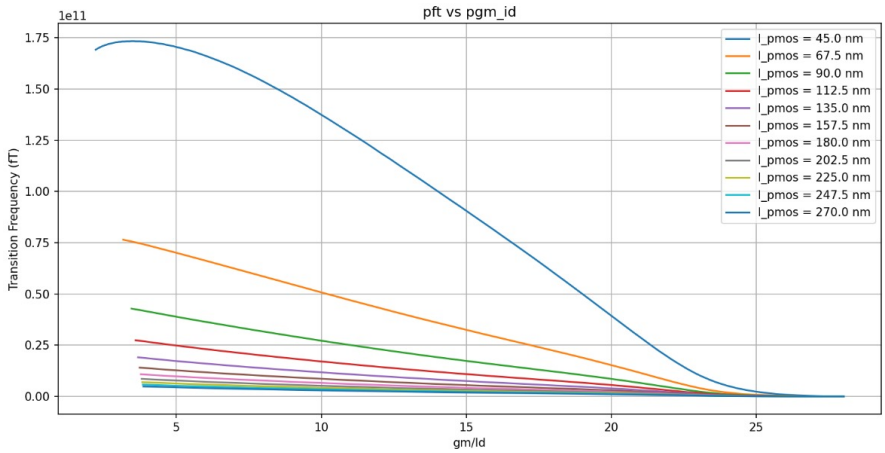

Figure 7: PMOS Techplots after Python postprocessing - fT

4. FET Sizes

We are providing the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 4: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	0.267m/90n	10	48.75	37.5	27.2 GHz
Diff-Amp pmos	660n/90n	10	41.01	37.5	27.2 GHz
Diff-Amp nmos	284n/90n	10	41.01	88	61 GHz
Current Mirror nmos	1.608u/270n	10	155	154	8.38 GHz

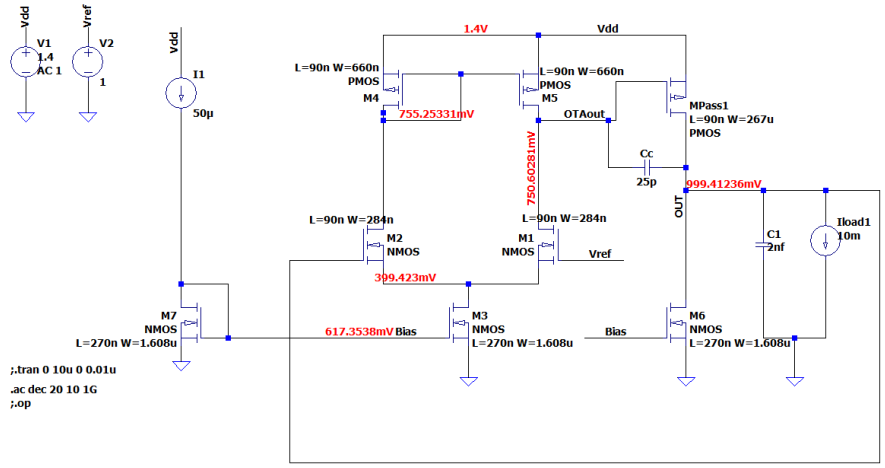

Figure 8: FET sizes and characteristics.

5. Stability Analysis

For Heavy load we get the following curve:

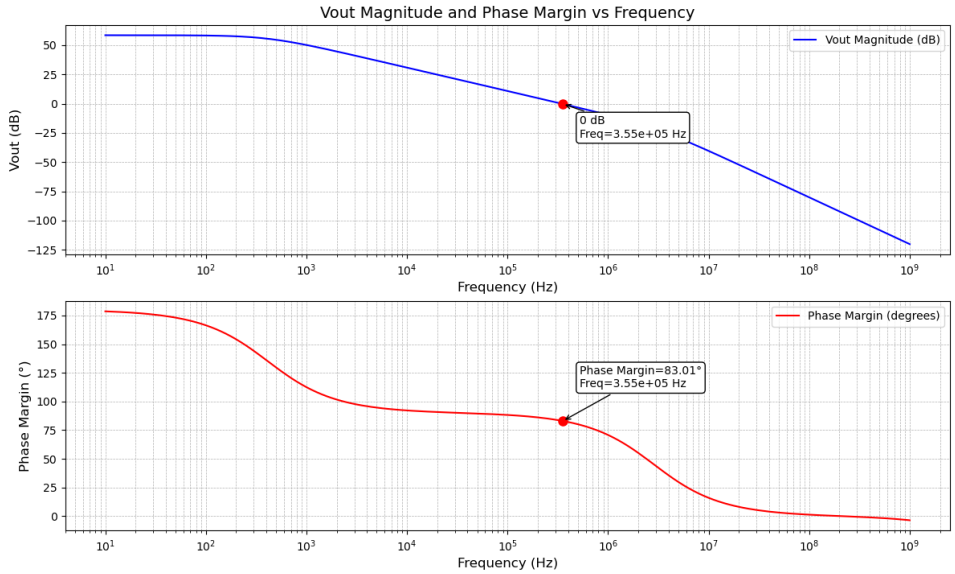

Figure 9: Output on Python

For Light load we get the following curve

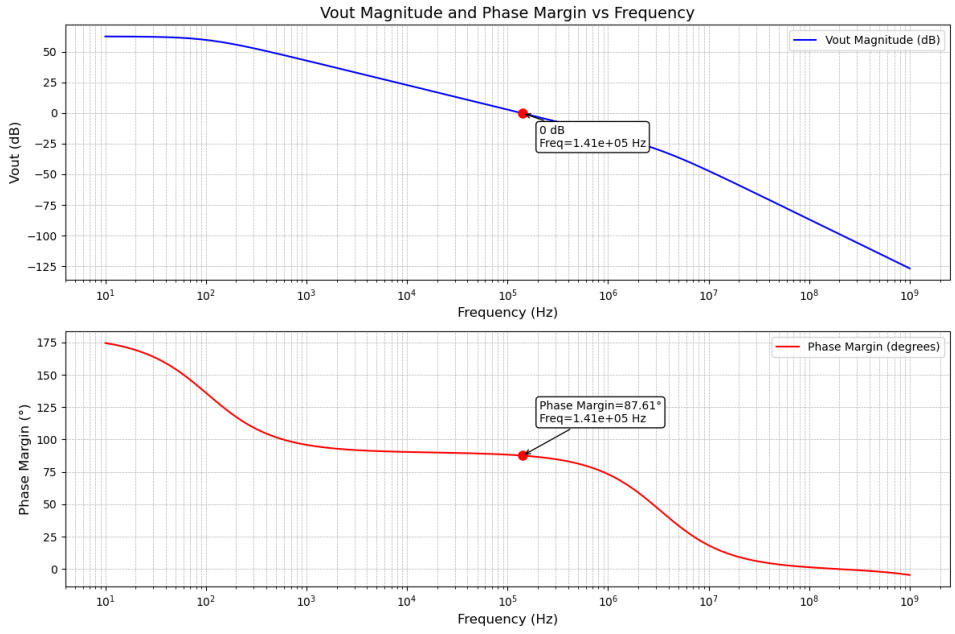

Figure 10: Output on Python

From the above analysis, we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. We can also observe a lesser phase margin of 76 degrees for the heavy load case than that of the light load case. From this analysis, we can say that when we apply light load, we get a more stable system.

Table 5: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	58.5	61.02
Unity Gain Bandwidth (kHz)	342.992	137
Phase Margin (degrees)	83.23	87.67
Pole 1 (Hz)	414.634	103.8
Pole 2 (MHz)	2.87	3.32

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at it's output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as PSRR = 20log(vout/vin), where vout and vin refer to magnitudes of input and output ripples. In Figure 12, the PSRR of LDO is divided into two distinct regions (region 1 and region 2).Region 1 covers the low and mid frequency range till the regulator bandwidth frequency (reg), where PSRR primarily depends on the loop gain (LG) of the regulator. Region 2 starts after reg, where PSRR is independent of LG and is dominated by output parasitics, PCB impedance, etc.

7. PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

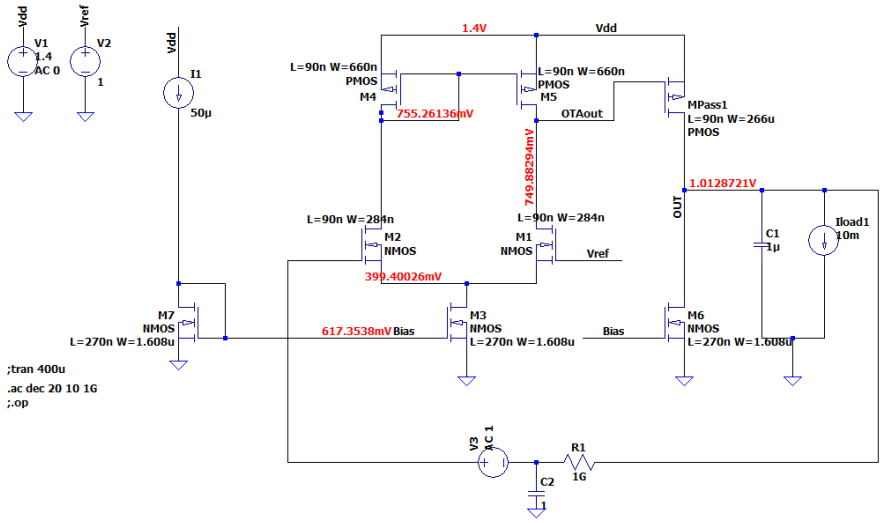

Figure 11: Schematic

Explanation of the artifact used:-

In order to calculate the loop gain we have given a RC circuit in the feedback loop alongwith a AC source with amplitude 1 (as we want to maintain an AC voltage of 1V) at the output. At the same time we also need to bias the circuit and provide a dc voltage to the gate of the nmos in the differential amplifier and for this we are giving the RC circuit which will prevent the flow of dc current to ground but will send any AC signal at the output to ground at high frequency. Also the drop across the resistor will be very less as we have given a very high resistance with very negligible current (since current going into the gate of the mosfet is zero). Thus we will bias the circuit and also calculate the loop gain.

Output Log File:-

```
Semiconductor Device Operating Points:
                          --- BSIM4 MOSFETS ---
Name:       m1          m2          m3          m6          m7
Model:     nmos        nmos        nmos        nmos        nmos
Id:      2.48e-05    2.47e-05    4.94e-05    5.08e-05    5.00e-05
Vgs:     6.01e-01    6.00e-01    6.17e-01    6.17e-01    6.17e-01
Vds:     3.50e-01    3.56e-01    3.99e-01    1.01e+00    6.17e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:     4.66e-01    4.66e-01    4.69e-01    4.69e-01    4.69e-01
Vdsat:   1.43e-01    1.42e-01    1.61e-01    1.61e-01    1.61e-01
Gm:      2.44e-04    2.44e-04    4.95e-04    5.09e-04    5.01e-04
Gds:     5.16e-06    5.08e-06    3.19e-06    2.12e-06    2.29e-06
Gmb      5.63e-05    5.62e-05    1.16e-04    1.19e-04    1.18e-04
Cbd:     1.29e-16    1.28e-16    7.20e-16    6.38e-16    6.86e-16
Cbs:     2.27e-16    2.27e-16    1.29e-15    1.29e-15    1.29e-15

Name:       m4          m5        mpass1
Model:     pmos        pmos        pmos
Id:     -2.47e-05   -2.47e-05   -1.01e-02
Vgs:    -6.45e-01   -6.45e-01   -6.50e-01
Vds:    -6.45e-01   -6.50e-01   -3.87e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00
Vth:    -4.84e-01   -4.84e-01   -4.87e-01
Vdsat:  -1.76e-01   -1.76e-01   -1.78e-01
Gm:      2.46e-04    2.46e-04    9.88e-02
Gds:     4.95e-06    4.95e-06    2.52e-03
Gmb      5.20e-05    5.21e-05    2.09e-02
Cbd:     2.80e-16    2.80e-16    1.19e-13
Cbs:     5.28e-16    5.28e-16    2.13e-13
```

Figure 12: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	**Type**	V_{ds} **(V)**	V_{gs}/V_{sg} **(V)**	V_t **(V)**	$V_{gs}/V_{sg} - V_t$ **(V)**	**Operating Region**
M1	PMOS	0.651	0.651	0.489	0.162	Saturation
M2	PMOS	0.64	0.651	0.489	0.162	Saturation
M3	PMOS	0.367	0.64	0.481	0.159	Saturation
M4	NMOS	0.734	0.734	0.4	0.334	Saturation
M5	NMOS	0.368	0.609	0.468	0.141	Saturation
M6	NMOS	0.358	0.609	0.468	0.141	Saturation
M7	NMOS	0.391	0.734	0.468	0.266	Saturation
M8	NMOS	1.03	0.734	0.466	0.268	Saturation

Table 6: Transistor Parameters and Operating Regions

Output on Python:-

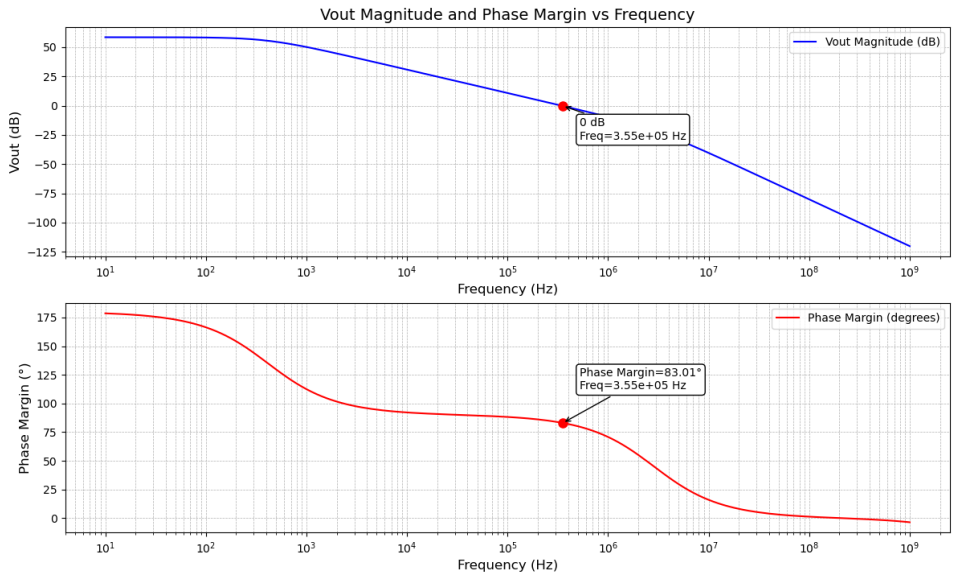

Figure 13: Output on Python

Phase margin

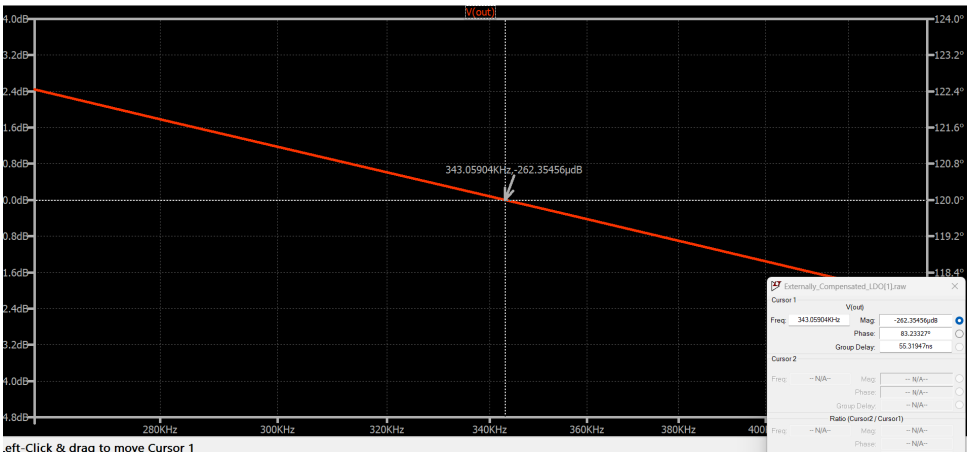

Figure 14: Phase margin

The phase margin is 76.77

The output voltage (Loop gain) comes out to be close to 58.3db . The formula for loop gain is Adiff Apass where Adiff is differential amplifier gain and Apass is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

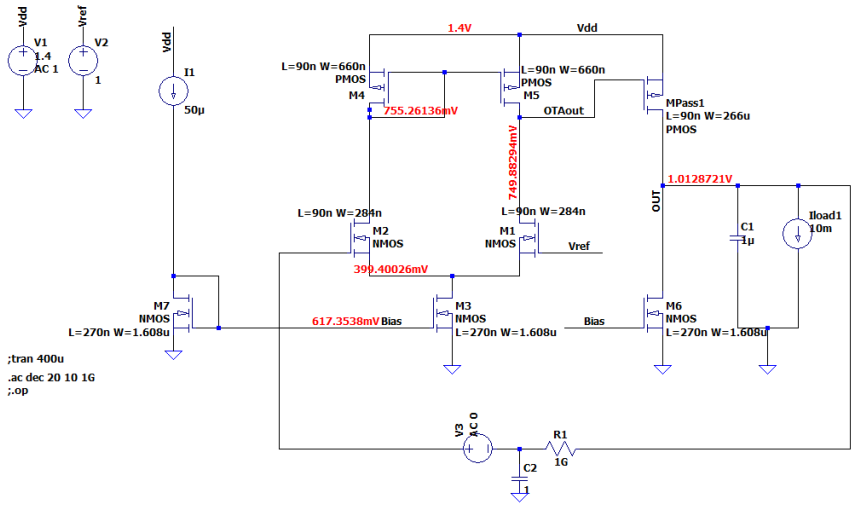

Figure 15: Schematic

Explanation of the artifact used:-

In order to calculate the open loop PSRR we need to send an AC signal from the source which in our case is VDD. Here we are giving an AC 1 signal in the source. This signal is given to the source of the passfet and the source of pmos in the diffamp. We will ideally want very bad PSRR in the diffamp as we want the OTA output to have all the AC noise such that Vsg of pmos = 0 (small signal analysis). Thus all the noise will get rejected and we will get a noise free dc voltage at the output of the LDO. Here in order to calculate the open loop PSRR we have a RC circuit to bias the differential amplifier. You can see AC 0 in the circuit indicating that there is an open loop in the circuit . From here we have calculated the open loop PSRR in the circuit. Since there is no feedback in the circuit we can thus say that there will be noise at the output and thus the rejection will be very poor.

Output on Python:-

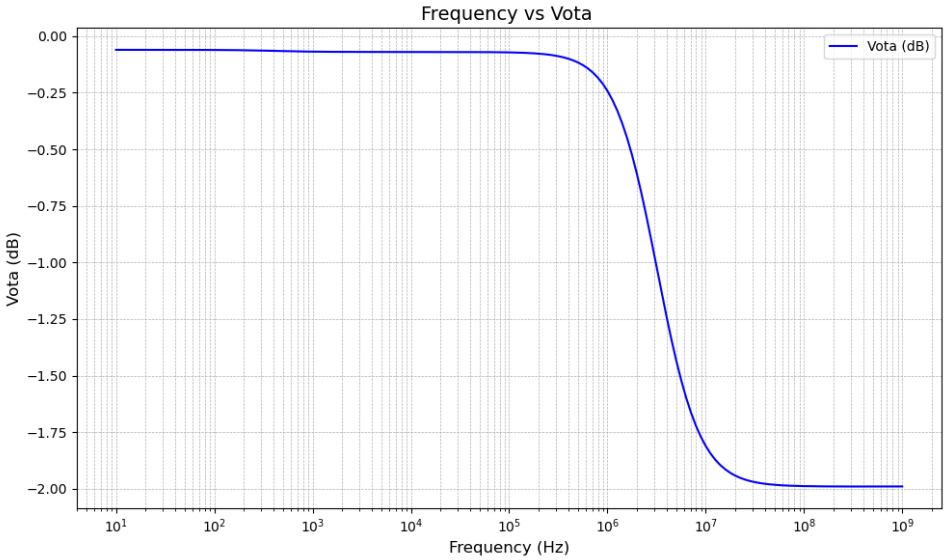

Figure 16: Output on Python

Case 3:- Closed Loop PSRR Calculation

Schematic

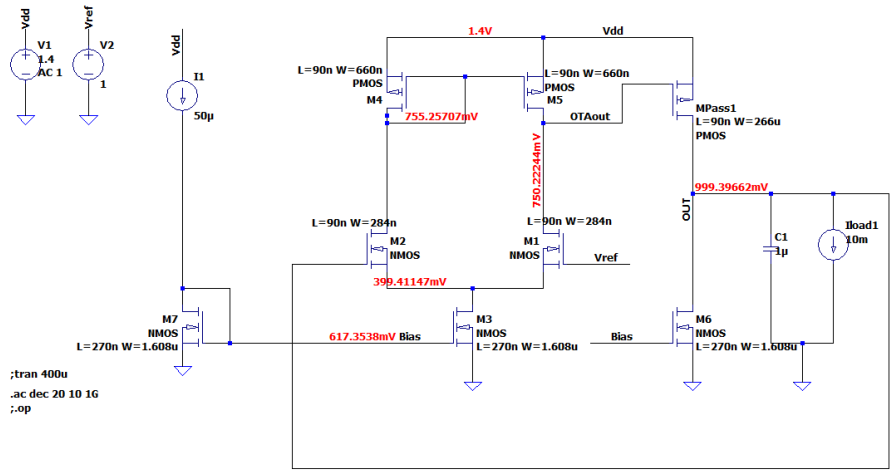

Figure 17: Schematic

Explanation of the artifact used:-

In this case we can see that we have given a AC source in the voltage source VDD. We want to see the negative feedback in the circuit due to which we will get the output voltage cancelled out (small signal analysis). Here we should observe a high PSRR according to our specifications (60db) which tells us that our sizing is perfect. For this circuit we have

given a feedback from the output terminal to the input of the diffamp which indicates the feedback path.

Output on Python:-

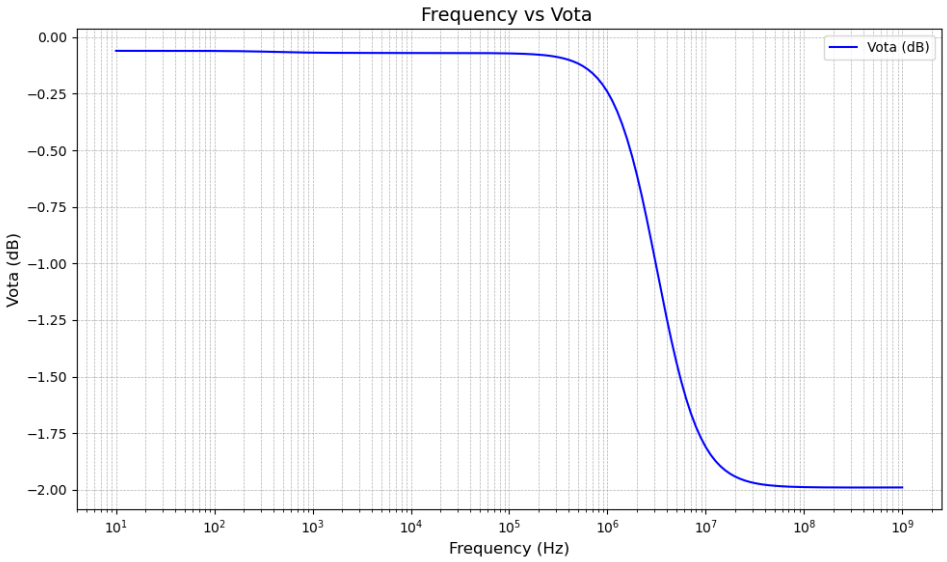

Figure 18: Output on Python

Light Load (2ma)

Case 1:- Loop gain analysis

Schematic

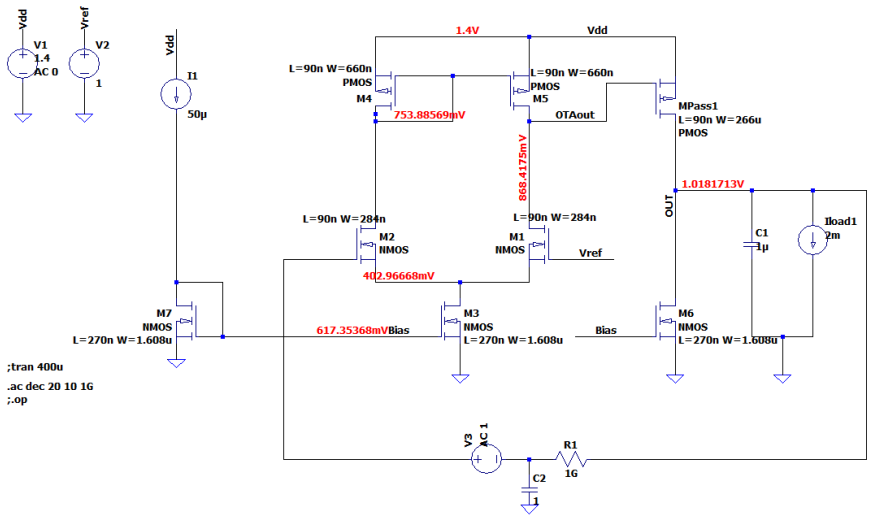

Figure 19: Schematic

Output Log File:-

Semiconductor Device Operating Points:

--- BSIM4 MOSFETS ---

Name:	m1	m2	m3	m6	m7
Model:	nmos	nmos	nmos	nmos	nmos
Id:	2.44e-05	2.50e-05	4.94e-05	5.09e-05	5.00e-05
Vgs:	5.97e-01	6.02e-01	6.17e-01	6.17e-01	6.17e-01
Vds:	4.65e-01	3.51e-01	4.03e-01	1.02e+00	6.17e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.65e-01	4.66e-01	4.69e-01	4.69e-01	4.69e-01
Vdsat:	1.41e-01	1.43e-01	1.61e-01	1.61e-01	1.61e-01
Gm:	2.44e-04	2.45e-04	4.96e-04	5.09e-04	5.01e-04
Gds:	4.33e-06	5.20e-06	3.15e-06	2.12e-06	2.29e-06
Gmb	5.63e-05	5.65e-05	1.16e-04	1.19e-04	1.18e-04
Cbd:	1.25e-16	1.29e-16	7.19e-16	6.38e-16	6.86e-16
Cbs:	2.27e-16	2.27e-16	1.29e-15	1.29e-15	1.29e-15

Name:	m4	m5	mpass1
Model:	pmos	pmos	pmos
Id:	-2.50e-05	-2.44e-05	-2.05e-03
Vgs:	-6.46e-01	-6.46e-01	-5.32e-01
Vds:	-6.46e-01	-5.32e-01	-3.82e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.84e-01	-4.85e-01	-4.87e-01
Vdsat:	-1.77e-01	-1.76e-01	-9.51e-02
Gm:	2.48e-04	2.43e-04	3.58e-02
Gds:	5.00e-06	5.19e-06	6.59e-04
Gmb	5.24e-05	5.15e-05	7.38e-03
Cbd:	2.80e-16	2.87e-16	1.20e-13
Cbs:	5.28e-16	5.28e-16	2.13e-13

Figure 20: Output Log Details

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	**Type**	V_{ds} **(V)**	V_{gs}/V_{sg} **(V)**	V_t **(V)**	$V_{gs}/V_{sg} - V_t$ **(V)**	**Operating Region**
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.522	0.652	0.490	0.162	Saturation
M3	PMOS	0.364	0.522	0.481	0.041	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.485	0.607	0.468	0.139	Saturation
M6	NMOS	0.355	0.609	0.468	0.141	Saturation
M7	NMOS	0.393	0.734	0.468	0.266	Saturation
M8	NMOS	1.04	0.734	0.466	0.268	Saturation

Table 7: Transistor Data Table

Output on Python:-

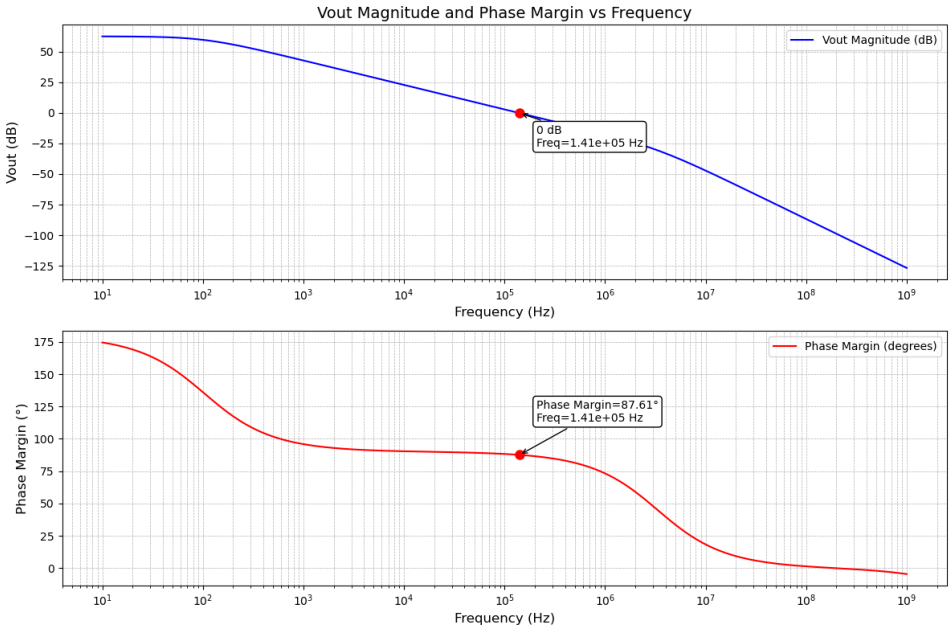

Figure 21: Output on Python

Phase margin

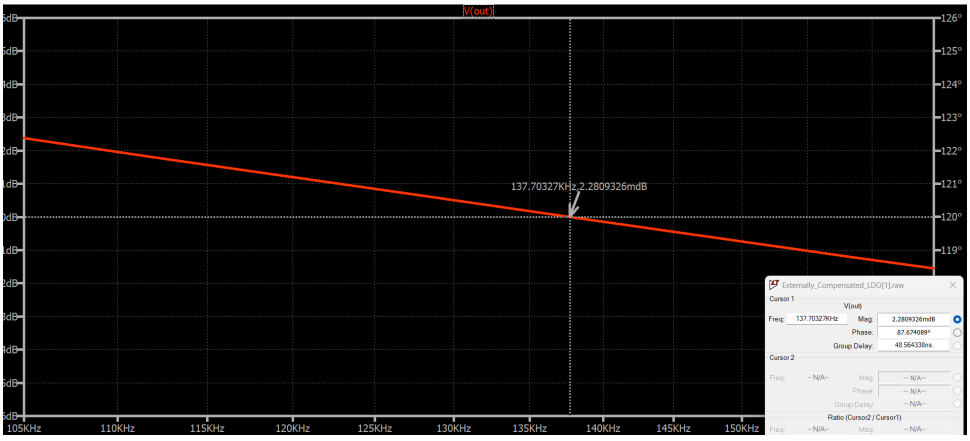

Figure 22: Phase margin

The phase margin obtained is 84.95 degrees. This value is more than that of the value obtained for heavy load. Thus proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR calculation

Schematic

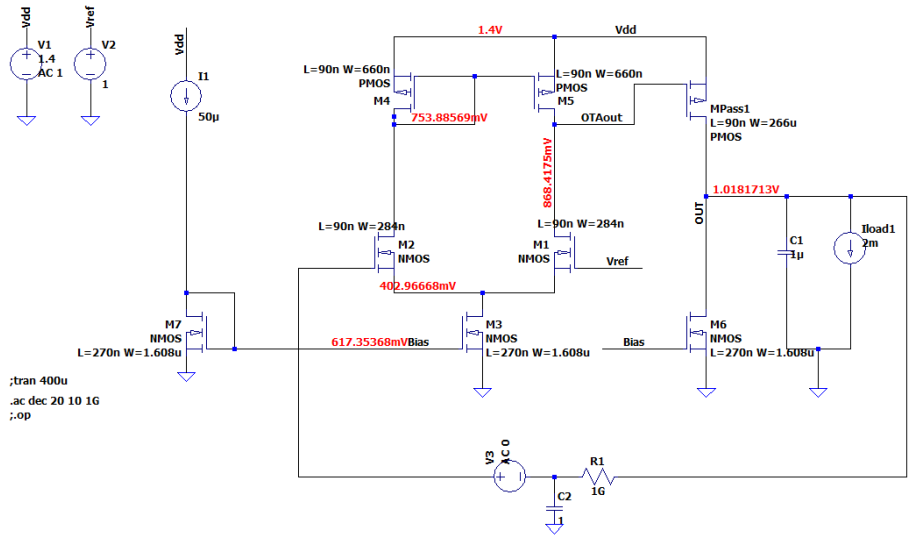

Figure 23: Schematic

Output on Python:-

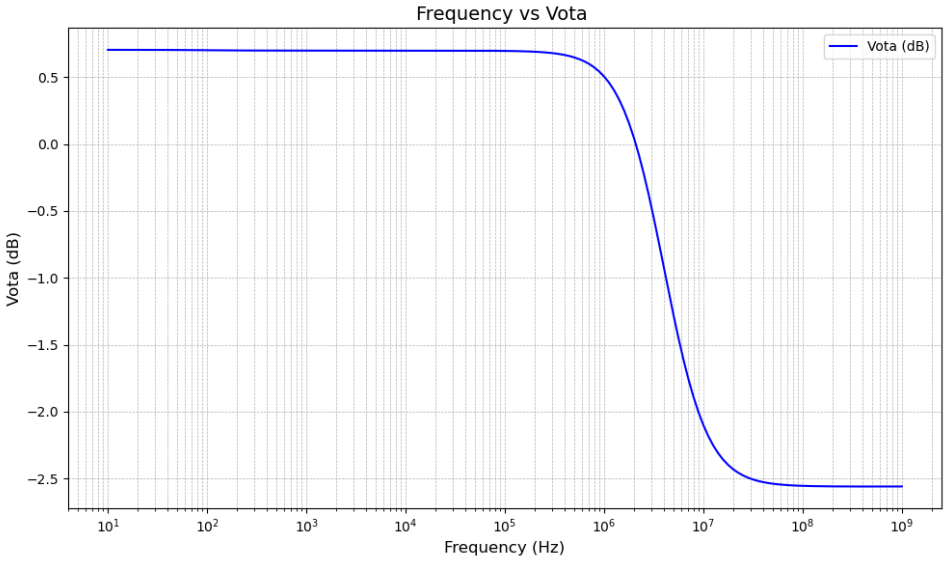

Figure 24: Output on Python

Case 3:- Closed loop PSRR calculation

Schematic

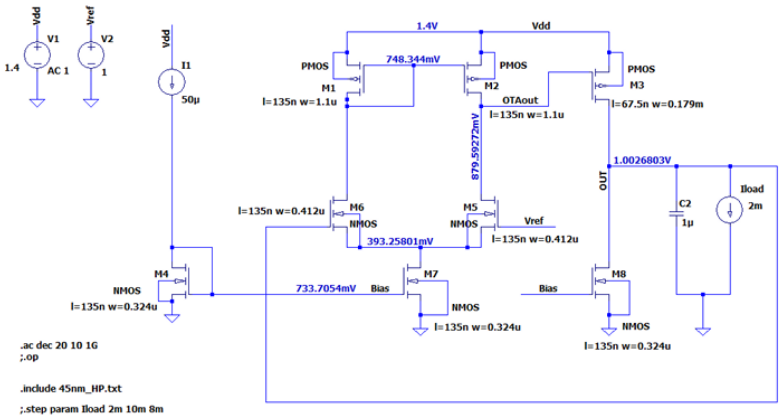

Figure 25: Schematic

Output on Python:-

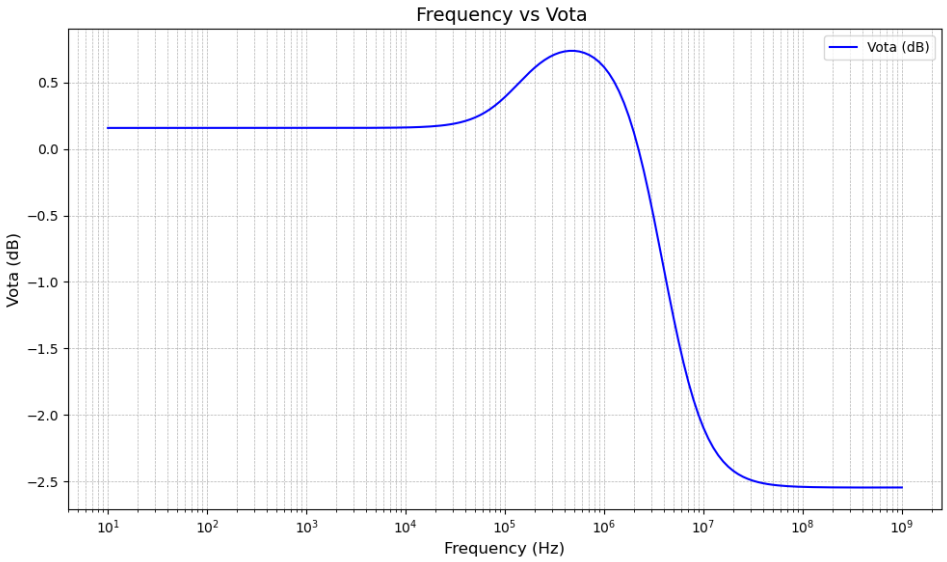

Figure 26: Output on Python

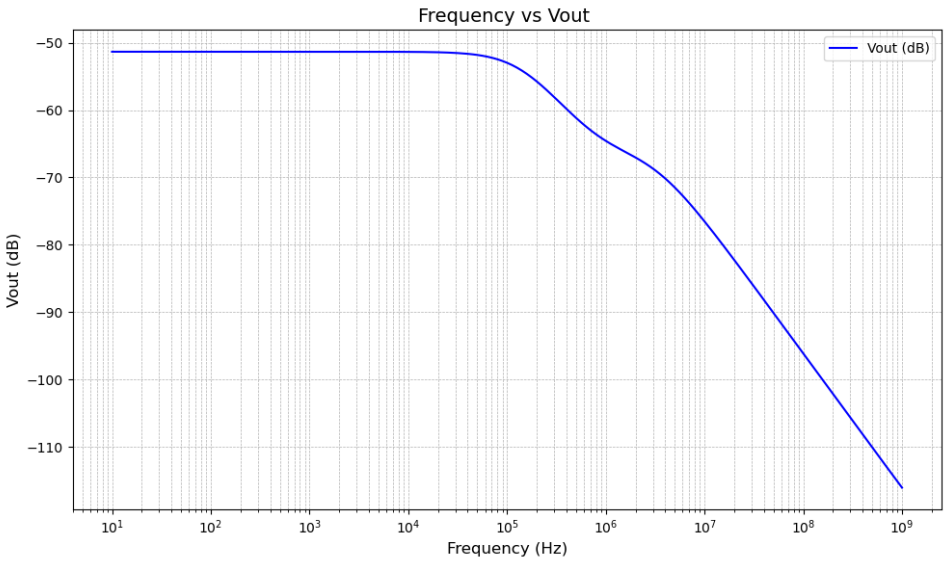
Frequency vs Vout
Vout (dB)
−50
−60
−70
−80
−90
−100
−110
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
Frequency (Hz)

Figure 27

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

Output on Python:-

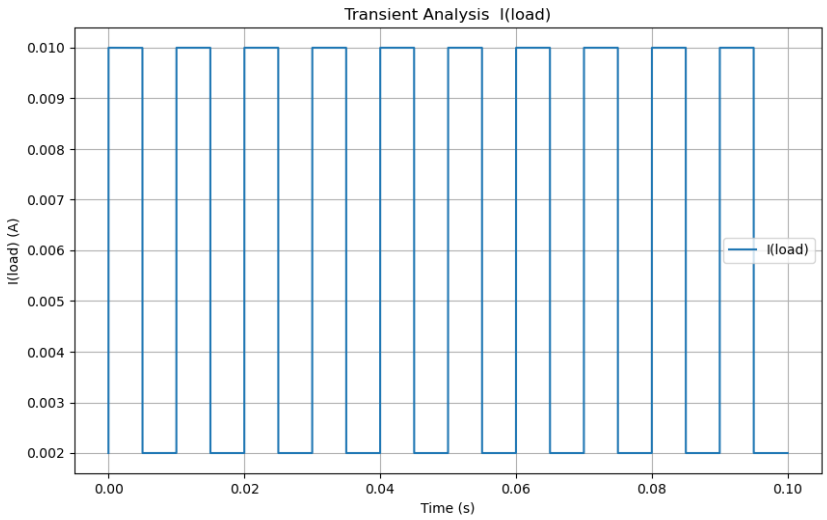

Figure 28: Output on Python

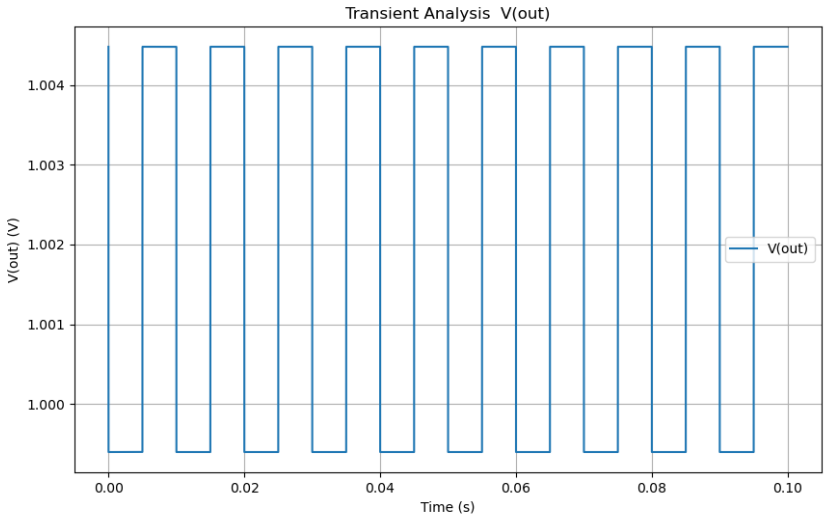

Figure 29: Phase margin

2.Internally Compensated LDO

PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Light Load (2ma)

Schematic

Case 1:- Loop gain analysis:-

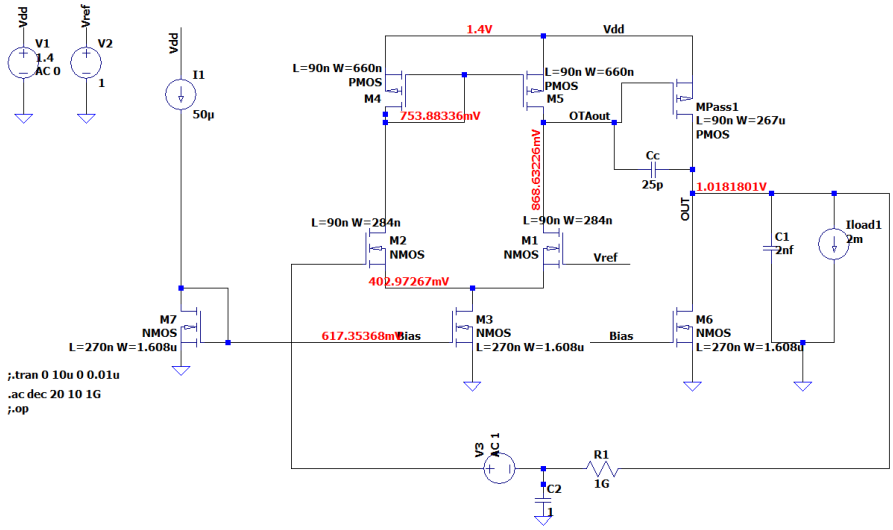

Figure 30: Schematic

Explanation of the artifact used:-

Output Log File:-

SPICE Output Log: C:\Users\csa91\AppData\Local\Microsoft\Windows\INetCache\IE\FHAE0CQW\Internally_Compensated_LDO[1].log

```
                          --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m6           m7
Model:      nmos         nmos         nmos         nmos         nmos
Id:      2.44e-05     2.50e-05     4.94e-05     5.09e-05     5.00e-05
Vgs:     5.97e-01     6.02e-01     6.17e-01     6.17e-01     6.17e-01
Vds:     4.66e-01     3.51e-01     4.03e-01     1.02e+00     6.17e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.65e-01     4.66e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.41e-01     1.43e-01     1.61e-01     1.61e-01     1.61e-01
Gm:      2.44e-04     2.45e-04     4.96e-04     5.09e-04     5.01e-04
Gds:     4.33e-06     5.20e-06     3.15e-06     2.12e-06     2.29e-06
Gmb      5.63e-05     5.65e-05     1.16e-04     1.19e-04     1.18e-04
Cbd:     1.25e-16     1.29e-16     7.19e-16     6.38e-16     6.86e-16
Cbs:     2.27e-16     2.27e-16     1.29e-15     1.29e-15     1.29e-15

Name:       m4           m5        mpass1
Model:      pmos         pmos         pmos
Id:     -2.50e-05    -2.44e-05    -2.05e-03
Vgs:    -6.46e-01    -6.46e-01    -5.31e-01
Vds:    -6.46e-01    -5.31e-01    -3.82e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.84e-01    -4.85e-01    -4.87e-01
Vdsat:  -1.77e-01    -1.76e-01    -9.50e-02
Gm:      2.48e-04     2.43e-04     3.58e-02
Gds:     5.00e-06     5.19e-06     6.59e-04
Gmb      5.24e-05     5.15e-05     7.39e-03
Cbd:     2.80e-16     2.87e-16     1.20e-13
Cbs:     5.28e-16     5.28e-16     2.14e-13
```

Figure 31: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	**Type**	V_{ds} **(V)**	V_{gs}/V_{sg} **(V)**	V_t **(V)**	$V_{gs}/V_{sg} - V_t$ **(V)**	**Operating Region**
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.522	0.652	0.490	0.162	Saturation
M3	PMOS	0.364	0.522	0.481	0.041	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.485	0.607	0.468	0.139	Saturation
M6	NMOS	0.355	0.609	0.468	0.141	Saturation
M7	NMOS	0.393	0.734	0.468	0.266	Saturation
M8	NMOS	1.04	0.734	0.466	0.268	Saturation

Table 8: Transistor Parameters and Operating Regions

Output on Python:-

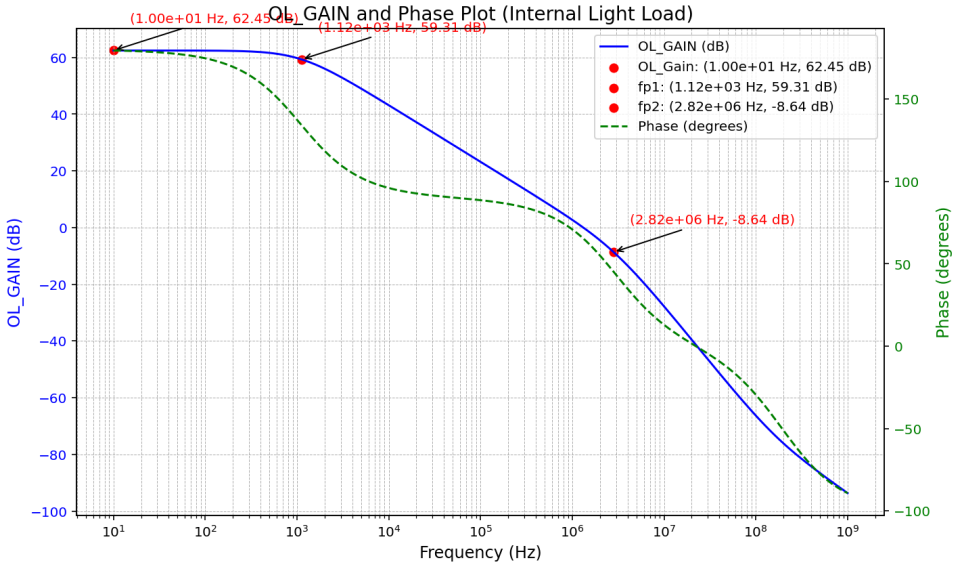

Figure 32: Output on Python

Phase margin

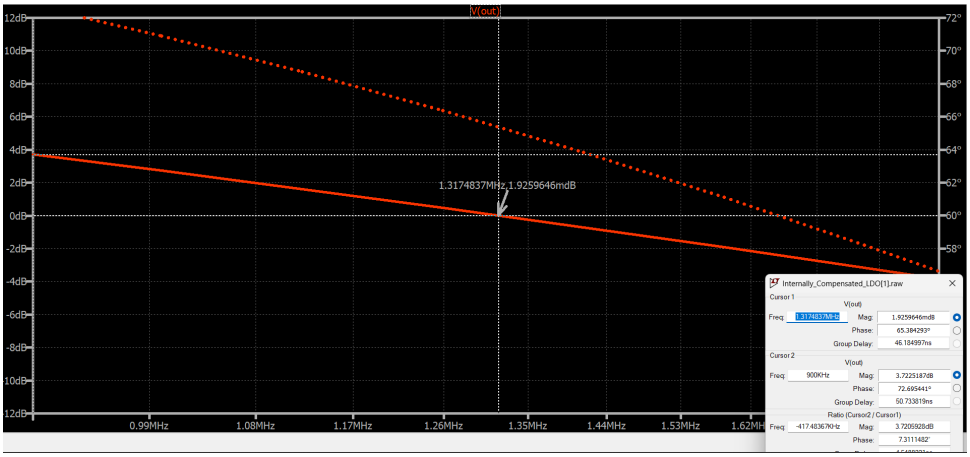

Figure 33: Phase margin

Case 2:- Open Loop PSRR calculation

Schematic

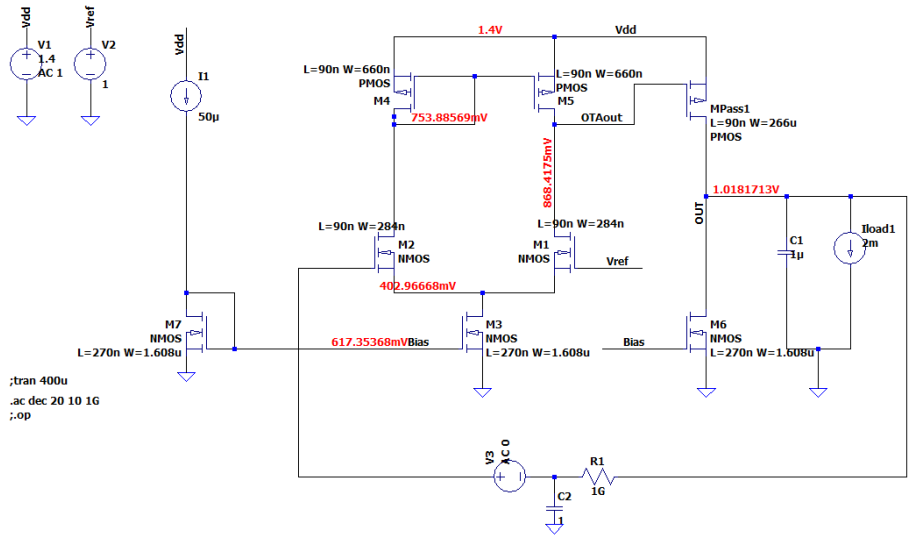

Figure 34: Schematic

Output on Python:-

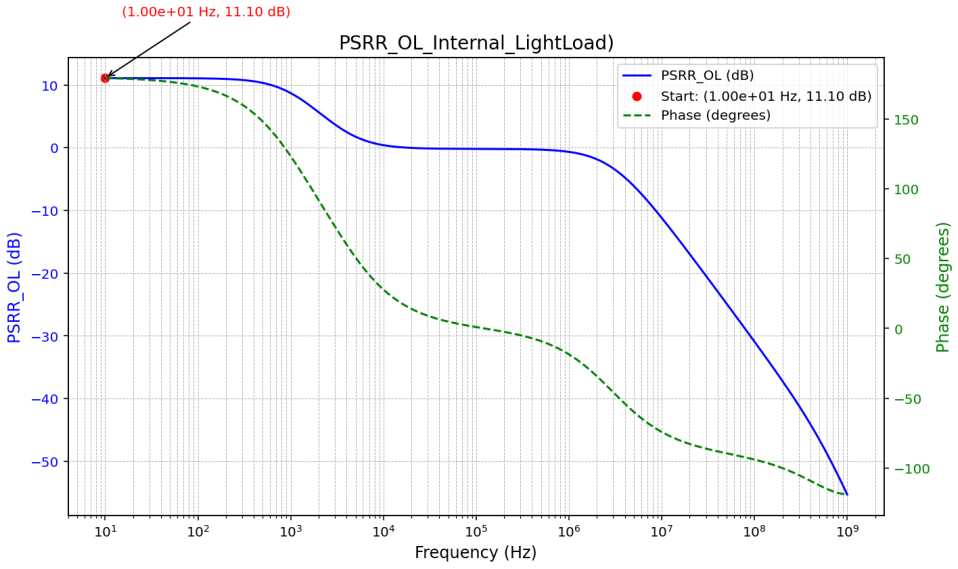

Figure 35: Output on Python

Case 3:- Closed loop PSRR calculation

Schematic

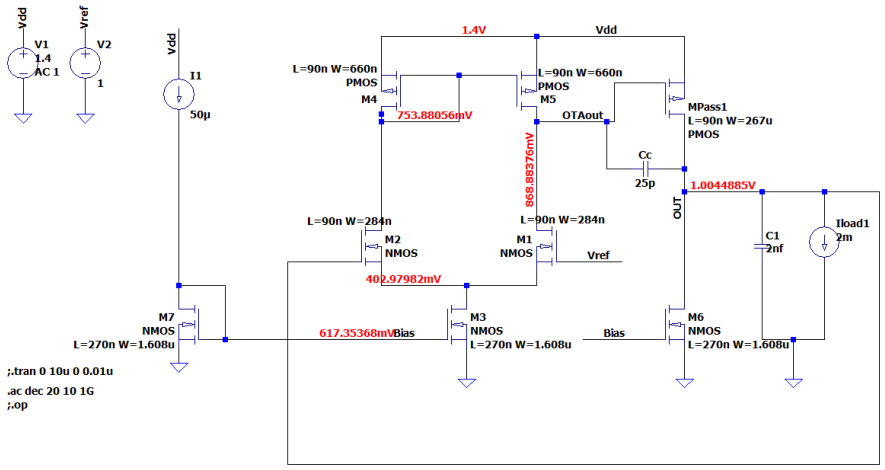

Figure 36: Schematic

Output on Python:-

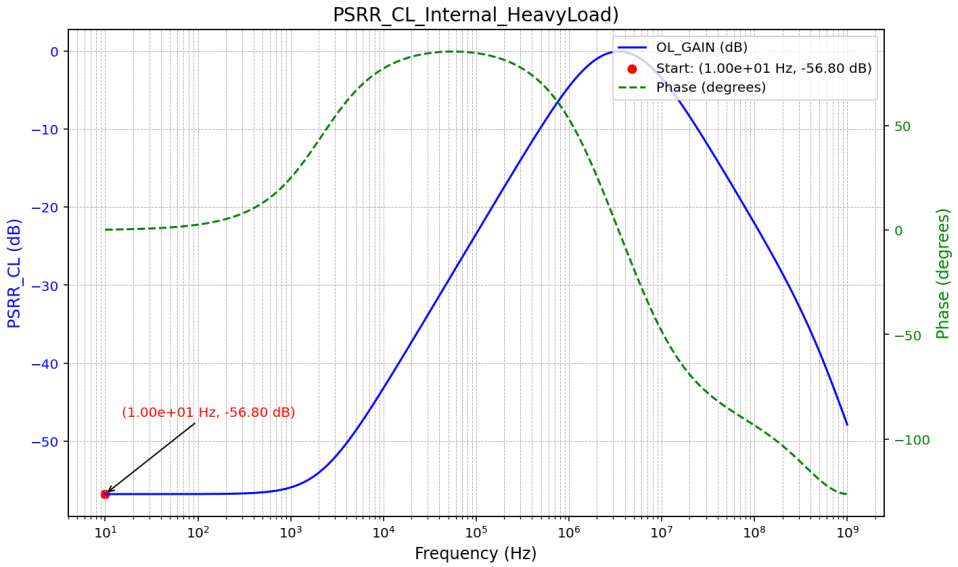

Figure 37: Output on Python

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

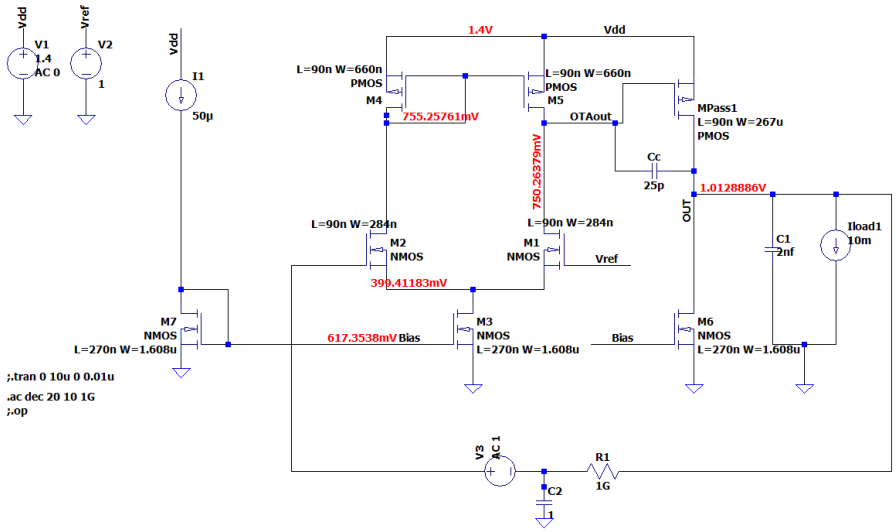

Figure 38: Schematic

Explanation of the artifact used:-

Output Log File:-

```
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:       m1          m2          m3          m6          m7
Model:      nmos        nmos        nmos        nmos        nmos
Id:      2.48e-05    2.47e-05    4.94e-05    5.08e-05    5.00e-05
Vgs:     6.01e-01    6.00e-01    6.17e-01    6.17e-01    6.17e-01
Vds:     3.51e-01    3.56e-01    3.99e-01    1.01e+00    6.17e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:     4.66e-01    4.66e-01    4.69e-01    4.69e-01    4.69e-01
Vdsat:   1.43e-01    1.42e-01    1.61e-01    1.61e-01    1.61e-01
Gm:      2.44e-04    2.44e-04    4.95e-04    5.09e-04    5.01e-04
Gds:     5.16e-06    5.08e-06    3.19e-06    2.12e-06    2.29e-06
Gmb      5.63e-05    5.62e-05    1.16e-04    1.19e-04    1.18e-04
Cbd:     1.29e-16    1.28e-16    7.20e-16    6.38e-16    6.86e-16
Cbs:     2.27e-16    2.27e-16    1.29e-15    1.29e-15    1.29e-15

Name:       m4          m5          mpass1
Model:      pmos        pmos        pmos
Id:     -2.47e-05   -2.47e-05   -1.01e-02
Vgs:    -6.45e-01   -6.45e-01   -6.50e-01
Vds:    -6.45e-01   -6.50e-01   -3.87e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00
Vth:    -4.84e-01   -4.84e-01   -4.87e-01
Vdsat:  -1.76e-01   -1.76e-01   -1.78e-01
Gm:      2.46e-04    2.46e-04    9.90e-02
Gds:     4.95e-06    4.95e-06    2.52e-03
Gmb      5.20e-05    5.21e-05    2.10e-02
Cbd:     2.80e-16    2.80e-16    1.20e-13
Cbs:     5.28e-16    5.28e-16    2.14e-13
```

Figure 39: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.651	0.651	0.489	0.162	Saturation
M2	PMOS	0.640	0.651	0.489	0.162	Saturation
M3	PMOS	0.367	0.640	0.481	0.159	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.368	0.609	0.468	0.141	Saturation
M6	NMOS	0.358	0.609	0.468	0.141	Saturation
M7	NMOS	0.391	0.734	0.468	0.266	Saturation
M8	NMOS	1.03	0.734	0.466	0.268	Saturation

Table 9: Updated Transistor Parameters and Operating Regions

Output on Python:-

Phase margin

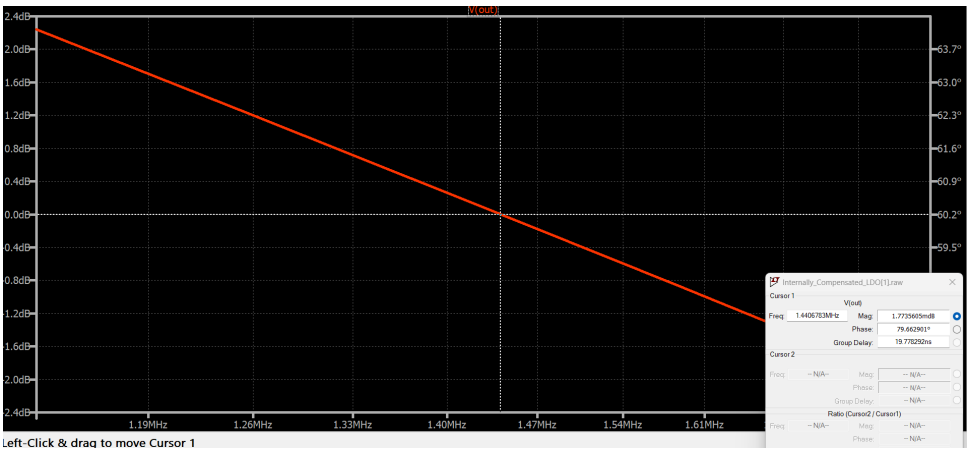

Figure 40: Phase margin

Case 2:- Open Loop PSRR calculation

Schematic

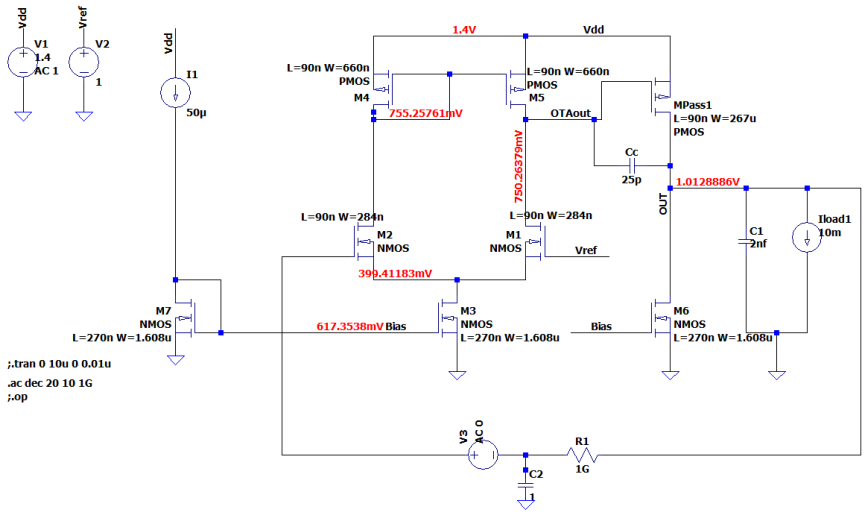

Figure 41: Schematic

Output on Python:-

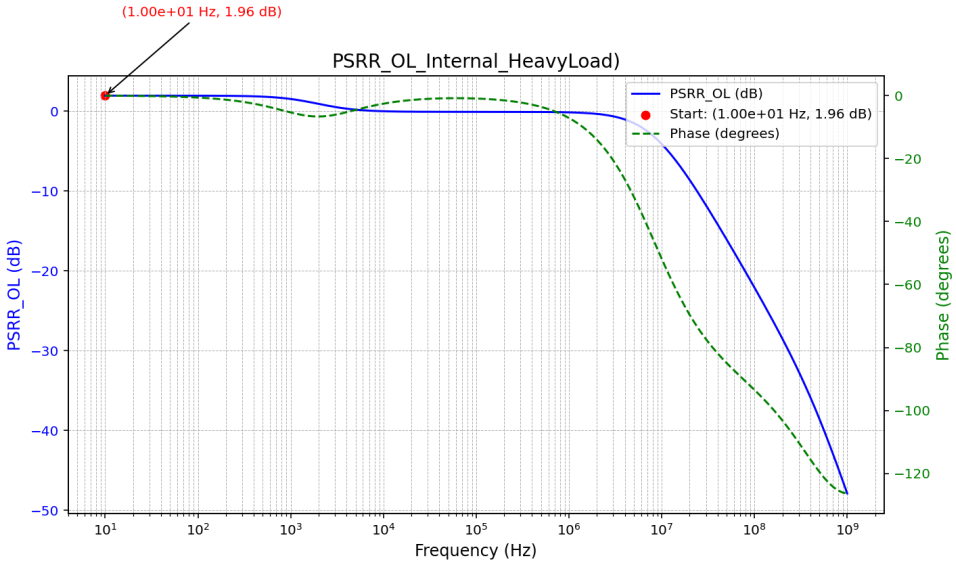

Figure 42: Output on Python

Case 3:- Closed loop PSRR calculation

Schematic

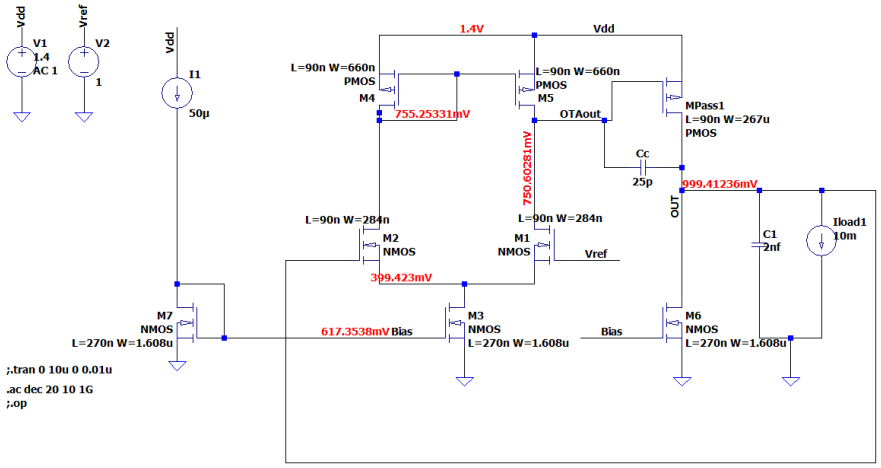

Figure 43: Schematic

Output on Python:-

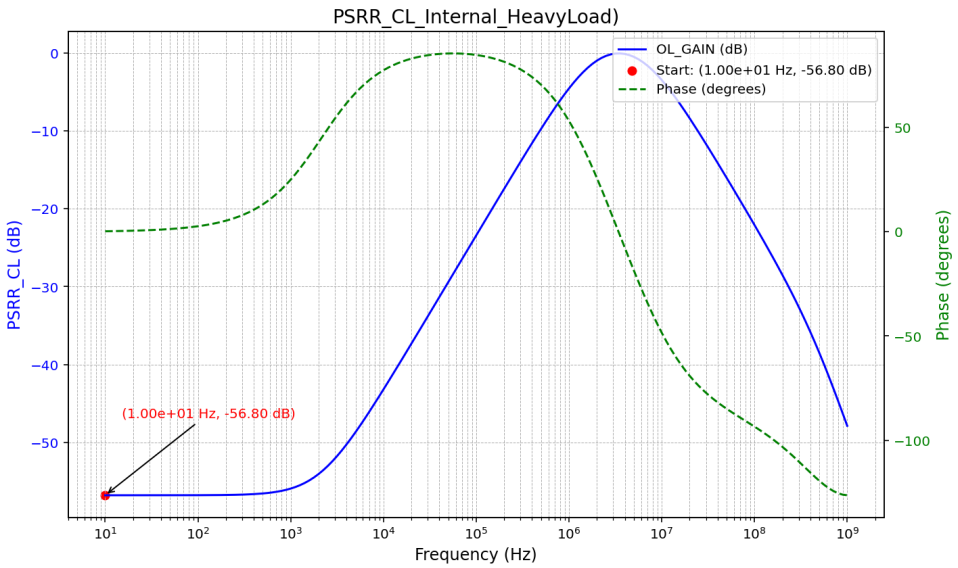

Figure 44: Output on Python

Transient Analysis

Schematic

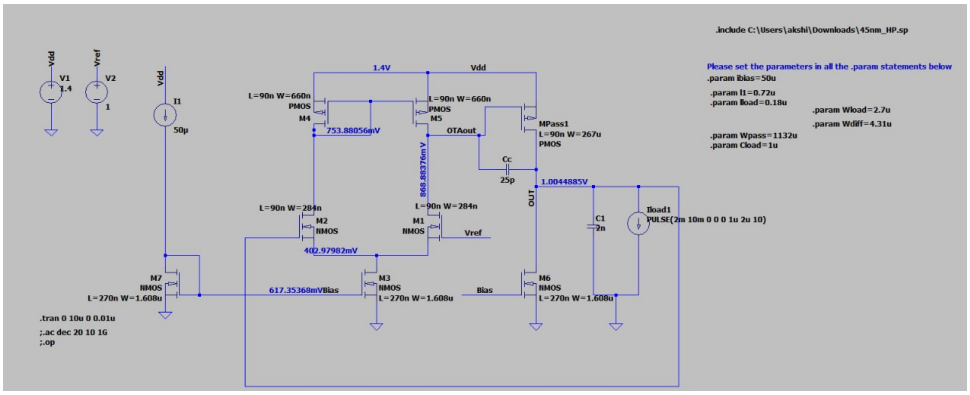

Figure 45: Schematic

Iload Vs Time

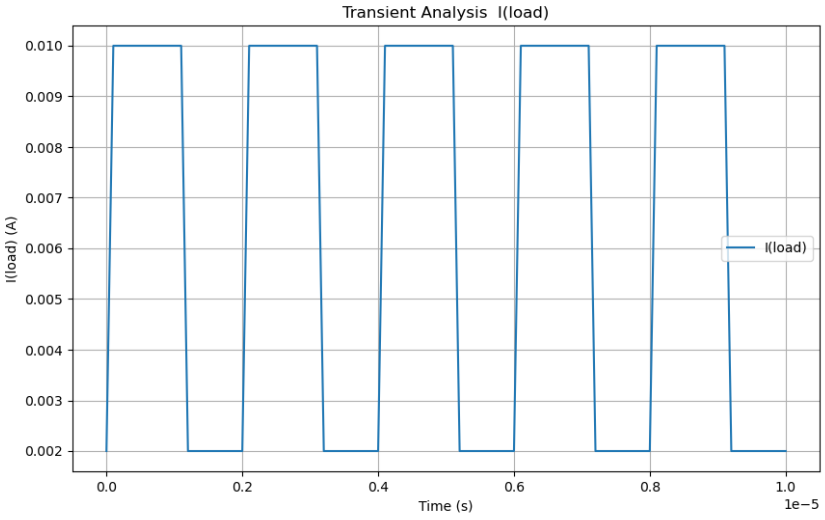

Figure 46: Iload Vs Time

Vout vs Time

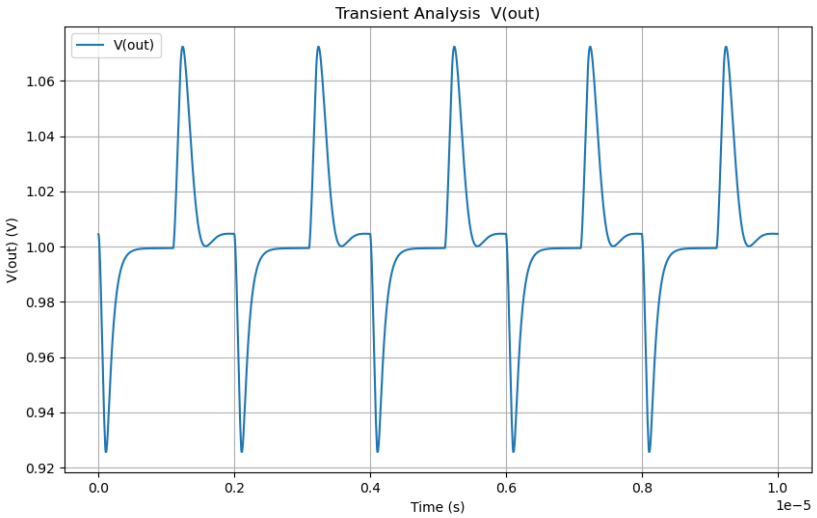

Figure 47: Vout vs Time

FET Sizes

we Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 10: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	0.267m/90n	10	24.18	55.62	50.76 GHz
Diff-Amp pmos	660n/90n	10	97.93	22.71	11.71 GHz
Diff-Amp nmos	284/90n	10	93.43	60.51	30 GHz
Current Mirror nmos	1.608u/270n	10	155	154.1	30 GHz

The value of the capacitance for the internal capcitor is 24.97pf

Stability Analysis

For Heavy load we get the following curve:

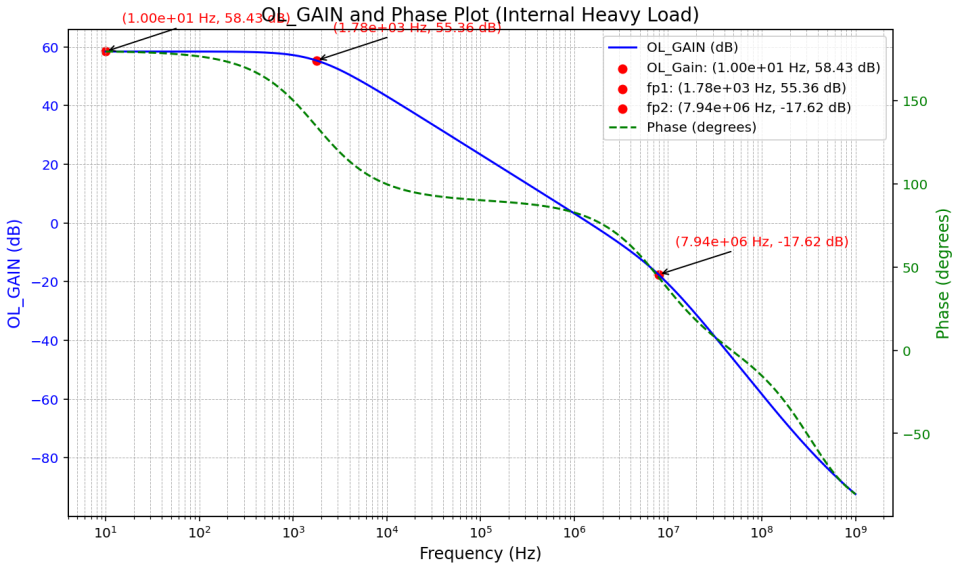

Figure 48: Output on Python

For Light load we get the following curve

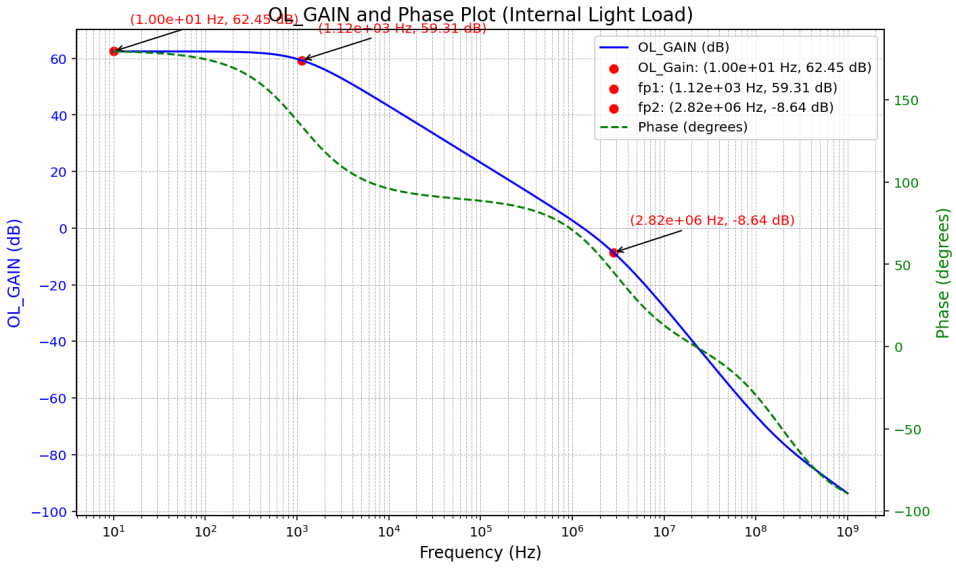

Figure 49: Output on Python

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. From the phase margin also we can observe that we observe a lesser phase margin of 76 degrees for the heavy load case than that of the light load case. From this analysis, we can say that we get a more stable system when we apply light load.