









Outline

- Introduction to DaCe
- DaFlEx overview
- DaFlEx first steps and goals







DaCe Overview

Domain Scientist

Problem Formulation

$$\frac{\partial u}{\partial t} - \alpha \nabla^2 u = 0$$

Python

DSLs

TensorFlow

MATLAB



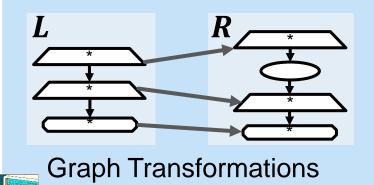
Scientific Frontend



Performance Engineer



Data-Centric Intermediate Representation (SDFG)



Transformed Dataflow



System

Hardware Information

Compiler

CPU Binary Runtime **GPU Binary**

FPGA Modules







Dataflow Programming in DaCe

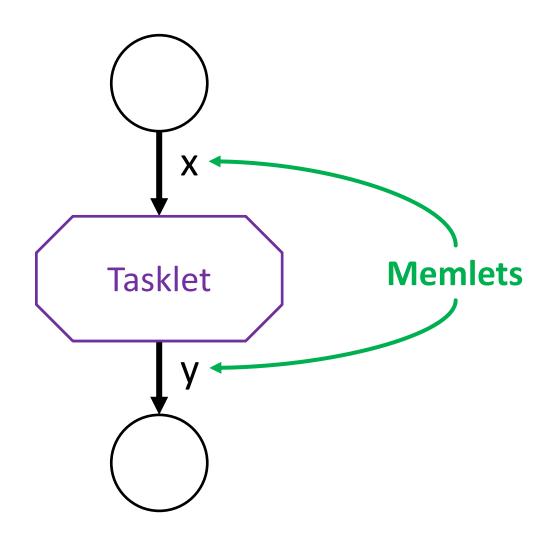
$$y = x^2 + \sin\frac{x}{\pi}$$







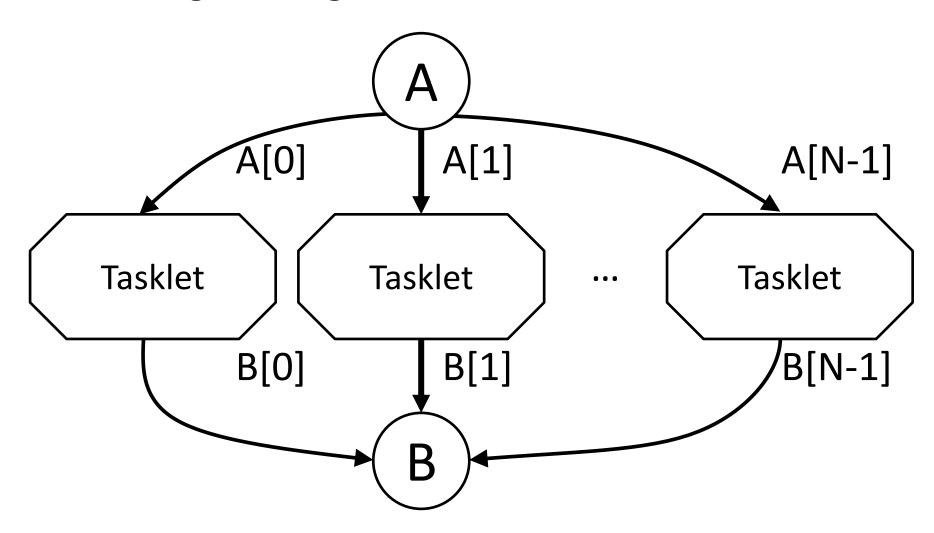
Dataflow Programming in DaCe







Parallel Dataflow Programming

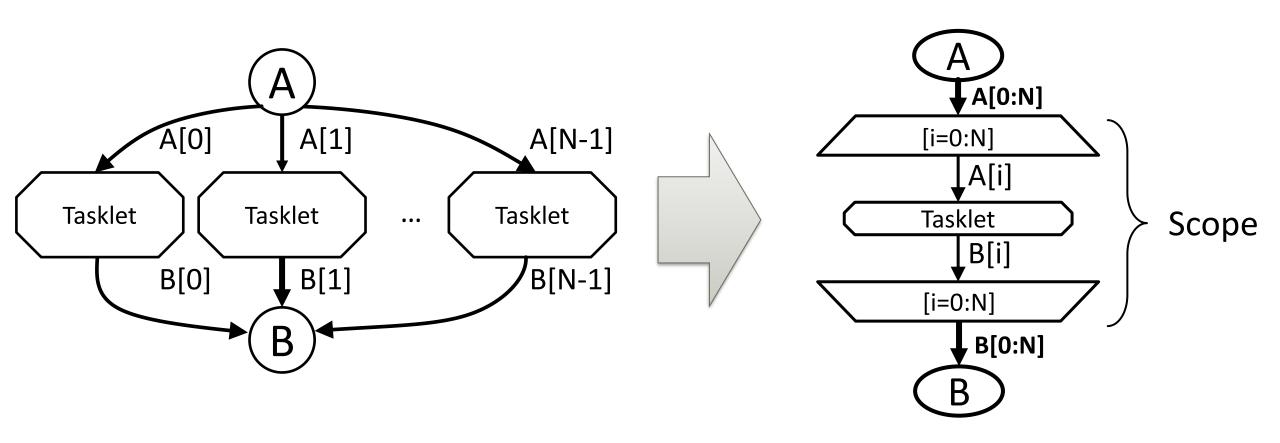








Parallel Dataflow Programming



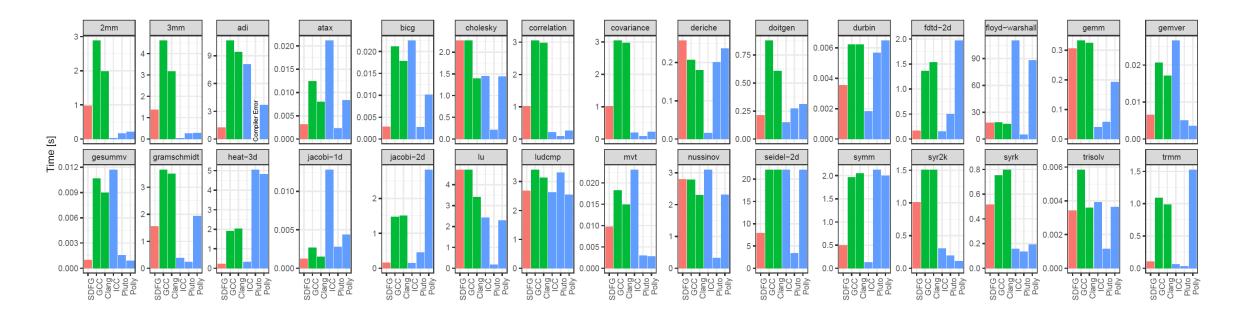






Performance Evaluation: Polybench (CPU)

- Polyhedral benchmark with 30 applications
- Without any transformations, achieves 1.43x (geometric mean) over general-purpose compilers



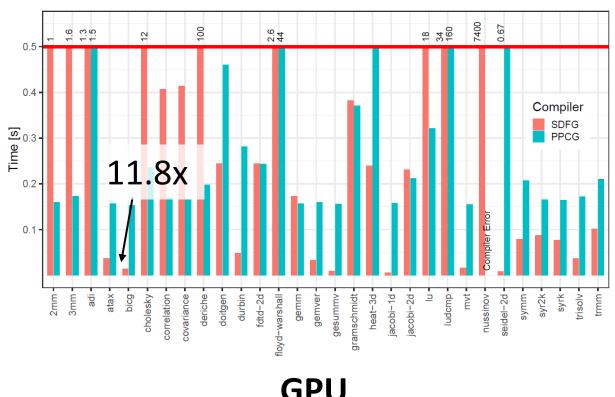






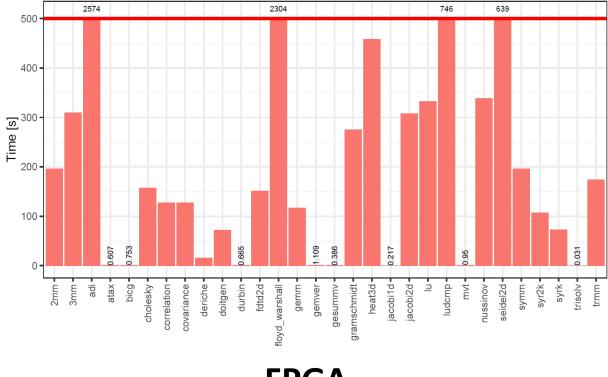
Performance Evaluation: Polybench (GPU, FPGA)

Automatically transformed from CPU code



GPU

(1.12x geomean speedup)



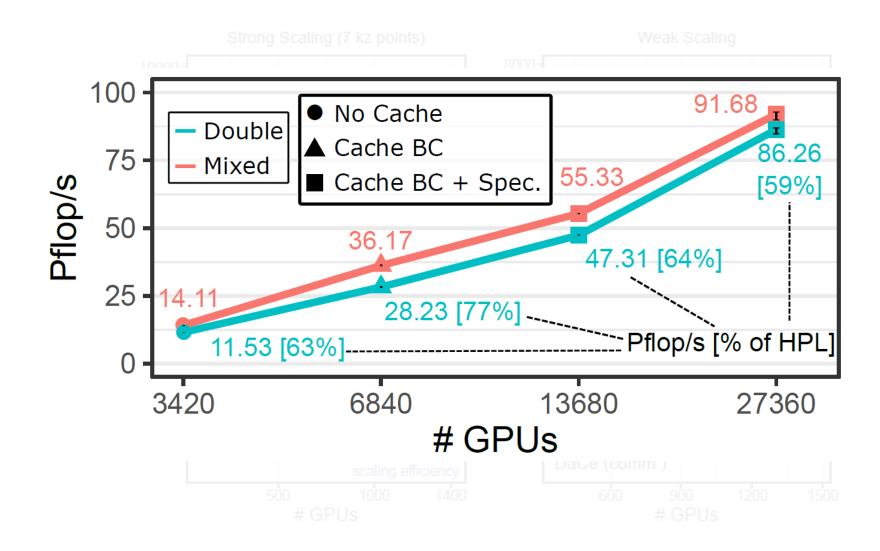
FPGA

The **first** full set of placed-and-routed Polybench





Performance Evaluation: OMEN

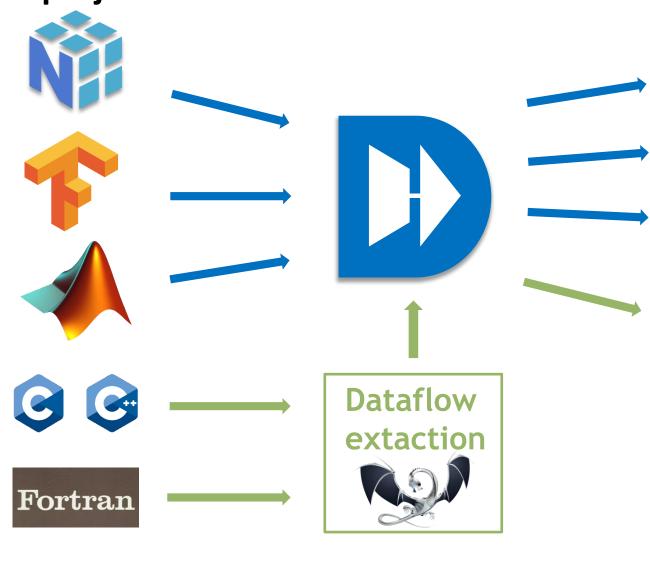








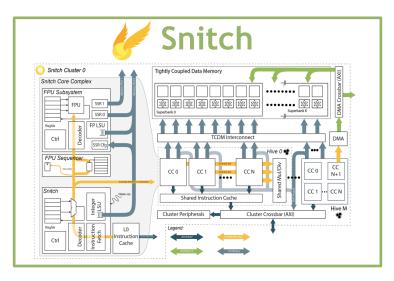
DaFlEx – project overview







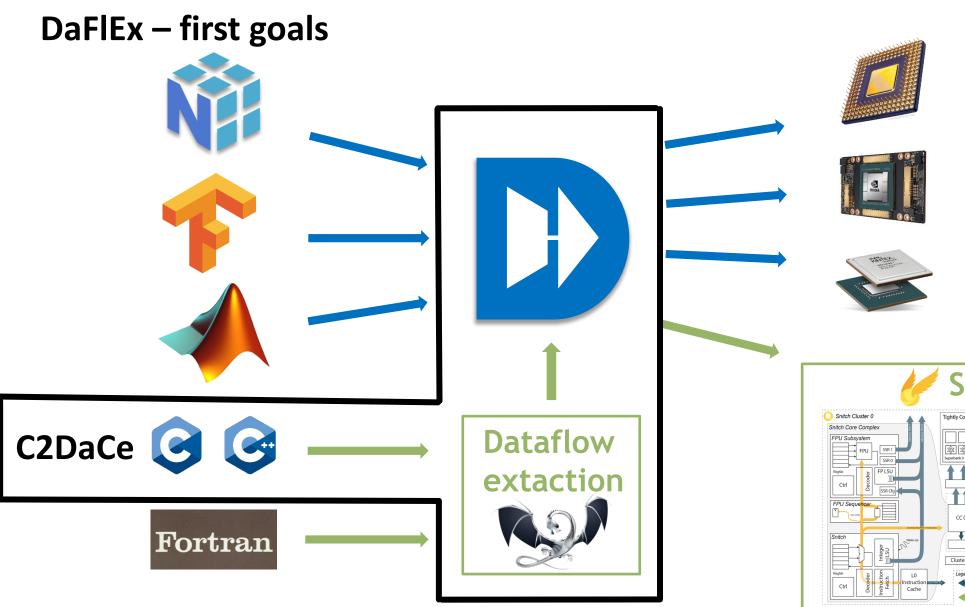


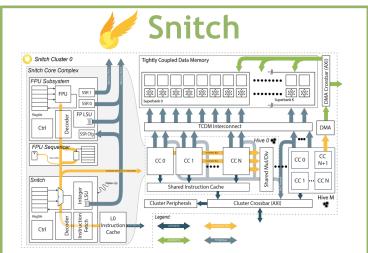










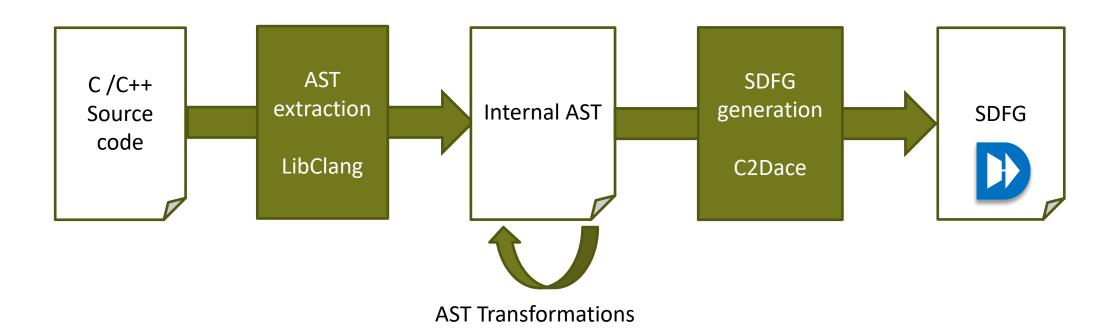








Dataflow extaction pipeline for C/C++

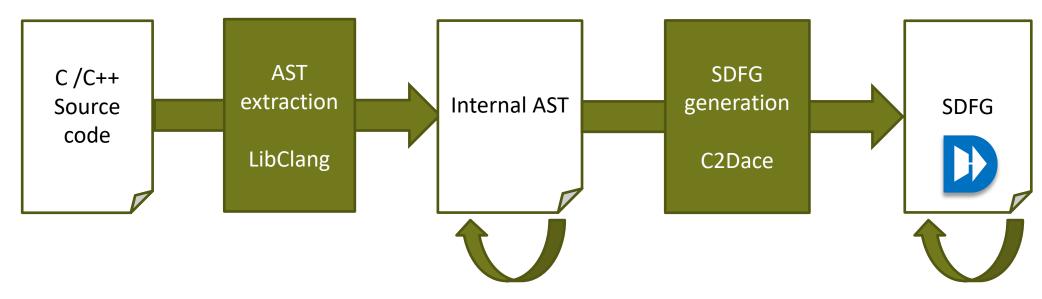


- Array index extraction
- Function call isolation
- Separating variable declaration and initialization





Dataflow extaction pipeline for C/C++



Candidates:

- Polybench
- LULESH
- C HPC codes?

SDFG Transformations

- Symbol promotion
- Create WCR accesses where necessary
- Loop to Map





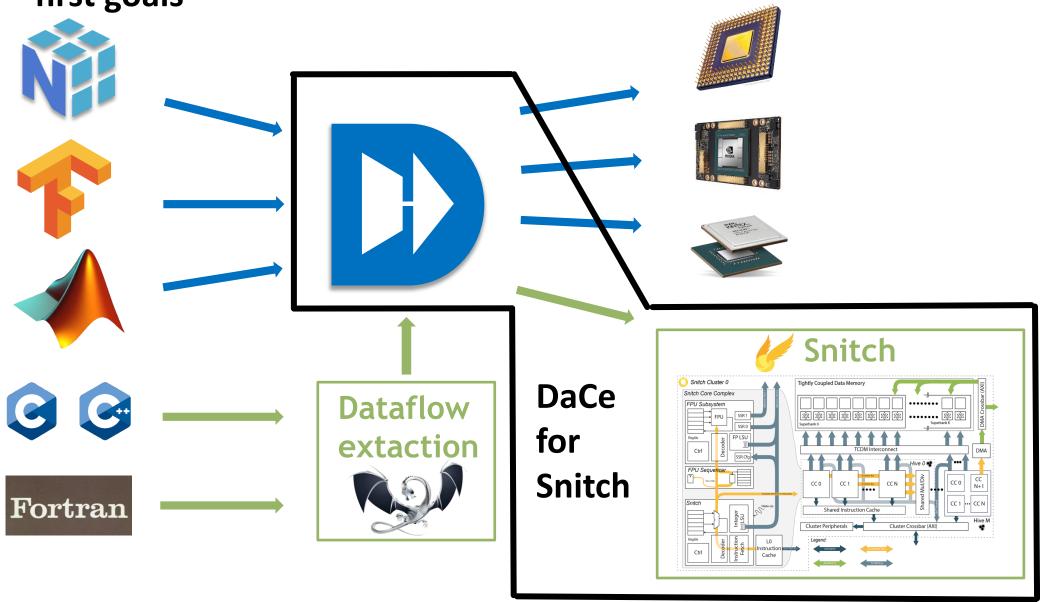
C2DACE

C Language	SDFG Equivalent		C Language	SDFG Equivalent
Declarations and Types			Statements	
Primitive data type	Scalar data container		Compound (blocks)	Nested SDFG
Type qualifier (const,volatile)	Implicit, hints provided are inherent to the SDFG representation Data container properties (e.g., life-time, storage location) Access node		Branching (if,switch)	Branch conditions on state transition edges
Storage class (static,auto,register, etc.)			Iteration (for, while,dowhile)	Nested SDFG for compound state-ment, with states and state transi-tions for loop logic
Pointer			Function flow	Edge to SDFG exit state, using helpervariable to
Array	Array data (Data contai C Language SDFG Equiver Parallelism		valent	ion if within same SDFG,otherwise:
Structure			d d	
Union	Data container references	- Parametric Map scope		alent
C Language	SDFG Equivalent		Functions	
Expressions and Assignments		Function calls (with	Nested SDFG for content, memlets reduce shape	
Operators (e.g.,	Tasklet with incoming and outgoingmemlets for read/written operands		source)	of inputs and outputs
Unary,Binary)			External/Library calls	Tasklet with library state
Compound assignments	Tasklet		Recursion	Unsupported
Array expression	Memlet		Function pointers	No equivalent, unsupported





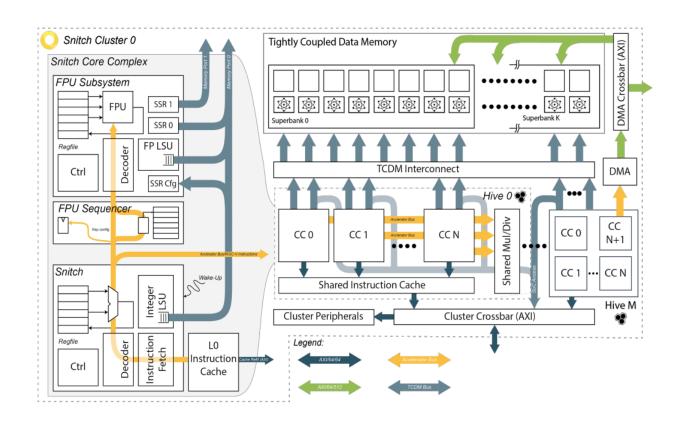
DaFlEx – first goals











RV32IMAFDXfrepXssrXsdma



- Streaming Semantic Registers
 Register-memory interface
- DMA Engine
 Asynchronous Data Movement
- Floating Point Repetition
 Hardware loops for the FPU









DaCe code generation for the Snitch



Goal – create a new codegeneration backend to leverage Snitch's custom extensions for data movement, specifically:

TCDM/DMA Double buffering from host memory to TCDM

SSR Hot-loop without load/store overhead

Frep Hardware loops for the FPU

Concept – from an SDFG emit the SSR configuration and express parallelism u sing OpenMP



Thank you!

