The diagram shows a systolic array for matrix multiplication with processing elements PE 11, PE 12, PE 21, PE 22.

Inputs across the top: a_{11}, b_{12}, a_{12}, b_{22}

Second level labels: a_{11}, b_{11}, a_{12}, b_{21}

Left side inputs: a_{21}, 0, 0

Between PE 11 and PE 12: $a_{11}b_{11}$ | $a_{11}b_{12}$

Below PE 11: b_{12}, a_{21}, b_{11}, a_{22}, b_{22}

Lower level: a_{21}, b_{11}, a_{22}, b_{21}

Between PE 21 and PE 22: $a_{21}b_{11}$ | $a_{21}b_{12}$

Outputs on the right:

$$a_{11}b_{11} + a_{12}b_{21} \qquad a_{11}b_{12} + a_{12}b_{22}$$

$$a_{21}b_{11} + a_{22}b_{21} \qquad a_{21}b_{12} + a_{22}b_{22}$$

1. after start clock signal, one clock later, next row operand is available — Both start signal — posedge activity. & operand latching.

2. Done signal goes high (negative edge activity), one clock later result is generated. (negative edge)