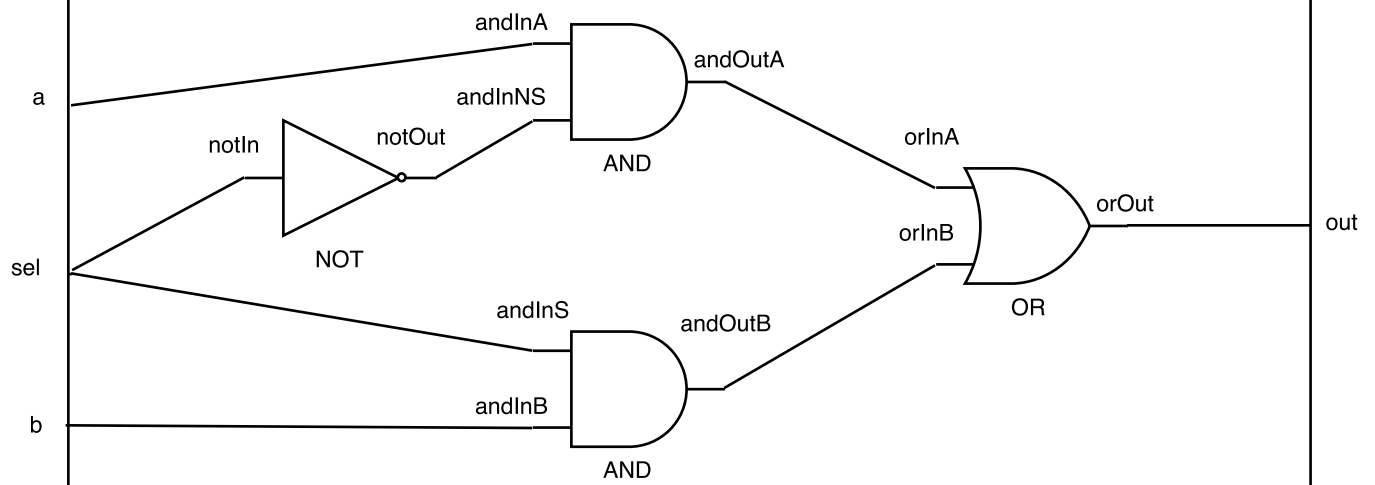
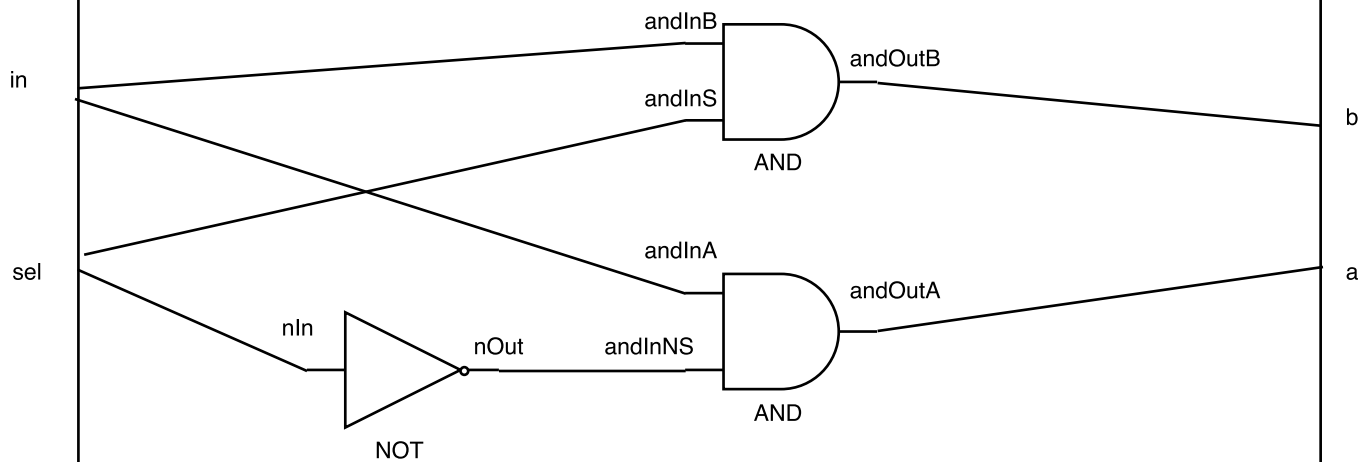


## Mux

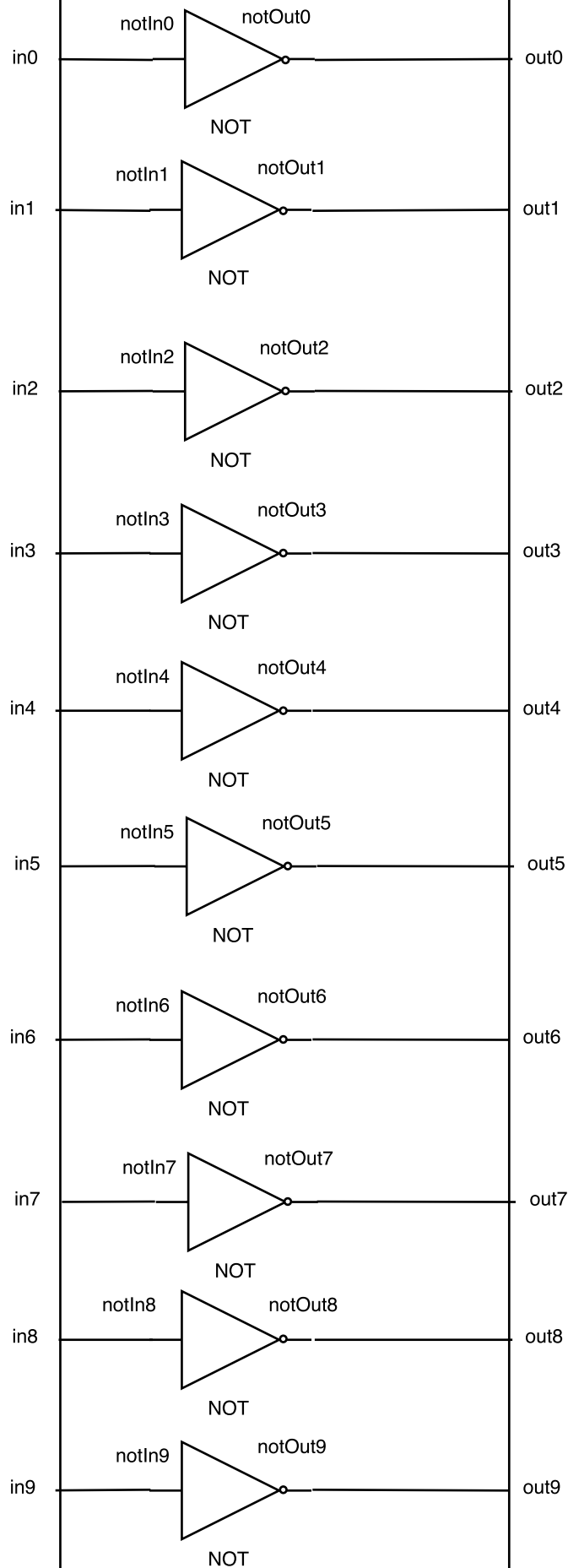


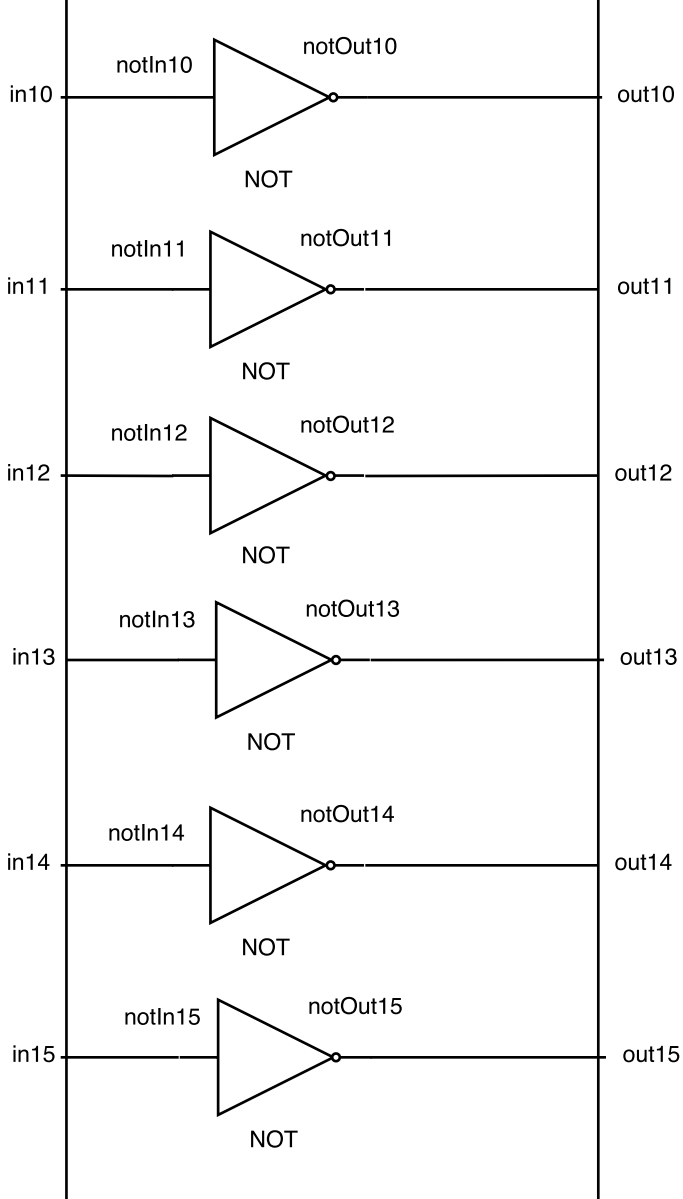
## DMux



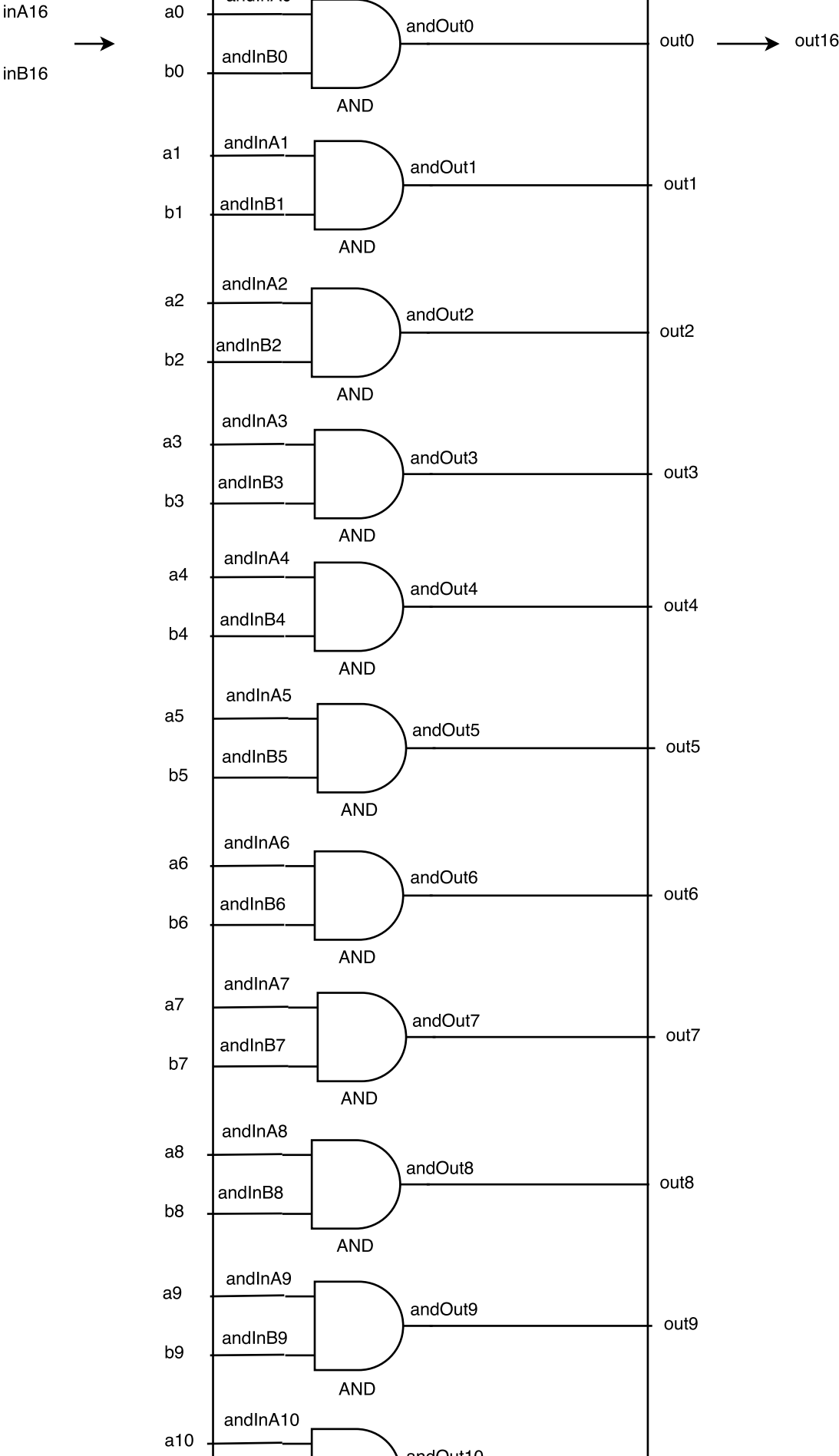
# NOT16

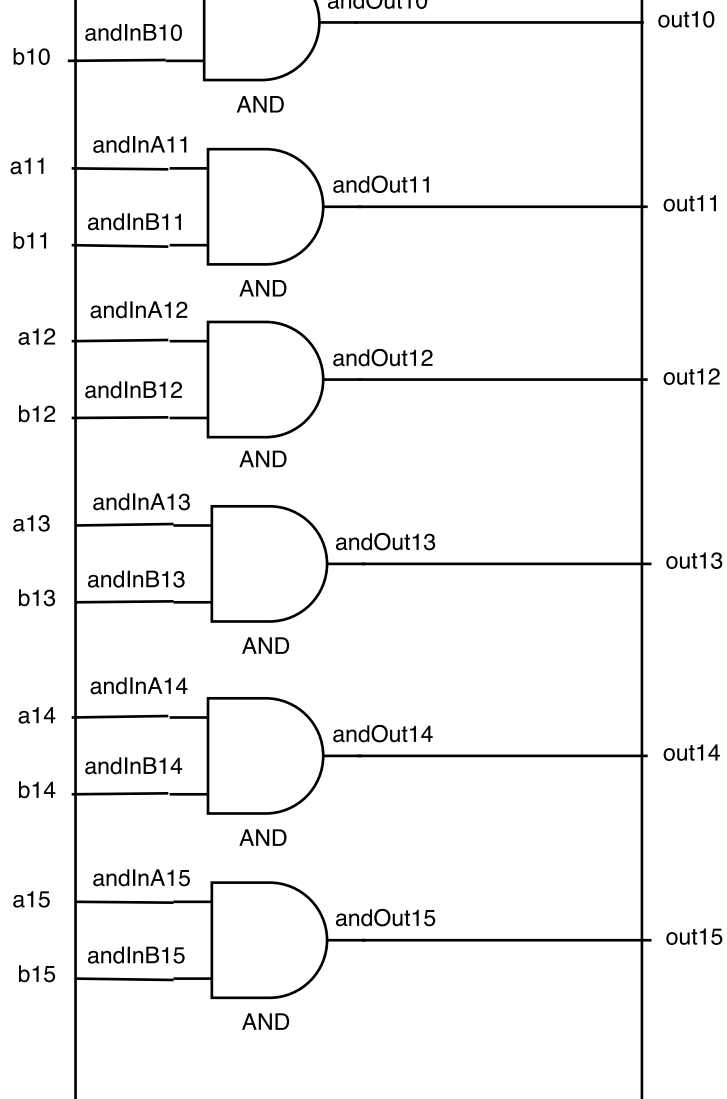
in16 → in0      out0 → out16





**AND16**





# OR16

inA16



inB16

a0

orInA0

orInB0

orOut0

out0



out

a1

orInA1

orInB1

orOut1

out1

b1

a2

orInA2

orInB2

orOut2

out2

b2

a3

orInA3

orInB3

orOut3

out3

b3

a4

orInA4

orInB4

orOut4

out4

b4

a5

orInA5

orInB5

orOut5

out5

b5

a6

orInA6

orInB6

orOut6

out6

b6

a7

orInA7

orInB7

orOut7

out7

b7

a8

orInA8

orInB8

orOut8

out8

b8

a9

orInA9

orInB9

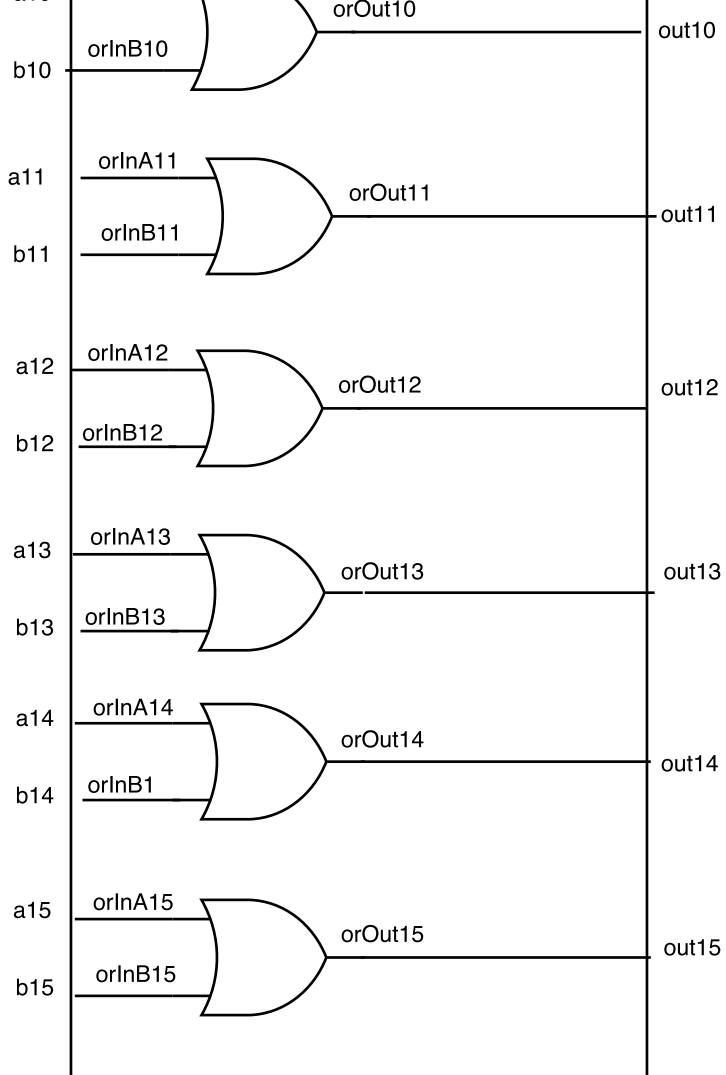
orOut9

out9

b9

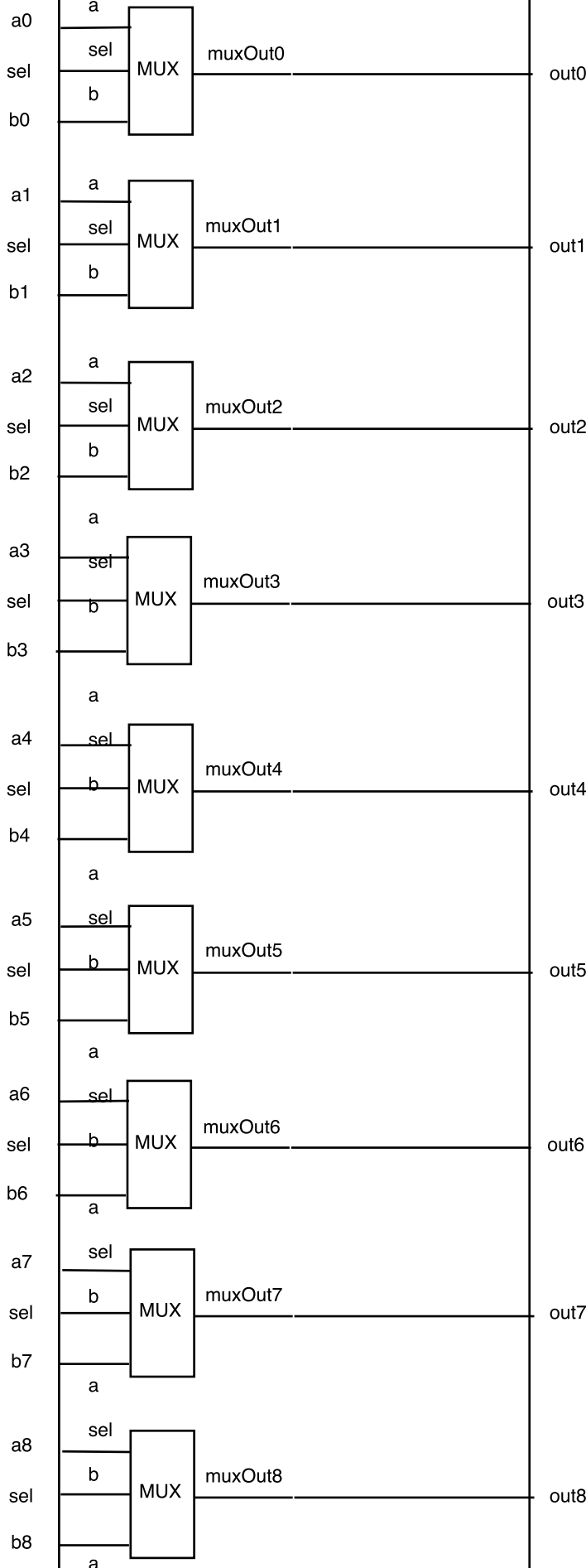
a10

orInA10



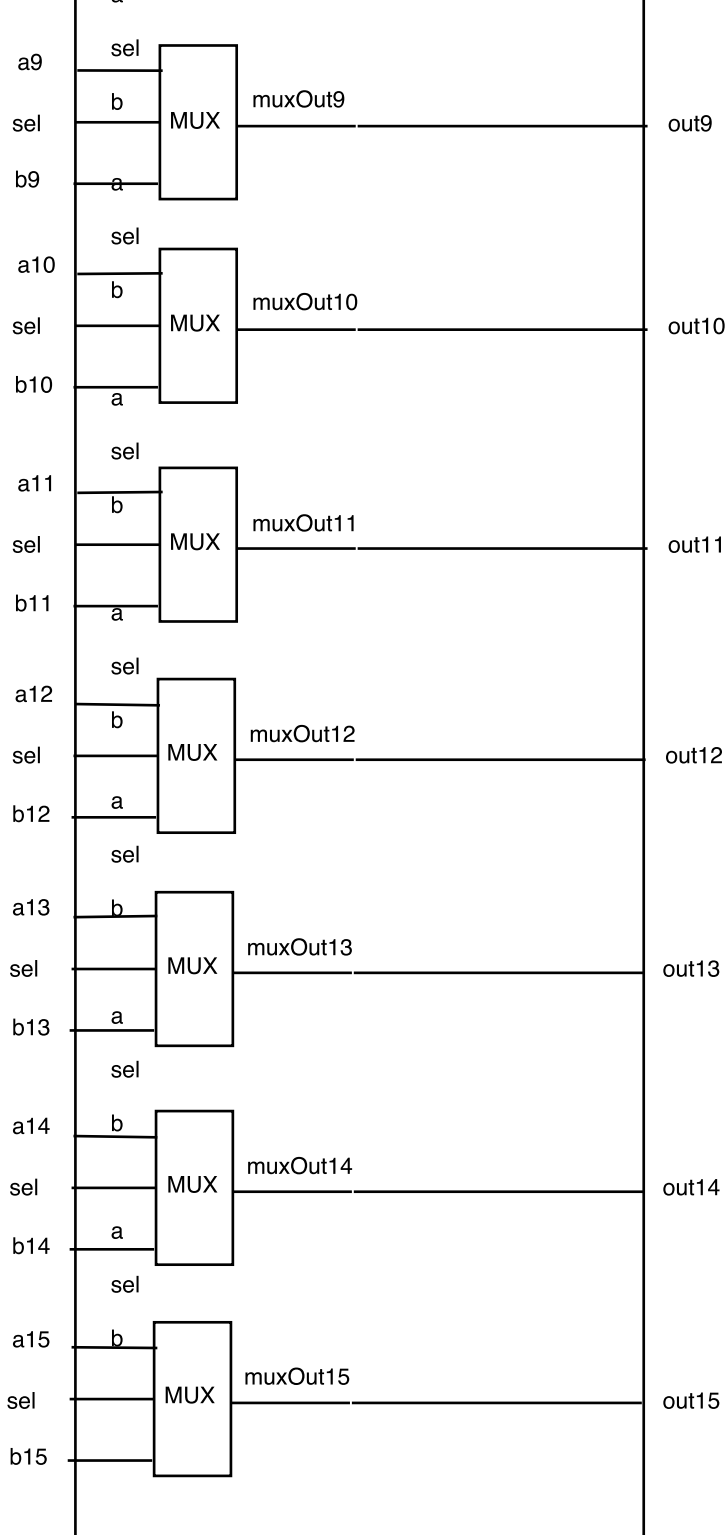
# MUX16

inA16  
sel  
inB16

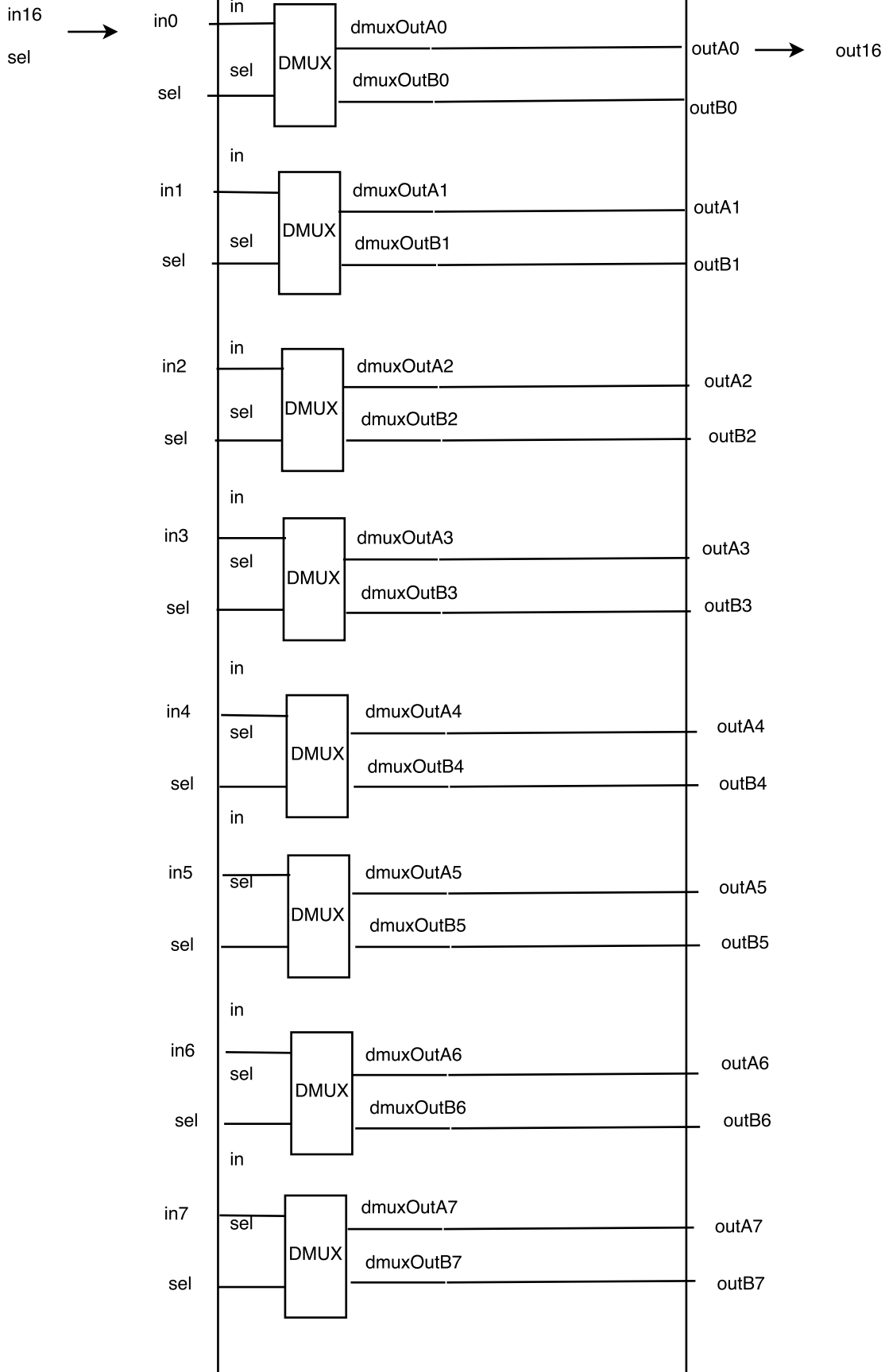


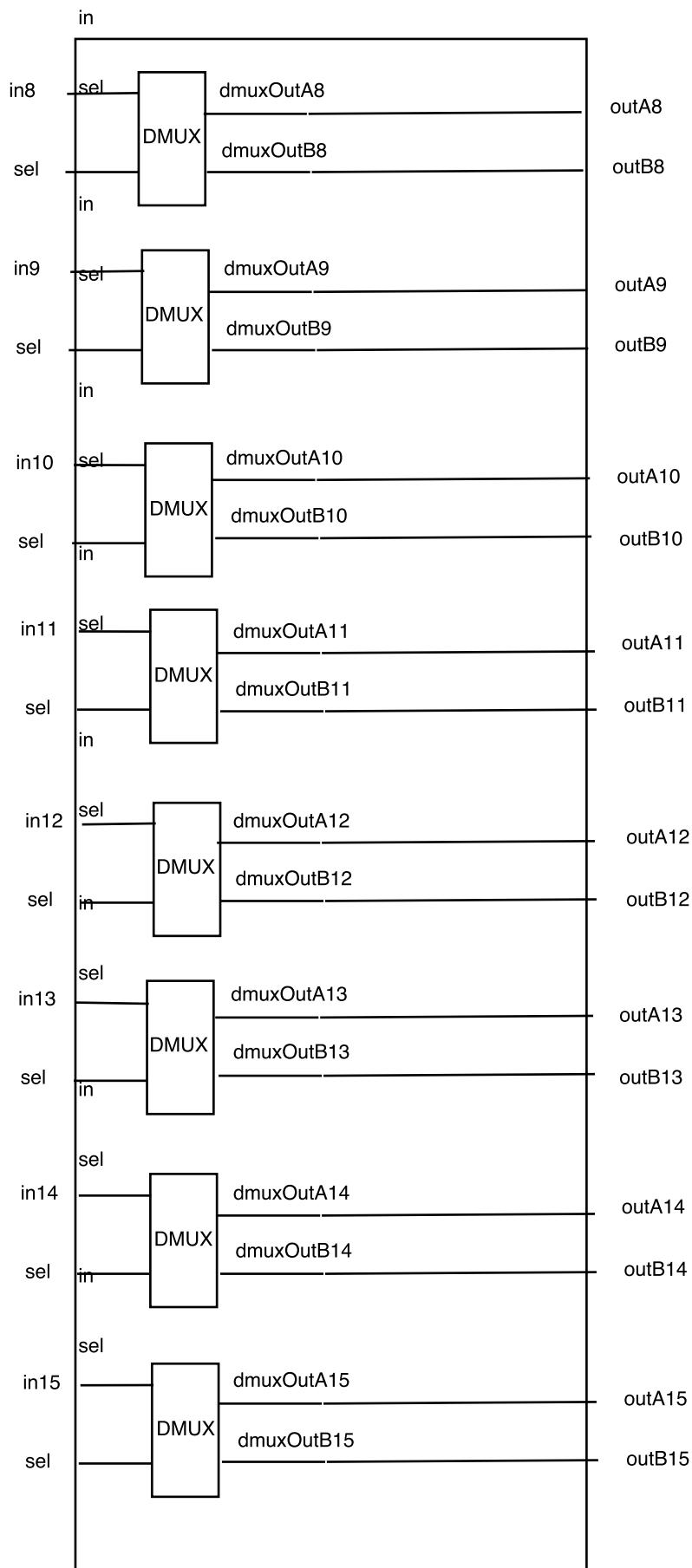
out16





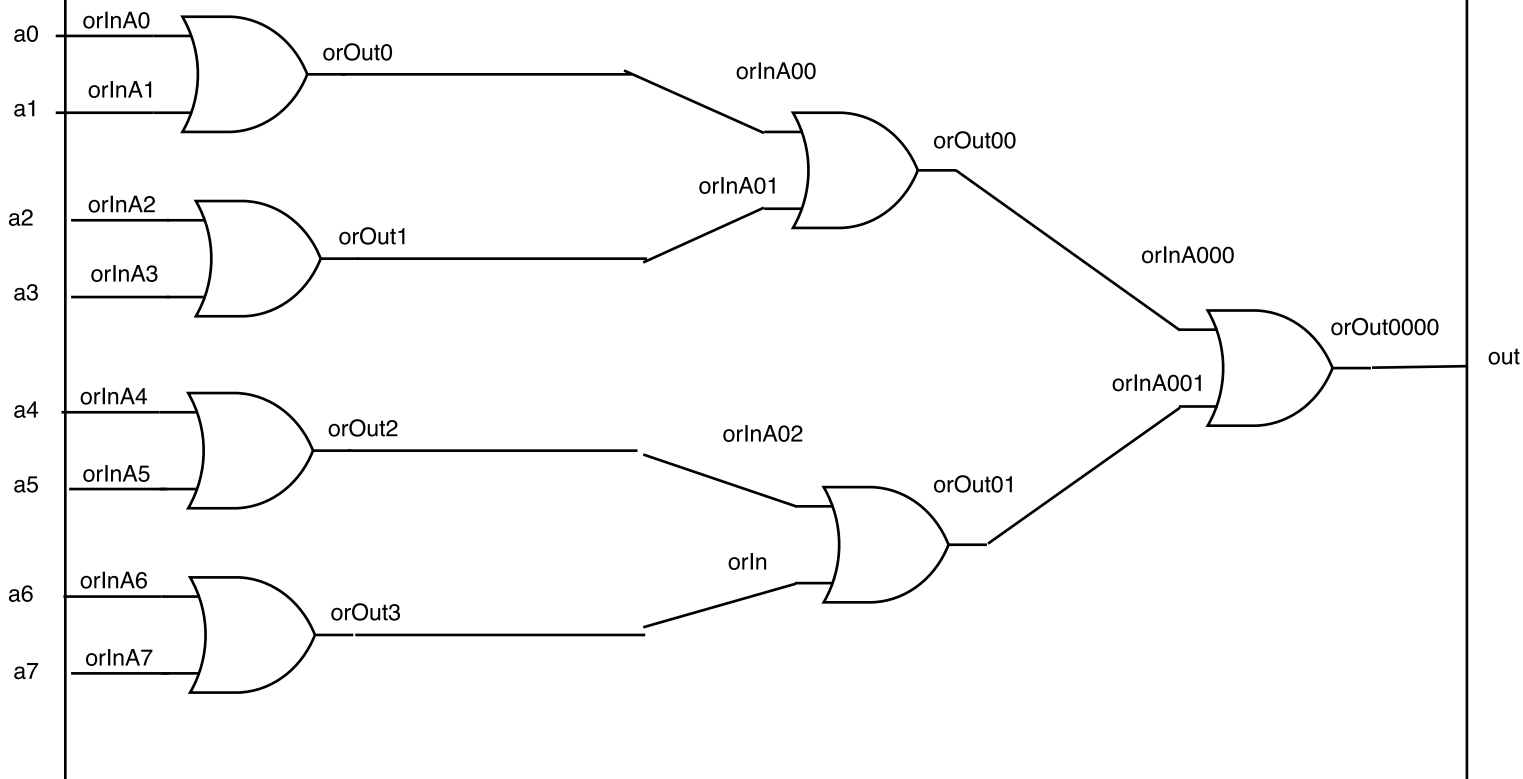
# DMUX16



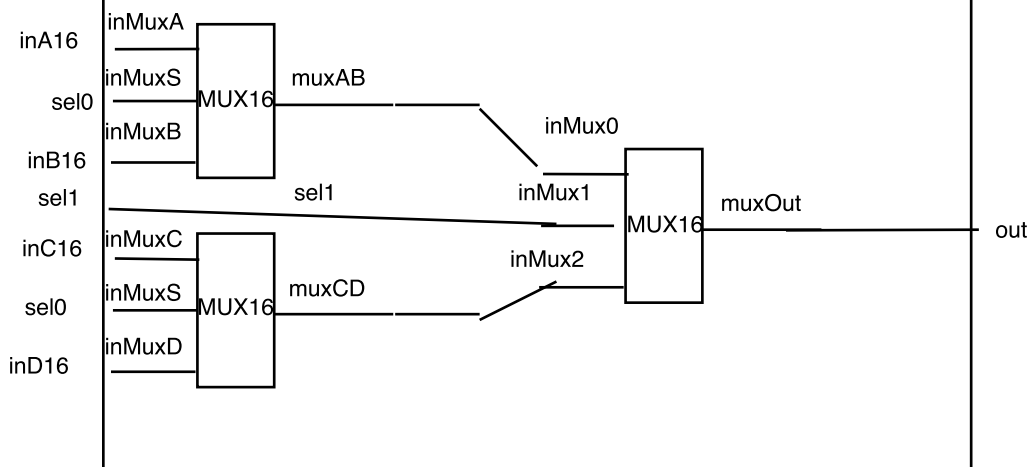


inA8  
↓

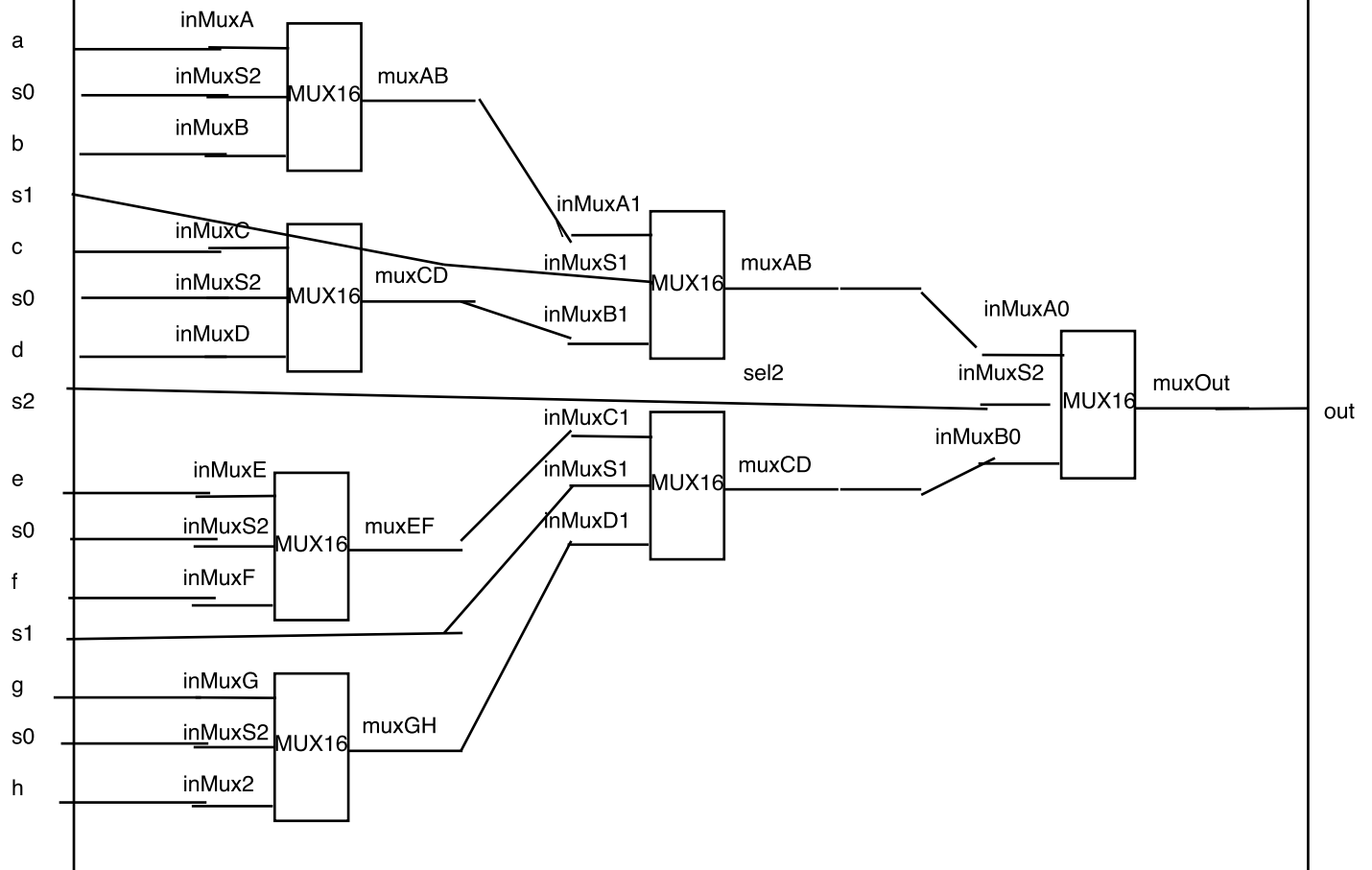
## OR8Way



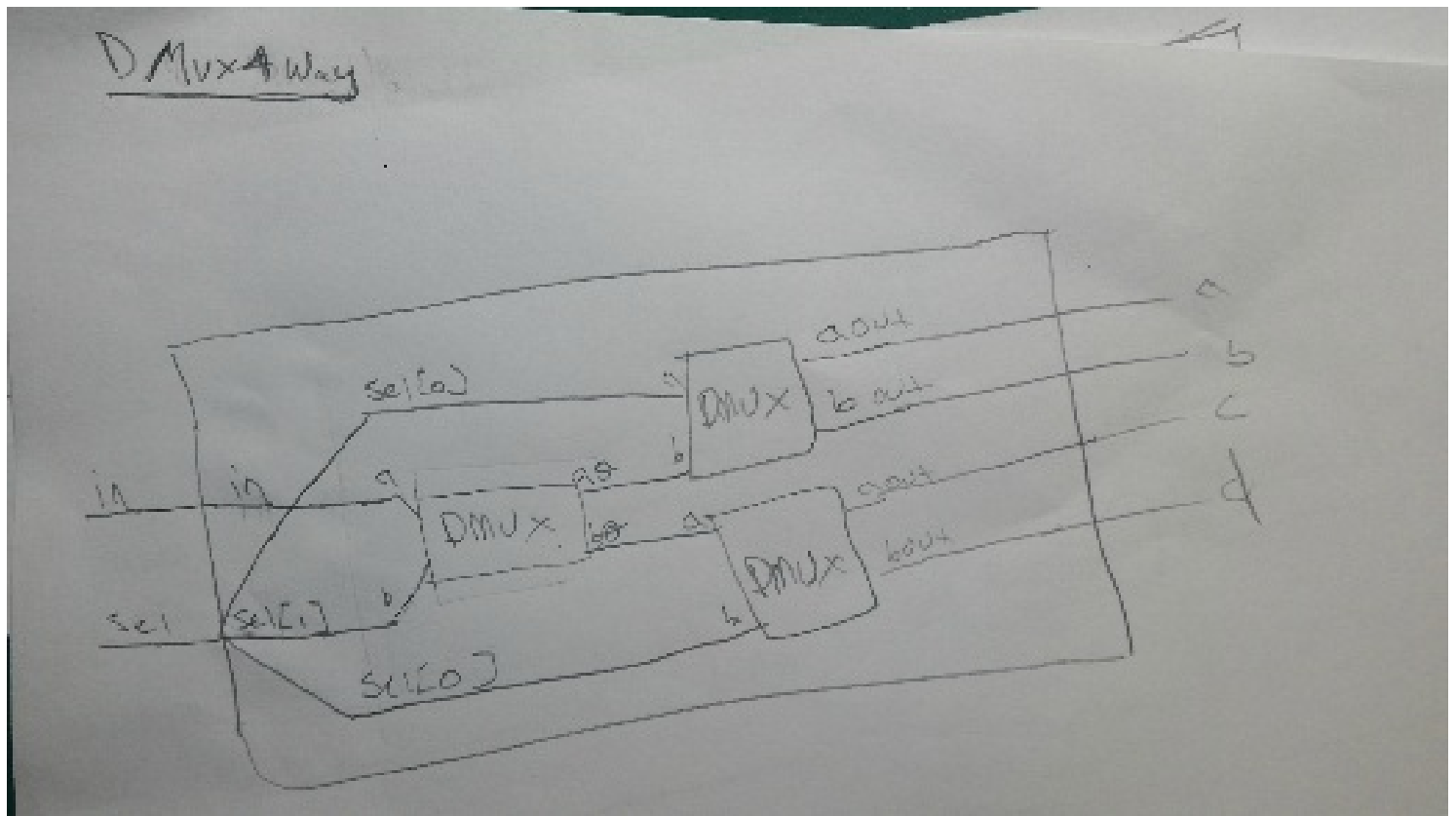
## Mux4Way16



# Mux8Way16



## DMux4Way



## DMux8Way

