Freescale Semiconductor
User Guide

APS12XDT512SLKUG
Rev. A, 7/2006

APPLICATION MODULE STUDENT LEARNING KIT FEATURING FREESCALE MC9S12XDT512

For use with the following part numbers:

CSM12D with MC9S12XDT512 chipset
APS12XDT512SLK
PBS12XDT512SLK

freescale™
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REVISION HISTORY

Date	Rev	Comments
July 26, 2005	A	Initial Release
March 7, 2006	B	Updated document format. Updated IO header table.
July 28, 2006	C	Updated document. Split into DT256 and DT512

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the APS12XDT512SLK board:

a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS B product.

b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development module uses option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed - jumper is installed such that 2 pins are connected together

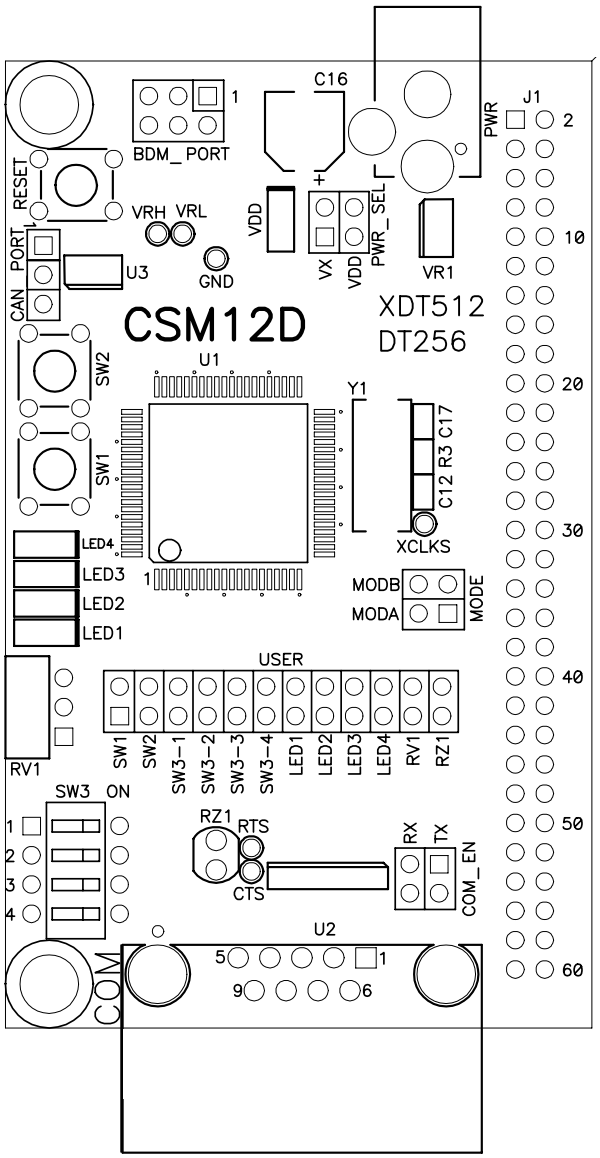
Jumper off, out, or idle - jumper is installed on 1 pin only. It is recommended that jumpers be idled by installing on 1 pin so they will not be lost.

FEATURES

The APS12XDT512SLK is an educational development module supporting the Freescale MC9S12XDT512 or the MC9S12DP256 MCU's. This module is designed to be used with the Project Board Student Learning Kit (PBMCUSLK) or as a stand-alone board. Application development is quick and easy with the included software tools, and examples. The module may be programmed from the on-board BDM header or from the integrated USB-ML12 BDM on the MCUSLKA. A single 60-pin connector directly interfaces to the MCUSLKA.

Features:

- MC9S12XDT512 MCU, 80 LQFP (-100)
- X-GATE Co-Processor
- 512 KB Flash EEPROM
- 4KB EEPROM
- 20 KB SRAM
- 8-ch, 10-bit, ATD w/ external trigger
- 8-bit Enhanced Capture Timer with IC, OC, and Pulse Accumulate capabilities
- 7-ch, 8-bit PWM
- 9 KBI inputs
- 56 GPIO
- 3 CAN Channels
- CAN 2.0 A/B PHY w/ 3-pos header
- 2 SCI Channels
- RS-232 transceiver w/ 2 DB9 connectors
- 2 SPI Channels
- 1 IIC Channel
- 4 MHz Clock Oscillator
- Low Voltage Reset Supervisor
- Power Input Selection Header
- On-board 5V regulator
- Power Input from MCU I/O Connector
- Power Output from MCU I/O Connector
- User Components Provided
- 1 DIP Switch, 4-pos
- 3 Push Button Switches: 2 User, RESET
- 5 LED Indicators: 4 User, +5V
- Jumpers
- USER_EN
- PWR_SEL
- COM_EN
- Connectors
- 1 60-pos pin-header providing access to MCU IO signals
- 2.0mm barrel connector power input
- 6-pin BDM interface connector
- 3-pos CAN connector
- DB9 COM connectors



Specifications:
Module Size 3.5” x 2.5”
Power Input: +9V typical, +6V to +20V

References

Reference documents are provided on the support CD in Acrobat Reader format.

APS12XDT512SLK_UG_A.pdf	APS12XDT512SLK User Guide (this document)
HCS12DT256SLKSCHEMREVC.pdf	APS12DT256SLK Schematic Rev. C
HCS12XDT512SLKSCHEMREVC.pdf	APS12XDT512SLK Schematic Rev. C
APS12XDT512SLK_QSG.pdf	Quick Start Guide for the stand alone operation
APS12XDT512SLK_DEMO.zip	CodeWarrior Project to support APS12XDT512SLK_QSG
PBS12XDT512SLK_QSG.pdf	Quick Start Guide for use with the Project Board (PBMCUSLK)
PBS12XDT512SLK_DEMO.zip	CodeWarrior Project to support PBS12XDT512SLK_QSG
9S12XDP512V2_ZIP.zip	MC9S12XDP512 Device User Guide
AN2546.pdf	S12X Load RAM and Execute (LRAE) Program Application Note
AN2615.pdf	HC(S)12 and S12X Family Compatibility
AN2685.pdf	How to Configure and Use the XGATE on S12X Devices
AN2708.pdf	An Introduction to the External Bus Interface on the HC(S)12X

GETTING STARTED

The module ships from the factor with a small demonstration pre-programmed into flash memory. This program will print a welcome message out the COM connector and flash the LED’s. The Quick Start Guide included in the module kit will describe the steps necessary to configure board for operation.

Programming the module requires the use of a BDM such as P&E Microcomputer System’s BDM Multilink. There is no BDM included in the kit when shipped. This is a separate item. The included CodeWarrior IDE from Metrowerks also supports programming the module. Refer to the CodeWarrior quick-start and user manual for further details.

Operating Modes

The APS12XDT512SLK board operates in two operating modes: Run Mode, or Debug Mode. Run Mode allows user application code to execute from Power-On or Reset. Debug Mode supports the development and debug of application code. See the related sections below for quickly starting the board in the desired operation mode.

RUN MODE

Run mode allows user application to execute when power is applied to the board. Use the following settings to configure the APS12XDT512SLK board for RUN Mode to get started quickly.

1. Connect a COM port serial communication cable between board and host PC if needed for the application. Launch supporting host communication software as needed.

2. Connect auxiliary equipment to board as required by application.

3. Configure the board option jumpers for run mode.

Table 1: Run Mode Setup

PWR_SEL	PWR (pos 2)
COM_EN	As Required
USER	As Required

4. Apply power to the board.

5. The programmed application should begin to execute.

Debug Mode

Debug Mode supports application development and debug. Debug mode is available to the user through the integrated USB-BDM on the PBMCUSLK or an external HC(S)12 BDM cable. Refer to the PBMCUSLK User Guide for details on using the integrated USB-BDM. A 6-pin BDM interface header (BDM_PORT) supports the use of an external HC(S)12 BDM cable.

The steps below describe using an ***external*** HC(S)12 BDM cable to access DEBUG mode.

1. Install and launch P&E PKG12Z tool set, CodeWarrior Development Studio, or other software capable of communicating with the HC(S)12 MCU.

2. Connect the HC(S)12 BDM cable to the BDM_PORT header.

3. Connect COM port serial communication cable between board and host PC if needed by the application. Launch supporting host communication software as needed.

4. Connect auxiliary equipment to the module if needed by the application.
5. Configure the board option jumpers for DEBUG mode.

Table 2: BDM Mode Setup

PWR_SEL	PWR
COM_EN	As Required
USER	As Required

6. Connect the supplied USB cable between an available USB port on the host PC and the USB connector on the board.
7. Hosting development software will establish DEBUG communication.

DEvelopment support

Software Development

Software development will require the use of an HC(S)12 assembler or compiler and a host PC operating a debug interface. The assembler should also support the HC(S)12 X-Gate command set if attempting application development on the MC9S12XDT512 MCU. Supplied with this board is the CodeWarrior Development Studio along with the Axiom IDE for Windows for debugging and flash programming.

MEMORY MAP

The APS12XDT512SLK is designed to support the MC9S12D family of MCU's specifically the MC9S12XDT512. This section shows the default memory map for both MCU's immediately out of reset. Refer to the Device User Guide for the specific MCU installed for further details.

MC9S12XDT512

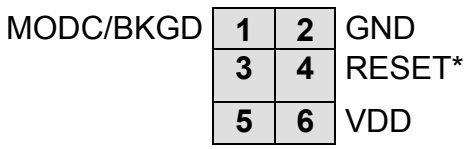
Table 3: XDT512 Memory Map

0x0000 – 0x07FF	Registers	2 K bytes	
0x0800 – 0x0BFF	Paged EEPROM	4K bytes	4 – 1Kb pages
0x0C00 – 0x0FFF	Fixed EEPROM	1K bytes	
0x1000 – 0x1FFF	Paged RAM	20 KB	5 – 4Kb pages
0x2000 – 0x3FFF	Fixed RAM	8K bytes	
0x4000 – 0x7FFF	FIXED FLASH	16 KB	1K, 2K, 4K, 8K Protected Boot Sector
0x8000 – 0xBFFF	Paged FLASH	512K bytes	32 – 16Kb pages
0xC000 – 0xFEFF	FIXED FLASH	16 KB	2K, 4K, 8K, 16K Protected Boot Sector
0xFF00 – 0xFFFF	Vectors	255 bits	

BDM_PORT Header

A 6-pin BDM port header allows connection of a HC(S)12 compatible BDM cable for application development. Refer to the BDM cable documentation for details on use of the BDM cable with this module.

Figure 1: BDM_PORT



See the HC12 Reference Manual for complete DEBUG documentation

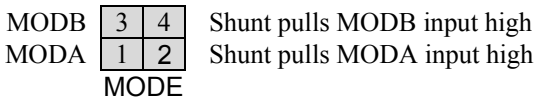
Expanded Mode Operation

For the APS12XDT512SLK module, expanded mode operation is not supported or available to the user. The data bus is not bonded out on the MCU. Operational modes include only single-chip mode. *Please refer to the APS12DT256SLK for expanded mode operation capable device.*

MODE

By default, the MC9S12XDT512 MCU's are configured for single-chip operation. The MODE option header allows the user to configure the board for expanded bus operation. In default configuration, this header is not installed in default configurations.

Figure 2: MODE Option Header



NOTE: Expanded bus mode operation is supported only when a 9S12DT256 MCU is installed on the MCU.

POWER

The APS12XDT512SLK is designed to be used with and powered from the PBMCUSLK. The APS12XDT512SLK will source power from the PBMCUSLK through connector J1. The module may also be used as a stand-alone platform. As a stand-alone platform, the module may be powered through the 2.1mm barrel connector and on-board regulator or through connector J1. The module may also be configured to provide power to external circuitry connected to J1. When powering external circuitry, do not exceed the maximum output current limit of the on-board regulator.

The on-board voltage regulator (VR1) accepts power input through a 2.1mm barrel connector (PWR). Input voltage may range from +7V to +18V. The voltage regulator (VR1) provides a +5V fixed output voltage with current output limited to 250mA. Over-temperature and over-current limit built into the voltage regulator provides protection from excessive stresses. Do not exceed the maximum output current limit of VR1 when attempting to power off-board circuitry through connector J1.

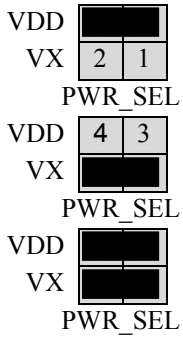
POWER SELECT

Power may be applied to the board through a 2.0mm barrel connector, or through connector J1. Optionally, power may be routed through connector J1 to supply external circuitry. Power selection is achieved by using a 4-pos selection header. When attached to the MCUSLKA, power is provide by the project board through connector J1.

Use caution when configuring this selection header. Applying power to the module through the on-board regulator and connector J1 at the same time may cause damage to the module.

PWR_SEL

Figure 3: PWR_SEL Option Header



Source power input from barrel connector PWR.

Source power input from connector J1.

Source power from barrel connector PWR and supply power to external circuitry connected to J1.

NOTE: Exercise caution when configuring this selection header. Improper configuration may damage the module.

RESET Switch

The RESET switch provides a method to apply an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. Pressing the reset switch causes the reset supervisor at LV1 to assert RESET for 150 ms. A pull-up bias resistor allows normal MCU operation. Shunt capacitance ensures an adequate input pulse width.

Low Voltage RESET

A DS1813, low-voltage supervisor at LV1 protects the APS12XDT512SLK under-voltage conditions. LV1 will assert RESET when the 5V rail falls below the trip point of 4.62V. LV1 will asserted RESET for approximately 150ms after voltage returns to nominal.

Timing

Timing input to the MCU is provided by a 4 MHz, fundamental frequency, crystal oscillator. The oscillator exhibits a frequency tolerance of ±30ppm. The timing input is configured for full-swing Pierce mode operation in both MCU configurations.

The XCLKS output is routed to test point VIA located near the MCU. The internal clock ECLKX2 is available at this via if needed. The user can also use the XCLKS signal via to configure the 9S12XDT512 for low-power Pierce mode timing input. Refer to the 9S12XDT512 Device User Guide for details.

COMMUNICATIONS

The APS12XDT512SLK module provides the user with 1 COM port and 1 CAN port on the module. COM1 is links to SCI0 on the MCU. The RS-232 channel is configured as a DCE device. This allows a straight through cable between the module and the host PC.

Both MCU's provide 2 additional CAN ports, 2 SPI ports, and 1IIC port. Access to these communications ports is provided through connector J1. Physical layer support is not provide for these feature and must be provided by the user in needed. Refer to the MCU Device User Guide for details

RS-232

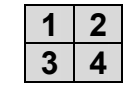
An RS-232 translator provides RS-232 to TTL/CMOS logic level translation on the COM connector. The COM connector is a 9-pin Dsub, right-angle connector. A ferrite bead on shield ground provides conducted immunity protection. Communication signals TXD and RXD are routed from the transceiver to the MCU. Communications signals TXD and RXD also connect to general purpose Port S signals on the MCU.

Table 4: COM Connections

MCU Port	COM Signal	I/O PORT CONNECTOR
PS1/TXD0	TXD0	J1-5
PS0/RXD0	RXD1	J1-7
PS3/TXD1	TXD1	J1-40
PS2/RSXD1	RXD1	J1-38

Communications signals Tx/Rx route to connector J1 for use off-module if desired. When using these signal to drive off-module RS-232 devices or when attempting alternate communications protocols such at IrDA or LIN, the user should disconnect the on-board RS-232 transceiver. The COM_EN header block allows the user to selectively disable each of the 4 communications signals.

Figure 4: COM_EN Header

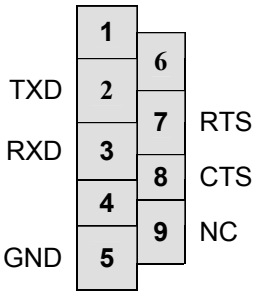


Enable/Disable TX to transceiver
Enable/Disable RX to transceiver

COM Connector

A standard 9-pin Dsub connectors provide external connection for COM1. The Dsub shell is connected to board ground through a ferrite bead. The ferrite bead provides noise isolation on the RS-232 connection. The figure below details the DB9 connector.

Figure 5: COM Connector



Female DB9 connector that interfaces to the MCU internal SCI0 serial port via the RS232 transceiver. It provides simple 2 wire asynchronous serial communications without flow control. Flow control is provided at test points on the board. A straight-through cable is used to connect the module to a DTE device such as a host PC.

Pins 1, 4, and 6 are connected together.
Pins 7 and 8 are connected together.

MSCAN

The APS12XDT512SLK provides one PCA82C250 high-speed CAN physical interface. A 3-pin connector provides connectivity to the off-board CAN bus. The CAN PHY connects to the CAN0 channel on the MCU. The PHY supports data rates up to 1 Mbps with slew-rate control. The figure below shows the pin-out of the CAN_PORT connector.

Figure 6. CAN_PORT Connector

1	CAN_H
2	GND
3	CAN_L

The CAN PHY connects to the CAN0 channel in the MCU

Both MCU's provide support for additional CAN channels. All CAN channels supported are routed to the connector J1 for use if needed. Consult the Device User Guide for the installed MCU for further details.

VRH/VRL

MCU inputs VRH and VRL provide the upper and lower voltage reference for the analog to digital (ATD) converter. By default, VRH is tied to VDD and VRL is tied to ground. Adequate filtering has been added to provide a voltage reference with minimal ripple. Either, or both, references may be isolated to provide alternate ATD input references. A test point via on each signal, labeled VRH, or VRL, provides an easy way to attach an alternate reference voltage.

A 0-ohm configuration resistor allows isolation of each reference voltage. Removing R10 isolates VRH while removing R12 isolates VRL. Install a suitably sized 0-ohm resistors in these locations to restore the board to its default configuration.

Care must be exercised when using alternate input references. The associated configuration resistor must be removed before applying an alternate voltage reference or the board may be damaged. Also, no input protection is provided; incorrect configuration will damage the MCU. The table below summarizes the changes necessary to use alternate VRH and/or VRL.

Table 5: ATD Reference Voltage

	Installed (Default)	Removed
R4	VRH = VDD	VRH provided by user
R5	VRL = GND	VRL provided by user

NOTE: Damage to the board may result if an alternate reference voltage is attached without first removing the associated configuration resistor.

USER I/O

User I/O includes 2 push button switches, one 4-position DIP switch, 4 green LEDs, a potentiometer, and a photo-sensor. The sections below provide details on each User I/O. The User option header block enables or disables each User I/O individually.

Switches

The APS12XDT512SLK target board provides 2 push button switches and one 4-position DIP switch for user input. Each push button switch is an active low input with a pull-up resistor bias to prevent indeterminate input conditions. Pressing a push-button switch causes a low logic input on the associated input.

Each DIP switch position is an active low input. Use of the DIP switches requires enabling the associated PORTB pull-ups internal to the MCU prevent indeterminate input conditions. Moving a DIP switch position to ON causes a low logic level on the associated input. Table 6 shows the associated connection signal for each switch. Table 7 shows the associated USER enable position to enable each switch.

LED's

The APS12XDT512SLK target board provides 4 green LEDs for output indication. Each LED is an active low output. A current-limit resistor prevents excessive diode current. Writing a low logic level to an LED output causes the associated LED to turn on. Table 6 shows the associated connection signal for each LED. Table 7 shows the associated USER enable position to enable each LED.

POT

A single-turn, 3/8 inch, 5K ohm trimmer potentiometer (POT) has been provided as user, analog input. The part is decoupled to minimize noise during adjustment. The POT connects

to analog input PAD05/AN05 on the MCU. Table 6 shows the associated connection signal for the POT. Table 7 shows the associated USER enable position to enable the POT.

Photo-Sensor

A 4mm photocell light sensor exhibiting 23K – 33K ohms of output resistance has been provided. Output resistance is inversely related to incident light intensity. A gain stage (U5) amplifies the sensor output before connecting to the MCU. The SENSOR connects to analog input PAD04/AN04 on the MCU. Table 6 shows the associated signal connection for the sensor. Table 7 shows the associated USER enable position to enable the sensor.

Signals

The following table shows the connections for each user I/O device.

Table 6: User I/O

USER	Ref Des	Signal	Device
1	SW1	PP0/KWP0/PWM0/MISO1	Push Button Switch
2	SW2	PP1/KWP1/PWM1/MOSI1	Push Button Switch
3	SW3-1	PB0/ADDR0/DATA0	4-pos DIP Switch
4	SW3-2	PB1/ADDR1/DATA1	4-pos DIP Switch
5	SW3-3	PB2ADDR2/DATA2	4-pos DIP Switch
6	SW3-4	PB3/ADDR3/DATA3	4-pos DIP Switch
7	LED1	PB4/ADDR4/DATA4	Green LED
8	LED2	PB5/ADDR5/DATA5	Green LED
9	LED3	PB6/ADDR6/DATA6	Green LED
10	LED4	PB7/ADDR7/DATA7	Green LED
11	RV1	PAD05/AN05	Potentiometer
12	RZ1	PAD04/AN04	Light Sensor

Enables

The User option header block enables or disables each User I/O device individually. User I/O includes 4 green LEDs, 2 push button switches, one 4-position DIP switch, a Light Sensor, and a potentiometer. Installing a shunt enables the associated option. Removing a shunt disables the associated option. The table below shows the configuration option for each USER I/O.

Table 7: USER Option Header

			Shunt		
	USER		Installed	Removed	Description
SW1	**1**	**2**	Enable	Disable	Push Button Switch 1
SW2	**3**	**4**	Enable	Disable	Push Button Switch 2
SW3-1	**5**	**6**	Enable	Disable	DIP Switch Position 1
SW3-2	**7**	**8**	Enable	Disable	DIP Switch Position 2
SW3-3	**9**	**10**	Enable	Disable	DIP Switch Position 3
SW3-4	**11**	**12**	Enable	Disable	DIP Switch Position 4
LED1	**13**	**14**	Enable	Disable	LED 1
LED2	**15**	**16**	Enable	Disable	LED 2
LED3	**17**	**18**	Enable	Disable	LED 3
LED4	**19**	**20**	Enable	Disable	LED 4
RV1	**21**	**22**	Enable	Disable	Potentiometer
RZ1	**23**	**24**	Enable	Disable	Light Sensor

MCU I/O PORT

Connector J1 provides access to the MC9S12XDT512 and MC9S12DT256 I/O signals. The figures below show the pin-out for the MCU I/O connector. Only signal XCLS is not available at connector J1.

Figure 7: Connector J1

V_{AUX}	1	2	PE1/IRQ*
GND	3	4	RESET*
PS1/TXD0	5	6	MODC/BKGD
PS0/RXD0	7	8	PP7/KWP7/PWM7/SCK2
PP0/KWP0/PWM0/MISO1	9	10	PAD07/AN07
PP1/KWP1/PWM1/MOSI1	11	12	PAD06/AN06
PT0/IOC0	13	14	PAD05/AN05
PT1/IOC1	15	16	PAD04/AN04
PM4/RXCAN2/RXCAN0/RXCAN4/MOSI0	17	18	PAD00/AN00
PM2/RXCAN1/RXCAN0/MISO0	19	20	PAD01/AN01
PM5/TXCN2/TXCAN0/TXCAN4/SCK0	21	22	PAD02/AN02
PM3/TXCAN1/TXCAN0/SS0*	23	24	PAD03/AN03
PA7	25	26	PJ7/KWJ7/TXCAN4/SCL0
PA6	27	28	PJ6/KWJ6/RXCAN4/SDA0
PA5	29	30	PP2/KPP2/PWM2/SCK1
PA4	31	32	PP3/KWP3/PWM3/SS1*
PA3	33	34	PP4/KWP4/PWM4/MISO2
PA2	35	36	PP5/KWP5/PWM5/MOSI2
PA1	37	38	PS2/RXD1
PA0	39	40	PS3/TXD1
PB7	41	42	PE0/XIRQ*
PB6	43	44	PE2
PB5	45	46	PE3
PB4	47	48	PE4
PB3	49	50	PT2/IOC2
PB2	51	52	PT3/IOC3
PB1	53	54	PT4/IOC4
PB0	55	56	PT5/IOC5
PM1/TXCAN0	57	58	PT6/IOC6
PM0/RXCAN0	59	60	PT7/IOC7

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