MC9S12NE64
Device User Guide
V01.04

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Motorola, Inc.

Revision History

Version Number	Revision Date	Author	Description of Changes
01.00	25.MAR.03		Original Version.
01.01	01.MAY.03		Updated.
01.02	08.MAY.03		Updated register table. Electrical section.
01.03	27.MAY.03		Updated per initial SoCGuide review.
01.04	07.OCT.03		Typo fixes, Updated electricals.

Table of Contents

Section 1 Introduction

Section 2 Signal Description

Section 3 System Clock Description

Section 4 Modes of Operation

Section 5 Resets and Interrupts

Section 18 Port Integration Module (PIM) Block Description

Section 19 Flash EEPROM 64K Block Description

Section 20 RAM 8K Block Description

Appendix A Electrical Characteristics

Appendix B Electrical Specifications

Appendix C External Bus Timing

Appendix D Package Information

List of Figures

List of Tables

Document References

The Device User Guide provides information about the MC9S12NE64 device made up of standard HCS12 blocks and the HCS12 processor core. This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block Guides of the implemented modules. In a effort to reduce redundancy, all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-1 Document References

Block Guide	Acronym	Version	Document Order Number
Analog to Digital Converter: 10-Bit, 8 Channels	ATD_10B8C	V02	S12ATD10B8CV2/D
Background Debug Module	BDM	V04	S12BDMV4/D
Central Processor Unit	CPU	V02	S12CPUV2/D
Clock and Reset Generator	CRG	V04	S12CRGV4/D
Debug Module	DBG	V01	S12DBGV1/D
Ethernet Media Access Controller	EMAC	V01	S12EMACV1/D
Ethernet Physical Transceiver	EPHY	V01	S12EPHYV1/D
64Kbyte Flash EEPROM	FTS64K	V02	S12FTS64KV2/D
Inter IC Bus	IIC	V02	S12IICV2/D
Interrupt	INT	V01	S12INTV1/D
Multiplexed Expanded Bus Interface	MEBI	V03	S12MEBIV3/D
Module Mapping Control	MMC	V04	S12MMCV4/D
Oscillator	OSC	V02	S12OSCV2/D
Port Integration Module	PIM_9NE64	V01	S12PIM9NE64V1/D
Serial Communications Interface	SCI	V03	S12SCIV3/D
Serial Peripheral Interface	SPI	V03	S12SPIV3/D
Timer: 16-Bit, 4 Channels	TIM_16B4C	V01	S12TIM16B4CV1/D
Voltage Regulator	VREG_PHY	V01	S12VREGPHYV1/D

Part Number

Table 0-2 lists the part number coding based on the package and temperature.

Table 0-2 Package Option Summary

Package	Device	Part Number	Mask Set	Temp. Options	Flash	RAM	I/O
80QFP	MC9S12NE128	MC9S12NE128	TBD	C	128K	12K	38
112LQFP	MC9S12NE128	MC9S12NE128	TBD	C	128K	128K	70
80QFP	MC9S12NE64	MC9S12NE64	0L19S	C	64K	8K	38
112LQFP	MC9S12NE64	MC9S12NE64	0L19S	C	64K	8K	70

Figure 0-1 provides an ordering number example.

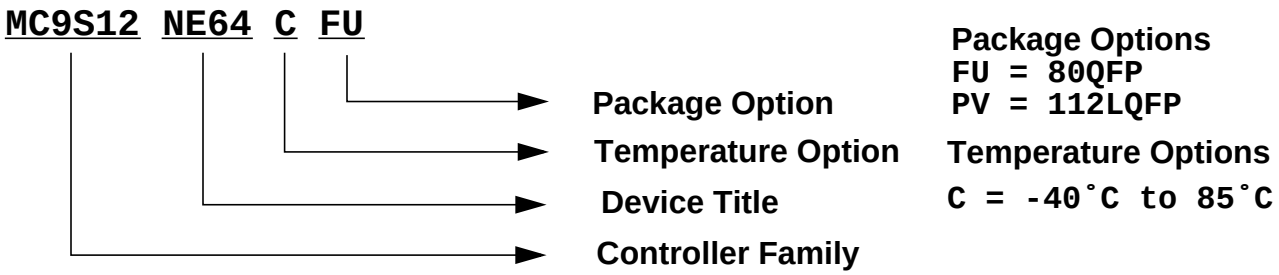


Figure 0-1 Order Part Number Coding

Table 0-3 lists the part number coding based on the package and temperature.

Table 0-3 Package Option Summary

Part Number	Mask Set	Temp	Package	Speed	Description
MC9S12NE128CFU	TBD	-40˚C, 85˚C	80QFP	25MHz	
MC9S12NE128CPV	TBD	-40˚C, 85˚C	112LQFP	25MHz	
MC9S12NE64CFU	0L19S	-40˚C, 85˚C	80QFP	25MHz	
MC9S12NE64CPV	0L19S	-40˚C, 85˚C	112LQFP	25MHz	

Section 1 Introduction

1.1 Overview

The MC9S12NE-Family is a 112/80 pin low cost, low-end connectivity applications MCU family. The MC9S12NE-Family is comprised of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 64K bytes of Flash EEPROM, 8K bytes of RAM, Ethernet Media Access Controller (EMAC) with integrated 10/100M Physical transceiver (EPHY), two asynchronous serial communications interface modules (SCI), a serial peripheral interface (SPI), one Inter IC Bus (IIC), a 4-channel 16-bit timer module (TIM), a 8-channel 10-bit analog-to-digital converter (ADC), up to 21 pins available as Keypad Wake-Up inputs (KWU) and two additional external asynchronous interrupts. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. Furthermore, an on-chip bandgap based voltage regulator (VREG) generates the internal digital supply voltage of 2.5V (VDD) from a 3.15V to 3.45V external supply range. The MC9S12NE-Family has full 16-bit data paths throughout. The 112 pin package version has a total of 70 I/O port pins and 10 input only pins available. The 80 pin package version has a total of 38 I/O port pins and 10 input only pins available.

1.2 Features

- 16-bit HCS12 CORE
  - HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer’s model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
  - MMC (memory map and interface)
  - INT (interrupt control)
  - BDM (background debug mode)
  - DBG12 (enhanced debug12 module, including breakpoints and change-of-flow trace buffer)
  - MEBI: Multiplexed Expansion Bus Interface (available only in 112 pin package version)
- Wake-up interrupt inputs
  - Up to 21-port bits available for wake up interrupt function with digital filtering
- Memory options
  - 64K Bytes of Flash EEPROM
  - 8K Bytes of RAM
- Analog-to-Digital Converter
  - One 8-channel module with 10-bit resolution.

  - External conversion trigger capability
- Timer Module (TIM)
  - 4-Channel Timer
  - Each Channel Configurable as either Input Capture or Output Compare
  - Simple PWM Mode
  - Modulo Reset of Timer Counter
  - 16-Bit Pulse Accumulator
  - External Event Counting
  - Gated Time Accumulation
- Serial interfaces
  - Two asynchronous serial communications interface (SCI)
  - One synchronous serial peripheral interface (SPI)
  - One inter-IC bus (IIC)
- Ethernet Media Access Controller (EMAC)
  - IEEE 802.3u Medium-Independent Interface (MII)
  - IEEE 802.3x Full Duplex and Flow Control
  - MII Management Interface
  - Address Recognition
    i. frames with broadcast address are always accepted or always rejected
    ii. exact match for single 48-bit individual (unicast) address
    iii. hash (64-bit hash) check of group (multicast) addresses
    iv. promiscuous mode
  - Ethertype Filter
  - Loopback Mode
  - Two Receive and One Transmit FIFO Buffer Interfaces
- Ethernet 10/100M Transceiver (EPHY)
  - IEEE 802.3 Compliant
  - Digital Adaptive Equalization
  - Half and Full duplex
  - Auto-Negotiation Next Page Ability
  - Baseline Wander Correction
  - 125 Mhz Clock Generator and Timing Recovery
  - Integrated wave-shaping circuitry

  - Loopback modes
- CRG (Clock Reset Generator Module)
  - Windowed COP watchdog
  - Real time interrupt
  - Clock monitor
  - Pierce oscillator
  - Phase-locked loop clock frequency multiplier
  - Limp home mode in absence of external clock
  - 25 MHz crystal oscillator reference clock
- Operating frequency
  - 50MHz equivalent to 25MHz Bus Speed for single chip
  - 32MHz equivalent to 16MHz Bus Speed in expanded bus modes
- Internal 2.5V Regulator
  - Supports an input voltage range from 3.3V +/- 5%
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
- 80-Pin QFP or 112-Pin LQFP package
  - Up to 70 I/O lines with 3.3V input and drive capability (112 pin package)
  - Up to 2 dedicated 3.3V input only lines (IRQ, XIRQ)
  - 3.3V 8 A/D converter inputs and 3.3V input only lines
- Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints
  - Enhanced DBG12 debug features

1.3 Modes of Operation

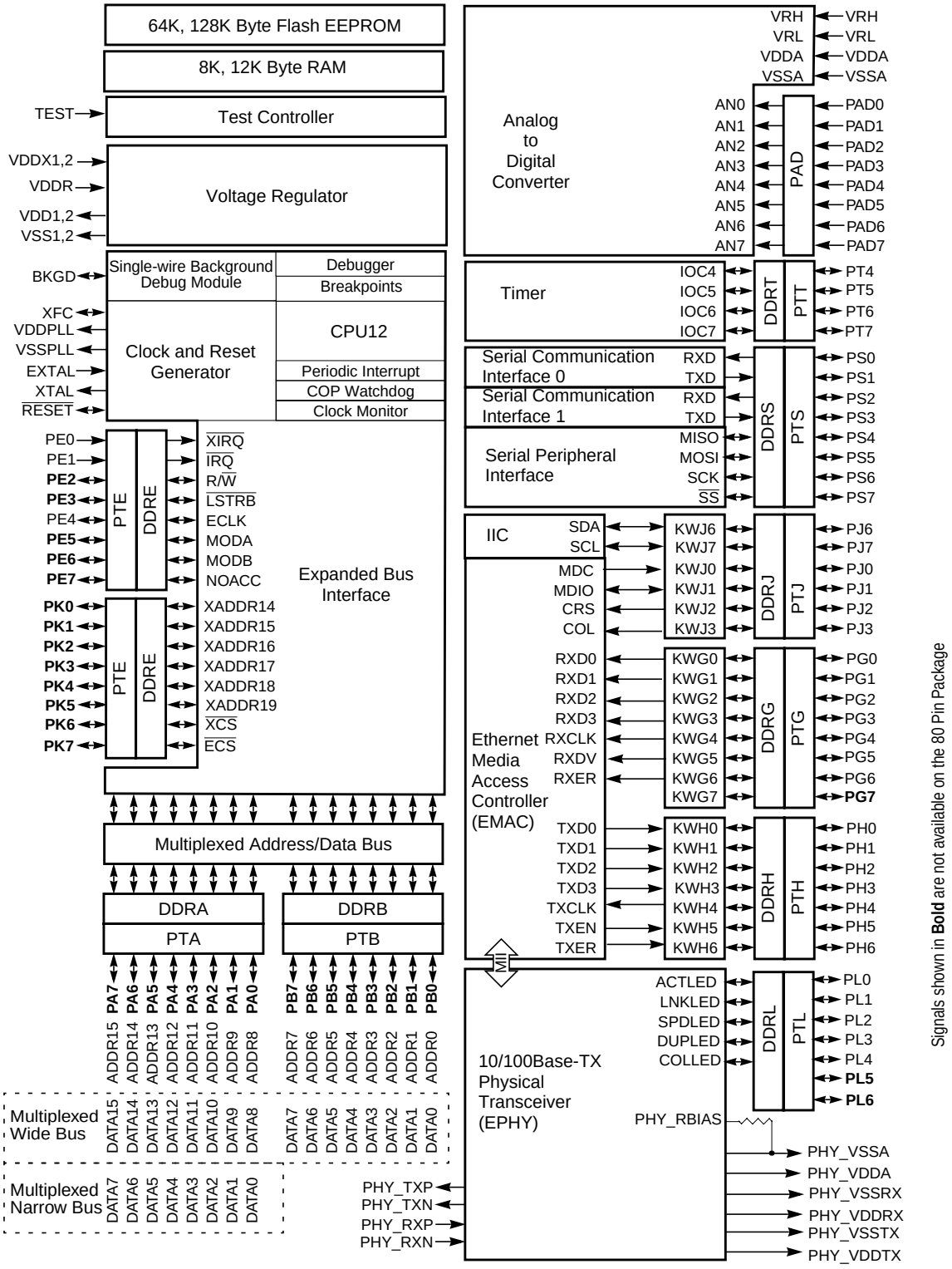
- Normal modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode[1]
  - Normal Expanded Narrow Mode[1]
  - Emulation Expanded Wide Mode[1]

NOTES:
1. Expanded modes are only available in the 112 pin package version.

  - Emulation Expanded Narrow Mode[1]
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode[1] (Motorola use only)
  - Special Peripheral Mode[1] (Motorola use only)
- Each of the above modes of operation can be configured for three Low power submodes
  - Stop Mode
  - Pseudo Stop Mode
  - Wait Mode
- Secure operation, preventing the unauthorized read and write of the memory contents.

1.4 Block Diagram

Figure 1-1 MC9S12NE-Family Block Diagram



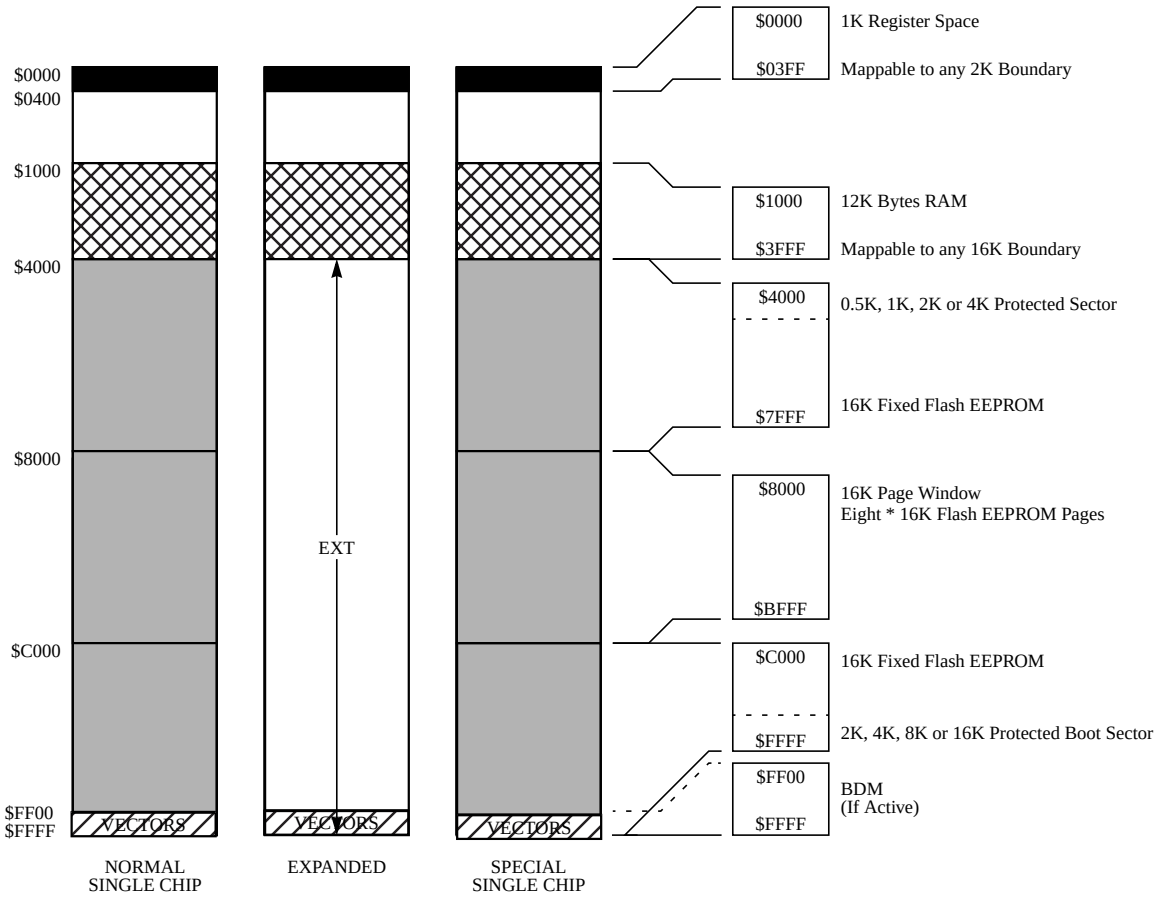
1.5 Device Memory Map

Table 1-1 shows the device register map of the MC9S12NE-Family after reset. **Figure 1-3** and **Figure 1-3** illustrate the full device memory map with flash and RAM.

Table 1-1 Device Register Map Overview

Address	Module	Size
$0000 - $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 - $0019	Reserved	2
$001A - $001B	Device ID register (PARTID)	2
$001C - $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 - $002F	CORE (DBG)	16
$0030 - $0033	CORE (PPAGE, Port K)	4
$0034 - $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 - $006F	Standard Timer 16-bit 4 channels (TIM)	48
$0070 - $007F	Reserved	16
$0080 - $009F	Analog to Digital Converter 10-bit 8 channels (ATD)	32
$00A0 - $00C7	Reserved	40
$00C8 - $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 - $00D7	Serial Communications Interface 1 (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI)	8
$00E0 - $00E7	Inter IC Bus (IIC)	8
$00E8 - $00FF	Reserved	24
$0100- $010F	Flash Control Register	16
$0110 - $011F	Reserved	16
$0120 - $0123	Ethernet Physical Interface (EPHY)	4
$0124 - $013F	Reserved	28
$0140 - $016F	Ethernet Media Access Controller (EMAC)	48
$0170 - $023F	Reserved	208
$0240 - $026F	Port Integration Module (PIM)	48
$0270 - $03FF	Reserved	400

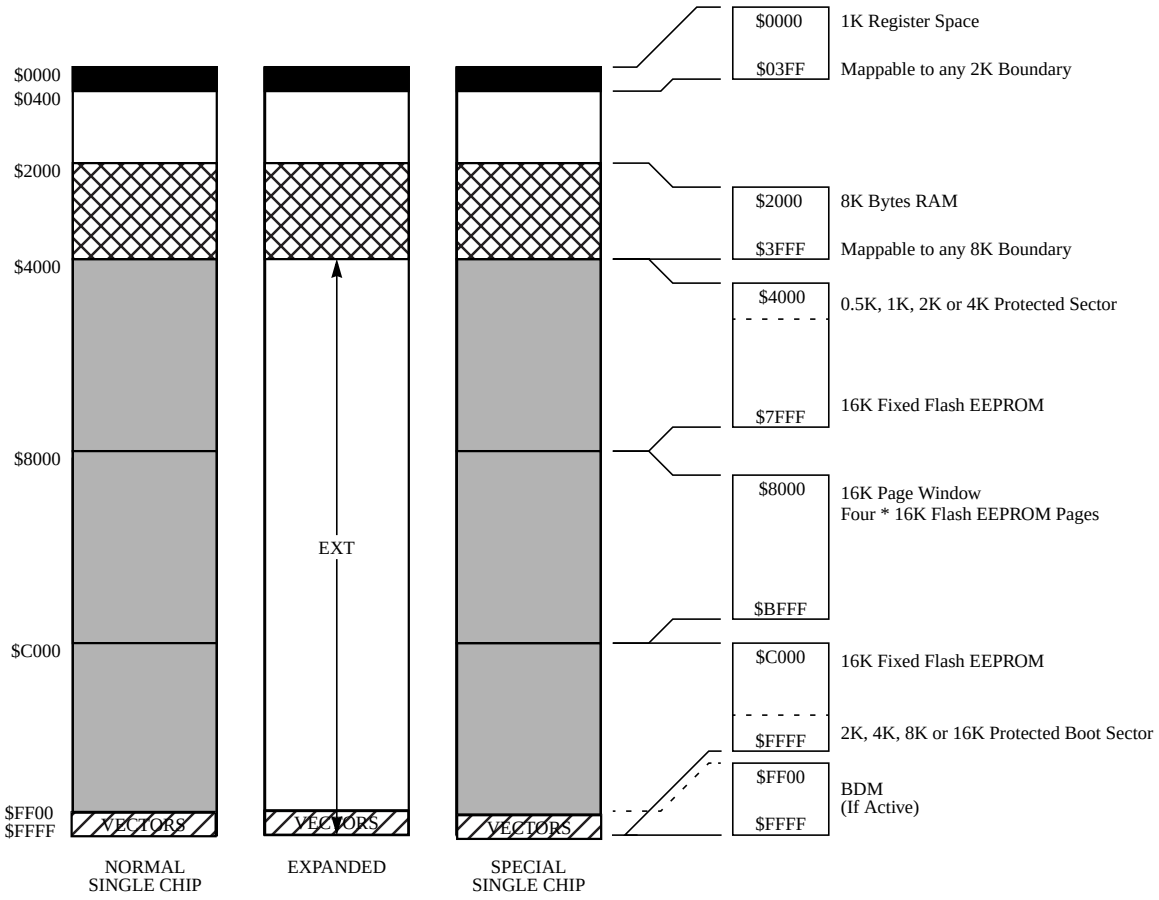
Figure 1-2 MC9S12NE128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0400 - $1FFF: 12K RAM (1K RAM hidden behind Register Space)

Figure 1-3 MC9S12NE64 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0400 - $1FFF: 7K RAM (1K RAM hidden behind Register Space)

1.6 Detailed Register Map

The following tables show the detailed register map of the MC9S12NE64. For detailed information about register function please refer to the appropriate block guide.

$0000 - $000F MEBI map 1 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read:	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		Write:								
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMCTL
		Write:								
$0014	MTST0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0015 - $0016 INT map 1 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		Write:								

$0017 - $0017 MMC map 2 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017	MTST1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0018 - $0019 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018 - $0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$001A - $001B Miscellaneous Peripherals (Device User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D MMC map 3 of 4 (Core User Guide, Device User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E MEBI map 2 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $002F DBG (including BKP) map 1 of 1 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020	DBGC1	read	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
	-	write								
$0021	DBGSC	read	AF	BF	CF	0	TRG			
	-	write								
$0022	DBGTBH	read	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	-	write								
$0023	DBGTBL	read	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	-	write								
$0024	DBGCNT	read	TBF	0	CNT					
	-	write								
$0025	DBGCCX	read	PAGSEL		EXTCMP					
	-	write								
$0026	DBGCCH	read	Bit 15	14	13	12	11	10	9	Bit 8
		write								
$0027	DBGCCL	read	Bit 7	6	5	4	3	2	1	Bit 0
	-	write								
$0028	DBGC2	read	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
	BKPCT0	write								
$0029	DBGC3	read	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
	BKPCT1	write								
$002A	DBGCAX	read	PAGSEL		EXTCMP					
	BKP0X	write								
$002B	DBGCAH	read	Bit 15	14	13	12	11	10	9	Bit 8
	BKP0H	write								
$002C	DBGCAL	read	Bit 7	6	5	4	3	2	1	Bit 0
	BKP0L	write								
$002D	DBGCBX	read	PAGSEL		EXTCMP					
	BKP1X	write								
$002E	DBGCBH	read	Bit 15	14	13	12	11	10	9	Bit 8
	BKP1H	write								
$002F	DBGCBL	read	Bit 7	6	5	4	3	2	1	Bit 0
	BKP1L	write								

$0030 - $0031 MMC map 4 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read: Write:	ECS	XCS	XAB19	XAB18	XAB17	XAB16	XAB15	XAB14
$0033	DDRK	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0034 - $003F CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:								
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:								
$0036	CTFLG TEST ONLY	Read:	TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0
		Write:								
$0037	CRGFLG	Read:	RTIF	PROF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:								
$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		Write:								
$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:								
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:								
$003D	FORBYP TEST ONLY	Read:	RTIBYP	COPBYP	0	PLLBYP	0	0	FCM	0
		Write:								
$003E	CTCTL TEST ONLY	Read:	TCTL7	TCTL6	TCTL5	TCTL4	TCLT3	TCTL2	TCTL1	TCTL0
		Write:								
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	0	0	0	0
		Write:								
$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4				
$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	0	0	0	0
		Write:								

$0040 - $006F TIM (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	0	0	0	0
		Write:								
$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	0	0	0	0
		Write:								
$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
$0049	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$004A	TCTL3	Read:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Write:								
$004B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$004C	TIE	Read:	C7I	C6I	C5I	C4I	0	0	0	0
		Write:								
$004D	TSCR2	Read:	TOI	0	0	0	TCRE	PR2	PR1	PR0
		Write:								
$004E	TFLG1	Read:	C7F	C6F	C5F	C4F	0	0	0	0
		Write:								
$004F	TFLG2	Read:	TOF	0	0	0	0	0	0	0
		Write:								
$0050	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0051	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0052	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0053	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0054	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0055	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0056	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0057	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0058	TC4 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0059	TC4 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0040 - $006F TIM (Timer 16 Bit 4 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$005A	TC5 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005B	TC5 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005C	TC6 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005D	TC6 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$005E	TC7 (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$005F	TC7 (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0060	PACTL	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
$0061	PAFLG	Read:	0	0	0	0	0	0	PAOVF	PAIF
		Write:								
$0062	PACNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0063	PACNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0064	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0065	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0066	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0067	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0068	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0069	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006A	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006B	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$006F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0070 - $007F Reserved

$0070 - $007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $009F ATD (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATDCTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATDCTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATDCTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATDCTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATDCTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATDCTL5	Read:	DJM	DSGN	SCAN	MULT	0	CC	CB	CA
		Write:								
$0086	ATDSTAT0	Read:	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATDTEST0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0089	ATDTEST1	Read:	0	0	0	0	0	0	0	SC
		Write:								
$008A	ATDSTAT0	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008B	ATDSTAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	ATDDIEN0	Read:	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
		Write:								
$008D	ATDDIEN1	Read:	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		Write:								
$008E	PORTAD0	Read:	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
		Write:								
$008F	PORTAD1	Read:	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		Write:								
$0090	ATDDR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATDDR0L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0092	ATDDR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$0080 - $009F ATD (Analog to Digital Converter 10 Bit 8 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0093	ATDDR1L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0094	ATDDR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATDDR2L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0096	ATDDR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATDDR3L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$0098	ATDDR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATDDR4L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009A	ATDDR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATDDR5L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009C	ATDDR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATDDR6L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								
$009E	ATDDR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009F	ATDDR7L	Read:	Bit7	Bit6	0	0	0	0	0	0
		Write:								

$00A0 - $00C7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00A0 - $00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCIBDH	Read: Write:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
$00C9	SCIBDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00CA	SCICR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00CB	SCICR2	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00CC	SCISR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCISR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00CE	SCIDRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCIBDH	Read:	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCIBDL	Read:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Write:								
$00D2	SCICR1	Read:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		Write:								
$00D3	SCICR2	Read:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Write:								
$00D4	SCISR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00D5	SCISR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00D6	SCIDRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D8 - $00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPICR1	Read:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		Write:								
$00D9	SPICR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPIBR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPISR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00D8 - $00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00DD	SPIDR	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00E7 IIC (Inter-IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	IBAD	Read:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		Write:								
$00E1	IBFD	Read:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		Write:								
$00E2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00E3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00E4	IBDR	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$00E5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E8 - $00FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E8-$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (fts64k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN1	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
$0102	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (fts64k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	0	0
		Write:								
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0109	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010A	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010B	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$010C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110 - $011F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0120 - $0123 Ethernet Physical Transceiver (EPHY)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	EPHYCTL0	Read:	EPHYEN	ANDIS	DIS100	DIS10	LEDEN	EPHYWAI	0	EPHYIEN
		Write:								
$0121	EPHYCTL1	Read:	*TRIMEN*	0	0	PHYADD4	PHYADD3	PHYADD2	PHYADD1	PHYADD0
		Write:								
$0122	EPHYSR	Read:	0	0	100DIS	10DIS	0	0	0	EPHYIF
		Write:								
$0123	EPHYTST	Read:	*SLPT1*	*SLPT0*	*AMPT1*	*AMPT0*	*BGT3*	*BGT2*	*BGT1*	*BGT0*
		Write:								

$0124 - $013F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0124 - $013F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0140 - $016F Ethernet Media Access Controller (EMAC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	NETCTL	Read:	EMACE	0	0	ESWAI	EXTPHY	MLB	FDX	0
		Write:								
$0141	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0142	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0143	RXCTS	Read:	RXACT	0	0	RFCE	0	PROM	CONMC	BCREJ
		Write:								
$0144	TXCTS	Read:	TXACT	0	CSLF	PTRC	SSB	0	0	0
		Write:							TCMD	
$0145	ETCTL	Read:	PET	0	0	EMW	IPV6	ARP	IPV4	IEEE
		Write:								
$0146	ETYPE	Read:	ETYPE[15:8]							
		Write:								
$0147	ETYPE	Read:	ETYPE[7:0]							
		Write:								
$0148	PTIME	Read:	PTIME[15:8]							
		Write:								
$0149	PTIME	Read:	PTIME[7:0]							
		Write:								
$014A	IEVENT	Read:	RFCIF	0	BREIF	RXEIF	RXAOIF	RXBOIF	RXACIF	RXBCIF
		Write:								
$014B	IEVENT	Read:	MMCIF	0	LCIF	ECIF	0	0	TXCIF	0
		Write:								
$0141C	IMASK	Read:	RFCIE	0	BREIE	RXEIE	RXAOIE	RXBOIE	RXACIE	RXBCIE
		Write:								
$014D	IMASK	Read:	MMCIE	0	LCIE	ECIE	0	0	TXCIE	0
		Write:								
$014E	SWRST	Read:	MACRST	0	0	0	0	0	0	0
		Write:								
$014F	reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0150	MPADR	Read:	0	0	0	PADDR				
		Write:								
$0151	MRADR	Read:	0	0	0	RADDR				
		Write:								
$0152	MWDATA	Read:	WDATA[15:8]							
		Write:								

$0140 - $016F Ethernet Media Access Controller (EMAC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0123	MWDATA	Read:	WDATA[7:0]							
		Write:								
$0154	MRDATA	Read:	RDATA[15:8]							
		Write:								
$0155	MRDATA	Read:	RDATA[7:0]							
		Write:								
$0156	MCMST	Read:	0	0	BUSY	NOPRE	MDCSEL			
		Write:	OP							
$0157	reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0158	BUFCFG	Read:	0	BUFMAP			0	MAXFL[10:8]		
		Write:								
$0159	BUFCFG	Read:	MAXFL[7:0]							
		Write:								
$015A	RXAEFP	Read:	0	0	0	0	0	RXAEFP[10:8]		
		Write:								
$015B	RXAEFP	Read:	RXAEFP[7:0]							
		Write:								
$015C	RXBEFP	Read:	0	0	0	0	0	RXBEFP[10:8]		
		Write:								
$015D	RXBEFP	Read:	RXBEFP[7:0]							
		Write:								
$015E	TXEFP	Read:	0	0	0	0	0	TXEFP[10:8]		
		Write:								
$015F	TXEFP	Read:	TXEFP[7:0]							
		Write:								
$0160	MCHASH	Read:	MCHASH[63:56]							
		Write:								
$0161	MCHASH	Read:	MCHASH[55:48]							
		Write:								
$0162	MCHASH	Read:	MCHASH[47:40]							
		Write:								
$0163	MCHASH	Read:	MCHASH[39:32]							
		Write:								
$0164	MCHASH	Read:	MCHASH[31:24]							
		Write:								
$0165	MCHASH	Read:	MCHASH[23:16]							
		Write:								
$0166	MCHASH	Read:	MCHASH[15:8]							
		Write:								
$0167	MCHASH	Read:	MCHASH[63:56]							
		Write:								
$0168	MACAD	Read:	MACAD0[55:48]							
		Write:								
$0169	MACAD	Read:	MACAD1[47:32]							
		Write:								

$0140 - $016F Ethernet Media Access Controller (EMAC)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$016A	MACAD	Read:	MACAD2[31:24]							
		Write:								
$016B	MACAD	Read:	MACAD3[23:16]							
		Write:								
$016C	MACAD	Read:	MACAD4[15:8]							
		Write:								
$016D	MACAD	Read:	MACAD5[7:0]							
		Write:								
$016E	MISC	Read:	INDEX			0	0	MISC[10:8]		
		Write:								
$016F	MISC	Read:	MISC[7:0]							
		Write:								

$0170 - $023F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0170 - $023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0240 - $026F PIM (Port Interface Module)

$0240	PTT	Read:	0	0	0	0	PTT3	PTT2	PTT1	PTT0
		Write:								
$0241	PTIT	Read:	0	0	0	0	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0242	DDRT	Read:	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
		Write:								
$0243	RDRT	Read:	0	0	0	0	RDRT3	RDRT2	RDRT1	RDRT0
		Write:								
$0244	PERT	Read:	0	0	0	0	PERT3	PERT2	PERT1	PERT0
		Write:								
$0245	PPST	Read:	0	0	0	0	PPST3	PPST2	PPST1	PPST0
		Write:								
$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTS	Read:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
		Write:								
$0249	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$024A	DDRS	Read:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
		Write:								

$0240 - $026F PIM (Port Interface Module)

$024B	RDRS	Read:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
		Write:								
$024C	PERS	Read:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
		Write:								
$024D	PPSS	Read:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
		Write:								
$024E	WOMS	Read:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250	PTG	Read:	PTG7	PTG6	PTG5	PTG4	PTG3	PTG2	PTG1	PTG0
		Write:								
$0251	PTIG	Read:	PTIG7	PTIG6	PTIG5	PTIG4	PTIG3	PTIG2	PTIG1	PTIG0
		Write:								
$0252	DDRG	Read:	DDRG7	DDRG6	DDRG5	DDRG4	DDRG3	DDRG2	DDRG1	DDRG0
		Write:								
$0253	RDRG	Read:	RDRG7	RDRG6	RDRG5	RDRG4	RDRG3	RDRG2	RDRG1	RDRG0
		Write:								
$0254	PERG	Read:	PERG7	PERG6	PERG5	PERG4	PERG3	PERG2	PERG1	PERG0
		Write:								
$0255	PPSG	Read:	PPSG7	PPSG6	PPSG5	PPSG4	PPSG3	PPSG2	PPSG1	PPSG0
		Write:								
$0256	PIEG	Read:	PIEG7	PIEG6	PIEG6	PIEG4	PIEG3	PIEG2	PIEG1	PIEG0
		Write:								
$0257	PIFG	Read:	PIFG7	PIFG6	PIFG5	PIFG4	PIFG3	PIFG2	PIFG1	PIFG0
		Write:								
$0258	PTH	Read:	0	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0259	PTIH	Read:	0	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$025A	DDRH	Read:	0	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$025B	RDRH	Read:	0	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$025C	PERH	Read:	0	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$025D	PPSH	Read:	0	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$025E	PIEH	Read:	0	PIEH6	PIEH6	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$025F	PIFH	Read:	0	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0260	PTJ	Read:	PTJ7	PTJ6	0	0	PTJ3	PTJ2	PTJ1	PTJ0
		Write:								
$0262	PTIJ	Read:	PTIJ7	PTIJ6	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
		Write:								
$0262	DDRJ	Read:	DDRJ7	DDRJ6	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
		Write:								

$0240 - $026F PIM (Port Interface Module)

$0263	RDRJ	Read:	RDRJ7	RDRJ6	0	0	RDRJ3	RDRJ2	RDRJ1	RDRJ0
		Write:								
$0264	PERJ	Read:	PERJ7	PERJ6	0	0	PERJ3	PERJ2	PERJ1	PERJ0
		Write:								
$0265	PPSJ	Read:	PPSJ7	PPSJ6	0	0	PPSJ3	PPSJ2	PPSJ1	PPSJ0
		Write:								
$0266	PIEJ	Read:	PIEJ7	PIEJ6	0	0	PIEJ3	PIEJ2	PIEJ1	PIEJ0
		Write:								
$0267	PIFJ	Read:	PIFJ7	PIFJ6	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
		Write:								
$0268	PTL	Read:	0	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		Write:								
$0269	PTIL	Read:	0	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		Write:								
$026A	DDRL	Read:	0	DDRL6	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		Write:								
$026B	RDRL	Read:	0	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		Write:								
$026C	PERL	Read:	0	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		Write:								
$026D	PPSL	Read:	0	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		Write:								
$026E	WOML	Read:	0	WOML6	WOML5	WOML4	WOML3	WOML2	WOML1	WOML0
		Write:								
$026F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0270 - $03FF Reserved space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0270 - $3FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

1.7 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses $001A and $001B after reset. The read-only value is a unique part ID for each revision of the chip. **Table 1-2 Assigned Part ID Numbers** shows the assigned part ID number.

Table 1-2 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12NE128	TBD	$8100
MC9S12NE-Family	0L19S	$8200

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-3** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-3 Memory size registers

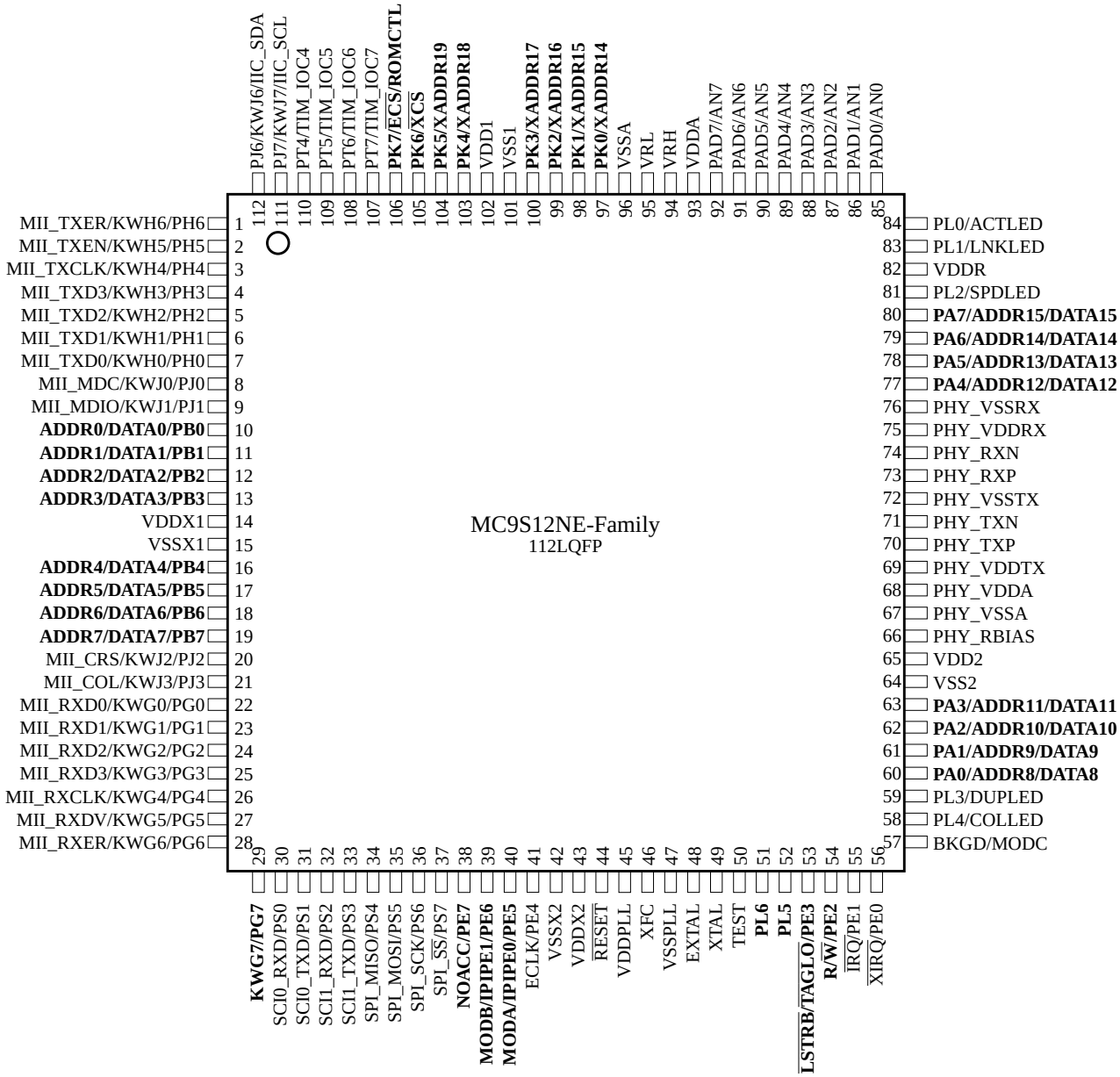
	Register name	Value
MC9S12NE128	MEMSIZ0	$05
MC9S12NE128	MEMSIZ1	$80
MC9S12NE-Family	MEMSIZ0	$03
MC9S12NE-Family	MEMSIZ1	$80

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12NE-Family is available in a 112-pin low profile quad flat pack (LQFP) and in a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in the Signal Descriptions. Figure 2-1 and Figure 2-2 show the pin assignments.



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 2-1 Pin assignments 112 LQFP for MC9S12NE-Family

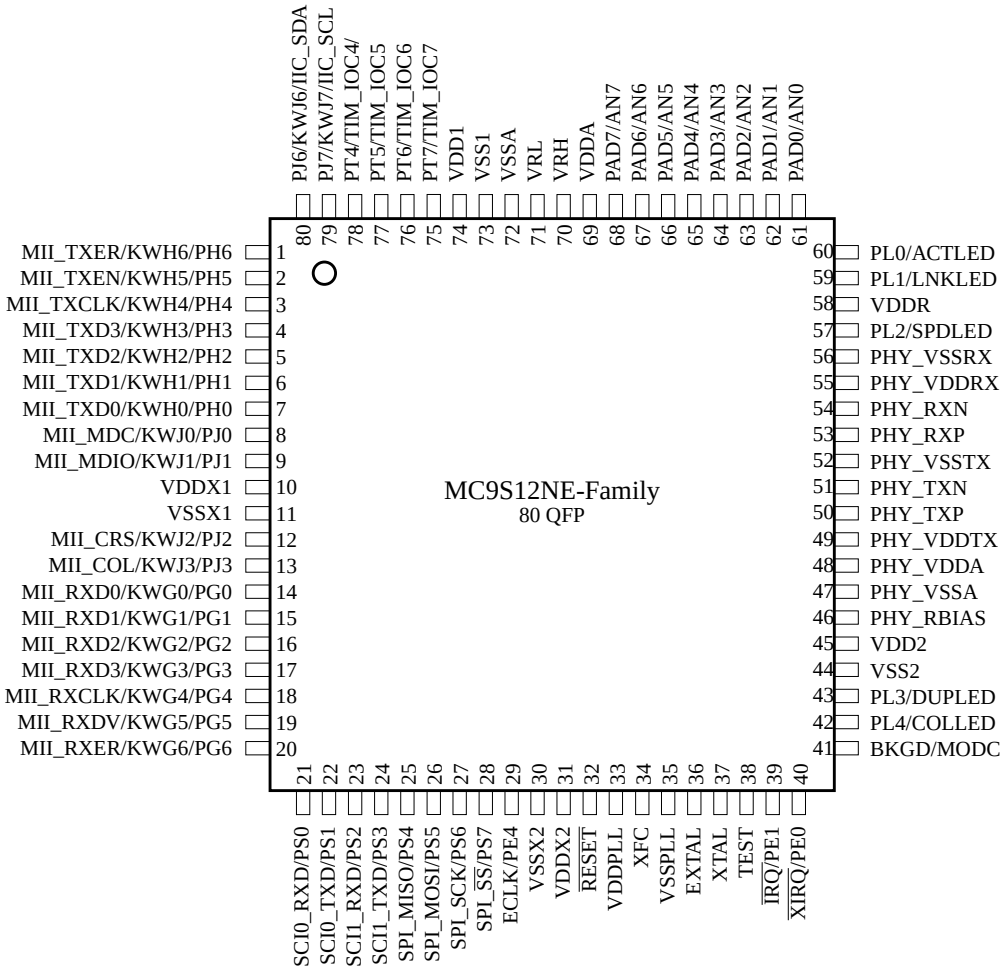


Figure 2-2 Pin assignments in 80 QFP for MC9S12NE-Family

2.2 Signal Properties Summary

Table 2-1 Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description	Reset State
				CTRL	Reset STATE		
EXTAL	—	—	VDDPLL	NA	NA	Oscillator pins	Input
XTAL	—	—	VDDPLL	NA	NA		Output
XFC	—	—	VDDPLL	NA	NA	PLL loop filter pin	
$\overline{\text{RESET}}$	—	—	VDDX	None	None	External reset pin	Input
TEST	—	—	VDDX	None	None	Test only pin. Must be grounded.	Input
BKGD	MODC	$\overline{\text{TAGHI}}$	VDDX	None	UP	Background debug; mode pin; tag signal high	Input
PE7	**NOACC**		**VDDX**	**PUCR**	**UP**	**Port E I/O pin; access**	**Input**
PE6	**IPIPE1**	**MODB**	**VDDX**	**While $\overline{\text{RESET}}$ pin is low: Down**		**Port E I/O pin; pipe status; mode selection**	**Input**
PE5	**IPIPE0**	**MODA**	**VDDX**	**While $\overline{\text{RESET}}$ pin is low: Down**		**Port E I/O pin; pipe status; mode selection**	**Input**
PE4	ECLK	—	VDDX	PUCR	UP	Port E I/O pin; bus clock output	Input
PE3	**$\overline{\text{LSTRB}}$**	**$\overline{\text{TAGLO}}$**	**VDDX**	**PUCR**	**UP**	**Port E I/O pin; low strobe; tag signal low**	**Input**
PE2	**R/$\overline{\text{W}}$**	**—**	**VDDX**	**PUCR**	**UP**	**Port E I/O pin; R/$\overline{\text{W}}$ in expanded modes**	**Input**
PE1	$\overline{\text{IRQ}}$	—	VDDX	PUCR	UP	Port E input; external interrupt pin	Input
PE0	$\overline{\text{XIRQ}}$	—	VDDX	PUCR	UP	Port E input; non-maskable interrupt pin	Input
PA[7:0]	**ADDR[15:8]/ DATA[15:8]**	**—**	**VDDX**	**PUCR**	**Disabled**	**Port A I/O pin; multiplexed address/data**	**Input**
PB[7:0]	**ADDR[7:0] / DATA[7:0]**	**—**	**VDDX**	**PUCR**	**Disabled**	**Port B I/O pin; multiplexed address/data**	**Input**
PAD[7:0]	AN[7:0]	---	VDDA	None	None	Port AD Input Pins; ATD inputs	Input
PK[7]	**$\overline{\text{ECS}}$**	**ROMCTL**	**VDDX**	**PUCR**	**UP**	**Port K I/O Pin; Emulation Chip Select;**	**Input**
PK[6]	**$\overline{\text{XCS}}$**	**—**	**VDDX**	**PUCR**	**UP**	**Port K I/O Pin; External Chip Select**	**Input**
PK[5:0]	**XADDR [19:14]**	**—**	**VDDX**	**PUCR**	**UP**	**Port K I/O Pins; Extended Addresses**	**Input**
PG7	**—**	**KWG7**	**VDDX**	**PERG/ PPSG**	**Disabled**	**Port G I/O Pin; Interrupt**	**Input**
PG6	MII_RXER	KWG6	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Error; Interrupt	Input
PG5	MII_RXDV	KWG5	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Data Valid; Interrupt	Input
PG4	MII_RXCLK	KWG4	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Clock; Interrupt	Input
PG3	MII_RXD3	KWG3	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Data; Interrupt	Input
PG2	MII_RXD2	KWG2	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Data; Interrupt	Input

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description	Reset State
				CTRL	Reset STATE		
PG1	MII_RXD1	KWG1	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Data; Interrupt	Input
PG0	MII_RXD0	KWG0	VDDX	PERG/ PPSG	Disabled	Port G I/O Pin; EMAC MII Receive Data; Interrupt	Input
PH6	MII_TXER	KWH6	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Error; Interrupt	Input
PH5	MII_TXEN	KWH5	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Enable; Interrupt	Input
PH4	MII_TXCLK	KWH4	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Clock; Interrupt	Input
PH3	MII_TXD3	KWH3	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Data; Interrupt	Input
PH2	MII_TXD2	KWH2	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Data; Interrupt	Input
PH1	MII_TXD1	KWH1	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Data; Interrupt	Input
PH0	MII_TXD0	KWH0	VDDX	PERH/ PPSH	Disabled	Port H I/O Pin; EMAC MII Transmit Data; Interrupt	Input
PJ7	IIC_SCL	KWJ7	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; IIC SCL; Interrupt	Input
PJ6	IIC_SDA	KWJ6	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; IIC SDA; Interrupt	Input
PJ3	MII_COL	KWJ3	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; EMAC MII Collision; Interrupt	Input
PJ2	MII_CRS	KWJ2	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; EMAC MII Carrier Sense; Interrupt	Input
PJ1	MII_MDIO	KWJ1	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; EMAC MII Management Data I/O; Interrupt	Input
PJ0	MII_MDC	KWJ0	VDDX	PERJ/ PPSJ	Disabled	Port J I/O Pin; EMAC MII Management Data Clock; Interrupt	Input
PL6	**—**	**—**	**VDDX**	**PERL/ PPSL**	**Disabled**	**Port L I/O Pin**	**Input**
PL5	**—**	**—**	**VDDX**	**PERL/ PPSL**	**Disabled**	**Port L I/O Pin**	**Input**
PL4	COLLED	—	VDDX	PERL/ PPSL	Disabled	Port L I/O Pin; EPHY Collision LED	Input
PL3	DUPLED	—	VDDX	PERL/ PPSL	Disabled	Port L I/O Pin; EPHY Full Duplex LED	Input
PL2	SPDLED	—	VDDX	PERL/ PPSL	Disabled	Port L I/O Pin; EPHY 100Mbps LED	Input
PL1	LNKLED	—	VDDX	PERL/ PPSL	Disabled	Port L I/O Pin; EPHY Valid Link LED	Input
PL0	ACTLED	—	VDDX	PERL/ PPSL	Disabled	Port L I/O Pin; EPHY Transmit or Receive LED	Input
PS7	SPI_$\overline{SS}$	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SPI $\overline{SS}$ signal	Input

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Power Domain	Internal Pull Resistor		Description	Reset State
				CTRL	Reset STATE		
PS6	SPI_SCK	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SPI SCK signal	Input
PS5	SPI_MOSI	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SPI MOSI signal	Input
PS4	SPI_MISO	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SPI MISO signal	Input
PS3	SCI1_TXD	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SCI1 transmit signal	Input
PS2	SCI1_RXD	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SCI1 receive signal	Input
PS1	SCI0_TXD	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SCI0 transmit signal	Input
PS0	SCI0_RXD	—	VDDX	PERS/ PPSS	Disabled	Port S I/O Pin; SCI0 receive signal	Input
PT[7:4]	TIM_IOC[7:4]	—	VDDX	PERT/ PPST	Disabled	Port T I/O Pins; timer TIM input cap. output compare	Input
PHY_TXN	—	—	PHY_VDDTX	NA	NA	Twisted Pair Output -	Analog Output
PHY_TXP	—	—	PHY_VDDTX	NA	NA	Twisted Pair Output +	Analog Output
PHY_RXN	—	—	PHY_VDDRX	NA	NA	Twisted Pair Input -	Analog Input
PHY_RXP	—	—	PHY_VDDRX	NA	NA	Twisted Pair Input +	Analog Input
RBIAS	—	—	PHY_VSSA	NA	NA	Bias Control: 12.4K 1.0% external resistor	Analog Input

NOTE: *Signals shown in bold are not available in the 80 pin package.*

NOTE: *If the port pins are not bonded out in the chosen package the user should initialize the registers to be inputs with enabled pull resistance to avoid excess current consumption. This applies to the following pins:*

(80QFP): Port A[7:0], Port B[7:0], Port E[7,6,5,3,2], Port K[7:0]; Port G[7]; Port L[6:5]

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the external clock and crystal driver pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

RESET is an active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit. External circuitry connected to the RESET pin should not include a large capacitance that would interfere with the ability of this signal to rise to a valid logic one within 32 ECLK cycles after the low drive is released. Upon detection of any reset, an internal circuit drives the RESET pin low and a clocked reset sequence controls when the MCU can begin normal processing. The $\overline{\text{RESET}}$ pin includes an internal pull up device.

2.3.3 TEST — Test Pin

The TEST pin is reserved for test and must be tied to ground in all applications.

2.3.4 XFC — PLL Loop Filter Pin

Dedicated pin used to create the PLL loop filter. See appendix **B.4.3.1**and the CRG Block Guide for more detailed information.

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High & Mode Pin

The BKGD / $\overline{\text{TAGHI}}$ / MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of RESET. In MCU expanded modes of operation, when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. This pin always has an internal pull up.

2.3.6 PA[7:0] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA[7:0] are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PA[7:0] pins are not available in the 80 pin package version.

2.3.7 PB[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB[7:0] are general purpose input or output pins. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus. PB[7:0] pins are not available in the 80 pin package version.

2.3.8 PE7 / NOACC — Port E I/O Pin 7

PE7 is a general purpose input or output pin. During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or free cycle. This signal will assert when the CPU is not using the bus.

2.3.9 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when RESET is low. PE6 is not available in the 80 pin package version.

2.3.10 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of RESET. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when RESET is low. PE5 is not available in the 80 pin package version.

2.3.11 PE4 / ECLK— Port E I/O Pin 4 / E-Clock Output

PE4 is a general purpose input or output pin. In Normal Single Chip mode PE4 is configured with an active pull-up while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. In all modes except Normal Single Chip Mode, the PE4 pin is initially configured as the output connection for the internal bus clock(ECLK). ECLK is used as a timing reference and to demultiplex the address and data in expanded modes. The ECLK frequency is equal to 1/2 the crystal frequency out of reset. The ECLK output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. All clocks, including the ECLK, are halted when the MCU is in STOP mode. It is possible to configure the MCU to interface to slow external memory. ECLK can be stretched for such accesses. The PE4 pin is initially configured as ECLK output with stretch in all expanded modes. Reference the MISC register (EXSTR[1:0] bits) for more information. In normal expanded narrow mode, the ECLK is available for use in external select decode logic or as a constant speed clock for use in the external application system.

2.3.12 PE3 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3 / Low-Byte Strobe ($\overline{\text{LSTRB}}$)

PE3 can be used as a general-purpose I/O in all modes and is an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. PE3 can also be configured as a Low-Byte Strobe ($\overline{\text{LSTRB}}$). The $\overline{\text{LSTRB}}$ signal is used in write operations, so external low byte writes will not be possible until this function is enabled. $\overline{\text{LSTRB}}$ can be enabled by setting the LSTRE bit in the PEAR register. In Expanded Wide and Emulation Narrow modes, and when BDM tagging is enabled, the $\overline{\text{LSTRB}}$ function is multiplexed with the $\overline{\text{TAGLO}}$ function. When enabled a logic zero on the $\overline{\text{TAGLO}}$ pin at the falling edge of ECLK will tag the low byte of an instruction word being read into the instruction queue. PE3 is not available in the 80 pin package version.

2.3.13 PE2 / R/$\overline{\text{W}}$ — Port E I/O Pin 2 / Read/$\overline{\text{Write}}$

PE2 can be used as a general-purpose I/O in all modes and is configured as an input with an active pull-up out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register. If the read/$\overline{\text{write}}$ function is required it should be enabled by setting the RDWE bit in the PEAR register. External writes

will not be possible until the read/$\overline{\text{write}}$ function is enabled. The PE2 pin is not available in the 80 pin package version.

2.3.14 PE1 / $\overline{\text{IRQ}}$ — Port E input Pin 1 / Maskable Interrupt Pin

PE1 is always an input and can always be read. The PE1 pin is also the $\overline{\text{IRQ}}$ input used for requesting an asynchronous interrupt to the MCU. During reset, the I bit in the condition code register (CCR) is set and any $\overline{\text{IRQ}}$ interrupt is masked until software enables it by clearing the I bit. The $\overline{\text{IRQ}}$ is software programmable to either falling edge-sensitive triggering or level-sensitive triggering based on the setting of the IRQE bit in the IRQCR register. The $\overline{\text{IRQ}}$ is always enabled and configured to level-sensitive triggering out of reset. It can be disabled by clearing IRQEN bit in the IRQCR register. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

2.3.15 PE0 / $\overline{\text{XIRQ}}$ — Port E input Pin 0 / Non Maskable Interrupt Pin

PE0 is always an input and can always be read. The PE0 pin is also the $\overline{\text{XIRQ}}$ input for requesting a nonmaskable asynchronous interrupt to the MCU. During reset, the X bit in the condition code register (CCR) is set and any $\overline{\text{XIRQ}}$ interrupt is masked until MCU software enables it by clearing the X bit. Because the $\overline{\text{XIRQ}}$ input is level sensitive triggered, it can be connected to a multiple-source wired-OR network. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPEE in the PUCR register.

2.3.16 PK7 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). In expanded modes the PK7 pin can be used to determine the reset state of the ROMCTL bit in the MISC register. At the rising edge of $\overline{\text{RESET}}$, the state of the PK7 pin is latched to the ROMCTL bit. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to the HCS12 V1.5 Core User Guide for further details. PK7 is not available in the 80 pin package version.

2.3.17 PK6 / $\overline{\text{XCS}}$ — Port K I/O Pin 6

PK6 is a general purpose input or output pin. During MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, this pin is used as an external chip select signal for most external accesses that are not selected by ECS. There is an active pull-up on this pin while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to section Multiplexed External Bus Interface (MEBI) of the HCS12 V1.5 Core User Guide for further details. PK6 is not available in the 80 pin package version.

2.3.18 PK[5:0] / XADDR[19:14] — Port K I/O Pins [5:0]

PK[5:0] are general purpose input or output pins. In MCU expanded modes of operation, when the EMK bit in the MODE register is set to 1, PK[5:0] provide the expanded address XADDR[19:14] for the external bus. There are active pull-ups on PK[5:0] pins while in reset and immediately out of reset. The pullup can be turned off by clearing PUPKE in the PUCR register. Refer to section Multiplexed External Bus Interface (MEBI) of the HCS12 V1.5 Core User Guide for further details. PK[5:0] are not available in the 80 pin package version.

2.3.19 PAD[7:0] / AN[7:0] — Port AD Input Pins [7:0]

PAD[7:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the ATD_10B8C Block Guide for information about pin configurations.

2.3.20 PG7 / KWG7 — Port G I/O Pin 7

PG7 is a general purpose input or output pin. It can be configured to generate an interrupt(KWG7) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide for information about pin configurations.

2.3.21 PG6 / MII_RXER / KWG6 — Port G I/O Pin 6

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive error (MII_RXER) signal. It can be configured to generate an interrupt(KWG6) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.22 PG5 / MII_RXDV / KWG5 — Port G I/O Pin 5

PG5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data valid (MII_RXDV) signal. It can be configured to generate an interrupt(KWG5) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG5 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.23 PG4 / MII_RXCLK / KWG4 — Port G I/O Pin 4

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive clock (MII_RXCLK) signal. It can be configured to generate an interrupt(KWG4) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.24 PG3 / MII_RXD3 / KWG3 — Port G I/O Pin 3

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD3) signal. It can be configured to generate an interrupt(KWG3) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.25 PG2 / MII_RXD2 / KWG2 — Port G I/O Pin 2

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD2) signal. It can be configured to generate an interrupt(KWG2) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.26 PG1 / MII_RXD1 / KWG1 — Port G I/O Pin 1

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD1) signal. It can be configured to generate an interrupt(KWG1) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.27 PG0 / MII_RXD0 / KWG0 — Port G I/O Pin 0

PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD0) signal. It can be configured to generate an interrupt(KWG0) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PG0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.28 PH6 / MII_TXER / KWH6 — Port H I/O Pin 6

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit error (MII_TXER) signal. It can be configured to generate an interrupt(KWH6) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.29 PH5 / MII_TXEN / KWH5 — Port H I/O Pin 5

PH5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Enabled (MII_TXEN) signal. It can be configured to generate an interrupt(KWH5) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH5 pin is configured

as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.30 PH4 / MII_TXCLK / KWH4 — Port H I/O Pin 4

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Clock (MII_TXCLK) signal. It can be configured to generate an interrupt(KWH4) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.31 PH3 / MII_TXD3 / KWH3 — Port H I/O Pin 3

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit data (MII_TXD3) signal. It can be configured to generate an interrupt(KWH3) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.32 PH2 / MII_TXD2 / KWH2 — Port H I/O Pin 2

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit data (MII_TXD2) signal. It can be configured to generate an interrupt(KWH2) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.33 PH1 / MII_TXD1 / KWH1 — Port H I/O Pin 1

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit data (MII_TXD1) signal. It can be configured to generate an interrupt(KWH1) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.34 PH0 / MII_TXD0 / KWH0 — Port H I/O Pin 0

PH6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit data (MII_TXD0) signal. It can be configured to generate an interrupt(KWH0) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PH0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.35 PJ7 / IIC_SCL / KWJ7 — Port J I/O Pin 7

PJ6 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (IIC_SCL) for the IIC module (IIC). It can be configured to generate an interrupt(KWJ7) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the IIC Block Guide for information about pin configurations.

2.3.36 PJ6 / IIC_SDA / KWJ6 — Port J I/O Pin 6

PJ6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (IIC_SDL) for the IIC module (IIC). It can be configured to generate an interrupt(KWJ6) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the IIC Block Guide for information about pin configurations.

2.3.37 PJ3 / COL / KWJ3 — Port J I/O Pin 3

PJ3 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the collision (MII_COL) signal. It can be configured to generate an interrupt(KWJ3) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.38 PJ2 / CRS / KWJ2 — Port J I/O Pin 2

PJ2 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the carrier sense (MII_CRS) signal. It can be configured to generate an interrupt(KWJ2) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.39 PJ1 / MDIO / KWJ1 — Port J I/O Pin 1

PJ1 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the Management Data I/O (MII_MDIO) signal. It can be configured to generate an interrupt(KWH1) causing the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.40 PJ0 / MDC / KWJ0 — Port J I/O Pin 0

PJ0 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the management data clock(MII_MDC) signal. It can be configured to generate an interrupt(KWJ0) causing

the MCU to exit STOP or WAIT mode. While in reset and immediately out of reset the PJ0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EMAC Block Guide for information about pin configurations.

2.3.41 PL6 — Port L I/O Pin 6

PL6 is a general purpose input or output pin. While in reset and immediately out of reset the PL6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide for information about pin configurations.

2.3.42 PL5 — Port L I/O Pin 5

PL5 is a general purpose input or output pin. While in reset and immediately out of reset the PL5 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide for information about pin configurations.

2.3.43 PL4 / COLLED — Port L I/O Pin 4

PL4 is a general purpose input or output pin. When the internal Ethernet Physical Transceiver (EPHY) is enabled it becomes the collision status signal (COLLED). While in reset and immediately out of reset the PL4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EPHY Block Guide for information about pin configurations.

2.3.44 PL3 / DUPLED — Port L I/O Pin 3

PL3 is a general purpose input or output pin. When the internal Ethernet Physical Transceiver (EPHY) is enabled it becomes the duplex status signal (DUPLED). While in reset and immediately out of reset the PL3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EPHY Block Guide for information about pin configurations.

2.3.45 PL2 / SPDLED — Port L I/O Pin 2

PL2 is a general purpose input or output pin. When the internal Ethernet Physical Transceiver (EPHY) is enabled it becomes the speed status signal (SPDLED). While in reset and immediately out of reset the PL2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EPHY Block Guide for information about pin configurations.

2.3.46 PL1 / LNKLED — Port L I/O Pin 1

PL1 is a general purpose input or output pin. When the internal Ethernet Physical Transceiver (EPHY) is enabled it becomes the link status signal (LNKLED). While in reset and immediately out of reset the PL1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EPHY Block Guide for information about pin configurations.

2.3.47 PL0 / ACTLED — Port L I/O Pin 0

PL0 is a general purpose input or output pin. When the internal Ethernet Physical Transceiver (EPHY) is enabled it becomes the active status signal (ACTLED). While in reset and immediately out of reset the PL0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the EPHY Block Guide for information about pin configurations.

2.3.48 PS7 / SPI_$\overline{SS}$ — Port S I/O Pin 7

PS7 is a general purpose input or output. When the Serial Peripheral Interface (SPI) is enabled PS7 becomes the slave select pin $\overline{SS}$. While in reset and immediately out of reset the PS7 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.49 PS6 / SPI_SCK — Port S I/O Pin 6

PS6 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS6 becomes the serial clock pin, SCK. While in reset and immediately out of reset the PS6 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.50 PS5 / SPI_MOSI — Port S I/O Pin 5

PS5 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS5 is the master output (during master mode) or slave input (during slave mode) pin. While in reset and immediately out of reset the PS5 pin is configured as a high impedance input pin Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.51 PS4 / SPI_MISO — Port S I/O Pin 4

PS4 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS4 is the master input (during master mode) or slave output (during slave mode) pin. While in reset and immediately out of reset the PS4 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SPI Block Guide for information about pin configurations.

2.3.52 PS3 / SCI1_TXD — Port S I/O Pin 3

PS3 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) transmitter is enabled the PS3 pin is configured as the transmit pin, TXD, of SCI1. While in reset and immediately out of reset the PS3 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.53 PS2 / SCI1_RXD — Port S I/O Pin 2

PS2 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) receiver is enabled the PS2 pin is configured as the receive pin RXD of SCI1. While in reset and immediately out of reset the PS2 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.54 PS1 / SCI0_TXD — Port S I/O Pin 1

PS1 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) transmitter is enabled the PS1 pin is configured as the transmit pin, TXD, of SCI0. While in reset and immediately out of reset the PS1 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.55 PS0 / SCI0_RXD — Port S I/O Pin 0

PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0. While in reset and immediately out of reset the PS0 pin is configured as a high impedance input pin. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the SCI Block Guide for information about pin configurations.

2.3.56 PT[7:4] / IOC1[7:4]— Port T I/O Pins [7:4]

PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4]. While in reset and immediately out of reset the PT[7:4] pins are configured as a high impedance input pins. Consult the Port Integration Module (PIM) PIM_9NE64 Block Guide and the TIM_16B4C Block Guide for information about pin configurations.

2.3.57 PHY_TXP - EPHY Twisted Pair Output +

Ethernet twisted pair output pin. This pin is hi-z out of reset.

2.3.58 PHY_TXN - EPHY Twisted Pair Output -

Ethernet twisted pair output pin. This pin is hi-z out of reset.

2.3.59 PHY_RXP - EPHY Twisted Pair Input +

Ethernet twisted pair input pin. This pin is hi-z out of reset.

2.3.60 PHY_RXN - EPHY Twisted Pair Input -

Ethernet twisted pair input pin. This pin is hi-z out of reset.

2.3.61 PHY_RBIAS - EPHY Bias Control Resistor

Connect a 12.4K(1.0%) external resistor, RBIAS, between PHY_RBIAS pin and PHY_VSSA. This resistor should be placed as close a possible to the chip pin. Stray capacitance should be kept to less than 10pF (>50pF may cause instability). No high speed signals should go in the region of RBIAS.

2.4 Power Supply Pins

2.4.1 VDDX1\2, VSSX1\2 — Power & Ground Pins for I/O & Internal Voltage Regulator

External power and ground for I/O drivers. Bypass requirements depend on how heavily the MCU pins are loaded.

2.4.2 VDDR — Power Pin for Internal Voltage Regulator

External power for internal voltage regulator.

2.4.3 VDD1, VDD2, VSS1, VSS2 — Core Power Pins

Power is supplied to the MCU through VDD and VSS. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground input pins for the voltage regulator and the analog to digital converter.

2.4.5 PHY_VDDA, PHY_VSSA — Power Supply Pins for EPHY Analog

Power is supplied to the Ethernet Physical Transceiver(EPHY) PLLs through PHY_VDDA and PHY_VSSA. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.6 PHY_VDDRX, PHY_VSSRX — Power Supply Pins for EPHY Receiver

Power is supplied to the Ethernet Physical Transceiver(EPHY) receiver through PHY_VDDRX and PHY_VSSRX. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.7 PHY_VDDTX, PHY_VSSTX — Power Supply Pins for EPHY Transmitter

External power is supplied to the Ethernet Physical Transceiver(EPHY) transmitter through PHY_VDDTX and PHY_VSSTX. This 2.5V supply is derived from the internal voltage regulator. There is no static load on those pins allowed. The internal voltage regulator is turned off, if VDDR is tied to ground.

2.4.8 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the reference voltage input pins for the analog to digital converter.

2.4.9 VDDPLL, VSSPLL — Power Supply Pins for PLL

Provides operating voltage and ground for the Oscillator and the Phased-Locked Loop. This allows the supply voltage to the Oscillator and PLL to be bypassed independently.This 2.5V voltage is generated by the internal voltage regulator. The internal voltage regulator is turned off, if VDDR is tied to ground.

Table 2-2 MC9S12NE-Family Power and Ground Connection Summary

Mnemonic	Nominal Voltage	Description
VDDR	3.3 V	External power and ground, supply to internal voltage regulator. To disable voltage regulator attach VREGEN to VSSX.
VDDX1 VDDX2	3.3 V	External power and ground, supply to pin drivers.
VSSX	0 V	
VDDA	3.3 V	Operating voltage and ground for the analog-to-digital converter, the reference for the internal voltage regulator and the digital-to-analog converters, allows the supply voltage to the A/D to be bypassed independently.
VSSA	0 V	
VRH	3.3 V	Reference voltage high for the ATD converter.
VRL	0 V	Reference voltage low for the ATD converter.
PHY_VDDTX PHY_VDDRX PHY_VDDA	2.5 V	Internal power and ground generated by internal regulator for Internal Ethernet Physical Transceiver (EPHY). These also allow an external source to supply the EPHY voltages and bypass the internal voltage regulator.
PHY_VSSTX PHY_VSSRX PHY_VSSA	0V	
VDD1 VDD2	2.5 V	Internal power and ground generated by internal regulator. These also allow an external source to supply the core VDD/VSS voltages and bypass the internal voltage regulator.
VSS1 VSS2	0V	
VDDPLL	2.5 V	Provides operating voltage and ground for the Phased-Locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
VSSPLL	0 V	

NOTE: *All VSS pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use*

bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.

Section 3 System Clock Description

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules. Consult the CRG Block Guide for details on clock generation.

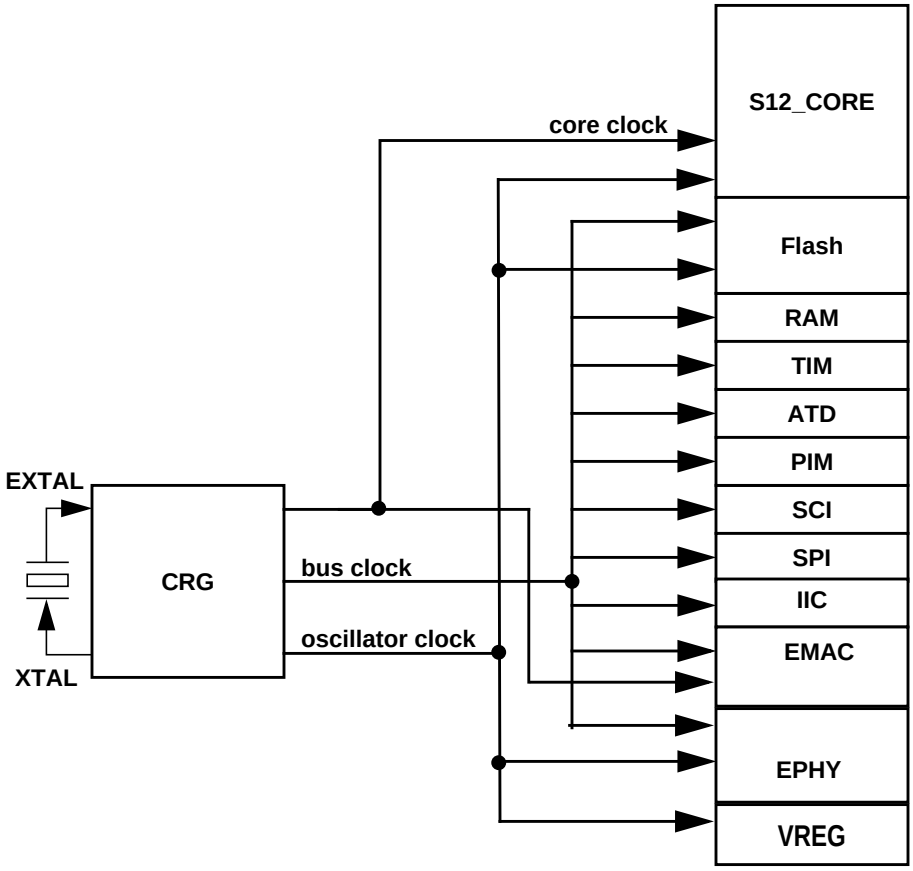


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12NE64. Each mode has an associated default memory map and external bus configuration controlled by a further pin.

Three low power modes exist for the device.

4.2 Chip Configuration Summary

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset. The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal. The ROMCTL signal allows the setting of the ROMON bit in the MISC register thus controlling whether the internal Flash is visible in the memory map. ROMON = 1 mean the Flash is visible in the memory map. The state of the ROMCTL pin is latched into the ROMON bit in the MISC register on the rising edge of the reset signal.

Table 4-1 Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PP6 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	0	1	Emulation Expanded Narrow, BDM allowed
			1	0	
0	1	0	X	0	Special Test (Expanded Wide), BDM allowed
0	1	1	0	1	Emulation Expanded Wide, BDM allowed
			1	0	
1	0	0	X	1	Normal Single Chip, BDM allowed
1	0	1	0	0	Normal Expanded Narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal Expanded Wide, BDM allowed
			1	1	

For further explanation on the modes refer to the Core User Guide.

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,

- Operation in single-chip mode,
- Operation from external memory with internal FLASH disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH, the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH. Once this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

The microcontroller features three main low power modes. Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode. An important source of information about the clock system is the Clock and Reset Generator User Guide (CRG).

4.4.1 Stop

Executing the CPU STOP instruction stops all clocks and the oscillator thus putting the chip in fully static mode. Wake up from this mode can be done via reset or external interrupts.

4.4.2 Pseudo Stop

This mode is entered by executing the CPU STOP instruction. In this mode the oscillator is still running and the Real Time Interrupt (RTI) or Watchdog (COP) sub module can stay active. Other peripherals are turned off. This mode consumes more current than the full STOP mode, but the wake up time from this mode is significantly shorter.

4.4.3 Wait

This mode is entered by executing the CPU WAI instruction. In this mode the CPU will not execute instructions. The internal CPU signals (address and databus) will be fully static. All peripherals stay active. For further power consumption the peripherals can individually turn off their local clocks.

4.4.4 Run

Although this is not a low power mode, unused peripheral modules should not be enabled in order to save power.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts. System resets can be generated through external control of the $\overline{\text{RESET}}$ pin, through the clock and reset generator module CRG or through the low voltage reset (LVR) generator of the voltage regulator module. Refer to the CRG and VREG User Guides for detailed information on reset generation.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	–
$FFFC, $FFFD	Clock Monitor fail reset	None	COPCTL (CME, FCME)	–
$FFFA, $FFFB	COP failure reset	None	COP rate select	–
$FFF8, $FFF9	Unimplemented instruction trap	None	None	–
$FFF6, $FFF7	SWI	None	None	–
$FFF4, $FFF5	XIRQ	X-Bit	None	–
$FFF2, $FFF3	IRQ	I-Bit	INTCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	CRGINT (RTIE)	$F0
$FFE8 to $FFEF	Reserved			
$FFE6, $FFE7	Standard Timer channel 4	I-Bit	T0IE (T0C4I)	$E6
$FFE4, $FFE5	Standard Timer channel 5	I-Bit	T0IE (T0C5I)	$E4
$FFE2, $FFE3	Standard Timer channel 6	I-Bit	T0IE (T0C6I)	$E2
$FFE0, $FFE1	Standard Timer channel 7	I-Bit	T0IE (T0C7I)	$E0
$FFDE, $FFDF	Standard Timer overflow	I-Bit	T0MSK2 (T0OI)	$DE
$FFDC, $FFDD	Pulse accumulator overflow	I-Bit	PACTL0 (PAOVI0)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL0 (PAI0)	$DA
$FFD8, $FFD9	SPI	I-Bit	SPCR1 (SPIE, SPTIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	$D2
$FFD0, $FFD1	Reserved			
$FFCE, $FFCF	Port J	I-Bit	PTJIF (PTJIE)	$CE
$FFCC, $FFCD	Port H	I-Bit	PTHIF (PTHIE)	$CC
$FFCA, $FFCB	Port G	I-Bit	PTGIF (PTGIE)	$CA
$FFC8, $FFC9	Reserved			
$FFC6, $FFC7	CRG PLL lock	I-Bit	PLLCR (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	PLLCR (SCMIE)	$C4
$FFC2, $FFC3	Reserved			
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR(IBIE)	$C0

Table 5-1 Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFBA to $FFBF	Reserved			
$FFB8, $FFB9	FLASH	I-Bit	FCNFG (CCIE, CBEIE)	$B8
$FFB6, $FFB7	EPHY Interrupt	I-Bit	EPHYCTL0 (EPHYIE)	$B6
$FFB4, $FFB5	EMAC Receive Buffer A Complete	I-Bit	IMASK(RXACIE)	$B4
$FFB2, $FFB3	EMAC Receive Buffer B Complete	I-Bit	IMASK(RXBCIE)	$B2
$FFB0, $FFB1	EMAC Frame Transmission Complete	I-Bit	IMASK(TXCIE)	$B0
$FFAE, $FFAF	EMAC Receive Flow Control	I-Bit	IMASK (RFCIE)	$AE
$FFAC, $FFAD	EMAC MII Management transfer Complete	I-Bit	IMASK(MMCIE)	$AC
$FFAA, $FFAB	EMAC Receive error	I-Bit	IMASK (RXAIE)	$AA
$FFA8, $FFA9	EMAC Receive Buffer A Overrun	I-Bit	IMASK(RXAOIE)	$A8
$FFA6, $FFA7	EMAC Receive Buffer B Overrun	I-Bit	IMASK(RXBOIE)	$A6
$FFA4, $FFA5	EMAC Babbling receive error	I-Bit	IMASK (BREIE)	$A4
$FFA2, $FFA3	EMAC Late collision	I-Bit	IMASK(LCIE)	$A2
$FFA0, $FFA1	EMAC Excessive collision	I-Bit	IMASK(ECIE)	$A0
$FF80 to $FF9F	Reserved			

5.3 Resets

Resets are a subset of the interrupts featured in**Table 5-1**. The different sources capable of generating a system reset are summarized in **Table 5-2**.

5.3.1 Reset Summary Table

Table 5-2 Reset Summary

Reset	Priority	Source	Vector
Power-on Reset	1	CRG Module	$FFFE, $FFFF
External Reset	1	RESET pin	$FFFE, $FFFF
Low Voltage Reset	1	VREG Module	$FFFE, $FFFF
Clock Monitor Reset	2	CRG Module	$FFFC, $FFFD
COP Watchdog Reset	3	CRG Module	$FFFA, $FFFB

5.3.2 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block Guides for register reset states. Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM Block Guide for reset configurations of all peripheral module ports.

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), the Debug module (DBG), and background debug mode module (BDM).

Section 7 Voltage Regulator (VREG) Block Description

Consult the VREG Block Guide for information about the dual output linear voltage regulator. The VREG is part of the IPBus domain.

7.1 VDDR (*VREGEN)*

On the MC9S12NE-Family the VDDR pin is used to enable or disable the internal voltage 3.3V to 2.5V regulator. If this pin is tied low VDD1/2, VDDPLL, PHY_VDDRX, PHY_VDDTX, and PHY_VDDA must be supplied externally.

7.2 VDD1, VDD2, VSS1, VSS2

In both the 112 pin LQFP and the 80 pin QFP package versions, both internal VDD and VSS of the 2.5V domain are bonded out on 2 sides of the device as two pin pairs (VDD1, VSS1 & VDD2, VSS2). VDD1 and VDD2 are connected together internally. VSS1 and VSS2 are connected together internally. This allows systems to employ better supply routing and further decoupling.

Section 8 Recommended PCB Layout (Need to Update)

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic capacitor connected as near as possible to the corresponding pins (C1 - C6).
- Central point of the ground star should be the VSSX pin.
- Use low ohmic low inductance connections between VSS1, VSS2 and VSSX.
- VSSPLL must be directly connected to VSSX.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C7, C8, C11 and Q1 as small as possible.

- Do not place other signals or supplies underneath area occupied by C7, C8, C10 and Q1 and the
- connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Table 8-1 Recommended decoupling capacitor choice

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	100 .. 220nF
C2	VDD2 filter cap	ceramic X7R	100 .. 220nF
C3	VDDA filter cap	ceramic X7R	100nF
C4	VDDX2 filter cap	X7R/tantalum	>=100nF
C5	VDDPLL filter cap	ceramic X7R	100nF
C6	VDDX1 filter cap	X7R/tantalum	>=100nF
C7	PHY_VDDA filter cap	ceramic X7R	100 .. 220nF
C8	PHY_VDDTX filter cap	ceramic X7R	100 .. 220nF
C9	PHY_VDDRX filter cap	ceramic X7R	100 .. 220nF
R1	RBIAS resistor	1.0%	12.4K
C9	PLL loop filter cap	See PLL specification chapter	
C10	PLL loop filter cap		
R2	PLL loop filter res		
C11	OSC load cap		
C12	OSC load cap		
R3	OSC resistor		
R4	OSC resistor		
Q1	Quartz		

Figure 8-1 Recommended PCB Layout (112 LQFP)

NOTE : Oscillator in Pierce mode.

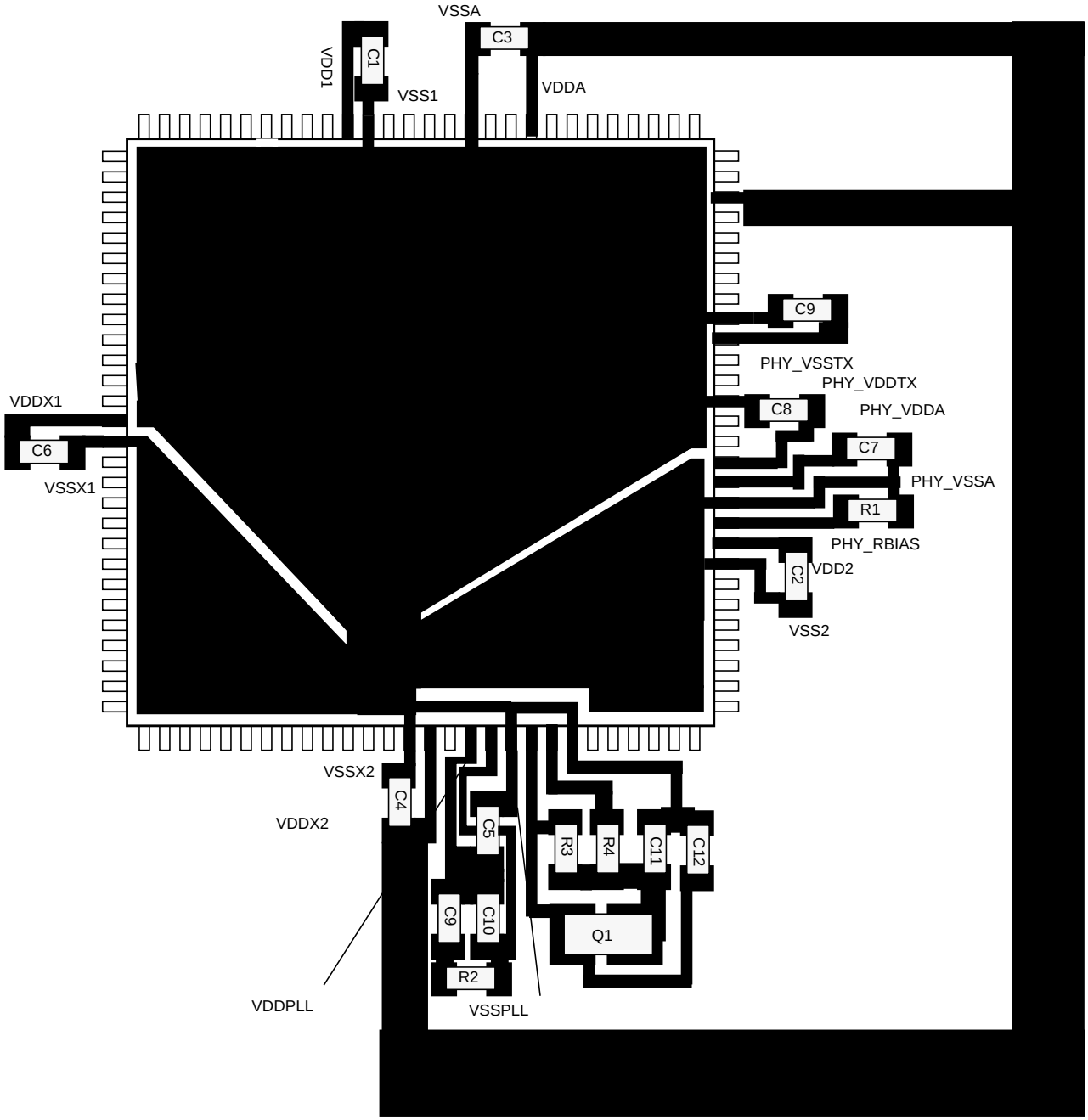
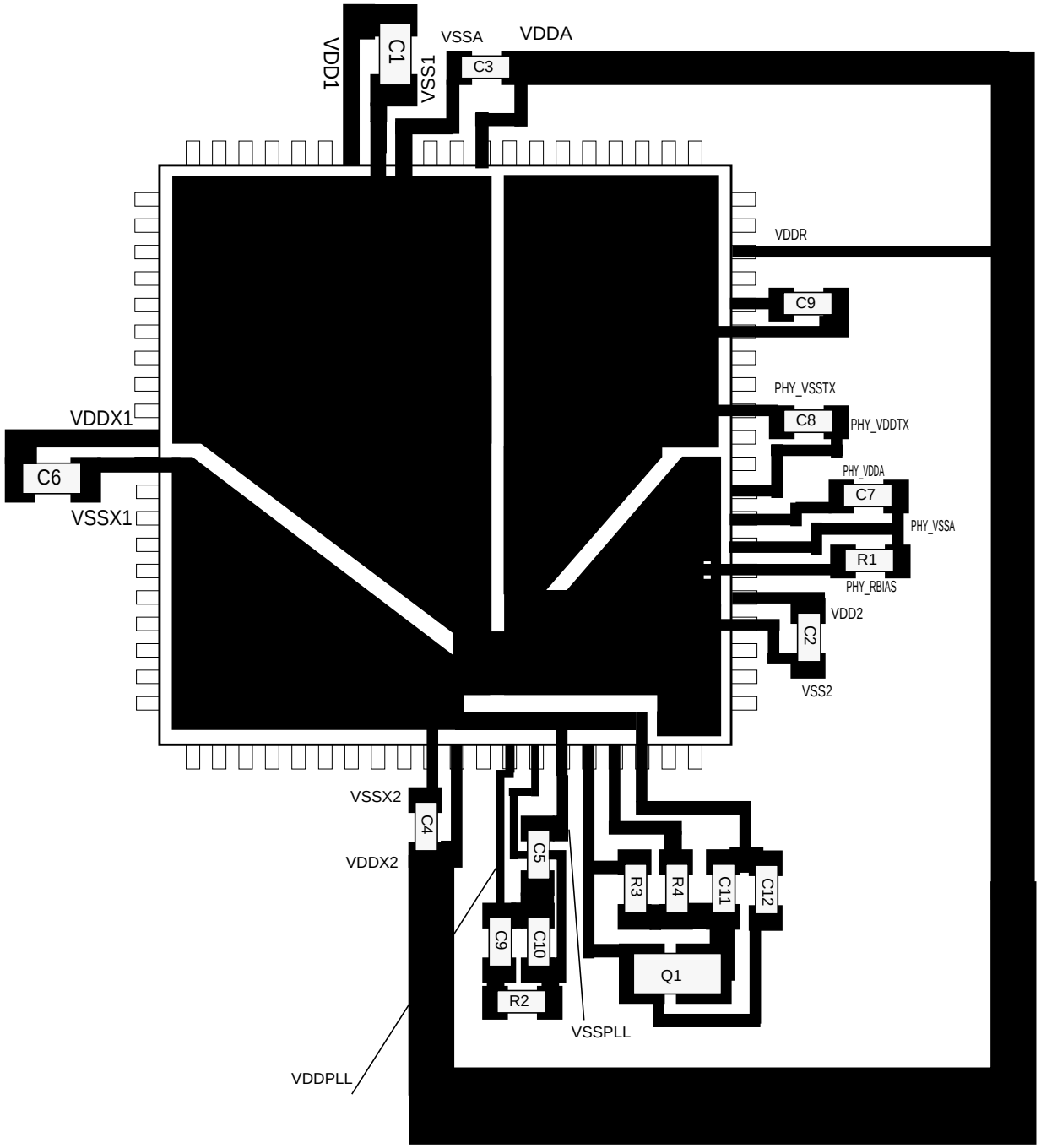


Figure 8-2 Recommended PCB Layout (80 QFP)

NOTE : Oscillator in Pierce mode.



Section 9 Clock Reset Generator (CRG) Block Description

Consult the CRG Block Guide for information about the Clock and Reset Generator module. The CRG is part of the IPBus domain.

The Low Voltage Reset feature uses the low voltage reset signal from the VREG module as an input to the CRG module. When the regulator output voltage supply to the internal chip logic falls below a specified threshold the LVR signal from the VREG module causes the CRG module to generate a reset. Consult the VREG Block User Guide for voltage level specifications.

9.1 $\overline{\text{XCLKS}}$

The $\overline{\text{XCLKS}}$ input signal is not available on the MC9S12NE-Family. The signal is internally tied low to select the Pierce Oscillator or External clock configuration.

Section 10 Oscillator (OSC) Block Description

The Pierce Oscillator is available on the 9S12NE-Family devices. Consult the OSC Block User Guide for information about the Oscillator module.

Section 11 Timer (TIM) Block Description

Consult the TIM_16B4C Block Guide for information about the Timer module. The TIM is part of the IPBus domain.

Section 12 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B8C Block Guide for further information about the A/D Converter module. The ATD is part of the IPBus domain.

Section 13 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interface modules (SCI0, SCI1). Consult the SCI Block Guide for information about the Serial Communications Interface module. The SCI is part of the IPBus domain.

Section 14 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block Guide for information about the Serial Peripheral Interface module. The SPI is part of the IPBus domain.

Section 15 Inter IC Bus (IIC) Block Description

Consult the IIC Block Guide for information about the Inter IC Bus module. The IIC is part of the IPBus domain.

Section 16 Ethernet Media Access Controller (EMAC)

Consult the EMAC Block Guide for information about the Ethernet Media Access Controller module. The EMAC is part of the IPBus domain.

16.1 EMAC MII external pin configuration

When the EMAC is configured for and external Ethernet physical transceiver internal pull-ups and pull-downs are not automatically configured on the MII inputs. Any internal pull-up or pull-down resistors, which may be required, need to be configured by setting the appropriate pull control registers in the Port Integration Module (PIM). This implementation allows the use of external pull-up and pull-down resistors where desired. Consult the PIM_9NE64 Block Guide for information about the Port Integration Module.

16.2 EMAC internal PHY configuration

When the EXTPHY bit, in the EMAC NETCTL register, is set to one the EMAC is configured to work with the internal EPHY block. Please see **Section 17 Ethernet Physical Transceiver (EPHY)** for more information regarding the EPHY block.

16.3 Low Power Operation

Special care must be taken when executing STOP and WAIT instructions while using the EMAC or undesired operation may result.

16.3.1 WAIT

Transmit and receive operations are not possible in WAIT mode if the CWAI bit is set in the CLKSEL register, since the clocks to the transmit and receive buffers are stopped. It is recommended that the EMAC ESWAI bit be set if WAIT mode is entered with the CWAI set.

16.3.2 STOP

During system low power Stop mode, the EMAC is immediately disabled. Any receive in progress is dropped and any PAUSE time-out is cleared. The user is required not to enter low power Stop mode when TXACT or BUSY are set.

Section 17 Ethernet Physical Transceiver (EPHY)

Consult the EPHY Block Guide for information about the Ethernet Physical Transceiver module. The EPHY is part of the IPBus domain. The EPHY also has MII register space which is not part of the MCU address space and not accessible via the IPBus. The MII registers can be accessed using the MDIO functions of the EMAC when the EMAC is configured for internal PHY operation.

The MII pins of the EPHY are not externally accessible. All communication and management of the EPHY must be done using the EMAC.

17.1 Low Power Operation

Special care must be taken when executing STOP and WAIT instructions while using the EPHY or undesired operation may result.

17.1.1 WAIT

Transmit and receive operations are not possible in WAIT mode if the CWAI bit is set in the CLKSEL register, since the clocks to the internal MII interface are stopped.

17.1.2 STOP

During system low power STOP mode, the EPHY is immediately reset and powered down. Upon exiting STOP mode the a start-up delay needs to be waited prior to initiating MDIO communications with the EPHY. See the **Section B.10 EPHY Electrical Characteristics**.

It is not possible to use an EPHY interrupt to wake the system from STOP mode.

Section 18 Port Integration Module (PIM) Block Description

Consult the PIM_9NE64 Block Guide for information about the Port Integration Module. The PIM is part of the IPBus domain.

Section 19 Flash EEPROM 64K Block Description

Consult the FTS64K Block Guide for information about the flash module.

Section 20 RAM 8K Block Description

This module supports single-cycle misaligned word accesses without wait states. The RAM is part of the HCS12 Bus domain.

In addition to operating as the CPU storage the, 8K or 12K system RAM also functions as the FIFO buffer when the EMAC module is enabled. When the EMAC is enabled the FIFO will occupy 0.375K to 4.5K of RAM with physical addresses starting at $0000 and ending at $017F up to $11FF, depending on the setting of the BUFMAP bits in the EAMC FIFO Buffer Configuration register (BUFCFG). The relative RAM address, which are controlled by settings in the Internal RAM Position register (INTRM) must be tracked in software.

The FIFO operation of the RAM is independent of the CPU and allows same cycle read/write access from the CPU and the EMAC. There is no hardware blocking mechanism implemented to prevent the CPU from accessing the FIFO RAM space, so care must be taken that the CPU does not corrupt the RAM FIFO contents.

Appendix A Electrical Characteristics

A.1 General

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values cannot be guaranteed by Motorola and are subject to change without notice.*

NOTE: *The part is specified and tested over the 3.3V range.*

This supplement contains the most accurate electrical information for the MC9S12NE-Family microcontroller available at the time of publication. The information should be considered **PRELIMINARY** and is subject to change.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate, under the "C" column heading.

P: Those parameters are guaranteed during production testing on each individual device.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. They are regularly verified by production monitors.

T: Those parameters are achieved by design characterization on a small sample size from typical devices. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12NE-Family utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL, the Ethernet Physical Transceiver (EPHY) as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter and portions of the EPHY.
The VDDX1, VDDX2, VSSX1, VSSX2 pairs supply the I/O pins, and internal voltage regulator
The VDDR supplies the internal voltage regulator, and is the VREGEN signal.
VDD1, VSS1, VDD2 and VSS2 are the supply pins for the digital logic.
VDDPLL, VSSPLL supply the oscillator and the PLL.
VSS1 and VSS2 are internally connected by metal.
VDD1 and VDD2 are internally connected by metal.
PHY_VDDA, PHY_VSSA are power Supply Pins for EPHY Analog
PHY_VDDRX, PHY_VSSRX are power Supply Pins for EPHY Receiver

PHY_VDDTX, PHY_VSSTX are power Supply Pins for EPHY Transmitter
VDDA, VDDX1, VDDX2 as well as VSSA, VSSX1, VSSX2 are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context*
VDD3 is used for either VDDA, VDDR, and VDDX1/VDDX2
VSS3 is used for either VSSA, VSSR, and VSSX1/VSSX2 unless otherwise noted.
IDD3 denotes the sum of the currents flowing into the VDDA, VDDR , and VDDX1/VDDX2 pins.
VDD is used for VDD1, VDD2, VDDPLL, PHY_VDDTX, PHY_VDDRX, and PHY_VDDA;
VSS is used for VSS1, VSS2, VSSPL, PHY_VSSTX, PHY_VSSRX, and PHY_VSSA.
IDD is used for the sum of the currents flowing into VDD1, VDD2.
I_{DDPHY} is used for the sum of currents flowing into PHY_VDDTX, PHY_VDDRX, and PHY_VDDA
V_{DDPHY} is used for PHY_VDDTX, PHY_VDDRX, and PHY_VDDA
V_{DDTX} is used for twisted pair differential voltage present on the PHY_TXP and PHY_TXN pins
I_{DDTX} is used for twisted pair differential current flowing into the PHY_TXP or PHY_TXN pins

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 3.3V I/O pins

Those I/O pins have a nominal level of 3.3V. This group of pins is comprised of all port I/O pins, the analog inputs, BKGD pin and the RESET inputs.The internal structure of these pins are identical, however some of the functionality may be disabled.

A.1.3.2 Analog Reference / Special function Analog

This group of pins is comprised of the VRH, VRL, TXN, TXP, RXN, RXP and RBIAS pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only, and should be tied to ground during normal operation.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD3} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD3}$) is greater than I_{DD3}, the injection current may flow out of VDD3 and could result in external power supply going out of regulation. Insure external VDD3 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS3} or V_{DD3}).

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD3}	-0.3	4.5	V
2	Digital Logic Supply Voltage[1]	V_{DD}	-0.3	3.0	V
3	PLL Supply Voltage (1)	V_{DDPLL}	-0.3	3.0	V
4	Voltage difference VDDX to VDDR and VDDA	Δ_{VDDX}	-0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	-0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	-0.3	6.5	V
7	Analog Reference	$V_{RH,}$ V_{RL}	-0.3	6.5	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	-0.3	3.0	V
9	TEST input	V_{TEST}	-0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins [2]	I_D	-25	+25	mA
11	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[3]	I_{DL}	-25	+25	mA
12	Instantaneous Maximum Current Single pin limit for TEST[4]	I_{DT}	-0.25	0	mA
13	Operating Temperature Range (ambient)	T_A	– 40	85	°C
14	Operating Temperature Range (junction)	T_J	– 40	125	°C
15	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
2. All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, V_{DDR} or V_{SSA} and V_{DDA}.
3. These pins are internally clamped to V_{SSPLL} and V_{DDPLL}
4. This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device

specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ohm
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Machine	Series Resistance	R1	0	Ohm
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	-	- 3 3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	-	V
2	C	Machine Model (MM)	V_{MM}	200	-	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	-	V
4	C	Latch-up Current at 125°C positive negative	I_{LAT}	+100 -100	-	mA
5	C	Latch-up Current at 27°C positive negative	I_{LAT}	+200 -200	-	mA

A.1.7 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Instead of specifying ambient temperature all parameters are specified for the more meaningful silicon junction temperature. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O and Regulator Supply Voltage	V_{DDX}	3.135	3.3	3.465	V
Analog Supply Voltage	V_{DDA}	3.135	3.3	3.465	V
Regulator Supply Voltage	V_{DDR}	3.135	3.3	3.465	V
Digital Logic Supply Voltage[1]	V_{DD}	2.375	2.5	2.625	V
PLL Supply Voltage (1)	V_{DDPLL}	2.375	2.5	2.625	V
Voltage Difference VDDX1/VSSX2 to VDDA	Δ_{VDDX}	-0.1	0	0.1	V
Voltage Difference VSSX/VSSX2 to VSSA	Δ_{VSSX}	-0.1	0	0.1	V
Oscillator[2]	f_{osc}	0.5	-	25	MHz
Bus Frequency	f_{bus}	0.5	-	25	MHz
Operating Junction Temperature Range	T_J	-40	-	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate VDD1, VDD2, VDDPLL, PHY_VDDRX, PHY_VDDTX and PHY_VDDA supplies out of the V_{DDX} and V_{DDR} supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. For the internal Ethernet Physical transceiver (EPHY) to operate properly a 25MHz oscillator is required.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

Two cases with internal voltage regulator enabled and disabled must be considered:

1. Internal Voltage Regulator disabled

$$P_{INT} = I_{DD} \cdot V_{DD} + I_{DDPLL} \cdot V_{DDPLL} + I_{DDA} \cdot V_{DDA} + I_{DDPHY} \cdot V_{DDPHY} + I_{DDTX} \cdot V_{DDTX}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX.

For R_{DSON} is valid:

$$R_{DSON} = \frac{V_{OL}}{I_{OL}}; \text{for outputs driven low}$$

respectively

$$R_{DSON} = \frac{V_{DD3(5)} - V_{OH}}{I_{OH}}; \text{for outputs driven high}$$

2. Internal voltage regulator enabled

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA} + I_{DDX} \cdot V_{DDX} + I_{DDTX} \cdot V_{DDTX}$$

I_{DDX} is the current shown in **Table A-7** and not the overall current flowing into VDDX, which additionally contains the current flowing into the external loads with output high.

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

Which is the sum of all output currents on I/O ports associated with VDDX.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	–	–	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	–	–	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	–	–	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	–	–	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	–	–	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	–	–	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	3	°C/W
6	T	Thermal Resistance Epad TQFP 80, single sided PCB	θ_{JA}	–	–	48	°C/W
7	T	Thermal Resistance Epad TQFP 80, double sided PCB with 2 internal planes	θ_{JA}	–	–	24	°C/W
8	T	Junction to Board QFP80	θ_{JB}	–	–	10	°C/W
9	T	Junction to Case QFP80[4]	θ_{JC}	–	–	0.7	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	–	–	2	°C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-3
3. PC Board according to EIA/JEDEC Standard 51-7
4. Thermal resistance between the die and the exposed die pad.

A.1.9 I/O Characteristics

This section describes the characteristics of all 3.3V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 Preliminary 3.3V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD3}	-	-	V
	T	Input High Voltage	V_{IH}	-	-	VDD3 + 0.3	V
2	P	Input Low Voltage	V_{IL}	-	-	0.35*V_{DD3}	V
	T	Input Low Voltage	V_{IL}	VSS3 - 0.3	-	-	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current (pins in high ohmic input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	-	2.5	µA
5	C	Output High Voltage (pins in output mode) Partial Drive I_{OH} = –0.75mA	V_{OH}	V_{DD3} – 0.4	-	-	V
6	P	Output High Voltage (pins in output mode) Full Drive I_{OH} = –4.5mA	V_{OH}	V_{DD3} – 0.4	-	-	V
7	C	Output Low Voltage (pins in output mode) Partial Drive I_{OL} = +0.9mA	V_{OL}	-	-	0.4	V
8	P	Output Low Voltage (pins in output mode) Full Drive I_{OL} = +5.5mA	V_{OL}	-	-	0.4	V
9	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	-	-	–60	µA
10	C	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	-6	-	-	µA
11	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	-	-	60	µA
12	C	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	6	-	-	µA
13	D	Input Capacitance	C_{in}		7	-	pF
14	T	Injection current[2] Single Pin limit Total Device Limit. Sum of all injected currents	I_{ICS} I_{ICP}	-2.5 -25	-	2.5 25	mA
15	P	Port G, H, and J Interrupt Input Pulse filtered[3]	t_{PIGN}			3	µs
16	P	Port G, H, and J Interrupt Input Pulse passed(3)	t_{PVAL}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Refer to **Section A.1.4 Current Injection**, for more details
3. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 25MHz bus frequency using a 25MHz oscillator.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P C P C	Run supply currents Single Chip, Internal regulator enabled, EPHY disabled Single Chip, Internal regulator enabled, EPHY Auto Negotiate[1] Single Chip, Internal regulator enabled, EPHY 100TX[1] Single Chip, Internal regulator enabled, EPHY 10BT[1]	I_{DD3}			65 285 265 185	mA
2	C C P	Wait Supply current All modules enabled All modules but EPHY enabled only RTI enabled	I_{DDW}			270 40 5	mA
3	C P C C C P	Pseudo Stop Current (RTI and COP enabled) -40°C 27°C 70°C 85°C 105°C 125°C	I_{DDPS}		TBD 600 TBD TBD TBD 1000	750 5000	µA
4	C C C C C C	Pseudo Stop Current (RTI and COP disabled) -40°C 27°C 70°C 85°C 105°C 125°C	I_{DDPS}		TBD 160 TBD TBD TBD 700	400 5000	µA
5	C P C C C P	Stop Current -40°C 27°C 70°C 85°C 105°C 125°C	I_{DDS}		TBD 30 TBD 200 TBD 500	100 5000	µA

NOTES:

1. When Calculating power consumption the additional current sunk by the TXN and TXP pins needs to be taken into account. See **Table 20-1 EPHY Twisted Pair Transmit pin Characteristics** for currents and voltages to use in the power calculations.

Table 20-1 EPHY Twisted Pair Transmit pin Characteristics

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Auto-Negotiate Transmiter current	I_{DDTX}			130	mA
2	C	Auto-Negotiate Transmiter voltage	V_{DDTX}			*VDD3*-1.1V	V
3	C	10BaseT Mode Transmiter current	I_{DDTX}			130	mA
4	C	10BaseT Mode Transmiter voltage	V_{DDTX}			*VDD3*-1.1V	V
5	C	100BaseTx Mode Transmiter current	I_{DDTX}			45	mA
6	C	100BaseTx Mode Transmiter voltage	V_{DDTX}			*VDD3*-0.95V	V

Appendix B Electrical Specifications

B.1 Voltage Regulator Operating Characteristics

This section describes the characteristics of the on chip voltage regulator (VREG_PHY).

Table 20-2 VREG_PHY - Operating Conditions

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	P	Input Voltages	$V_{VDDR,A,X}$	3.135	—	3.465	V
2	P	Regulator Current Reduced Power Mode Shutdown Mode	I_{REG}	— —	20 12	50 40	µA µA
3	P	Output Voltage Core Full Performance Mode Reduced Power Mode Shutdown Mode	V_{DD}	2.375 1.6 —	2.5 2.5 1	2.625 2.75 —	V V V
4	P	Output Voltage PLL Full Performance Mode Reduced Power Mode[2] Shutdown Mode	V_{DDPLL}	2.375 1.6 —	2.5 2.5 3	2.625 2.75 —	V V V
5	P	Low Voltage Reset[4] Assert Level Deassert Level	V_{LVRA} V_{LVRD}	2.25 —	— —	— 2.55	V V
7	C	Power-on Reset[5] Assert Level Deassert Level	V_{PORA} V_{PORD}	0.97 —	--- ---	— 2.05	V V

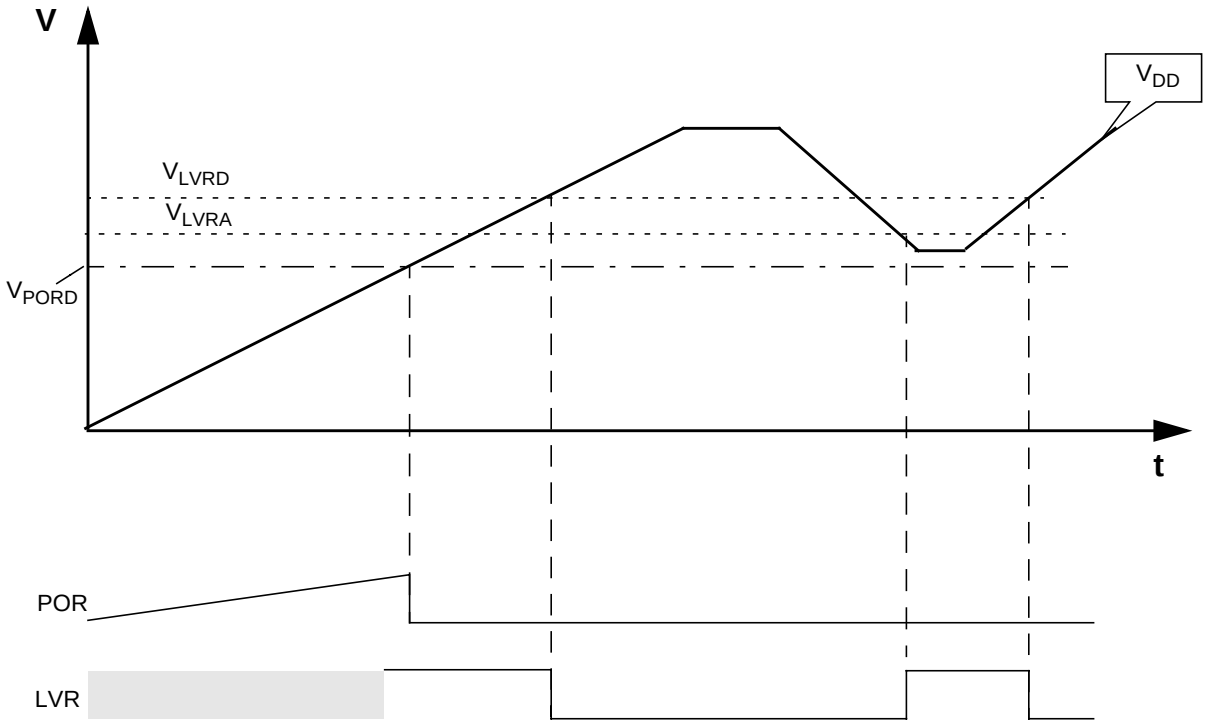
NOTES:
1. High Impedance Output
2. Current IDDPLL = 3mA (Pierce Oscillator)
3. High Impedance Output
4. Monitors V_{DD}, active only in Full Performance Mode. V_{LVRA} and V_{PORD} must overlap
5. Monitors V_{DD}. Active in all modes.

NOTE: *The electrical characteristics given in this section are preliminary and should be used as a guide only. Values in this section cannot be guaranteed by Motorola and are subject to change without notice.*

B.2 Chip Power-up and LVR graphical explanation

Voltage regulator sub modules POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in **Figure B-1**.

Figure B-1 Voltage Regulator - Chip Power-up and Voltage Drops (not scaled)



B.3 Output Loads

B.3.1 Resistive Loads

The on-chip voltage regulator is intended to supply the internal logic and oscillator circuits allows no external DC loads.

B.3.2 Capacitive Loads

The capacitive loads are specified in **Table B-1**. Ceramic capacitors with X7R dielectricum are required.

Table B-1 Voltage Regulator - Capacitive Loads

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	VDD external capacitive load	C_{DDext}	200	440	12000	nF
2	PHY_VDDTX external capacitive load	$C_{DDPLLext}$	90	220	5000	nF
2	PHY_VDDRX external capacitive load	$C_{DDPLLext}$	90	220	5000	nF
2	PHY_VDDA external capacitive load	$C_{DDPLLext}$	90	220	5000	nF
2	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

B.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

B.4.1 Startup

Table B-2 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table B-2 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}
7	P	LVR release level	V_{LVRR}	2.25			V
8	P	LVR assert level	V_{LVRA}			2.55	V

B.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

B.4.1.2 LVR

The release level V_{LVRR} and the assert level V_{LVRA} are derived from the V_{DD} Supply. They are also valid if the device is powered externally. After releasing the LVR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

B.4.1.3 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

B.4.1.4 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

B.4.1.5 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

B.4.1.6 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

B.4.2 Oscillator

The device features an internal Pierce oscillator. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up

time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table B-3 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (Colpitts) **(NOT AVALIABLE)**	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) [1,2]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}		8[3]	100[4]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [2]	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high	t_{EXTH}	9.5			ns
9	D	External square wave rise time	t_{EXTR}			1	ns
10	D	External square wave fall time	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V
		EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$	$0.7*V_{DDPLL}$			V
		EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$			V_{DDPLL}+ 0.3	V
		EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$			$0.3*V_{DDPLL}$	V
		EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$	V_{SSPLL}- 0.3			V
		EXTAL Pin Input Hysteresis[4]	$V_{HYS,EXTAL}$		250		mV

NOTES:
1. Depending on the crystal a damping series resistor might be necessary
2. $\overline{XCLKS}$ =0 during reset
3. f_{osc} = 4MHz, C = 22pF.
4. Maximum value is for extreme cases using high Q, low frequency crystals

B.4.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

B.4.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

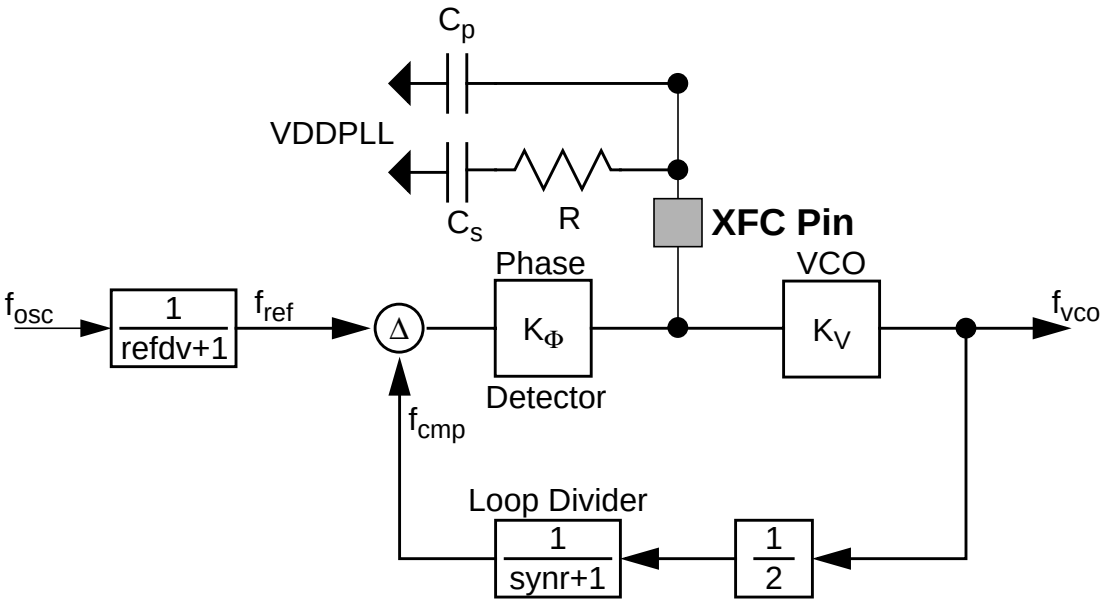


Figure B-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table B-4**.

The grey boxes show the calculation for f_{VCO} = 50MHz and f_{ref} = 1MHz. E.g., these frequencies are used for f_{OSC} = 4MHz and a 25MHz bus clock.

The VCO Gain at the desired VCO frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}} = -100 \cdot e^{\frac{(60-50)}{-100}} = -90.48\text{MHz/V}$$

The phase detector relationship is given by:

$$K_\Phi = -|i_{ch}| \cdot K_V = 316.7\text{Hz}/\Omega$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. ζ = 0.9 ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \quad \frac{1}{10} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 10}; (\zeta = 0.9)$$

$f_C < 25kHz$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1) \quad = 50$$

With the above values the resistance can be calculated. The example is shown for a loop bandwidth f_C=10kHz:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi} \quad = 2*\pi*50*10kHz/(316.7Hz/\Omega)=9.9k\Omega=\sim 10k\Omega$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9) \quad = 5.19nF =\sim 4.7nF$$

The capacitance C_p should be chosen in the range of:

$$C_s / 20 \leq C_p \leq C_s / 10 \quad C_p = 470pF$$

B.4.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure B-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure B-3**.

NOTE: *This section is under construction*

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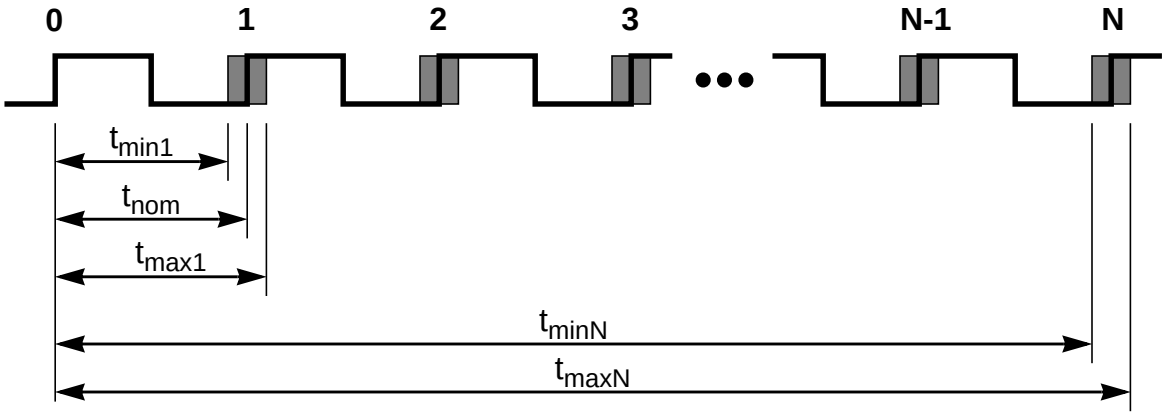


Figure B-3 Jitter Definitions

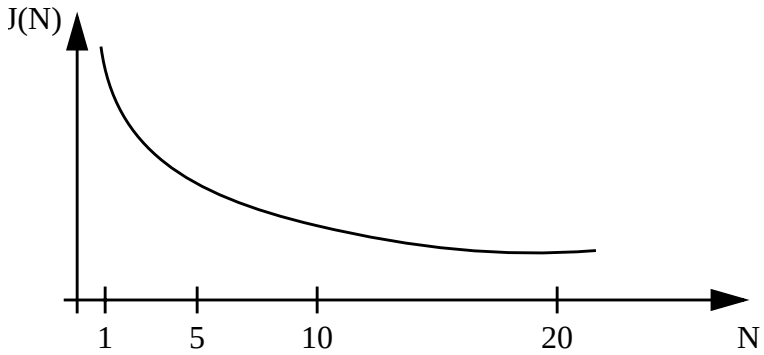
The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$



This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table B-4 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[(1)]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[(1)]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[(1)]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [(2)]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [(2)]	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		-100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1[(2)]	j_1			1.1	%
15	C	Jitter fit parameter 2[(2)]	j_2			0.13	%

NOTES:

1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$018, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

B.5 Flash NVM

B.5.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV register. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table B-5** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

B.5.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

B.5.1.2 Burst Programming

Flash programming where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

B.5.1.3 Sector Erase

Erasing a 512 byte Flash sectortakes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

B.5.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup times can be ignored for this operation.

Table B-5 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50[1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46[2]		74.5[3]	µs
5	D	Flash Burst Programming consecutive word	t_{bwpgm}	20.4[2]		31[3]	µs
6	D	Flash Burst Programming Time for 32 Words	t_{brpgm}	678.4[2]		1035.5[3]	µs
7	P	Sector Erase Time	t_{era}	20[4]		26.7[3]	ms
8	P	Mass Erase Time	t_{mass}	100[4]		133[3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11[5]		32778[6]	t_{cyc}

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f bus . Refer to formulae in Sections A.3.1.1 - A.3.1.4 for guidance.
4. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP} .
5. Minimum time, if first word in the array is not blank
6. Maximum time to complete check on an erased block.

B.5.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at <2ppm defects over lifetime at the operating conditions noted.

A program/erase cycle is specified as two transitions of the cell value from erased → programmed → erased, 1 → 0 → 1.

NOTE: *All values shown in **Table B-6** are target values and subject to further extensive characterization.*

Table B-6 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Data Retention at an average junction temperature of T_{Javg} = 85°C	t_{NVMRET}	15			Years
2	C	Data Retention at a junction temperature of T_J = 140°C	t_{NVMRET}	10			Years
3	C	Flash number of Program/Erase cycles	n_{FLPE}	10,000			Cycles

B.6 SPI Characteristics

This section provides electrical parametrics and ratings for the SPI.

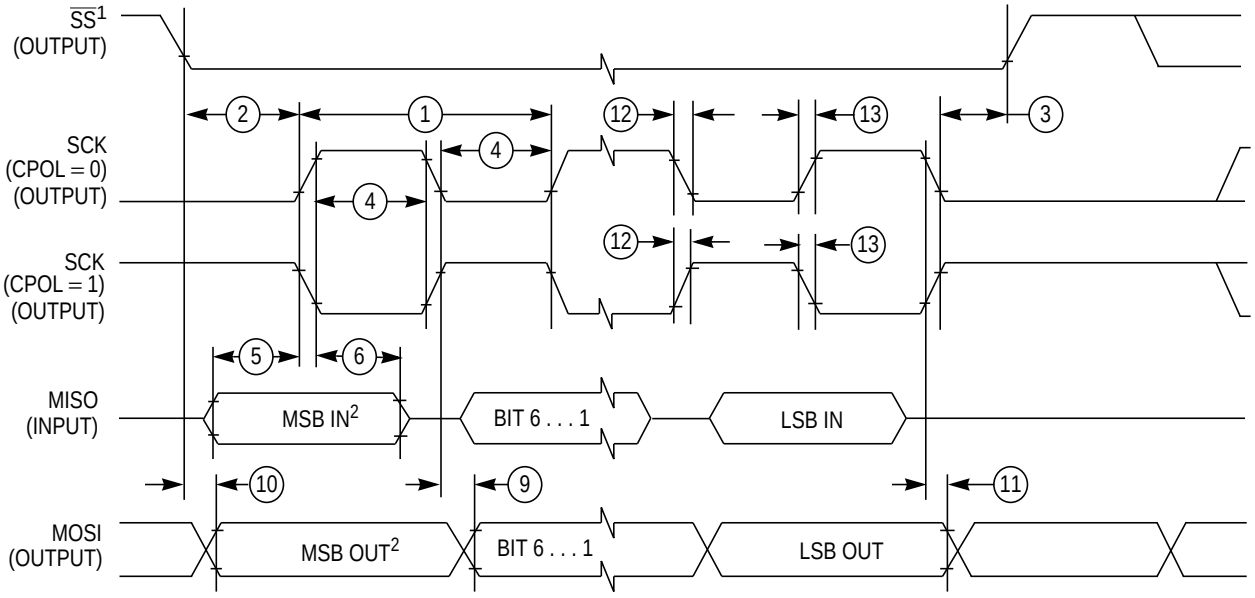
In **Table B-7** the measurement conditions are listed.

Table B-7 Measurement Conditions

Description	Value	Unit
Drive mode	full drive mode	—
Load capacitance C_{LOAD}, on all outputs	50	pF
Thresholds for delay measurement points	(20% / 80%) VDDX	V

B.6.1 Master Mode

In **Figure B-4** the timing diagram for master mode with transmission format CPHA=0 is depicted.

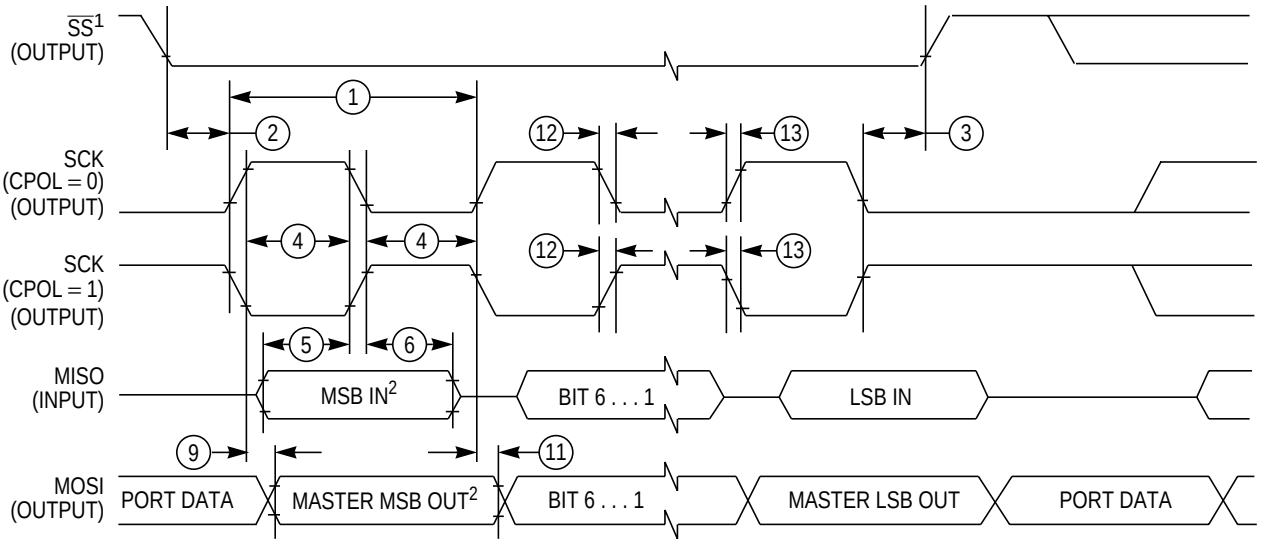


1.if configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure B-4 SPI Master Timing (CPHA=0)

In **Figure B-5** the timing diagram for master mode with transmission format CPHA=1 is depicted.



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure B-5 SPI Master Timing (CPHA=1)

In **Table B-8** the timing characteristics for master mode are listed.

Table B-8 SPI Master Mode Timing Characteristics

Num	C	Characteristic	Symbol				Unit
				Min	Typ	Max	
1	P	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	P	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	—	1/2	—	t_{sck}
3	D	Enable Lag Time	t_{lag}	—	1/2	—	t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	30	ns
10	D	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

B.6.2 Slave Mode

In **Figure B-6** the timing diagram for slave mode with transmission format CPHA=0 is depicted.

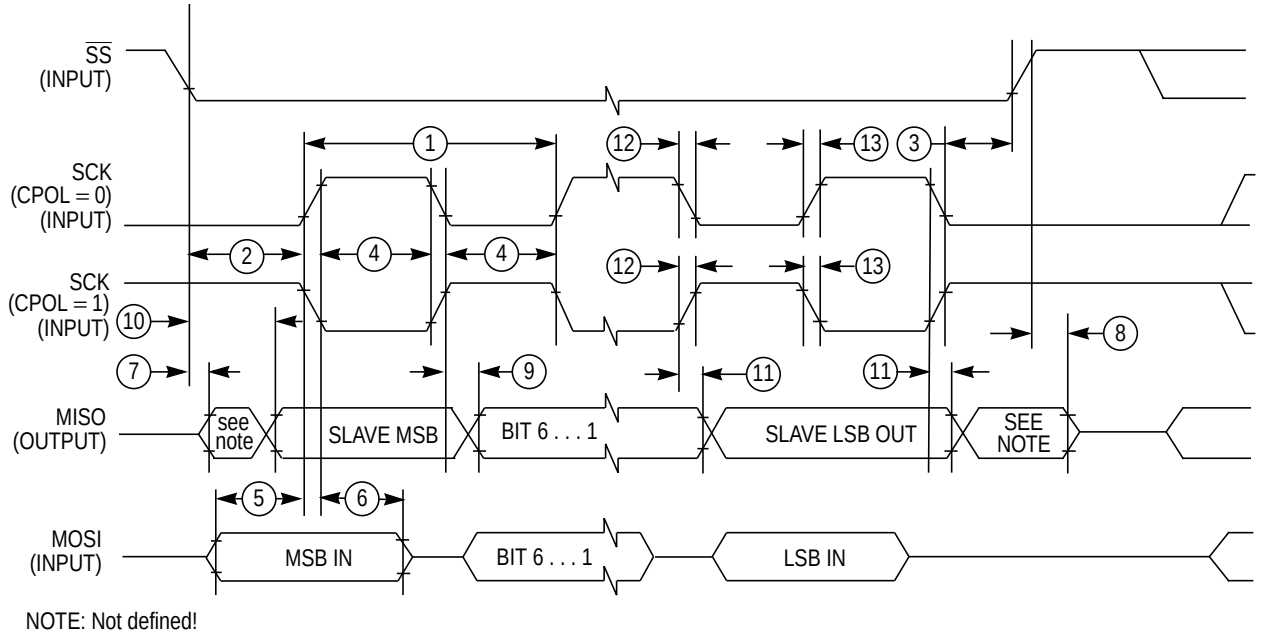
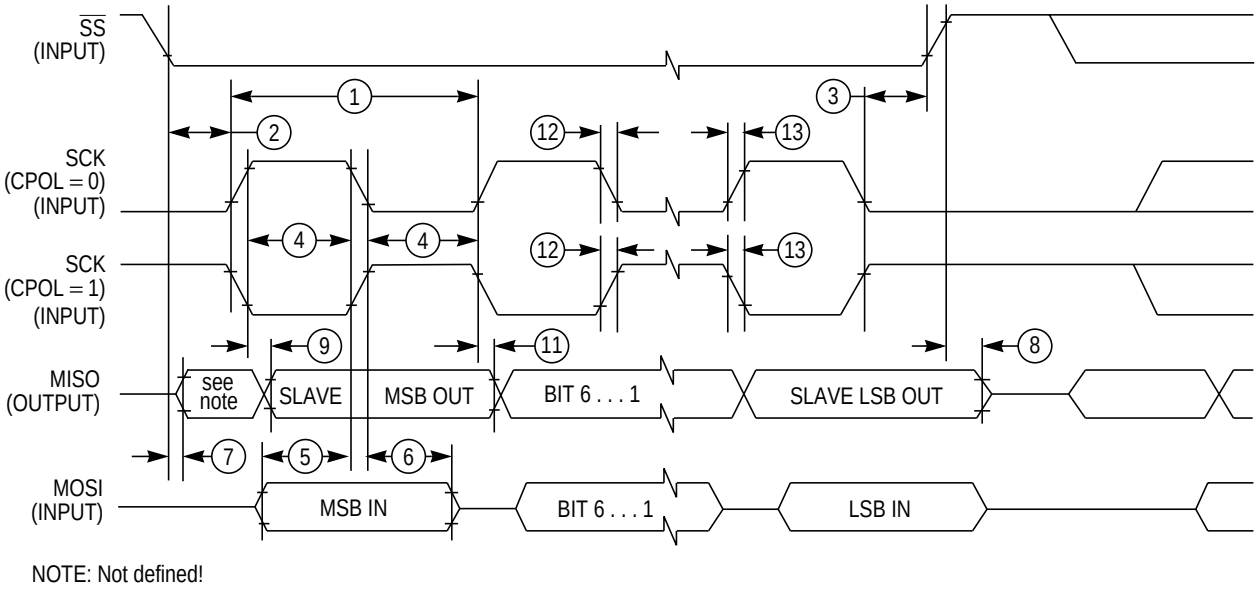


Figure B-6 SPI Slave Timing (CPHA=0)

In **Figure B-7** the timing diagram for slave mode with transmission format CPHA=1 is depicted.



NOTE: Not defined!

Figure B-7 SPI Slave Timing (CPHA=1)

In **Table B-9** the timing characteristics for slave mode are listed.

Table B-9 SPI Slave Mode Timing Characteristics

Num	C	Characteristic	Symbol	Min	Typ	Max	Unit
1	P	SCK Frequency	f_{sck}	DC	—	1/4	f_{bus}
1	P	SCK Period	t_{sck}	4	—	∞	t_{bus}
2	D	Enable Lead Time	t_{lead}	4	—	—	t_{bus}
3	D	Enable Lag Time	t_{lag}	4	—	—	t_{bus}
4	D	Clock (SCK) High or Low Time	t_{wsck}	4	—	—	t_{bus}
5	D	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	D	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
7	D	Slave Access Time (time to data active)	t_{a}	—	—	20	ns
8	D	Slave MISO Disable Time	t_{dis}	—	—	22	ns
9	D	Data Valid after SCK Edge	t_{vsck}	—	—	30 + t_{bus} [1]	ns
10	D	Data Valid after $\overline{SS}$ fall	t_{vss}	—	—	30 + t_{bus} [1]	ns
11	D	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	D	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	D	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

NOTES:
1. t_{bus} added due to internal synchronization delay

B.7 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

B.7.1 ATD Operating Characteristics - 3.3V Range

The **Table B-10** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
VSSA ≤ VRL ≤ VIN ≤ VRH ≤ VDDA. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table B-10 3.3V ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted; Supply Voltage 3.3V-10% <= V_{DDA} <= 3.3V+10%							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage	V_{RH}-V_{RL}	3.0	3.3	3.6	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[1] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles(1) Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Recovery Time (V_{DDA}=3.3 Volts)	t_{REC}			20	µs
7	P	Reference Supply current	I_{REF}			0.250	mA

NOTES:
1. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

B.7.2 Factors influencing accuracy

Three factors - source resistance, source capacitance and current injection - have an influence on the accuracy of the ATD.

B.7.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S

specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance are allowed.

B.7.2.2 Source capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

B.7.2.3 Current injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than VRH and $000 for values less than VRL unless the current is higher than specified as disruptive conditions.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table B-11 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	-	-	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 15	pF
3	C	Disruptive Analog Input Current	I_{NA}	-2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

B.7.3 ATD accuracy - 3.3V Range

Table B-12 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table B-12 3.3V ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} - V_{RL}$ = 3.328V. Resulting to one 8 bit count = 13mV and one 10 bit count = 3.25mV
f_{ATDCLK} = 2.0MHz

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		3.25		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1.5		1.5	Counts
3	P	10-Bit Integral Nonlinearity	INL	–3.5	±1.5	3.5	Counts
4	P	10-Bit Absolute Error[1]	AE	-5	±2.5	5	Counts
5	C	10-Bit Absolute Error at f_{ATDCLK}= 4MHz	AE		±7.0		Counts
6	P	8-Bit Resolution	LSB		13		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.5	±1.0	1.5	Counts
9	P	8-Bit Absolute Error(1)	AE	-2.0	±1.5	2.0	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure B-8**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

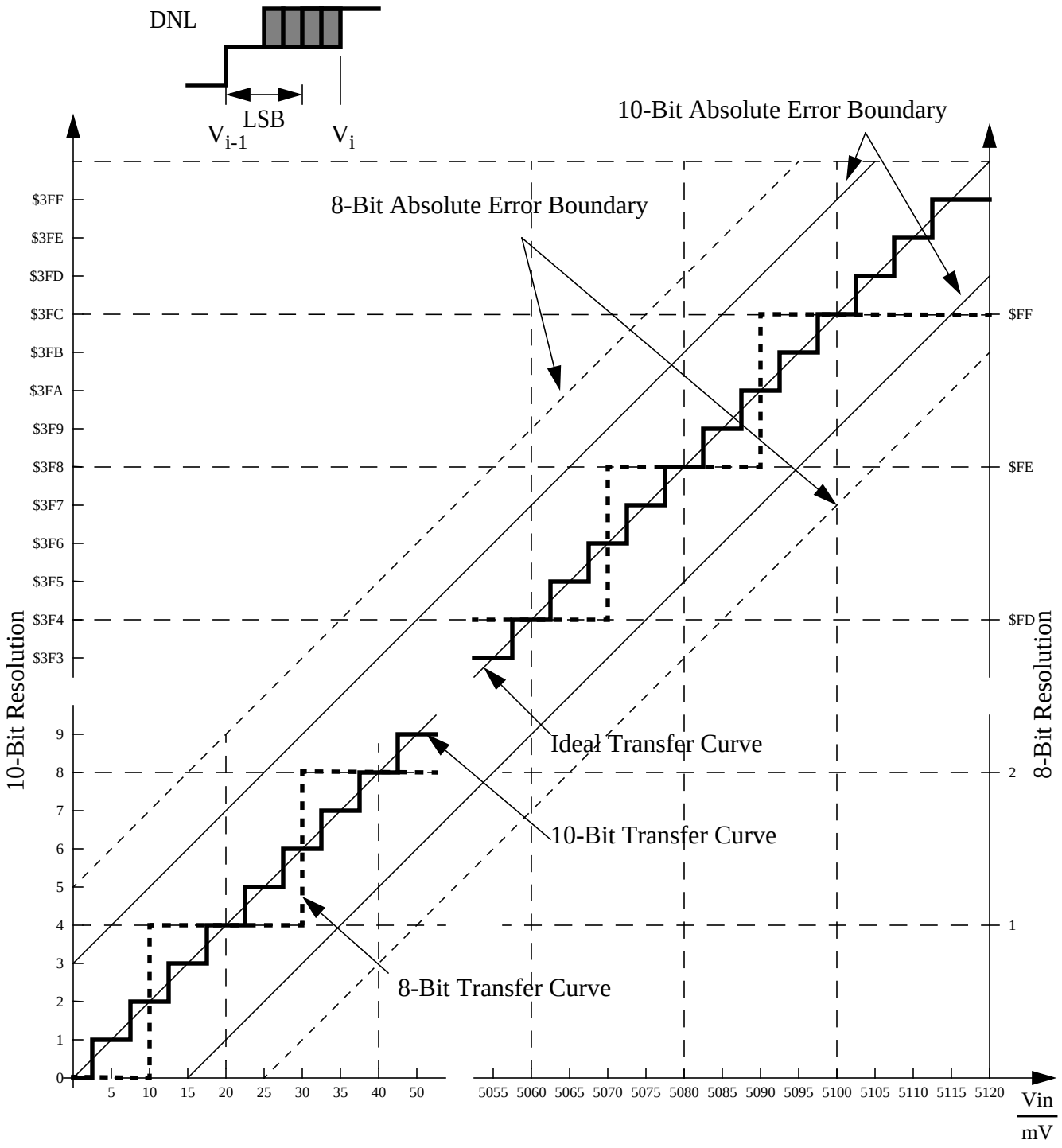


Figure B-8 ATD Accuracy Definitions

NOTE:Figure B-8 *shows only definitions, for specification values refer to* ***Table B-12*** *.*

B.8 EMAC Characteristics

This section describes the characteristics of the Ethernet Media Access Controller (EMAC).

B.9 MII Timing

The following MII timing is based on IEEE Std 802.3.

B.9.1 MII Receive Signal Timing (RXD[3:0], RXDV, RXER, RXCLK)

NUM	Characteristic	MIN	MAX	UNIT
M1	RXD[3:0], RXDV, RXER setup to RXCLK rise	10	-	ns
M2	RXCLK rise to RXD[3:0], RXDV, RXER hold	10	-	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

Table B-13 MII Receive Signal Timing

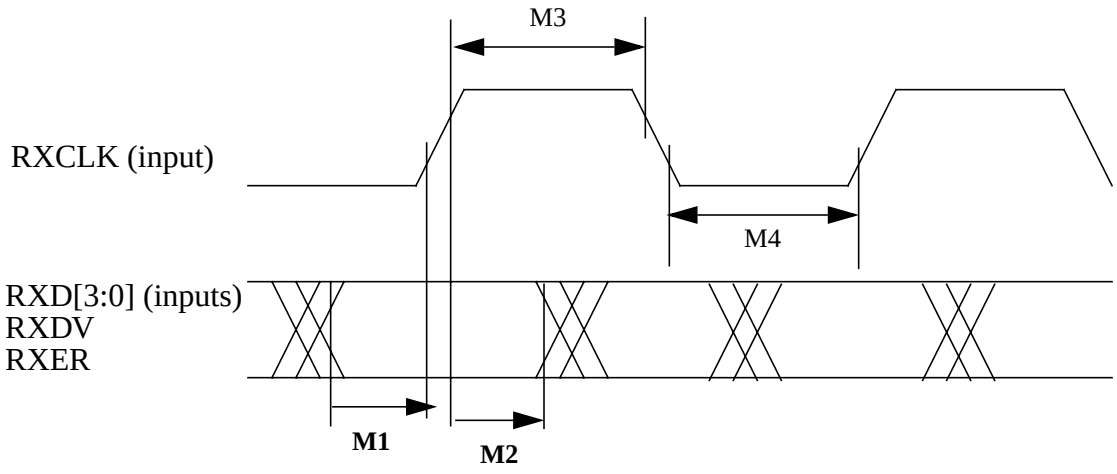


Figure B-9 MII Receive Signal Timing Diagram

B.9.2 MII Transmit Signal Timing (TXD[3:0], TXEN, TXER, TXCLK)

NUM	Characteristic	MIN	MAX	UNIT
M5	TXCLK rise to TXD[3:0], TXEN, TXER invalid	0	-	ns
M6	TXCLK rise to TXD[3:0], TXEN, TXER valid	-	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

Table B-14 MII Transmit Signal Timing

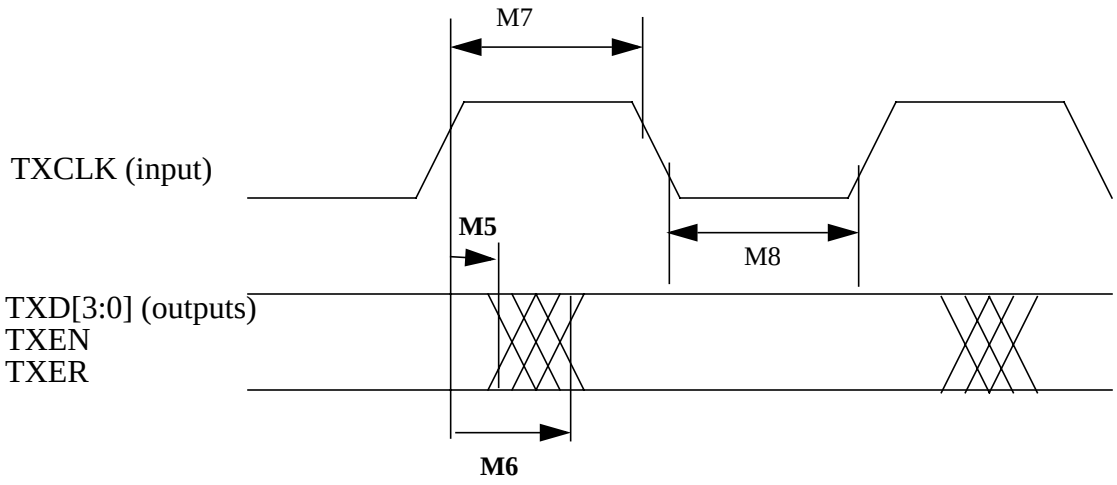


Figure B-10 MII Transmit Signal Timing Diagram

B.9.3 MII Asynchronous Inputs Signal Timing (CRS, COL)

NUM	Characteristic	MIN	MAX	UNIT
M9	CRS, COL minimum pulse width	1.5	-	TXCLK period

Table B-15 MII Transmit Signal Timing

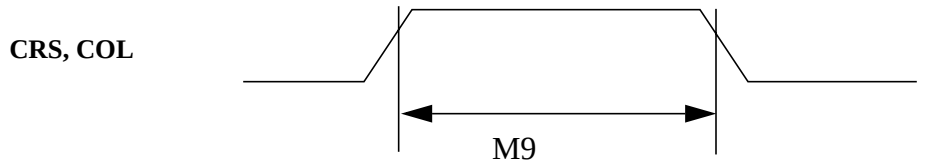


Figure B-11 MII Asynchronous Inputs Timing Diagram

B.9.4 MII Management Timing (MDIO,MDC)

NUM	Characteristic	MIN	MAX	UNIT
M10	MDC rise to MDIO (output) invalid	10	-	ns
M11	MDC rise to MDIO (output) valid	-	390	ns
M12	MDIO (input) setup to MDC rise	100	-	ns
M13	MDC rise to MDIO (input) hold	0	-	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

Table B-16 MII Management Signal Timing

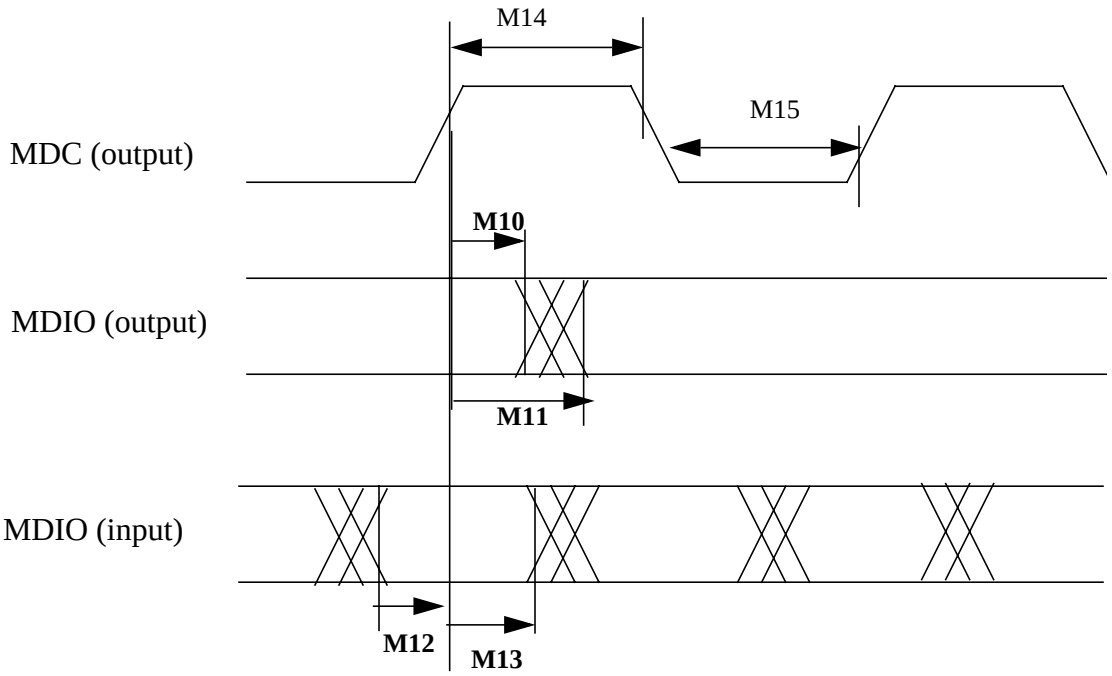


Figure B-12 MII Serial Management Channel Timing Diagram

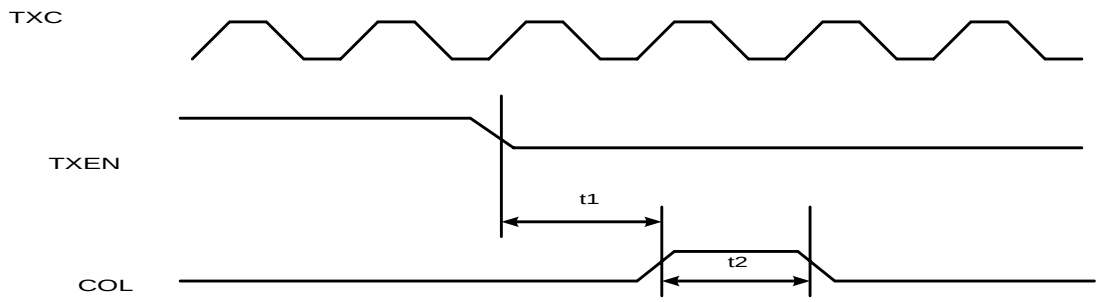
B.10 EPHY Electrical Characteristics

Table B-17 10Base-T SQE (Heartbeat) Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	COL (SQE) Delay after TXEN off	t1		1.0		µs
2	C	COL (SQE) Pulse duration	t2		1.0		µs

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure B-13 10Base-T SQE (Heartbeat) Timing



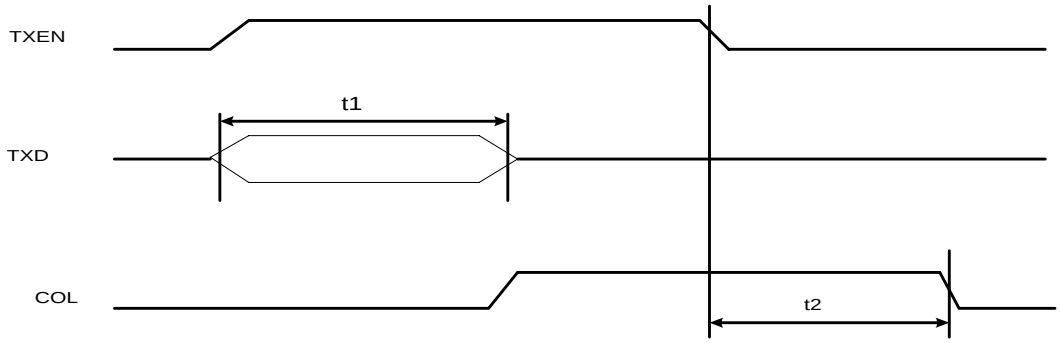
B.10.1 10Base-T Jab and Unjab Timing

Table B-18 10Base-T Jab and Unjab Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Maximum Transmit time	t1		98		ms
2	C	Unjab time	t2		525		ms

.Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure B-14 10Base-T SQE (Heartbeat) Timing



B.11 Auto Negotiation

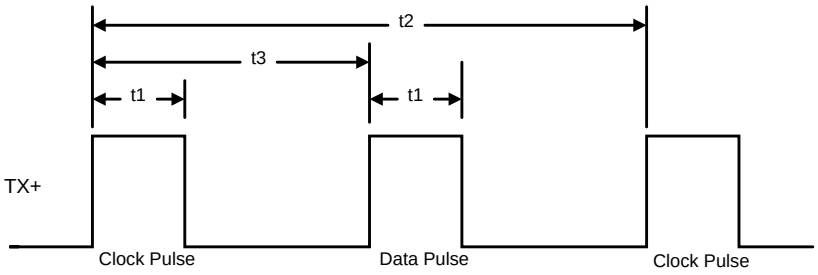
B.11.1 MII – 100Base-TX Transmit Timing Parameters

Table B-19 MII – Auto Negotiation and Fast Link Pulse Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Clock/Data pulse width	t1		100		ns
2	C	Clock pulse to Clock pulse	t2	111	125	139	µs
3	C	Clock pulse to Data pulse (Data = 1)	t3	55.5	62.5	69.5	µs
4	C	Pulses in a Burst	t4	17		33	#
5	C	FLP burst width	t5		2		ms
6	C	FLP burst to FLP burst	t6	8	16	24	ms

Typical values are at 25C.
1 BT = Bit Time = 100ns
These parameters are the minimum and maximum times as specified in section 24.6 of the IEEE 802.3u Standard

Figure B-15 A/N and Fast Link Pulse Timing



B.11.2 MII – 10Base-T Receive Timing

Table B-20 Auto Negotiation and Fast Link Pulse Timing

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Transmit FLNP width		1.25	1.5	1.75	µs
2	C	Receive FLNP width		1	1.5	2	µs
3	C	Clock/Data pulse width	t1		100		ns
4	C	Clock FLNP to Clock FLNP	t2	111	125	139	µs
5	C	Clock FLNP to Data FLNP (Data = 1)	t3	55.5	62.5	69.5	µs
6	C	Pulses in a Burst	t4	17		33	#
7	C	FLNP burst width	t5		2		ms
8	C	FLNP burst to FLNP burst	t6	8	16	24	ms

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure B-16 Fast Link Pulse Timing

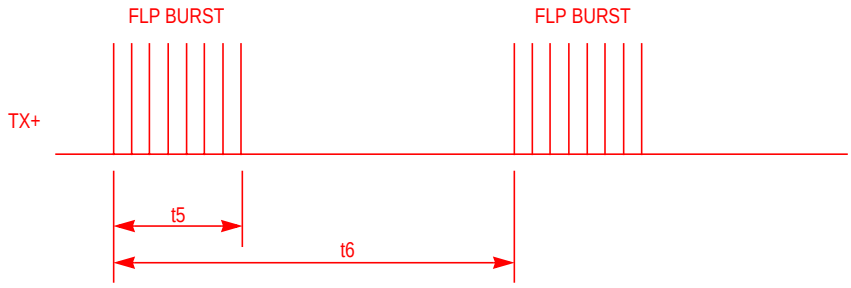


Figure B-17 AutoNegotiation Pulse Timing

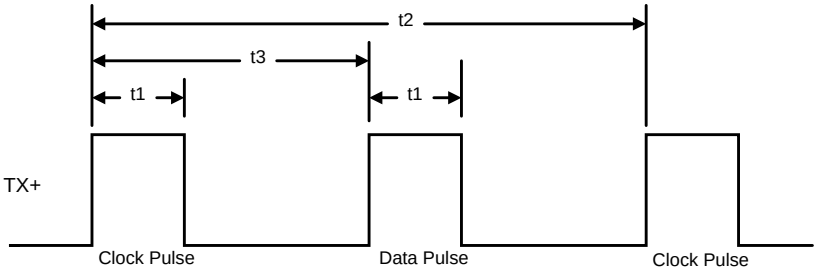
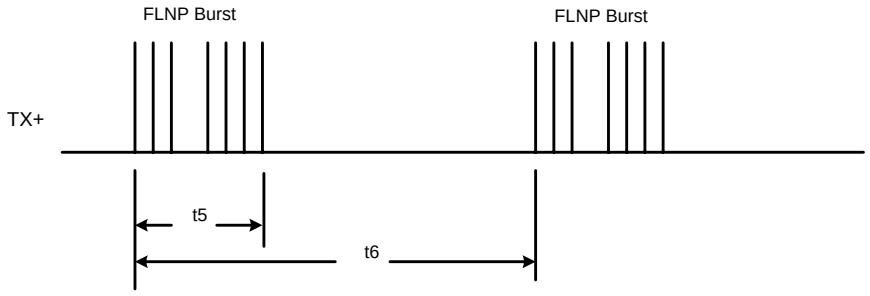


Figure B-18 Fast Link Pulse Timing



B.12 Electrical Specifications

Table B-21 10BaseT Transceiver Characteristics

Num	C	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	C	Peak Differential Output Voltage	VOP	2.2	2.5	2.8	V	With specified transformer and line replaced by 100ohm (+/-1%) load
2	C	Transmit Timing Jitter	-	0	2	11	ns	Using line model specified in the IEEE 802.3
3	C	Receive dc Input Impedance	Zin	-	10	-	kΩ	0.0 < Vin < 3.3V
4	C	Receive Differential Squelch Level	Vsquelch	300	400	585	mV	3.3MHz sine wave input

Table B-22 100BaseTX Transceiver Characteristics

Num	C	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	C	Transmit Peak Differential Output Voltage	VOP	0.95	1.00	1.05	V	With specified transformer and line replaced by 100ohm (+/-1%) load
2	C	Transmit Signal Amplitude Symmery	Vsym	98	100	102	%	With specified transformer and line replaced by 100ohm (+/-1%) load

Table B-22 100BaseTX Transceiver Characteristics

Num	C	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
3	C	Transmit Rise/Fall Time	Trf	3	4	5	ns	With specified transformer and line replaced by 100ohm (+/-1%) load
4	C	Transmit Rise/Fall Time Symmetry	Trfs	-0.5	0	+0.5	ns	See IEEE 802.3 for details
5	C	Transmit Overshoot/UnderShoot	Vosh	-	2.5	5	%	
6	C	Transmit Jitter	-	0	.6	1.4	ns	
7	C	Receive Common Mode Voltage	Vcm	-	1.6	-	V	VDDRX=2.5V
8	C	Receiver Maximum Input Voltage	Vmax	-	-	4.7	V	VDDRX=2.5V. Internal circuits protected by divider in shutdown

Appendix C External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure C-1** with the actual timing values shown on table **Table C-1**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

Figure C-1 General External Bus Timing

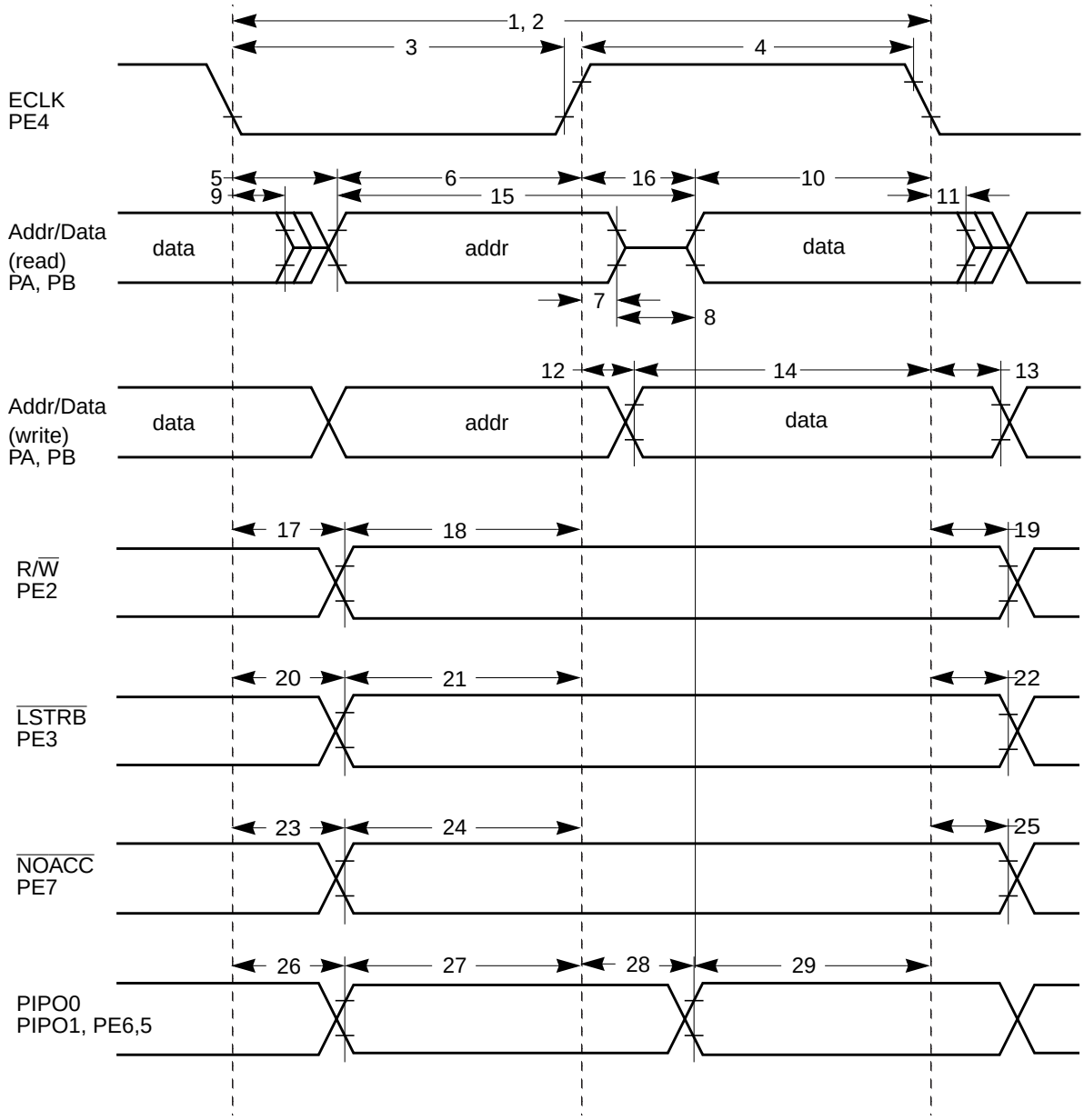


Table C-1 Expanded Bus Timing Characteristics (3.3V Range)

Conditions are VDDX=3.3V+/-5%, Junction Temperature -40˚C to +125˚C, C_{LOAD} = 50pF

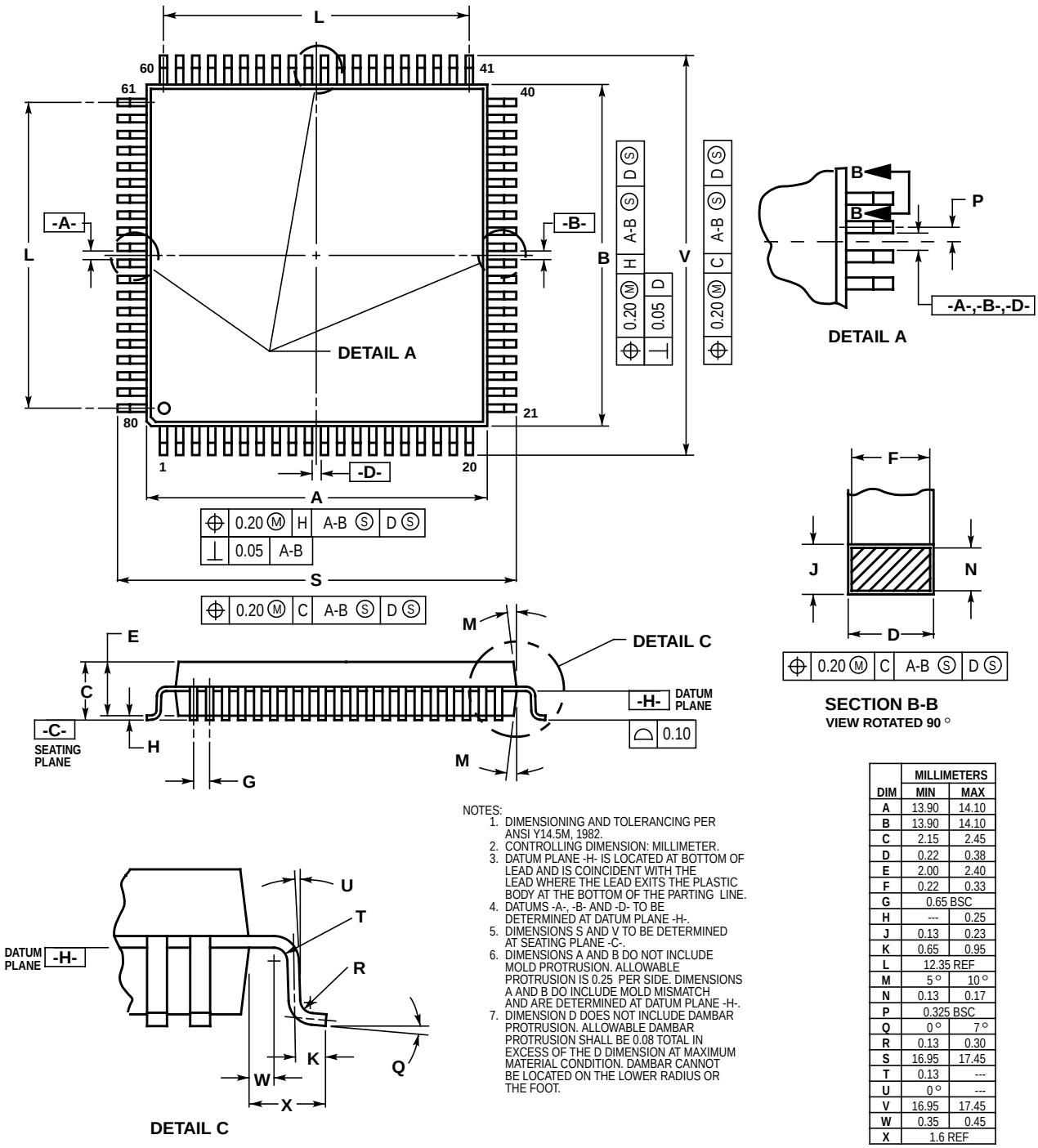
Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Frequency of operation (E-clock)	f_o	0		16.0	MHz
2	P	Cycle time	t_{cyc}	62.5			ns
3	D	Pulse width, E low	PW_{EL}	30			ns
4	D	Pulse width, E high[1]	PW_{EH}	30			ns
5	D	Address delay time	t_{AD}			16	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	16			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	15			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			15	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time(1) (PW_{EH}–t_{DDW})	t_{DSW}	15			ns
15	D	Address access time(1)	t_{ACCA}	29			ns
16	D	E high access time(1) (PW_{EH}–t_{DSR})	t_{ACCE}	15			ns
17	D	Read/write delay time	t_{RWD}			14	ns
18	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	16			ns
19	D	Read/write hold time	t_{RWH}	2			ns
20	D	Low strobe delay time	t_{LSD}			14	ns
21	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	16			ns
22	D	Low strobe hold time	t_{LSH}	2			ns
23	D	NOACC strobe delay time	t_{NOD}			14	ns
24	D	NOACC valid time to E rise (PW_{EL}–t_{LSD})	t_{NOV}	16			ns
25	D	NOACC hold time	t_{NOH}	2			ns
26	D	IPIPO[1:0] delay time	t_{P0D}	2		14	ns
27	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	16			ns
28	D	IPIPO[1:0] delay time(1)	t_{P1D}	2		25	ns
29	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

NOTES:

1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix D Package Information

D.1 80-pin QFP package

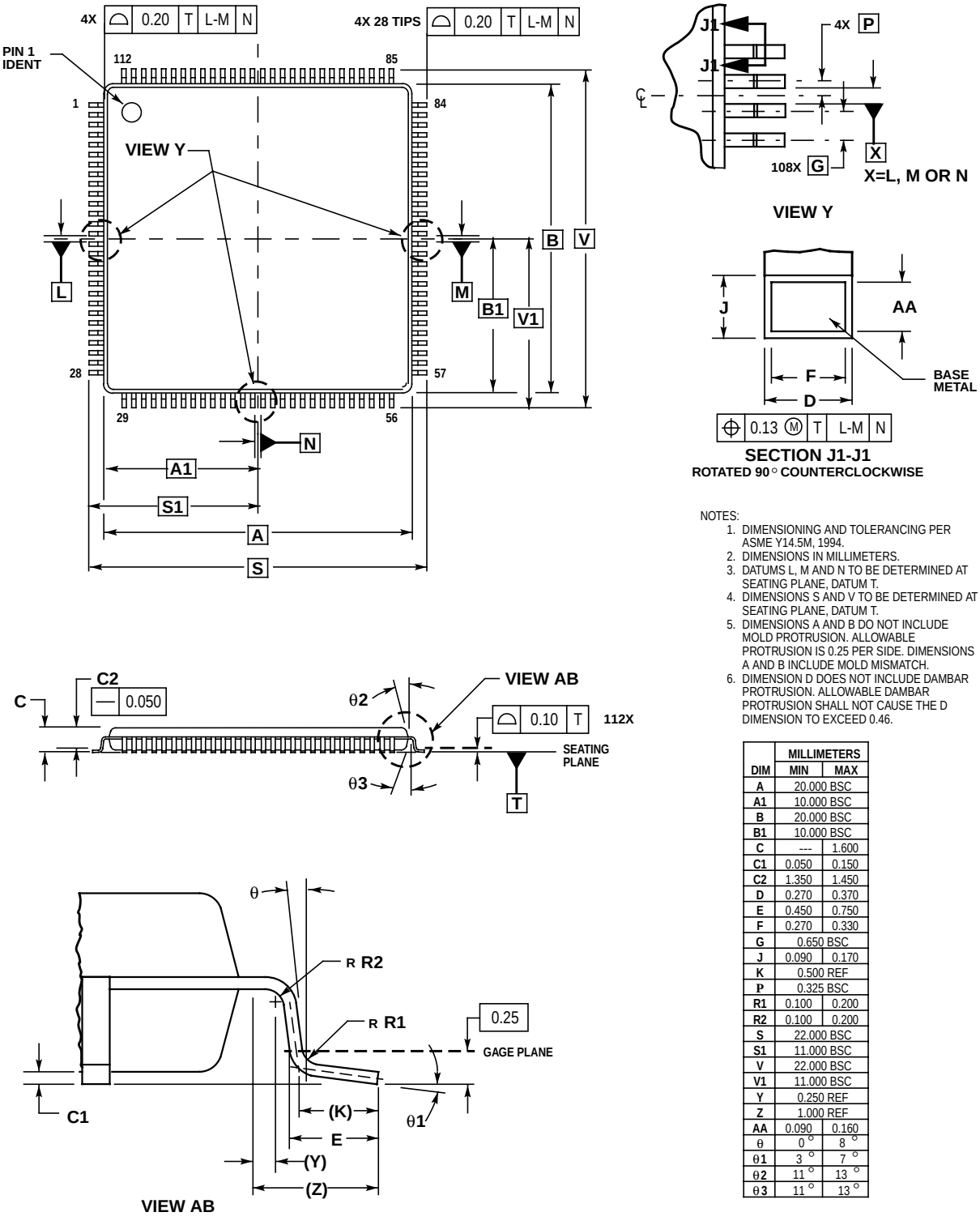


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure D-1 80-pin QFP Mechanical Dimensions (case no. 841B)

D.2 112-pin LQFP package



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Device User Guide End Sheet

FINAL PAGE OF
124
PAGES