Freescale Semiconductor
Mask Set Errata

MSE9S12UF32_1L47S
Rev. October 03, 2007

MC9S12UF32, Mask 1L47S

Introduction

This errata sheet applies to the following devices:

MC9S12UF32

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 1K79X. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0201" indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Errata System Tracking Numbers

MUCtsXXXXX is the tracking number for device errata. It can be used with the mask set and date code to identify a specific erratum.

Errata Summary

Errata Number	Module affected	Brief Description	Work-around
MUCts01498	ique	Security cannot be disabled via BDM unsecure command sequence	YES
MUCts01659	ata5hc	Invalid UDMA write sequence in a corner case	YES
MUCts01665	ique	Reset sequence in double buffer mode	YES
MUCts01861	S12_bdm	Possible manipulation of return address when exiting BDM active mode	YES
MUCts02415	S12_mebi	MEBI: Missing ECLK edge on first external access after mode switching	YES
MUCts03031	tim_16b8c	TIM:Normal Output Compare event happens on setting OC7M bit if OM/OL=0	YES

Security cannot be disabled via BDM unsecure command sequence — MUCts01498

Description

When security is enabled (MCU is reset with bits[1:0] of the flash security byte at address $FF0F set to '00', '01' or '11'), security cannot be disabled using the BDM mass erase/security byte reprogram sequence. A bug causes the blank check (performed by the BDM secure firmware) to fail and as a result the flash security byte cannot be reprogrammed to the unsecure state.

Workaround

Do not enable security by leaving bits[1:0] of the flash security byte programmed to '10'. (Ensure that these bits are programmed to '10' BEFORE resetting the MCU otherwise security will be enabled).

OR

The security can be disabled by reprogramming bits[1:0] of the security byte to '10' using a software routine embedded within the user program. The routine could, for example, be initiated by a user specified command issued through the SCI interface.

Invalid UDMA write sequence in a corner case — MUCts01659

Description

An invalid UDMA write sequence exists under a specific condition:
1) IQUE buffer is empty
2) ATA5HC controller buffer is not full
3) ATA device issues a transfer pausing with a termination sequence

4) USB receiver has just received a packet and stored it in the IQUE buffer
If all of the above conditions occur simultaneously, this will result in a word being missed and the transfer hanging.

Workaround

Monitor the IQUE buffer in software and swap buffer resources out if ~30
entries remain.

Reset sequence in double buffer mode — MUCts01665

Description

The default reset state for the read/write enable signal of the FSM Double Buffer Control circuit is low which allows read/write operations during reset. This will result in a cycle of false read/write acknowledge signals following reset if the Transmit Request or Receive Request signals are asserted.

Workaround

Change the QCnREQ value to $FF before resetting the IQUE module or Double Buffer Controller.

Possible manipulation of return address when exiting BDM active mode — MUCts01861

Description

Upon leaving BDM active mode, the CPU return address is stored temporarily for a few cycles in the BDM shift register. If a BDM command transmission is detected during this time, the return address will be manipulated in the BDM shift register. This situation is likely to occur when a CPU BGND instruction is executed in user code during debugging under the following conditions:

(i) The BDM module is not enabled AND
(ii) BDM commands are sent from the host

If this situation occurs, the CPU will execute BDM firmware and will check the status of the ENBDM bit in the BDMSTS register. If the BDM is disabled, the ENBDM bit will be clear, and hence the BDM firmware will be exited and the shift register manipulation described above will occur.

Workaround

Avoid using the BGND instruction when the ENBDM bit in the BDMSTS register is cleared.

MEBI: Missing ECLK edge on first external access after mode switching — MUCts02415

Description

If the ECLK is used as an external bus control signal (ESTR=1) the first external access is lost after switching from a single chip mode with enabled ECLK output to an expanded mode. The ECLK is erroneously held in the high phase thus the first external bus access does not generate a rising ECLK edge for the external logic to latch the address. The ECLK stretches low after the lost access resulting in all following external accesses to be valid.

Workaround

Enter expanded mode with ECLK output disabled (NECLK=1). Enable the ECLK after switching the mode before executing the first external access.

TIM:Normal Output Compare event happens on setting OC7M bit if OM/OL=0 — MUCts03031

Description

When an OC7M bit is set, an erroneous normal output compare event can happen on a timer port if the compare action is selected as "Timer disconnected from output pin logic ".

Corresponding configuration:
* TIOSx = 1 --> Output compare mode
* OMx = OLx = 0 --> Output compare logic disconnected from the pin
* OC7Mx = 1 --> Mask bit set for OC7 event

Workaround

Set OC7Mx = 1 only for channels where the output compare action should drive the pin, and OC7Mx = 0 for all other channels where the pin is required to be disconnected from the output compare logic.