EPHY
Block Guide
V01.00

Original Release Date: 06 OCT 2003
Revised: 06 OCT 2003

8/16 Bit Division - TSPG
Motorola, Inc.

Revision History

Version Number	Revision Date	Author	Description of Changes
V01.00	06 OCT 2003	Chad Lerma	Original draft.

Table of Contents

Section 4 Functional Description

Appendix A Electrical Specifications

List of Figures

List of Tables

Section 1 Introduction

1.1 Overview

The Ethernet Physical Transceiver (EPHY) is an IEEE 802.3u compliant 10/100 Ethernet PHY Transceiver. The EPHY module supports the 10/100 Mbps medium-independent interface (MII).

1.2 Features

- IEEE 802.3u Medium-Independent Interface (MII)
- IEEE 802.3 Compliant
- Digital Adaptive Equalization
- Single RJ45 connection
- Supports Auto-Negotiation
- 2.5V MII interface
- Baseline Wander Correction
- 2.5V CMOS
- Full/Half-duplex support in all modes
- 125 MHz Clock Generator and Timing Recovery
- Integrated wave-shaping circuitry
- Loop-back modes
- 1:1 Common Transformer
- Test Modes (Analog and Digital)
- Auto-Negotiation Next Page Ability
- Far-End Fault Detect.
- MDC rates up to 25 MHz.
- Supports MDIO preamble suppression
- Jumbo packet

1.3 Block Diagram

.

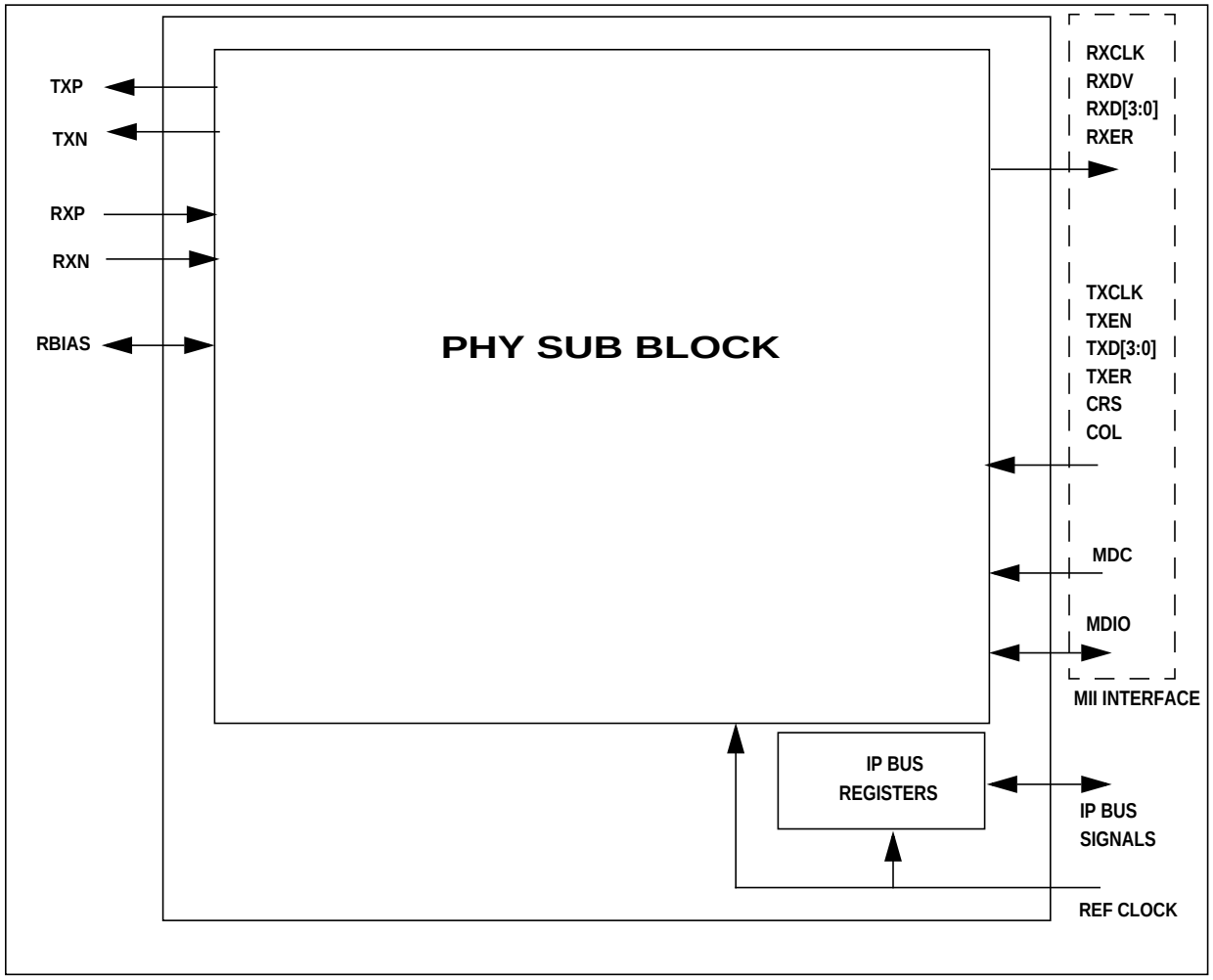
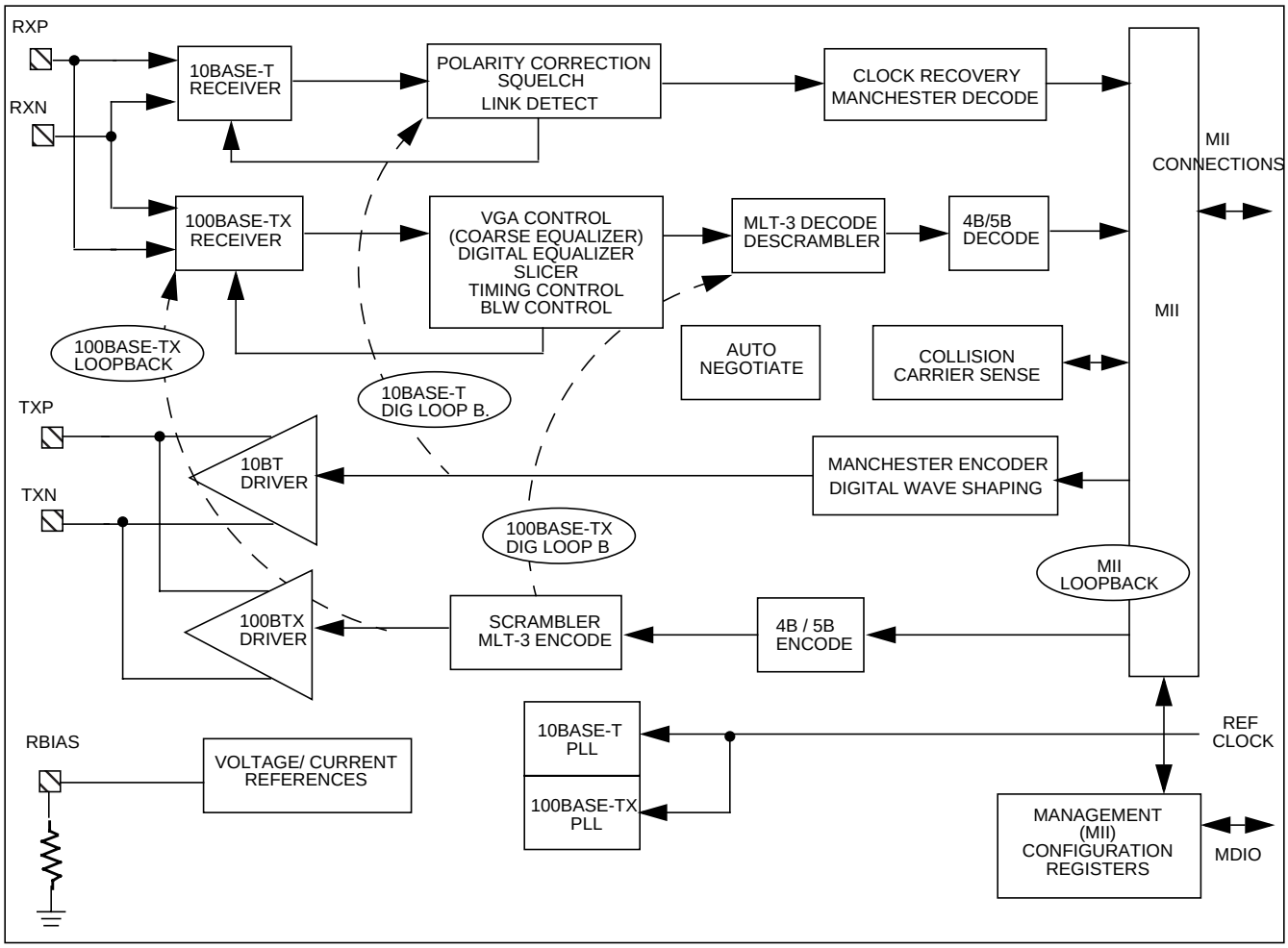


Figure 1-1 Ethernet Physical Transceiver (EPHY) Block Diagram

Figure 1-2 PHY SUB BLOCK Diagram



Section 2 External Signal Description

2.1 Overview

The EPHY module supports the twisted pair media interface and medium-independent interface (MII) which requires 18 I/O pins. The remaining two signals provide a MII Management interface. Each MII signal is described below.

2.2 Detailed Signal Descrip

2.2.1 PHY_TXP - EPHY Twisted Pair Output +

Ethernet twisted pair output pin. This pin is hi-z out of reset.

2.2.2 PHY_TXN - EPHY Twisted Pair Output -

Ethernet twisted pair output pin. This pin is hi-z out of reset.

2.2.3 PHY_RXP - EPHY Twisted Pair Input +

Ethernet twisted pair input pin. This pin is hi-z out of reset.

2.2.4 PHY_RXN - EPHY Twisted Pair Input -

Ethernet twisted pair input pin. This pin is hi-z out of reset.

2.2.5 PHY_RBIAS - EPHY Bias Control Resistor

Connect a 12.4K(1.0%) external resistor, RBIAS, between PHY_RBIAS pin and analog ground. This resistor should be placed as close a possible to the chip pin. Stray capacitance should be kept to less than 10pF (>50pF may cause instability). No high speed signals should go in the region of RBIAS.tions

2.2.6 TXCLK — MII Transmit Clock

This PHY output clock is used as a timing reference for TXD, TXEN, and TXER. It operates at 25% of the transmit data rate (25Mhz for 100 Mbps or 2.5Mhz for 10 Mbps).

2.2.7 TXD[3:0] — MII Transmit Data

TXD[3:0] is a transmit nibble of data to be transferred from a MAC to the PHY. The nibble is synchronized to the rising edge of TXCLK. When TXEN is asserted, the PHY accepts TXD[3:0], and when TXEN is de-asserted, TXD[3:0] has no meaning. TXD[0] is the least significant bit.**Table 2-1** summarizes the permissible encoding of TXD[3:0], TXEN and TXER.

TXEN	TXER	TXD[3:0]	Indication
0	0	0000 through 1111	Normal interframe
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 2-1 Permissible Encoding of TXD, TXEN and TXER

2.2.8 TXEN — MII Transmit Enable

TXEN indicates that there are valid nibbles being presented on the MII for transmission. It shall be synchronous with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TXEN will be negated prior to the first TXC following the final nibble of a frame. Assertion of this output signal indicates that there are valid nibbles being presented on the MII and the transmission can start. This signal is asserted with the first nibble of the preamble, remains asserted until all nibbles to be transmitted are presented to the PHY, and is negated following the final nibble of the frame.

2.2.9 TXER — MII Transmit Coding Error

Assertion of this input signal for one or more clock cycles while TXEN is asserted indicates that an MAC error has occurred on the Transmit Data stream. When operating in 100Base-TX the PHY will transmit one or more illegal symbols. It does not affect the transmission of data when the PHY is operating in 10Base-T mode, or when TXEN is de-asserted.

2.2.10 RXCLK — MII Receive Clock

The PHY provides this input clock which is used as a timing reference for RXD, RXDV, and RXER. It operates at 25% of the receive data rate (25Mhz for 100 Mbps or 2.5Mhz for 10 Mbps).

2.2.11 RXD[3:0] — MII Receive Data

RXD[3:0] is a receive nibble of data to be transferred from the PHY to a MAC. The nibble is synchronized to the rising edge of RXCLK. When RXDV is asserted, the RXD[3:0] is valid, and when RXDV is de-asserted, RXD[3:0] has no meaning. RXD[0] is the least significant bit. **Table 2-2** summarizes the permissible encoding of RXD, RXDV, and RXER, along with the specific indication provided by each code.

RXDV	RXER	RXD[3:0]	Indication
0	0	0000 through 1111	Normal interframe
0	1	0000	Normal interframe
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data reception with errors

Table 2-2 Permissible Encoding of RXD, RXDV and RXER

2.2.12 RXDV — MII Receive Data Valid

When this input signal is asserted, the PHY is indicating that a valid nibble is present on the MII. This signal remains asserted from the first recovered nibble of the frame through the last nibble. Assertion of RXDV will start no later than the Start Frame Delimiter (SFD).

2.2.13 RXER — MII Receive Error

RXDV is asserted by the PHY to indicate that a media error was detected during the transmission of the current frame. When RXDV is not asserted, RXER has no affect. This signal transitions synchronously with RXCLK.

2.2.14 CRS — MII Carrier Sense

This signal is asserted when the transmit or receive medium is in a non-idle state. When de-asserted, this signal indicates that the medium is in an idle state and a transmission can start. The CRS signal is synchronous to TXC or RXC. In the event of a collision, CRS remains asserted through the duration of the collision. In full duplex mode, this signal is undefined. This signal is not required to transition synchronously with TXCLK or RXCLK.

2.2.15 COL — MII Collision

This signal is asserted upon detection of a collision, and remains asserted while the collision persists. In full duplex mode, this signal is undefined.

2.2.16 MDC — MII Management Data Clock

This input signal from a MAC provides a timing reference to the PHY for data transfers on the MDIO signal. MDC is aperiodic, and has no maximum high or low times. The maximum clock frequency is 25 MHz.

2.2.17 MDIO — MII Management Data Input/Output

This bidirectional signal transfers control/status information between the PHY and MAC. Control information is driven by the MAC synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the MAC.

Section 3 Memory Map/Register Definition

3.1 Overview

This section provides a detailed description of all registers accessible in the EPHY.

3.2 Module Memory Map

Table 3-2 gives an overview of all registers in the EPHY memory map. The EPHY occupies 48 bytes in the memory space. The register address results from the addition of *base address* and *address offset.* The *base address* is determined at the MCU level. The *address offset* is defined at the module level.

Table 3-1 Module Memory Map

Address	Use	Access
$__00	Control Register 1	R/W
$__01	Control Register 2	R/W
$__02	Status Register	R/W
$__03	RESERVED	R

3.2.1 Ethernet Physical Transceiver Control Register 0

Address Offset $__00

	7	6	5	4	3	2	1	0
R W	EPHYEN	ANDIS	DIS100	DIS10	LEDEN	EPHYWAI	0	EPHYIEN
RESET:	0	1	1	1	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 Ethernet Physical Transceiver Control Register 0 (EPHYCTL0)

Read: Anytime

Write: See each bit description.

EPHYEN — EPHY Enable

This bit can be written anytime.

1 = Enables EPHY

0 = Disables EPHY

ANDIS — Auto Negotiation Disable

This bit can be written anytime, but the value is only latched in the ANE bit of the MII PHY Control Register(MII address 0.12) when the EPHYEN bit transitions from 0 to 1.

1 = Auto Negotiation is disabled after start-up. A 0 is latched in the ANE bit of the MII PHY Control Register(MII address 0.12), and upon completion of the start-up delay($D_{start\text{-}up}$), the EPHY will bypass auto-negotiation. The operational mode will be determined by the manual setting of MII registers.

0 = Auto Negotiation is enabled after start-up. A 1 is latched in the ANE bit of the MII PHY Control Register(MII address 0.12), and upon completion of the start-up delay($D_{start\text{-}up}$), the EPHY will enter auto-negotiation. The common operational mode will be automatically determined.

DIS100 — Disable 100 Base-TX PLL

This bit can be written anytime. Allows user to power down the clock generation PLL for 100 Base X clocks.

1 = Disables 100Base-TX PLL

0 = 100Base-TX PLL state determined by EPHY operation mode.

DIS10 — Disable 10BaseT PLL

This bit can be written anytime. Allows user to power down the clock generation PLL for 10 Base T clocks,

1 = Disables 10 Base-T PLL

0 = 10 Base-T PLL state determined by EPHY operation mode.

LEDEN — LED Drive Enable

This bit can be written anytime.

1 = Enables the EPHY to drive the LED signals to the port L.

0 = Disables the EPHY to drive the LED signals to the port L.

EPHYWAI — EPHY Module Stops While in Wait

This bit can be written anytime.

1 = Disables the EPHY module when the MCU is in the wait mode. EPHY interrupts cannot be used to get the MCU out of wait.

0 = Allows the EPHY module to continue running during wait.

EPHYIEN — EPHY Interrupt Enable

This bit can be written anytime.

1 = Enables EPHY Module Interrupts

0 = Disables EPHY Module Interrupts

3.2.2 Ethernet Physical Transceiver Control Register 1

Address Offset $__01

	7	6	5	4	3	2	1	0
R	0	0	0	PHYADD4	PHYADD3	PHYADD2	PHYADD1	PHYADD0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 Ethernet Physical Transceiver Control Register 1 (EPHYCTL1)

Read: Anytime

Write: See each bit description.

PHYADD4 - PHYADD0 — EPHY Address for MII Requests

These bits can be written anytime, but the EPHY Address is only latched to the MII PHY Address REGISTER(MII address 21.4:0) when the EPHYEN bit transitions from 0 to 1. Bit 4 is the MSB of the of the EPHY address.

3.2.3 Ethernet Physical Transceiver Status Register

Address Offset $__02

	7	6	5	4	3	2	1	0
R	0	0	100DIS	10DIS	0	0	0	EPHYIF
W								
RESET:	0	0	1	1	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 Ethernet Physical Transceiver Status Register (EPHYSR)

Read: Anytime

Write: See bit descriptions.

100DIS — EPHY Port Base 100X mode status

This bit is not writable. Read only. Output to indicate PHY port Base 100X mode status.
1 = EPHY Port Base 100X Disabled
0 = EPHY Port Base 100X Enabled

10DIS — EPHY Port Base 100X mode status

This bit is not writable. Output to indicate PHY port Base 10T mode status.

1 = EPHY Port Base 10T Disabled
0 = EPHY Port Base 10T Enabled

EPHYIF — EPHY Interrupt Flag

EPHYIF indicates when interrupt conditions have occurred. To clear this bit, write the bit to one.Write used in clearing mechanism (set bit causes corresponding bit to cleared)

1 = EPHY Interrupt has occurred
0 = EPHY Interrupt has not occurred

3.2.4 Ethernet Physical Transceiver TEST Register

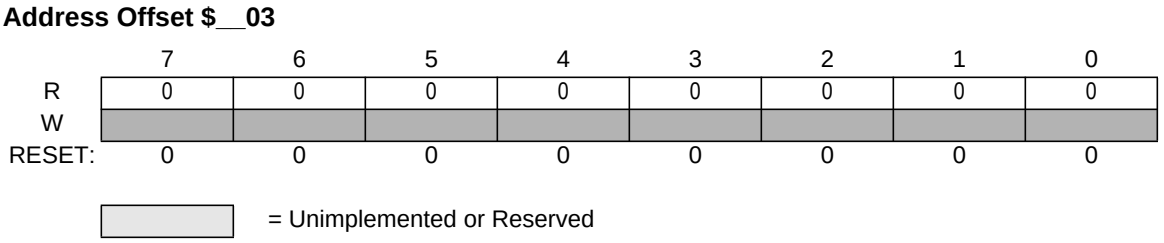


Figure 3-4 Ethernet Physical Transceiver TEST Register (EPHYTST)

Read: Anytime

Write: Only in test modes.

3.3 MII Registers - Memory Map

Table 3-2 gives an overview of all registers in the EPHY which are accessible via the MDIO. These registers are not part of the MCU memory map.

Table 3-2 Module Memory Map

Address		Use	Access
0	%00000	Control Register	Read/Write
1	%00001	Status Register	Read/Write[4]
2	%00010	PHY Identification Register 1	Read/Write[4]
3	%00011	PHY Identification Register 2	Read/Write[4]
4	%00100	Auto-Negotiation Advertisement Register	Read/Write
5	%00101	Auto-Negotiation Link Partner Ability Register	Read/Write[4]
6	%00110	Auto-Negotiation Expansion Register	Read/Write[4]

7	%00111	Auto-Negotiation Next Page Transmit	Read/Write
8	%01000	RESERVED	Read/Write[1]
9	%01001	RESERVED	Read/Write[1]
10	%01010	RESERVED	Read/Write[1]
11	%01011	RESERVED	Read/Write[1]
12	%01100	RESERVED	Read/Write[1]
13	%01101	RESERVED	Read/Write[1]
14	%01110	RESERVED	Read/Write[1]
15	%01111	RESERVED	Read/Write[1]
16	%10000	Interrupt Register	Read/Write
17	%10001	Proprietary Status Register	Read/Write[4]
18	%10010	Proprietary Control Register	Read/Write
19	%10011	10Base-T Bypass Control Register	Read/Write
20	%10100	Test and Trim Control Register	Read/Write[2]
21	%10101	PHY Address	Read/Write
22	%10110	RESERVED	Read/Write[1]
23	%10111	DSP Reset Control	Read/Write
24	%11000	100Base-X DSP Read Register	Read/Write[4]
25	%11001	100Base-X DSP Read Register	Read/Write[4]
26	%11010	100Base-X DSP Read Register	Read/Write[4]
27	%11011	100Base-X DSP Write Register	Read/Write
28	%11100	100Base-X DSP Write Register	Read/Write
29	%11101	100Base-X DSP Write Register	Read/Write

1. Always read $00
2. Only writable in special modes (test_mode = 1)
3. May be written once (test_mode = 0) but writes are always permitted when test_mode = 0
4. Write has no effect.

NOTE: Bit notation for MII registers is as follows: Bit 20.15 refers to MII register address 20 and bit number 15.

3.3.1 PHY Control Register

Register Address 0 (%00000)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RESET	LOOP BACK	DATA RATE	ANE	PDWN	ISOL	RAN	DPLX	COL TEST	0	0	0	0	0	0	0
W																
RESET:	0	0	1	X	0	0	0	1	0	0	0	0	0	0	0	0

Figure 3-5 Control Register

Read: Anytime.

Write: Anytime

Reset — EPHY Reset

Resetting a port is accomplished by setting this bit to a logical one.

1 = The PHY will reset the ports status and registers to the default values. The PHY will also reset the PHY to its initial state.Once the reset is complete the PHY will clear this bit automatically. The reset process will be completed within 1.3ms of this bit being set. When preamble is suppressed, the management interface may not receive an ST within 3 MDC clock cycles following a software reset.

0 = No effect

Loop-back — Digital Loop Back Mode

Enables Digital Loop Back Mode

1 = Enables Digital Loop Back Mode. Port will be placed in loop-back mode. Loop-mode will allow the TXD data to be sent to the RXD data circuitry within 512BT. The PHY will be isolated from the medium (no transmit or receive to the medium allowed) and the COL signal will remain de-asserted, unless this bit is set.

0 = Disables Digital Loop Back Mode

Data Rate — Speed Selection

The link speed will be selected either through the Auto-Negotiation process by manual speed selection. ANE allows manual speed selection when it is set to 0. When Auto-Negotiation is enabled DATA RATE bit can be read or written but its value does not need to reflect speed of the link.

1 = When Auto-Negotiation is disabled, selects 100 Mb/s operation

0 = When Auto-Negotiation is disabled, selects 10 Mb/s operation.

ANE — Auto-Negotiation Enable

When Auto-Negotiation is disabled DATARATE and DPLX determine the link configuration. When Auto-Negotiation is enabled bits DATARATE and DPLX do not effect the link.

1 = Enables Auto-Negotiation.

0 = Disables Auto-Negotiation

PDWN — Power Down

When this bit is set the port will be placed in a low power consumption mode.

1 = Port will be placed in a low power consumption mode.Normal operation will be allowed within 0.5s after bit PDWN and ISOL are changed to zero. During a transition to the power-down mode or when already in power down mode, the port will only respond to management function requests through the MI interface. All other port operations will be disabled. When power-down mode is exited, all register values are maintained. The port will start its operation based on the register values.

0 = Normal operation.

ISOL — Isolate

1 = Isolates the ports data path signals from the MII. The port will not respond to changes on TXD, TXEN, and TXER inputs, and it will present high impedance on TXC, RXC, RXDV, RXER, RXD, COL, and CRS outputs. The port will still respond to management transactions when in isolate mode.

0 = Normal operation

RAN — Restart Auto-Negotiation

1 = When Auto-Negotiation is enabled (ANE), the Auto-Negotiation process will be restarted. Once Auto-Negotiation indicates that it has been initialized this bit will be cleared. When bit ANE is cleared to indicate Auto-Negotiation is disabled, RAN should also be 0.

0 = Normal operation.

DPLX — Duplex mode

This mode can be selected either by the Auto-Negotiation process or by manual duplex selection. Manual duplex selection is only allowed when the Auto-Negotiation process is disabled (ANE=0). When the Auto-Negotiation process is enabled (ANE=1) the state of DPLX has no effect on the link configuration. When Loop-back (LOOPBACK =1) mode is asserted the value of DPLX will have no effect on the PHY.

1 = Indicates full duplex mode

0 = Indicates half duplex mode.

COL TEST — Collision Test

The Collision Test function will be enabled only if the Loop-back (LOOPBACK=1) mode of operation is also selected.

1 = Forces the PHY to assert the COL signal within 512BT from the assertion of TXEN and de-assert COL within 4BT of TXEN being de-asserted.

0 = Normal Operation

3.3.2 Status Register

This register advertises to the MII the capabilities of the port.

Register Address 1 (%00001)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	100-T4	100X-FD	100X-HD	10T FD	1T HD0	0	0	0	0	SUP-PRE	AN-COMP	REM FLT	AN ABL	LNK STST	JAB DT	EX CAP
W																
RESET:	0	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1

= Unimplemented or Reserved

Figure 3-6 Status Register

Read: Anytime.

Write: Writes have no effect.

100-T4 —100BASE-T4

1 = Indicates PHY support 100 BASET4 transmission

0 = Indicates the PHY does not support 100BASE-T4 transmission

100X-FD —100BASE-X Full-Duplex

1 = Indicates PHY supports 100BASE-X full-duplex mode
0 = Indicates PHY does not support 100BASE-X full-duplex mode

100X-HD —100BASE-X Half-Duplex

1 = Indicates the PHY supports 100BASE-X half-duplex mode
0 = Indicates the PHY does not support 100BASE-X half-duplex mode

10T-FD —10BASE-T Full Duplex

1 = Indicates the PHY supports 10BASE-T full-duplex mode
0 = Indicates the PHY does not support 10BASE-T full-duplex mode

1T-HD0 —10BASE-T Half Duplex

1 = Indicates the PHY supports 10BASE-T half-duplex mode
0 = Indicates the PHY does not support 10BASE-T half-duplex mode

SUPPRE —MF Preamble Suppression

1 = Indicates that management frames are not required to contain the preamble stream
0 = Indicates that management frames ARE required to contain the preamble stream

ANCOMP —Auto-Negotiation Complete

1 = Indicates that the Auto-Negotiation process has completed and that the contents of registers 4 through 7 are valid.
0 = Indicates that the Auto-Negotiation process has NOT completed and that the contents of registers 4 through 7 are NOT valid

REMFLT — Remote Fault

Possible Remote Faults (RF)

a. The link partner transmits the RF bit (5.13=1)
b. Link Partner Protocol is not 00001 (5.4:0)
c. Link Partner Advertises Only T4 Capability (5.9:5)
d. No common operation mode found between PHY and the link partner.

Once set, REMFLT is cleared each time register 1 is read via the management interface. REMFLT is also cleared by a PHY reset.

1 = Indicates when a remote fault condition has been detected.
0 = No fault detected

ANABL — Auto-Negotiation Ability

1 = Indicates that PHY has Auto-Negotiation Ability
0 = Indicates that PHY does not have Auto-Negotiation Ability

LINKSTST — Link Status

The PHY will set this bit when it determines that a valid link has been established. The occurrence of a link failure will cause LINKSTST to be cleared. Once cleared it should remain cleared until it is read via the management interface.

1 = Indicates a valid link has been established

0 = Indicates a valid link has NOT been established

JABDT —Jabber-detect

Once set, JABDT is cleared each time register 1 is read via the management interface. JABDT is also cleared by a PHY reset. For 100BASE-X operation this signal will always be cleared.

1 = Indicates that a jabber condition has been detected.

0 = Indicates that NO jabber condition has been detected.

EXCAP —Extended capability

1 = Indicates that the extended register set (registers 2-31) has been implemented in the PHY.

0 = Indicates that the extended register set (registers 2-31) has NOT been implemented in the PHY

3.3.3 EPHY Identifier Register 1

Provides the PHY identification code.

Register Address 2 (%00010)

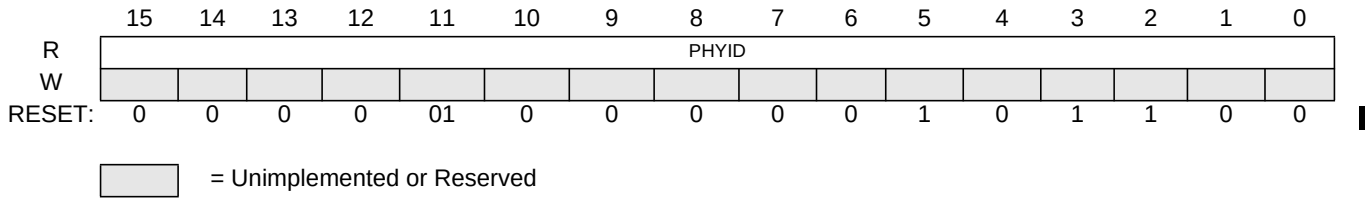


Figure 3-7 EPHY Identifier Register 1

Read: Anytime

Write: Writes have no effect. Read Only. Registers $_02 and $_03 provide the PHY identification code

PHYID — PHY ID Number

Organization unique identifier. 00-60-11 (hex). Composed of bits 3:18 of the OUI

3.3.4 EPHY Identifier Register 2

Register Address 3 (%00011)

Figure 3-8 EPHY Identifier Register 2

Read: Anytime

Write: Writes have no effect. Read Only

PHY ID — PHY ID Number Organization unique identifier. Composed of bits 15:10.

MODEL NUMBER — Manufacturers model number. Composed of bits 9:4.

REVISION NUMBER — Manufacturers revision number. Composed of bits 3:0.

3.3.5 Auto-Negotiate (A/N) Advertisement Register

The Auto-Negotiation (A/N) process requires four registers to communicate link information with its link partner: A/N Advertisement Register (Register 4), A/N Link Partner Ability Register (Register 5), A/N Expansion Register (Register 6), and the A/N Next Page Transmit Register (Register 7).

Register Address 4 (%00100)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NXTP	0	RFLT	0	0	FLCTL	0	TAF 100FD	TAF 100HD	TAF 10FD	TAF 10HD	SELECTOR FIELD [4:0]				
W																
RESET:	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1

= Unimplemented or Reserved

Figure 3-9 Auto Negotiate Advertisement Register (Addr4)

Read: Anytime.

Write: Never.

NXTP — Next Page

bit description
1 = Capable of sending next pages
0 = Not capable of sending next pages

RFLT — Remote Fault

bit description
1 = Remote fault
0 = No remote fault

FLCTL — Flow Control

bit description
1 = Advertise that the DTE (CAC) has implemented the optional MAC control sublayer and Pause function as specified in IEEE standard clause 31 and anex 31B of 802.3. Setting FLCTL has no effect except to set the corresponding bit in the FLP stream
0 = No MAC-based flow control

TAF 100FD — 100Base-TX Full Duplex

bit description
1 = 100Base TX full duplex capable
0 = Not 100Base TX full duplex capable

TAF 100HD — 100Base-TX Half Duplex

bit description
1 = 100Base TX half duplex capable
0 = Not 100Base TX half duplex capable

TAF 10FD — 10Base-T Full Duplex

bit description
1 = 10Base T full duplex capable
0 = Not 10Base T full duplex capable

TAF 10HD — 10Base-T Half Duplex

bit description
1 = 10Base T half duplex capable
0 = Not 10Base T half duplex capable

The ANE bit determines if the A/N process is enabled. A 1 in the ANE bit enables the A/N process, while a 0 disables it. When the A/N process is enabled, the values of the DPLX bit and the DATA RATE bit will have no effect on the link.

The RAN bit determines when the A/N process can start processing. When changed to a logical one this bit starts the A/N function to determine the link capabilities.

To inform the Management Interface (MI) that it has completed processing, ANCOMP is set by the A/N process. Once started the Auto-Negotiation process uses Link Code Words to exchange capability information and establish the Highest Common Denominator (HCD) for link transactions.

Auto-Negotiation (A/N) Advertisement (Addr 4)

Table 11 shows the contents of the A/N Advertisement register. On power-up, before A/N starts, the register has the Selector Field, bits 4.4:0, set to 00001 to indicate that it is an IEEE Std. 802.3 compliant. The Technology Ability Fields (4.9:5) are set according to the values in the MII status register (1.15:11). The MI can set the Technology Ability Field bits before renegotiations to allow management to auto-negotiate to an alternate common mode.

5.10 PHY Specific Registers

PHY also contains a number of registers to set its internal mode of operation. These registers can be set through the external management interface to determine capabilities such as speed, test-mode, circuit bypass mode, interrupt setting, etc. The PHY register set includes registers 16 through 29 and is summarized in Table 6.

3.3.6 Auto Negotiation Link Partner Ability (Base Page)

Register Address 5 (%00101) - BASE PAGE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NXTP	ACK	RFLT	TAF[1:0]		FCTL	TAF 100T4	TAF 100FD	TAF 100HD	TAF 10FD	TAF 10HD	SELECTOR FIELD [4:0]				
W																
RESET:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 3-10 Auto Negotiation Link Partner Ability Register (Base Page)

Read:

Write:

NXTP — Next Page

bit description
1 = Link partner capable of sending next pages
0 = Link partner not capable of sending next pages

ACK — Acknowledge

bit description
1 = Link Partner has received link code word
0 = Link Partner has not received link code word

RFLT — Remote Fault

bit description
1 = Remote fault
0 = No remote fault

FLCTL — Flow Control

bit description
1 = Advertise that the DTE (CAC) has implemented the optional MAC control sublayer and Pause function as specified in IEEE standard clause 31 and anex 31B of 802.3. Setting FLCTL has no effect on the PHY. It only advertises to the attached DTE (MAC) that the MAC connected to the link partner has implemented full-duplex flow control.
0 = No MAC-based flow control

TAF 100T4 — 100Base-T4 Full Duplex

bit description
1 = Link partner is 100Base-T4 capable
0 = Link partner is not 100Base-T4 capable

TAF 100FD — 100Base-TX Full Duplex

bit description
1 = Link partner is 100Base TX full duplex capable
0 = Link partner is not 100Base TX full duplex capable

TAF 100HD — 100Base-TX Half Duplex

bit description
1 = Link partner is 100Base TX half duplex capable
0 = Link partner is not 100Base TX half duplex capable

TAF 10FD — 10Base-T Full Duplex

bit description
1 = Link partner is10Base T full duplex capable
0 = Link partner is not 10Base T full duplex capable

TAF 10HD — 10Base-T Half Duplex

bit description
1 = Link partner is 10Base T half duplex capable
0 = Link partner is not 10Base T half duplex capable

3.3.7 Auto Negotiation Link Partner Ability (Next Page)

Register Address 5 (%00101) - NEXT PAGE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NXTP	ACK	MSGP	ACK2	TGL	Message/Unformatted Code Field [10:0]										
W																
RESET:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Figure 3-11 Auto Negotiation Link Partner Ability Register (Next Page)

Read: Anytime.

Write: See each field description.5.7 A/N Link Partner Ability (Addr5)

NXTP — Next Page

bit description
1 = Additional next pages will follow
0 = Last page transmitted

ACK — Acknowledge

bit description
1 = Link Partner has received link code word
0 = Link Partner has not received link code word

MSGP — Message Page

bit description
1 = Message page
0 = Unformatted page

TGL — Toggle

bid description

1 = Previous value of the transmitted link code word equalled 0

0 = Previous value of the transmitted link code word equalled 1

Message/Unformatted Code Field

Message code field — Predefined code fields defined in IEEE 802.3u-1995 Annex 28C.

Unformatted code filed — Eleven bit field containing an arbitrary value

Table 12 shows the contents of the A/N Link Partner Ability register. The register can only be read by the MI and will be written by the Auto-Negotiation process when it receives a Link Code Word advertising the capabilities of the link partner. This register has a dual purpose, exchange of Base Page information as shown in Table 12, and exchange of Next Page information as shown in Table 13.

3.3.8 Auto-Negotiation Expansion Register

Register Address 6 (%00110)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	PDFLT	LPNPA	NXTPA	PRCVD	LPANA
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

= Unimplemented or Reserved

Figure 3-12 Auto-Negotiation Expansion Register

Read: Anytime

Write: Never

PDFLT — Parallel Detection Fault

bit description

1 = Parallel detection fault has occurred

0 = Parallel detection fault has not occurred

LPNPA — Link Partner Next Page Able

bit description

1 = Link partner is next page able

0 = Link partner is not next page able

NXTPA — Next Page Able

bit description

1 =

0 =

PRCVD — Page Received

bit description

1 = Three identical and consecutive link code words have been received from link partner
0 = Three identical and consecutive link code words have not been received from link partner

LPANA — Link Partner A/N Able

bit description
1 = Link partner is A/N able
0 = Link partner is not A/N able

Read: Anytime.

Write: Never.

Table 14 shows the contents of the A/N Expansion register. The MI process can only read this register. This register contains information about the A/N capabilities of the ports link partner and information on the status of the parallel detection mechanism. Parallel Detection Fault (bit 6.4): This bit is set to one to indicate that zero or more than one of the NLP Receive Link Integrity Test Function for 100BASE-TX have indicated that the link is ready (link_status=READY) when the A/N wait timer has expired. Bit (6.4) will be reset to zero after a read of register 6. Link Partner Next Page Able (bit 6.3): Bit to indicate if the link partner has the capability of using NP. Next Page Able (bit 6.2): This bit is set to a logical one to inform the MI and the Link Partner that the port has Next Page capabilities. Page Received (bit 6.1): Bit is set to a logical one to indicate that a new Link Code Word has been received and stored in the A/N link partner ability register (register 5). This bit is reset to a logical zero once register 6 is read.Link Partner A/N Able (bit 6.0): Indicates if the link partner has A/N capabilities.

3.3.9 Auto Negotiation Next Page Transmit

Register Address 7 (%00111)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	NXTP	0	MSGP	ACK2	TGL	Message/Unformatted Code Field [10:0]										
W																
RESET:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 3-13 Auto Negotiation Next Page Transmit Register

Read: Anytime

Write: Never

5.9 A/N Next Page Transmit Register (Addr 7) Table 15 shows the contents of the A/N Next Page Transmit register. The MI writes to this register if it needs to exchange more information with the link partner. The PHY defaults to sending only a NULL Message Page to the link partner unless the STA overrides the values in the register. Next Pages will be transmitted until the link partner has no more pages to transmit and bit 7.15 has been set to zero by the STA.

NXTP — Next Page

bit description
1 = Additional next pages will follow
0 = Last page to transmit

MSGP — Message Page

bit description
1 = Message page
0 = Unformatted page

ACK2 — Acknowledge 2

bit description
1 = Will comply with message
0 = Cannot comply with message

TGL — Toggle

bit description
1 = Previous value of the transmitted link code word equalled 0
0 = Previous value of the transmitted link code word equalled 1

Message/Unformatted Code Field

Message code field — Predefined code fields defined in IEEE 802.3u-1995 Annex 28C.
Unformatted code filed — Eleven bit field containing an arbitrary value

3.3.10 Interrupt Control Register

Register Address 16 (%10000)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	ACKIE	PRIE	LCIE	ANIE	PDFIE	RFIE	JABIE	0	ACKR	PGR	LNK CNG	AN CNG	PDF	RMTF	JABI
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-14 Interrupt Control Register

Read: Anytime.

Write: Anytime

ACKIE — Acknowledge Bit Received Interrupt Enable

bit description
1 = Enable interrupt when the acknowledge bit is received from the link partner
0 = Disable interrupt when acknowledge bit is received

PRIE — Page Received INT Enable

bit description
1 = Enable interrupt when a new page is received
0 = Disable interrupt when a page is received

LCIE — Link Changed Enable

bit description
1 = Enable interrupt when the link status changes
0 = Disable interrupt when the link status changes

ANIE — Auto-Negotiation Changed Enable

bit description
1 = Enable interrupt when the state of the auto-negotiation state machine has changed since the last access of this register
0 = Disable interrupt when the state of the auto-negotiation state machine has changed since the last access of this register

PDFIE — Parallel Detect Fault Enable

bit description
1 = Enable interrupt on a parallel detect fault
0 = Disable interrupt on a parallel detect fault

RFIE — Remote Fault Interrupt Enable

bit description
1 = Enable interrupt on a parallel detect fault
0 = Disable interrupt on a parallel detect fault

JABIE — Jabber Interrupt Enable

bit description
1 = Enable setting interrupt on detection of a jabber condition
0 = Disable setting interrupt on detection of a jabber condition

ACKR — Acknowledge Bit Received

bit description
1 = Acknowledge bit has been received from the link partner
0 = Acknowledge bit has not been received since the last access of this register. (ACK bit 14 of the Auto-Negotiation Link Partner Ability Register was set by receipt of link code word)

PGR — Page Received

bit description
1 = A new page has been received from the link partner
0 = A new page has not been received from the link partner since the last access of this register (Bit 1 was set by a page received event)

LNK CHG — Link Changed

bit description
1 = The link status has changed since the last access of this register

0 = The link status has not changed since the last access of this register. (LNK bit 14 of the Proprietary Status Register was changed)

AN CHG — Auto-Negotiation Changed

bit description

1 = The auto-negotiation status has changed since the last access of this register

0 = The auto-negotiation status has not changed since the last access of this register

PDF — Parallel Detect Fault

bit description

1 = A parallel-detect fault has occurred since the last access of this register

0 = A parallel-detect fault has not been detected since the last access of this register. (Bit 4 was set by rising edge of parallel detection fault)

RMTF — Remote Fault

bit description

1 = A remote fault condition has been detected since the last access of this register

0 = A remote fault condition has not been detected since the last access of this register. (RMTF bit 4 of the Status Register was set by rising edge of a remote fault)

JABI — Jabber Interrupt

bit description

1 = A jabber condition has been detected since the last access of this register

0 = A jabber condition has not been detected since the last access of this register (JABD bit 1 of the Status Register was set by rising edge of jabber condition)

3.3.11 Proprietary Status Register

The MAC Unicast Address (MACAD) registers contains the 48-bit address used for exact match in the address recognition process by comparing it with the destination address field of unicast receive frames.

Register Address 17 (%10001)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	LNK	DPMD	SPD	0	ANNC	PRCVD	ANC MODE	0	0	PLR	0	0	0	0	0
W																
RESET:	0	1	1	1	0	0	0	(1)	0	0	0	0	0	0	0	0

Figure 3-15 Proprietary Status Register

Read: Anytime.

Write:

LNK — Link (duplicate of LNK bit 2 of the Status Register)

bit description
1 = Link is down
0 = Link is up

DPMD — Duplex Mode

bit description
1 = Full-Duplex
0 = Half-Duplex

SPD — Speed

bit description
1 = 100 Mbps
0 = 10 Mbps

ANNC — Auto-Negotiation Complete

bit description
1 = A-N complete
0 = A-N not complete

PRCVD — Page Received (Duplicate of ANC bit 5 of the Status Register)

bit description
1 = Three identical and consecutive link code words have been received
0 = Three identical and consecutive link code words have not been received

ANC MODE — Auto-Negotiation (A-N) Common Operating Mode

This bit is only valid when the ANNC bit 10 is 1
1 = A common operation mode was not found
0 = A-N is complete and a common operation mode has been found

PLR — Polarity Reversed (10Base-T)

bit description
1 = 10Base-T receive polarity is reversed
0 = 10Base-T receive polarity is normal

3.3.12 Proprietary Control Register

Register Address 18 (%10010)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	FE FLTD	MIILBD	0	1	JBDE	LNK TSTD	POL-CORD	ALGD	ENC BYP	SCR BYP	TRD ANALB	TR TST	0	0	0
W																
RESET:	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 Proprietary Control Register

The Miscellaneous (MISC) register provides visibility of internal counters used by the EMAC.

Read: Anytime.

Write: Anytime.

FE FLTD — Far End Fault Disable

bit description
1 = Far end fault detect is disabled
0 = Far end fault detect on receive and transmit is enabled. This applies only when auto-negotiation is disabled

MIILBO — MII Loop-Back Disable

bit description
1 = Disable MII loop-back
0 = MII transmit data is looped back to the MII receive pins

JBDE — Jabber Detect Enable (10Base-T)

bit description
1 = Enable Jabber Detection
0 = Disable Jabber Detection

LNK TSTD — Link Test Disable (10Base-T)

bit description
1 = Disable 10Base-T link integrity test
0 = 10Base-T link integrity test enabled

POL-CORD — Disable Polarity Correction (10Base-T)

bit description
1 = 10Base-T receive polarity correction is disabled
0 = 10Base-T receive polarity is automatically corrected

ALGD — Disable Alignment

bit description
1 = Un-aligned mode. Only available in symbol mode
0 = Aligned mode

ENC BYP — Encoder Bypass

bit description
1 = Symbol mode and bypass 4B/5B encoder and decoder
0 = Normal mode

SCR BYP — Scrambler Bypass Mode (100Base-TX)

bit description
1 = Bypass the scrambler and de-scrambler
0 = Normal

TRD ANALB — Transmit and Receive Disconnect and Analog Loopback

bit description
1 = Hi-Z twisted pair transmitter. Analog loop-back mode overrides and forces this bit
0 = Normal operation

TR TST — Transmit and Receive Test (100Base-TX)

bit description
1 = Transmit and receive data regardless of link status
0 = Normal operation

3.3.13 10Base-T Bypass Control Register

Register Address 19 (%10011)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BYP TFLT	RLPF BYP	10BTSQLVL[1:0]		10BT SQINH	SQE 10BT	10BTCLKRECBW[2:0]			0	0	0	0	0	0	0
W																
RESET:	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-17 10Base-T Bypass Control Register

The Miscellaneous (MISC) register provides visibility of internal counters used by the EMAC.

Read: Anytime.

Write: Anytime.

BYPTFLT — Bypass Transmit Filter (10Base-T)

bit description
1 = Bypass 10Base-T transmit digital filter
0 = use 10Base-T transmit digital filter

RLPF — Bypass Receive Low Pass Filter (10Base-T)

bit description
1 = Bypass 10Base-T receive low pass filter
0 = Use 10Base-T receive low pass filter

10BT SQLVL — 10Base-T Squelch level

bit description
00 = Use lowest squelch levels
01 = Use lower squelch levels
10 = Use Default squelch levels
11 = Use highest squelch levels

10BT SQINH — Squelch Inhibit (10Base-T)

bit description
1 = 10Base-T receive squelch function is disabled
0 = 10Base-T receive squelch function is enabled

SQE — SQE (10Base-T)

bit description
1 = Enable SQE
0 = Disable SQE

10BTCLKRECBW — 10BT Clock Recovery Bandwidth

Three-bit field used for timing recovery. This is the digital amount used in the clock recovery. A higher number means lower bandwidth.

3.3.14 100Base-TX Bypass Control Register

Register Address 20 (%10100)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	TRIM EN	PHASEADJ[2:0]			TAMPCTL[1:0]		TSLPCTL[1:0]		Test Mode[2:0]			SCRSEED[4:0]				
RESET:	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-18 100Base-TX Bypass Control Register

The Miscellaneous (MISC) register provides visibility of internal counters used by the EMAC.

Read: Anytime.

Write: Anytime.

TRIM EN — Trim Enable

bit description
1 = Output values of 20.11:8 to macro
0 = Diable writes to 20.11:8 and use value at pins

PHASEADJ[2:0] — Phase Adjustment Timing

Three-bit field used for timing recovery.

TAMPCTL[1:0] — 100Base-T Transmitter Amplitude Control

Two-bit field used for transmitter amplitude adjustment. Default is setting for TX_AMP_TRIM<1:0> pins, loaded on completion of reset. If TRIM EN bit 15 is set, value is updated upon completion of register write, and takes precedence over the TX_AMP_TRIM<1:0> pins. TAMPCTL[1:0] bits are read/writetable when bit 20.15 is set. If 20.15 is not set, the value of the TAMPCTL[1:0] bits are read-only.

SCRSEED — 100BT Scrambler Seed

Five-bit field used to initialize the scrambler seed, Default is 1111111 followed by the value of PHY<4:0>(bits 21.4:0). Following a register write, the scramble seed is set to the new value. Upon completion of reset, seed returns to the default.

3.3.15 PHY Address Register

Register Address 21 (%10101)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	PHY ADDR				
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X

= Unimplemented or Reserved

Figure 3-19 PHY Address Register

Read: Anytime.

Write: Anytime.

PHY ADDR — PHY Address

Five-bit field used to change the PHY address. Default is value written to the PHYADD[4:0] bits in the EPHYCTL0 register which is loaded upon at EPHY start-up or upon completion of a EPHY reset. Following register write, PHY address is set to the new register value.

3.3.16 DSP Reset Control

Register Address 23 (%10111)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ERR_THRESH					ERR_TIMER										MSE
W																RST
RESET:	0	1	0	1	0	1	1	1	0	0	0	1	1	1	0	0

= Unimplemented or Reserved

Figure 3-20 DSP Reset Control

Read: Anytime.

Write: Anytime.

ERR_THRESH

Five-bit field used to determine whether and at what periodic interval resets occur.

00000 = Do not reset
00001 = Reset on every error
11111 = Reset every 31 errors

ERR_TIMER

Ten-bit field
h000 = Do not reset
h001 =
h3FF =

MSE RST — MSE Reset Inhibit

bit description
1 = Do not reset DSP due to mse_good value
0 = Periodically reset DSP if mse_good (MSE_GOOD bit 15 of the 100Base-X DSP Read Register)

3.3.17 100Base-TX DSP Read Register (1)

Register Address 24 (%11000)

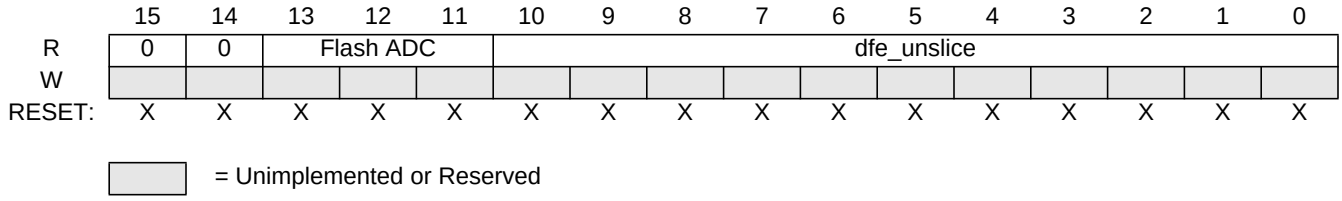


Figure 3-21 100Base-TX DSP Read Register (1)

This register is meaningful in 100Base-X operating mode only

Read: Anytime.

Write: Never.

Flash ADC

Output of the Flash ADC

dfe_unslice

Output of digital equalizer before slicer

3.3.18 100Base-TX DSP Read Register (2)

Register Address 25 (%11001)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MSE GD	WANDER							MSE							
W																
RESET:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

= Unimplemented or Reserved

Figure 3-22 100Base-TX DSP Read Register (2)

This register is meaningful in 100Base-X operating mode only

Read: Anytime.

Write: Never.

MSE GD — mse_good

bit description

1 = Mse meter indicates mse is below mse_good_thresh (mse_good_thresh bits 15:8 of the 100Base-X DSP Write Register)

0 = Mse meter indicates mse is above mse_good_thresh (mse_good_thresh bits 15:8 of the 100Base-X DSP Write Register)

3.3.19 100Base-TX DSP Read Register (3)

Register Address 26 (%11010)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SLDT	aeq					coef									
W																
RESET:	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

= Unimplemented or Reserved

Figure 3-23 100Base-TX DSP Read Register (3)

This register is meaningful in 100Base-X operating mode only

Read: Anytime.

Write: Never.

SLDT — Signal Detect

bit description

1 = Input signal present

0 = Input signal is below the signal threshold

aeq

Output of analog equalizer control block

coef

Coefficient value of digital equalizer — tap selected by coef_sel (COEFS bits 4:0 of the 100Base-X DSP Write Register

3.3.20 100Base-TX DSP Write Register (1)

Register Address 27 (%11011)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	AEQF	AEQFV					AEQO			AEQT					TIM MODE	RST DSP
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-24 100Base-TX DSP Write Register (1)

This register is meaningful in 100Base-X operating mode only

AEQF — aeq_force

bit description
1 = Force aeq_force_val (AEQFV bits 14:10) on output of analog equalizer control
0 = Normal output of analog equalizer control block

AEQFV — aeq_force_value

value to force onto output of analog equalizer control when aeq_force (awq_focre bit 15) is high

AEQO — aeq_offset

Analog equalizer control deadzone after convergence (.000xxx)

AEQT — aeq_threshold

Average magnitude threshold for analog equalizer control (.0xxxxx)

TIM MODE — Timing Mode

bit description
1 = Use Half T
0 = Use Mueller-Mueller

RST DSP — reset_dsp

bit description
1 = Hold entire DSP in reset

0 = Normal operation

3.3.21 100Base-TX DSP Write Register (2)

Register Address 28 (%11100)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	SDDS	WDDS	FFFZ	FFCI			FBFZ	FFMU		FBMU		COEFS				
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-25 100Base-TX DSP Write Register (2)

This register is meaningful in 100Base-X operating mode only

Read: Anytime.

Write: Anytime.

SDDS — sigdet_disable

bit description
1 = Disable signal detect
0 = Enable signal detect

WDDS — wander_disable

bit description
1 = Disable baseline wander control (hold in reset)
0 = Normal baseline wander operation

FFFZ — ff_freeze

bit description
1 = Freeze coefficients of digital equalizer forward filter
0 = Normal operation of digital equalizer forward filter

FFCI — ff_cursor_init

Value to initialize in cursor tap of forward filter when DSP is reset (0xx.x)

FBFZ — fb_freeze

bit description
1 = Freeze coefficients of digital equalizer feedback filter
0 = Normal operation of digital equalizer feedback filter

FFMU — ff_mu

Feedforward filter step size (00–11 : 2^{-14} –2^{-17})

FBMU — fb_mu

Feedforward filter step size (00–11 : 2^{-14} –2^{-17})

COEFS — coef_sel

Select which coefficient to output to coef (COEF bits 9:0 of 100Base-X DSP Read Register). 1..5 selects coefficients 0..4 of forward filter, 16..27 selects coefficients 0..11 of feedback filter.

3.3.22 100Base-TX DSP Write Register (3)

Register Address 29 (%11101)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	MSEGDT								WNDS		TIM1PFS			FTIMU	TMDS	TMUS
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-26 100Base-TX DSP Write Register (3)

This register is meaningful in 100Base-X operating mode only.

Read: Anytime.

Write: Anytime.

MSEGDT — mse_good_thresh

Threshold below which mse_good bit is asserted (0.xxxxxxxx)

WNES — wander_shift

Baseline wander loop gain (00–11 : 2^{-3} – 2^{-6})

TIM1PFS — timing_1pf_shift

Timing recovery loop bandwidth (Mode set by TIM MOD bit 1 in Addr 27 Register)
Half T: 000, 001, 010, 011: 50, 100, 200, 400 kHz
M-M: 010, 011, 100, 101: 50, 100, 200, 400 kHz

FTIMU — force_timing_up

bit description
1 = When bit changes from 0 to 1, a single pulse is output on timing recovery up signal
0 = Normal timing recovery operation

TMDS — timing_disable

bit description
1 = Timing recovery block is disabled
0 = Normal timing recovery operation

TMUS — timing_unq_sel

bit description

1 = Select unslice data input to timing recovery after digital equalizer

0 = Select unslice data input to timing recovery before digital equalizer

Section 4 Functional Description

The EPHY is an IEEE 802.3u compliant 10/100 Ethernet PHY Transceiver. The EPHY can be configured to support 10Base-T or 100Base-TX applications. The EPHY is configurable via internal registers which are accessible through the MII MDIO interface.

There are five basic modes of operation for the EPHY:

- Power-down / Initialization
- Auto-Negotiate
- 10Base-T
- 100Base-TX
- Low Power

4.1 Power Down / Initialization

Upon reset the EPHYEN bit, in the Ethernet Physical Transceiver Control Register 0 (EPHYCTL0), is cleared and EPHY is in its lowest power consumption state. All analog circuits are powered down. The twisted-pair transmitter and receiver pins (TXP, TXN, RXP, RXN) are tri-stated. The MII management interface is not accessible. All MII registers are initialized to their reset state. The ANDIS, DIS100, and DIS10 bits, in the EPHYCTL0 register, have no effect until the EPHYEN bit is set.

The EPHYEN bit can be set or cleared by a register write at any time. Prior to enabling the EPHY, setting EPHYEN to 1, the MII PHY address PHYADD[4:0] must be set in the Ethernet Physical Transceiver Control Register 1 (EPHYCTL1) , and the ANDIS, DIS100, DIS10 bits, in the EPHYCTL0 register, need to be configured for the desired start-up operation. Whenever the EPHYEN bit transitions from 0 to 1, MDIO communications must be delayed until the completion of a start-up delay period($D_{start\text{-}up}$, see **Figure 4-2**).

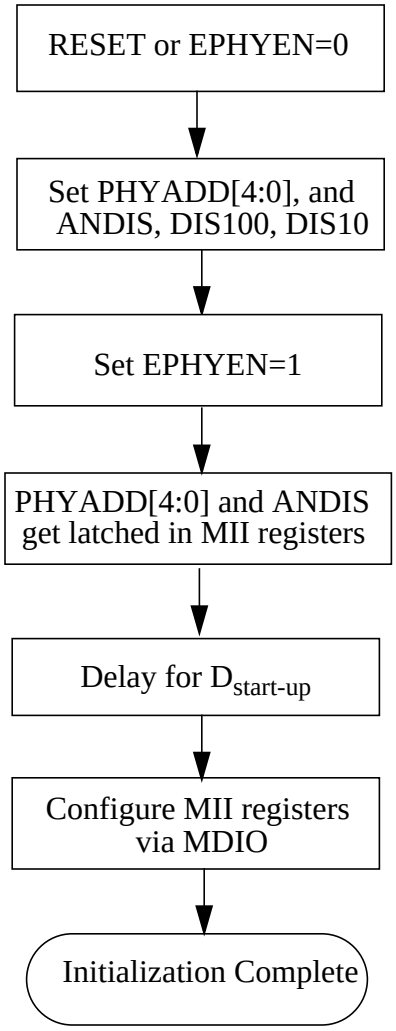


Figure 4-1 EPHY Start-up / Initialization Sequence

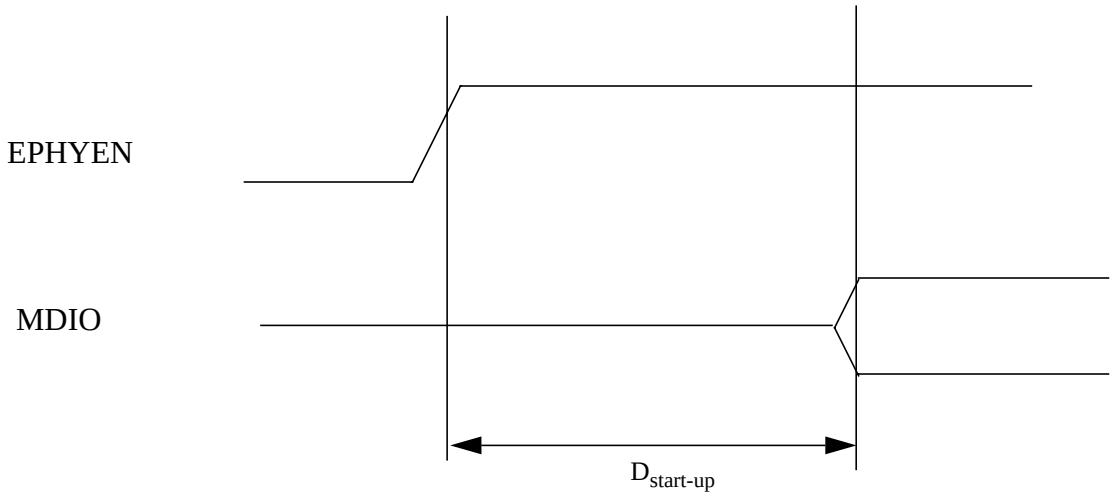


Figure 4-2 EPHY Start-up Delay

If the Auto-negotiation mode of operation is desired then the ANDIS bit in the EPHYCTL0 needs to be set to 0 and the DIS100, and DIS10 bits need to be cleared prior to setting EPHYEN to 1. Please refer to section **4.2 Auto-Negotiation**, for more information on auto-negotiation operation.

When the mode of operation will be set manually the ANDIS bit needs to be set to 1 in the EPHYCTL0 register and the DIS100, and DIS10 bits need to be cleared prior to setting EPHYEN to 1. Once the EPHYEN bit has been set and the start-up delay period is completed the mode of operation may be configured through MII registers. **Table 4-1** summarizes the MII register configuration and operational modes.

Table 4-1 Operational Configuration when Auto-Negotiation is disabled.

Bit 0.12 Auto Neg.	Bit 0.13 Data Rate	Bit 0.8 Duplex	Bit 18.6 Encoder Bypass	Bit 18.5 Scrambler Bypass	Bit 18.7 Symbol Unalign	Operation
0	0	1	X	X	X	10Base-T full-duplex
0	0	0	X	X	X	10Base-T half duplex
0	1	1	0	0	0	100Base-TX full-duplex
0	1	1	1	0	0	100Base-TX full-duplex with encoder bypass (Symbol mode) - aligned
0	1	1	1	0	1	100Base-TX full-duplex with encoder bypass (Symbol mode) - unaligned
0	1	1	1	1	0	100Base-TX full-duplex with scrambler and encoder bypassed (Symbol mode), aligned
0	1	1	1	1	1	100Base-TX full-duplex with scrambler and encoder bypassed (Symbol mode), unaligned
0	1	0	0	0	0	100Base-TX half duplex

4.2 Auto-Negotiation

Auto-Negotiation is used to determine the capabilities of the link partner. Auto-Negotiation is compliant with IEEE 802.3 clause 28. In this case the PHY will transmit Fast Link Pulse (FLP) bursts to share its capabilities with the link partner.

If the link partner is also capable of performing auto-negotiation, it will also send FLP bursts. The information shared through the FLP bursts will allow both link partners to find the highest common mode (if it exists).

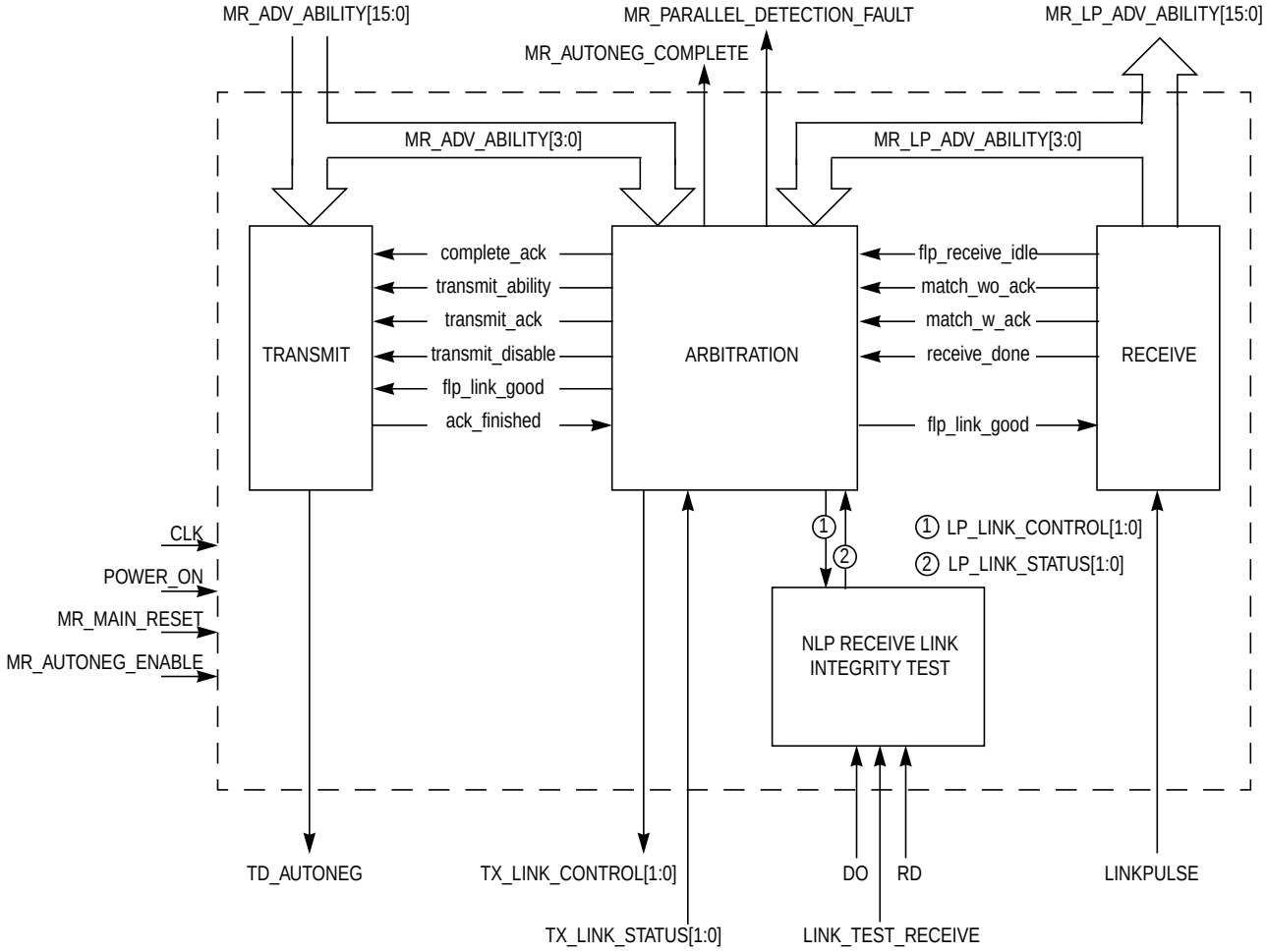
If no common mode is found the Remote Fault bit (1.4) will be set. A Remote Fault is defined as a condition in which the PHY and the link partner cannot establish a common operating mode. Programming register 4 () can set the different negotiation modes.

If the link partner does not support auto-negotiation it will transmit either Normal Link Pulses (NLP), for 10 Mb/s operation, or 100 Mb/s Idle symbols. Based on the received signal the PHY is then capable of determining if the link partner is 10 Mb/s capable or 100 Mb/s capable. This ability is called Parallel Detection. When using Parallel Detection the link will be configured as a half-duplex link. Once parallel detection has established the link configuration, the Remote Fault bit will be set if the operating mode does not match the pre-set operating modes.

When reading code words from the link partner, all 16 bits will be read before any register updates are made.

Figure 4-3 Auto-Negotiation shows the main blocks used in the Auto-Negotiation function. The Transmit block allows transmission of Fast Link Pulses to establish communications with partners that are auto-negotiation able. The Receive block determines the capabilities of the link partner and writes to the Link Partner Ability Register (Register 5). And, the arbitration block determines the highest common mode of operation to establish the link.

Figure 4-3 Auto-Negotiation



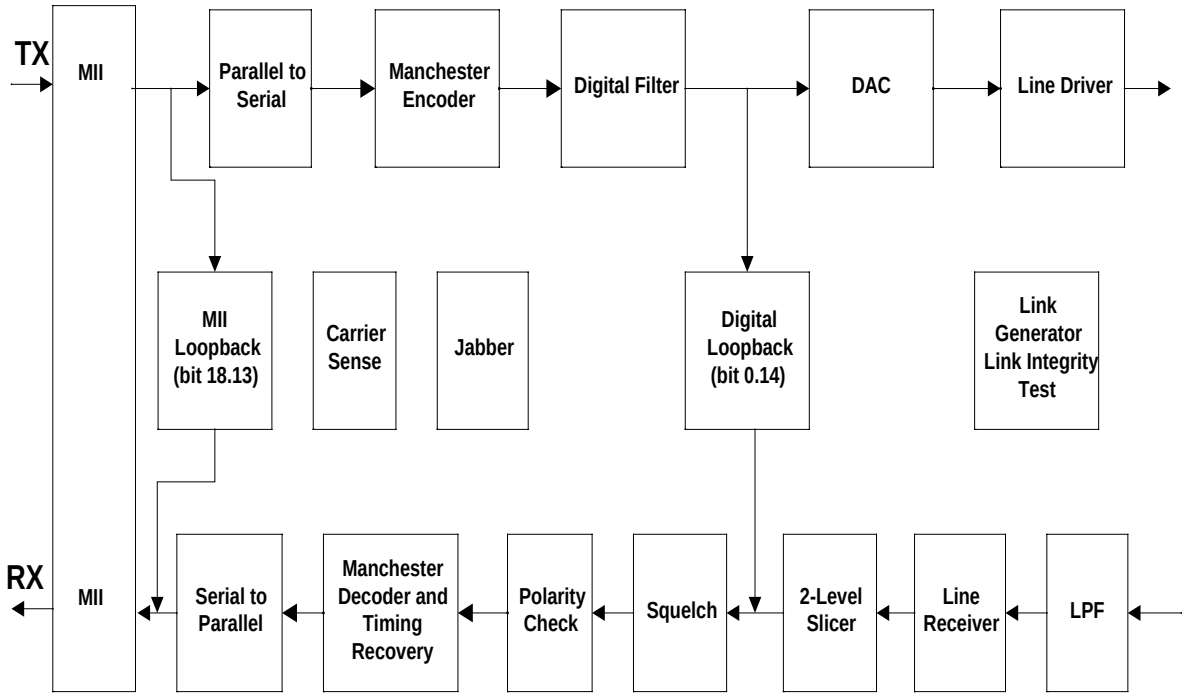
4.3 10Base-T

The 10Base-T interface implements the Physical Layer specification for a 10 Mb/s CSMA/CD LAN over two pairs of twisted-pair telephone wires. The specifications are given in clause 14 of the IEEE 802.3u standard.

When a port is operating in 10Base-T mode, Manchester encoding is used. When transmitting, nibbles from the MII are converted to a serial bit stream and then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted to nibbles for presentation to the MII.

A 2.5 MHz internal clock is used for nibble wide transactions. A 10 MHz internal clock is used for serial transactions.

Figure 4-4 10Base-TX Block Diagram



Parallel to Serial: This block takes the 4-bit wide nibbles from the MII and converts them to serial format before it is processed by subsequent blocks.

Manchester Encoder: The Manchester Encoder allows encoding of both the clock and data in one bit stream. A logical one is encoded as a zero when the clock is high and a one when the clock is low. A logical zero is encoded as a one when the clock is high and a zero when the clock is low.

Digital Filter: The Digital Filter performs pre-emphasis and low pass filtering of the input Manchester data.

DAC: Converts the digital data to an analog format before transmission on the media.

Carrier Sense: In half-duplex operation, carrier is asserted when either the transmit or receive medium is active. In full duplex carrier asserted only on reception of data. During receive, carrier sense is asserted during reception of a valid preamble, and de-asserted after reception of an EOF.

Loop-back: If asserted by bit 18.13 (MII Loop-back), then data received on the MII input lines is looped back to the MII output lines.

A second loop-back mode (Digital Loop-back) is enabled when bit 0.14 is asserted. This loop-back mode allows for the Manchester encoded and filtered data to be looped back to the Squelch block in the Receive path. All the 10Base-T digital functions are exercised during this mode. The Transmit and Receive channels are disconnected from the media.

MII Loop-back (18.13) should be disabled to allow for correct operation of the Digital Loop-back (0.14).

Link Generator: This block generates a 100ns duration pulse at the end of every 12ms period of the transmission path being idle (TXEN de-asserted). This pulse is used to keep the 10Base-T link alive in the absence of data transmission.

Link Integrity Test: This function is used to determine if the 10Base-T link is operational. If neither data nor a link pulse is received for 64ms, then the link is considered down. When the link goes down the transmit, loop back, collision detect, and SQE functions are disabled. The link down state is exited after receiving data or 4 link pulses.

Jabber: The Jabber function prevents the transmitter from erroneously transmitting for too long a period. The maximum time the device may transmit is 50,000 bit times.

When the jabber timer is exceeded the Transmit output goes idle for 0.525s.

This function can be disabled with the Jabber Inhibit register bit (18.10).

Squelch: This function is used to determine whether active data, a link pulse, or an idle condition exists on the 10Base-T receive channel.

When an idle or link pulse condition exists a higher squelch level is used for greater noise immunity. The squelch output is used to determine when the Manchester decoder should operate. The output is also used to determine when an end of packet is received.

Polarity Check: By examining the polarity of the received link pulses SHAWNEE can determine if the received signal is inverted. If the pulses are inverted then this function will change the polarity of the signal.

This feature is activated if eight inverted link pulses are received or four frames with inverted EOF are encountered.

Manchester Decoder and Timing Recovery: This block decodes the Manchester encoded data. The receive data and clock are recovered during this process.

Serial to Parallel: Converts the serial bit stream from the Manchester decoder to the required MII parallel format.

PMD Sublayer: Each port transmits and receives signals compliant with IEEE 802.3 Section 14.

Line Transmitter and Line Receiver: These analog blocks allow SHAWNEE to drive and receive data from the 10Base-T media.

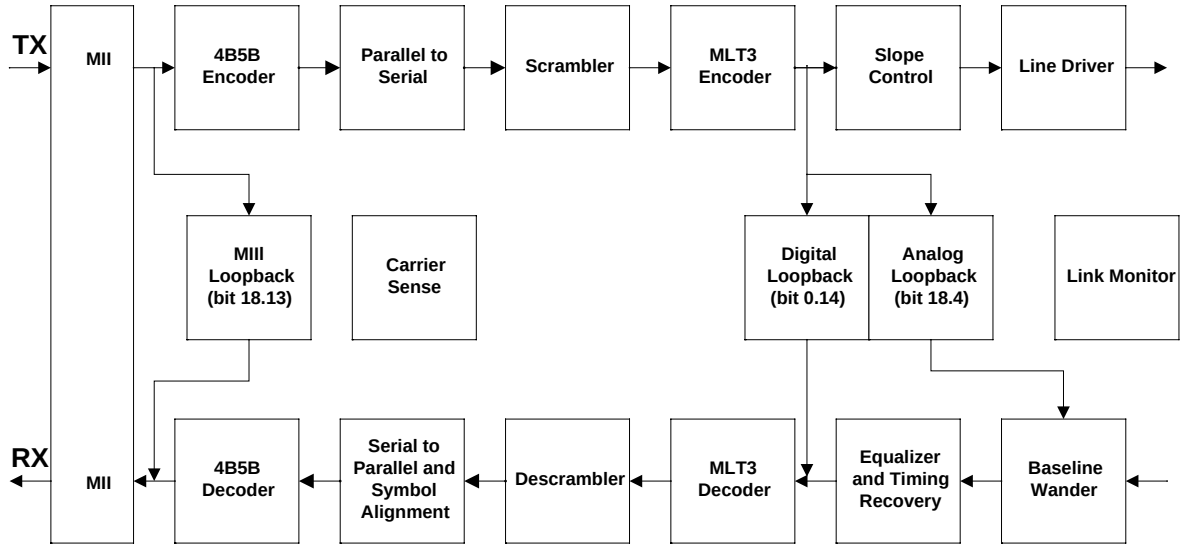
4.4 100BASE-TX

100BASE-TX specifies operation over two copper media: two pairs of shielded twisted-pair cable (STP) or two pairs of unshielded twisted-pair cables (Category 5 UTP).

The EPHY implementation includes the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) sublayer.

The block diagram for 100Base-TX operation is shown in.

Figure 4-5 100Base-TX Block Diagram



4.4.1 PCS Sublayer

The PCS sublayer is the MII interface that provides a uniform interface to the Reconciliation sublayer.

The services provided by the PCS include:

- Encoding/decoding of MII data nibbles to/from five-bit code-groups (4B/5B);
- Carrier Sense and Collision indications;
- Serialization/Deserialization of code-groups for transmission/reception on the PMA;
- Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA.

100BASE-X PCS Sublayer

Serial to Parallel and Symbol Alignment: This block looks for the occurrence of the “JK” symbol to align the serial bit stream and convert it to a parallel format.

For test, this alignment can be bypassed by Bit 18.7.

Carrier Sense: In full duplex mode, carrier sense is only asserted when the Receive channel is active**.** The carrier sense examines the received data bit stream looking for the SSD, the “JK” symbol pair. In the idle state, IDLE symbols (all logic ones) will be received. If the first 5-bit symbols received after an idle stream forms the “J” symbol (11000) it asserts the CRS signal. At this point the second symbol is checked to confirm the “K” symbol (10001). If successful, the following aligned data (symbols) are presented to the 4B/5B decoder. If the “JK” pair is not confirmed, the false carrier detect is asserted and the idle state is re-entered.

Carrier Sense is de-asserted when the ESD (end-of-stream) delimiter, the “TR” symbol pair, is found, or when an idle state is detected.

In half duplex, CRS is also asserted on transmit.

Parallel to Serial: This block takes parallel data and converts it to serial format.

4B/5B Encoder/Decoder: The 4B/5B Encoder converts the 4-bit nibbles from the Reconciliation sublayer to a 5-bit code group as specified in and **Table 4-3 4B/5B Control and Invalid Code Groups**.

The 4B/5B Decoder receives a 5-bit code group and converts it to a 4-bit nibble before it is sent to the MII.

When transmitting, the 4-bit MII nibbles are converted to the 5-bit code words shown in and **Table 4-3 4B/5B Control and Invalid Code Groups**. The first 14 nibbles transmitted are the preamble nibbles. The first two nibbles are replaced by the start-of-stream delimiter (SSD) “JK” symbols. Following the last nibble, the end-of-stream delimiter (ESD) “TR” symbols are added.

When receiving, the 5-bit code words are converted to 4-bit nibbles. If at least one invalid code word is detected, the status register is updated to indicate the error condition. The first two code words received are the SSD “JK” symbols. These two are replaced by the preamble nibbles. The ESD “TR” symbols are stripped from the data stream before they are sent to the MII.

Table 4-2 4B/5B Data Code Groups

MII Value 3210	PCS Code-group 43210	Description		MII Value 3210	PCS Code-group 43210	Description
0000	11110	Data 0		1000	10010	Data 8
0001	01001	Data 1		1001	10011	Data 9
0010	10100	Data 2		1010	10110	Data A
0011	10101	Data 3		1011	10111	Data B
0100	01010	Data 4		1100	11010	Data C
0101	01011	Data 5		1101	11011	Data D
0110	01110	Data 6		1110	11100	Data E
0111	01111	Data 7		1111	11101	Data F

Table 4-3 4B/5B Control and Invalid Code Groups

Symbol Name	PCS Code-group 43210	MII Value 3210	Description
I	11111	undefined	IDLE
J	11000	0101	Start of Stream Delimiter Part 1 of 2
K	10001	0101	Start of Stream Delimiter Part 2 of 2
T	01101	undefined	End-of-Stream Delimiter Part 1 of 2
R	00111	undefined	End-of-Stream Delimiter Part 2 of 2
H	00100	undefined	Transmit Error
V	00000,00001,00010,00011,00101,00110,01000,01100,10000,11001	undefined	Invalid Codes

4.4.2 PMA Sublayer

The PMA provides medium-independent means for the PCS and other bit-oriented clients (e.g. repeaters) to support the use of a range of physical media. For 100BASE-X the PMA performs the following functions:

- Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD;
- Generating a control signal indicating the availability of the PMD to a PCS or other client;
- Synchronization with the Auto-Negotiation function;
- Generating indications of carrier activity and carrier errors from the PMD; and,
- Recovery of clock from the NRZI data supplied by the PMD.

100BASE-X PMA Sublayer

Link Monitor: The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. If a failure is found normal operation will be disabled. As specified in the IEEE 802.3 standard, the link is operating reliably when a signal is detected for a period of 330µs.

Far End Fault: When the Auto-Negotiation function is disabled or the chip is in fiber mode, this function is used to exchange fault information between the PHY and the link partner.

100BASE-TX PMD

Scrambler/De-scrambler: The scrambler and de-scrambler used in SHAWNEE meet the ANSI Standard X3.263-1995 FDDI TP-PMD. The purpose of the scrambler is to randomize the 125 Mb/s data on transmission resulting in a reduction of the peak amplitudes in the frequency spectrum. The de-scrambler restores the received 5-bit code groups to their unscrambled values.

The Scrambler input data (plaintext) is encoded by modulo 2 addition of a key stream to produce a ciphertext bit stream. The key stream is a periodic sequence of 2047 bits generated by the recursive linear function X[n] = X[n-11] + X[n-9] (modulo 2).

The key stream sequence is implemented with an 11-bit Linear Feedback Shift Register (LFSR) whose input bit is the exclusive or of the 11^{th} and 9^{th} bits.

The De-scrambler decodes the input ciphertext data by using the same LFSR key stream implementation as in the scrambler.

The scrambler seed is initialized after completion of a reset to:

Bits 11:5 = 1111111

Bits 4:0 = PHY address

The lower 5 bits of the seed value can also be set via the management register 20.4:0. Upon write of this register, scrambler seed is reset.

When not transmitting data, the scrambler encodes and transmits idles. This allows a pattern to use by the de-scrambler to synchronize and decode the scrambled data.

The implementation of the scrambler and de-scrambler is as shown in Appendix G of the ANSI Standard X3.263-1995.

For test, the scrambler can be bypassed by setting bit 18.5. Scrambler Bypass Mode is a special type of interface for 100BTX operation that bypasses the Scrambler and De-scrambler operation. This mode is typically used for test so that input and output test vectors match. In this mode, idles are not sent and the MAC must provide idles.

MLT-3 Encoder/Decoder: An MLT-3 encoder is used in the transmit path to convert NRZ bit stream data from the PMA sublayer into a three-level code. This encoding results in a reduction in the energy over the critical frequency range. The MLT-3 decoder converts the received three-level code back to an NRZ bit stream.

Baseline Wander: The use of the Scrambler and MLT-3 encoding can cause long run lengths of zeroes and ones which can produce a DC component. The DC component cannot be transmitted through the isolation transformers and results in baseline wander. Baseline wander reduces noise immunity since the base line moves closer to either the positive or negative signal comparators.

To correct for this SHAWNEE uses DC restoration to restore the lost DC component of the recovered digital data to correct the baseline wander problem.

Timing Recovery: The timing recovery block locks onto the incoming data stream, extracts the embedded clock, and presents the data synchronized to the recovered clock.

In the event that the Receive path is unable to converge to the receive signal, it resets the "MSE Good" (bit 25.15) signal. The clock synthesizer provides a center frequency reference for operation of the clock recovery circuit in the absence of data.

Adaptive Equalizer: At a data rate of 125 Mb/s, the cable introduces significant distortion due to high frequency roll off and phase shift. The high frequency loss is mainly due to skin effect, which causes the conductor resistance to rise as the square of the frequency.

The Adaptive Equalizer will compensate for signal amplitude and phase distortion incurred from transmitting with different cable lengths.

Loop-back: If asserted by bit 0.14, then data encoded by the MLT3 Encoder block is looped back to the MLT3 Decoder block while the Transmit and Receive path are disconnected from the media.

A second loop-back mode for 100BASE-TX is available by setting bit 18.13 (MII Loop-back) to a logical 1. This loop-back mode takes the MII transmit data and loops it directly back to the MII receive pins. Again, the Transmit and Receive path are disconnected from the media.

MII Loop-Back has precedence over the Digital Loop-back if both are enabled at the same time.

A third loopback mode is available by setting bit 18.4 high. This Analog Loopback mode takes the MLT3 encoded data and loops it back through the Base Line Wander and the analog receive circuits.

Line Transmitter and Line Receiver: These analog blocks allow SHAWNEE to drive and receive data to/from the 100Base-TX media. The transmitter is designed to drive a 100-Ohm UTP cable.

Link Monitor: The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. If a failure is found normal operation will be disabled. As specified in the IEEE 802.3 standard, the link is operating reliably when a signal is detected for a period of 330µs.

Far End Fault: When the Auto-Negotiation function is disabled or the chip is in fiber mode, this function is used to exchange fault information between the PHY and the link partner.

4.4.3 PMD Sublayer

For 100Base-TX the ANSI X3.263: 199X (TP-PMD) standard is used. These signaling standards, called PMD sublayers, define 125 Mb/s, full duplex signaling systems that STP and UTP wiring.

100BASE-TX PMD

Scrambler/De-scrambler: The scrambler and de-scrambler used in SHAWNEE meet the ANSI Standard X3.263-1995 FDDI TP-PMD. The purpose of the scrambler is to randomize the 125 Mb/s data on transmission resulting in a reduction of the peak amplitudes in the frequency spectrum. The de-scrambler restores the received 5-bit code groups to their unscrambled values.

The Scrambler input data (plaintext) is encoded by modulo 2 addition of a key stream to produce a ciphertext bit stream. The key stream is a periodic sequence of 2047 bits generated by the recursive linear function X[n] = X[n-11] + X[n-9] (modulo 2).

The key stream sequence is implemented with an 11-bit Linear Feedback Shift Register (LFSR) whose input bit is the exclusive or of the 11^{th} and 9^{th} bits.

The De-scrambler decodes the input ciphertext data by using the same LFSR key stream implementation as in the scrambler.

The scrambler seed is initialized after completion of a reset to:

Bits 11:5 = 1111111

Bits 4:0 = PHY address

The lower 5 bits of the seed value can also be set via the management register 20.4:0. Upon write of this register, scrambler seed is reset.

When not transmitting data, the scrambler encodes and transmits idles. This allows a pattern to use by the de-scrambler to synchronize and decode the scrambled data.

The implementation of the scrambler and de-scrambler is as shown in Appendix G of the ANSI Standard X3.263-1995.

For test, the scrambler can be bypassed by setting bit 18.5. Scrambler Bypass Mode is a special type of interface for 100BTX operation that bypasses the Scrambler and De-scrambler operation. This mode is typically used for test so that input and output test vectors match. In this mode, idles are not sent and the MAC must provide idles.

MLT-3 Encoder/Decoder: An MLT-3 encoder is used in the transmit path to convert NRZ bit stream data from the PMA sublayer into a three-level code. This encoding results in a reduction in the energy over the critical frequency range. The MLT-3 decoder converts the received three-level code back to an NRZ bit stream.

Baseline Wander: The use of the Scrambler and MLT-3 encoding can cause long run lengths of zeroes and ones which can produce a DC component. The DC component cannot be transmitted through the isolation transformers and results in baseline wander. Baseline wander reduces noise immunity since the base line moves closer to either the positive or negative signal comparators.

To correct for this SHAWNEE uses DC restoration to restore the lost DC component of the recovered digital data to correct the baseline wander problem.

Timing Recovery: The timing recovery block locks onto the incoming data stream, extracts the embedded clock, and presents the data synchronized to the recovered clock.

In the event that the Receive path is unable to converge to the receive signal, it resets the "MSE Good" (bit 25.15) signal. The clock synthesizer provides a center frequency reference for operation of the clock recovery circuit in the absence of data.

Adaptive Equalizer: At a data rate of 125 Mb/s, the cable introduces significant distortion due to high frequency roll off and phase shift. The high frequency loss is mainly due to skin effect, which causes the conductor resistance to rise as the square of the frequency.

The Adaptive Equalizer will compensate for signal amplitude and phase distortion incurred from transmitting with different cable lengths.

Loop-back: If asserted by bit 0.14, then data encoded by the MLT3 Encoder block is looped back to the MLT3 Decoder block while the Transmit and Receive path are disconnected from the media.

A second loop-back mode for 100BASE-TX is available by setting bit 18.13 (MII Loop-back) to a logical 1. This loop-back mode takes the MII transmit data and loops it directly back to the MII receive pins. Again, the Transmit and Receive path are disconnected from the media.

MII Loop-Back has precedence over the Digital Loop-back if both are enabled at the same time.

A third loopback mode is available by setting bit 18.4 high. This Analog Loopback mode takes the MLT3 encoded data and loops it back through the Base Line Wander and the analog receive circuits.

Line Transmitter and Line Receiver: These analog blocks allow SHAWNEE to drive and receive data to/from the 100Base-TX media. The transmitter is designed to drive a 100-Ohm UTP cable.

4.5 Low Power

There are several reduced power configurations available for the EPHY.

4.5.1 STOP mode

If the MCU executes a STOP instruction the EPHY will be powered down and all internal MII registers reset to their default state. Upon exiting STOP mode the EPHY will exit the power-down state and latch the values previously written to the EPHYCTL0 and EPHYCTL1 registers. The MII registers will have to be re-initialized after the start-up delay($D_{start\text{-}up}$) has expired.

4.5.1.1 WAIT mode

If the MCU executes a WAIT instruction with the EPHYWAI bit set, the EPHY will be powered down and all internal MII registers reset to their default state. Upon exiting STOP mode the EPHY will exit the power-down state and latch the values previously written to the EPHYCTL0 and EPHYCTL1 registers. The MII registers will have to be re-initialized after the start-up delay($D_{start\text{-}up}$) has expired.

4.5.2 MII Power Down

This mode disconnects the PHY from the network interface (tri-state receiver and driver pins).

Setting bit 0.11 of the port enters this mode. In this mode the management interface is still accessible but all internal chip functions are in a zero power state.

In this mode all analog blocks except the PLL clock generator and band gap reference are in low power mode. All digital blocks except the MDIO interface and management registers are inactive.

4.6 Media Independent Interface (MII)

The EPHY has an internal Media Independent Interface (MII) as specified in the IEEE 802.3u standard. The MII interface meets all requirements of timing and latency established by the standard.

The MII interface has the following characteristics:

- It is capable of supporting both 10 Mb/s and 100 Mb/s data rates.
- Data and delimiters are synchronous to clock references.
- It provides independent four bit wide transmit and receive data paths.
- It provides a simple management interface

4.6.1 Transmit and Receive Data Paths

Both transmit and receive data paths are serviced with 7 signals: 4 data bits, Enable, Error, and Clock. Also provided are two media status signals, CRS (carrier sense) and COL (collision detect). A management interface is also included to provide access to management parameters and services.

4.6.1.1 MII Transmit Path Signals

TXC (transmit clock): TXC is a continuous clock, whose rising edge provides the timing reference for the transfer of the TXEN, TXD, TXER signals from the Reconciliation sub-layer to the PHY.

TXEN (transmit enable): TXEN indicates that the Reconciliation sub-layer is presenting nibbles on the MII for transmission. It shall be synchronous with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TXEN will be negated prior to the first TXC following the final nibble of a frame.

TXD (transmit data): TXD is a bundle of 4 data signals, TXD<3:0>, that is driven by the Reconciliation sub-layer. The data will be synchronous with the TXC and the values are valid when TXEN is asserted. TXD<0> represents the least significant bit.

TXD<4> is also provided for use when the PHY is in Symbol mode (Bit 18.6).

TXER (transmit coding error): When TXER is asserted for one or more TXC periods while TXEN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of TXER shall not affect the transmission of data when the PHY is operating at 10 Mb/s or when TXEN is de-asserted.

Summary: shows the possible combinations of values and the condition that each value describes.

Table 4-4 Transmit Path Permitted Codes

TXEN	TXER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit error propagation
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit error propagation

4.6.1.2 MII Receive Path Signals

RXC (Receive Clock): RXC is a continuous clock, whose rising edge provides the timing reference for the transfer of the RXDV, RXD, and RXER signals from the PHY to the Reconciliation sublayer and is sourced by the PHY. The PHY may recover RXC from the received data or it may derive the RXC from a nominal clock such as TXC.

When RXDV is asserted, RXC shall be synchronous with the recovered data, and shall have a frequency equal to 2.5 MHz for 10Base-T operation and 25 MHz for 100Base-X operation. The duty cycle is also between 35% and 65% inclusive.

If a loss of received signal from the medium causes the PHY to lose the recovered RXC reference, the PHY shall source the RXC from the nominal clock reference. Transitions between nominal and reference clocks shall occur only when RXDV is de-asserted.

RXDV (Receive Data Valid): RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD data bundle and that the data is synchronous to the RXC.

RXDV shall remain asserted from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RXC that follows the final nibble.

In order for a receive frame to be correctly interpreted by the Reconciliation sublayer and MAC sublayer, RXDV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

RXD (Receive Data): RXD is a bundle of 4 (5 for symbol mode) data signals that transition synchronously with respect to RXC. RXD is driven by the PHY.

For each RXC period in which RXDV is asserted the RXD data is transferred from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RXDV is de-asserted, RXD shall have no effect on the Reconciliation sublayer.

A complete formed SFD must be passed across the MII for the MAC sublayer to interpret it correctly.

RXER (Receive Error): RXER is asserted by the PHY to indicate the occurrence of an error in the frame currently being read.

Summary: Table 4-5 Receive Path Permitted Codes shows the possible combination of values and the condition that each value describes.

Table 4-5 Receive Path Permitted Codes

RXDV	RXER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data reception
1	1	0000 through 1111	Data reception with errors

4.6.2 MII Media Status Signals

CRS (Carrier Sense): CRS shall be asserted by the PHY when either the Transmit or Receive mediums are non-idle. When the Transmit and Receive mediums are idle then CRS should be de-asserted. This signal should also remain asserted throughout the duration of a collision condition.

CRS is not required to be synchronous to either TXC or RXC.

COL (Collision Detected): This signal is asserted when a collision is detected. This signal remains active (high) for the duration of the collision. This signal is asynchronous and is inactive during full-duplex operation.

SQE (Heartbeat): By default, the Signal Quality Error SQE) or heartbeat function is disabled. To enable this function set bit 19.10. When this function is enabled, COL is asserted for 5-15 BT after each packet.

4.6.3 Management Interface Frames

Frames transmitted on the MII Management Interface have the frame structure shown in **Figure 4-6** for a read request and in **Figure 4-7**for a write request.

Figure 4-6 Management Interface Read Frame

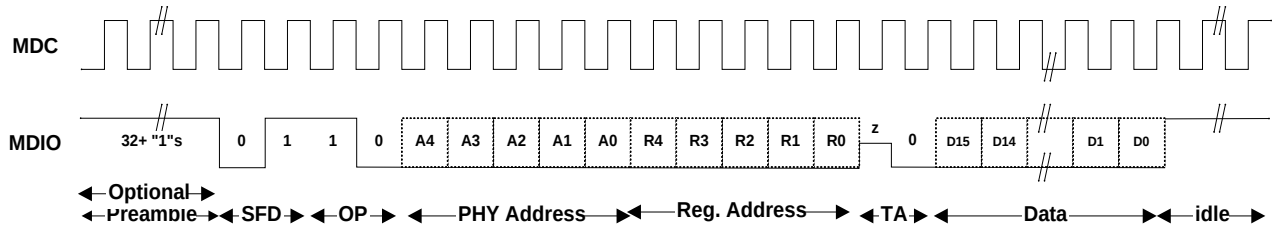
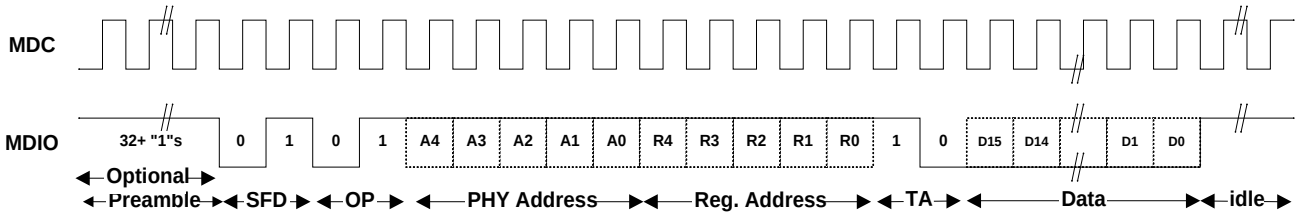


Figure 4-7 Management Interface Write Frame



IDLE: The IDLE condition on the MDIO is a high-impedance state. All three-state drivers shall be disabled and SHAWNEE's pull-up resistor will pull the MDIO line to logic one.

PRE (preamble): Optionally, at the beginning of each transaction, the STA may send a sequence of 32 contiguous logical one bits on MDIO with 32 corresponding cycles on MDC.

ST (start of frame): The start of frame pattern is indicated by a <01> pattern. This provides SHAWNEE a pattern it can use to establish synchronization. After this SHAWNEE will be ready to respond to any transaction. If unexpected or erroneous data is read in at any subsequent point in the frame, SHAWNEE will discard the frame and wait until the frame was expected to complete before looking for another ST.

When preamble is suppressed, ST is not allowed 3 MDC clock cycles following a software reset (Bit 0.15).

OP (operation code): The operation code allows a read transaction when it is set to <10> or a write operation when it is set to <01>.

PHYAD (PHY Address): The PHY address is five bits wide. The MSB of the PHY address is always transmitted first. SHAWNEE will accept STA operation when it is correctly addressed by the STA.

REGAD (Register Address): The Register Address is five bits wide allowing up to 32 registers to be addressed within each PHY. The first register address bit transmitted and received is the MSB of the address.

TA (turnaround): The turnaround time is a 2-bit time spacing between the REGAD field and the DATA field of management frame to avoid contention during a read transaction.

For a read transaction, both the STA and PHY shall remain in a high-impedance state for the first bit time of the turnaround. PHY will drive a zero bit during the second bit time of the turnaround of a read transaction.

During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround.

DATA: The data field is 16 bits wide to correspond to the width of the registers. The first data bit transmitted and received shall be bit 15 of the register being addressed.

Appendix A Electrical Specifications

A.1 MII – 100Base-TX

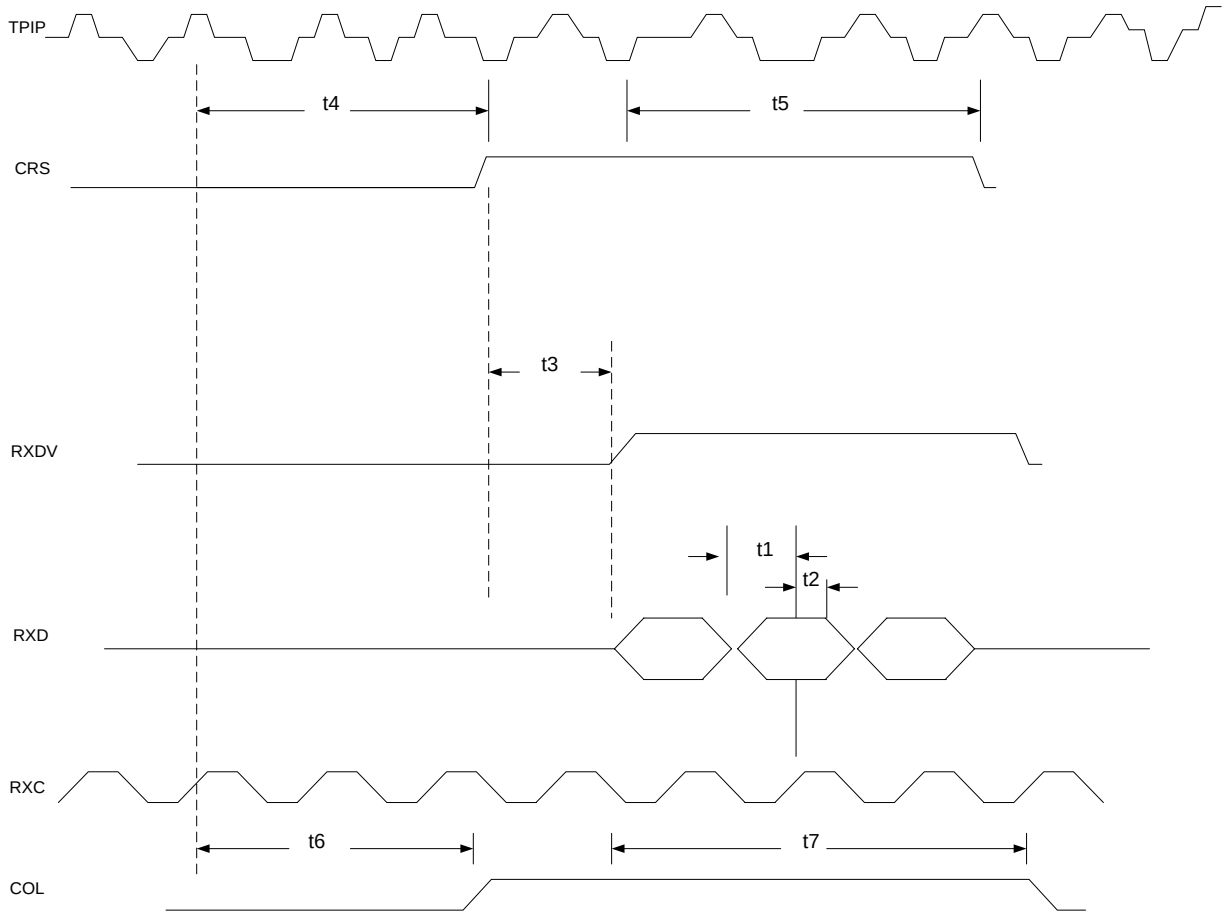
A.1.1 MII – 100Base-TX Receive Timing Parameters

Table A-1 MII – 100Base-TX Receive Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	RXD, RXDV, RXER Setup to RXC High	t1	10			ns
2	C	RXD, RXDV, RXER Hold to RXC High	t2	10			ns
3	C	100Base-TX Receive Timing 4B Mode					
4	C	CRS asserted to RXD, RXDV asserted	t3		4		BT
5	C	Receive start of “J” to CRS asserted	t4		19	20 [a]	BT
6	C	Receive start of “T” to CRS de-asserted	t5	13 [a]	23	24 [a]	BT
7	C	Receive start of “J” to COL asserted	t6		19	20 [a]	BT
8	C	Receive start of “T” to COL de-asserted	t7	13 [a]	23	24 [a]	BT
9	C	100Base-TX Receive Timing 5B Mode					
10	C	CRS asserted to RXD, RXDV asserted	t3		0-4		BT
11	C	Receive start of “J” to CRS asserted	t4		19		BT
12	C	Receive start of “T” to CRS de-asserted	t5		23		BT
13	C	Receive start of “J” to COL asserted	t6		19		BT
14	C	Receive start of “T” to COL de-asserted	t7		23		BT

Typical values are at 25C.
1 BT = Bit Time = 100ns
These parameters are the minimum and maximum times as specified in section 24.6 of the IEEE 802.3u Standard

Figure A-1 100Base-TX Receive Timing



A.1.2 MII – 100Base-TX Transmit Timing Parameters

Table A-2 MII – 100Base-TX Transmit Timing Parameters

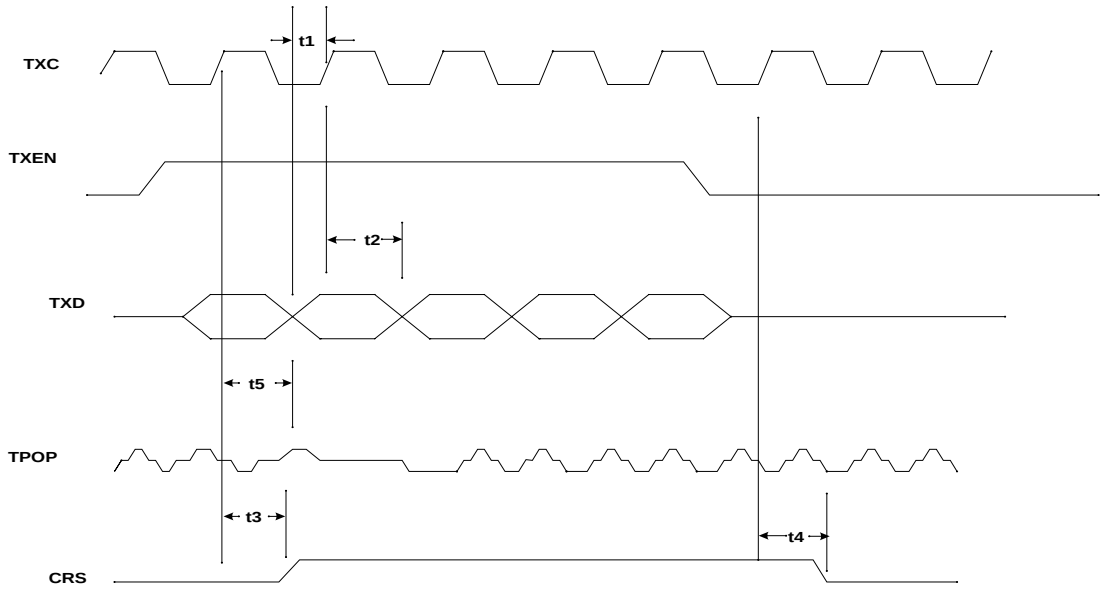
Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	TXD, TXEN, TXER Setup to TXC High	t1	10			ns
2	C	TXD, TXEN, TXER Hold to TXC High	t2	5			ns
3	C	**100Base-TX Transmit Timing 4B Mode**					
4	C	TXEN sampled to CRS asserted	t3	0 [a]	0	4 [a]	BT[1]
5	C	TXEN sampled to CRS de-asserted	t4	0 [a]	12	16 [a]	BT

Table A-2 MII – 100Base-TX Transmit Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
6	C	TXEN sampled to TPO out (Tx latency)	t5	6 [a]	7	14 [a]	BT
7	C	**100Base-TX Transmit Timing 5B Mode**					
8	C	TXEN sampled to CRS asserted	t3		0		BT
9	C	TXEN sampled to CRS de-asserted	t4		0		BT
10	C	TXEN sampled to TPO out (Tx latency)	t5		3		BT

Typical values are at 25C.
1 BT = Bit Time = 100ns
These parameters are the minimum and maximum times as specified in section 24.6 of the IEEE 802.3u Standard

Figure A-2 100Base-TX Transmit Timing



A.2 MII – 10Base-T

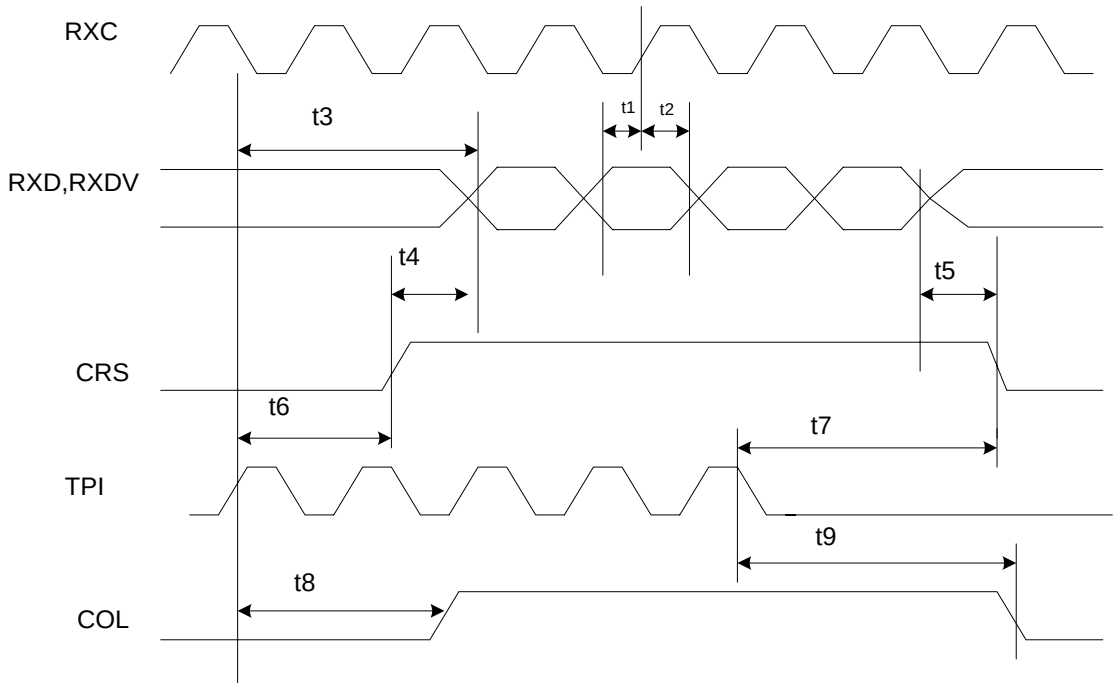
A.2.1 MII – 10Base-T Receive Timing

Table A-3 MII – 10Base-T Recieve Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	RXD, RXDV Setup to RXC High	t1		40		ns
2	C	RXD, RXDV Hold to RXC High	t2		30		ns
3	C	TPI in to RXD out (Rx latency)	t3		56		BT[1]
4	C	CRS asserted to RXD, RXDV asserted	t4		7		BT
5	C	RXD, RXDV de-asserted to CRS de-asserted	t5		0		BT
6	C	TPI in to CRS asserted	t6		49		BT
7	C	TPI quiet to CRS de-asserted	t7		3.5		BT
8	C	TPI in to COL asserted	t8		15.5		BT
9	C	TPI quiet to COL de-asserted	t9		1.8		BT

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure A-3 10Base-T Receive Timing



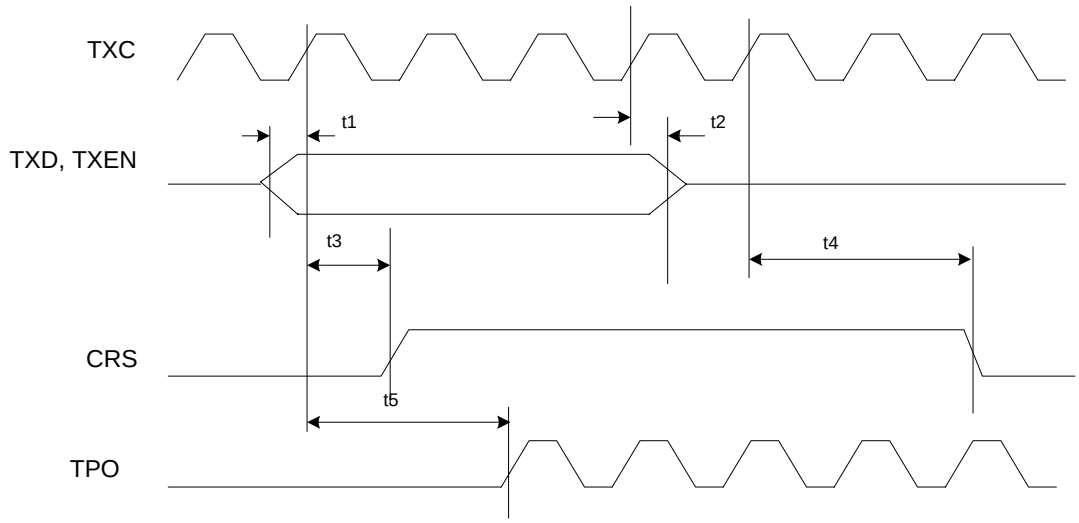
A.2.2 MII – 10Base-T Transmit Timing

Table A-4 MII – 10Base-T Transmit Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	TXD, TXEN Setup to TXC High	t1	10			ns
2	C	TXD, TXEN Hold to TXC High	t2	5			ns
3	C	TXEN sampled to CRS asserted	t3		2		BT[1]
4	C	TXEN sampled to CRS de-asserted	t4		2		BT
5	C	TXEN sampled to TPO out (Tx latency)	t5		2.3		BT

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure A-4 10Base-T Transmit Timing



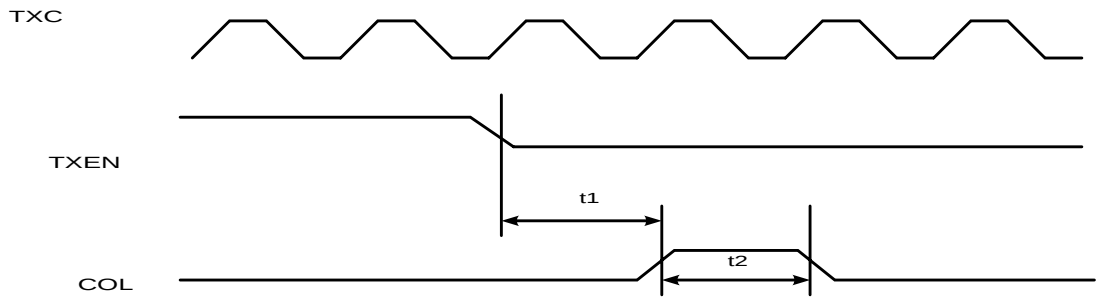
A.2.3 10Base-T SQE (Heartbeat) Timing

Table A-5 10Base-T SQE (Heartbeat) Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	COL (SQE) Delay after TXEN off	t1		1.0		µs
2	C	COL (SQE) Pulse duration	t2		1.0		µs

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure A-5 10Base-T SQE (Heartbeat) Timing



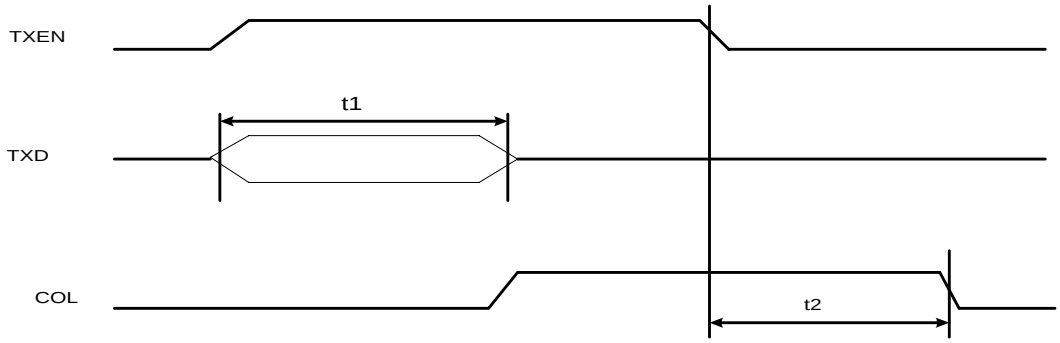
A.2.4 10Base-T Jab and Unjab Timing

Table A-6 10Base-T Jab and Unjab Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Maximum Transmit time	t1		98		ms
2	C	Unjab time	t2		525		ms

.Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure A-6 10Base-T SQE (Heartbeat) Timing



A.3 Auto Negotiation

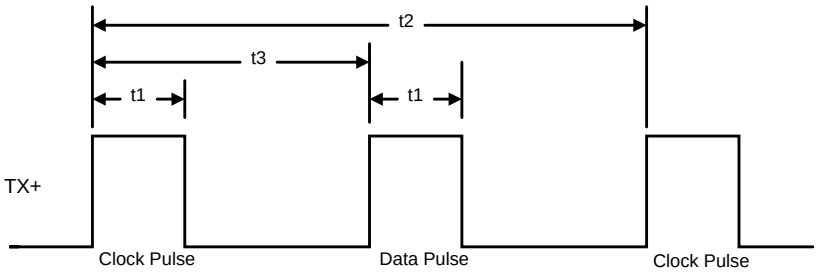
A.3.1 MII – 100Base-TX Transmit Timing Parameters

Table A-7 MII – Auto Negotiation and Fast Link Pulse Timing Parameters

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Clock/Data pulse width	t1		100		ns
2	C	Clock pulse to Clock pulse	t2	111	125	139	µs
3	C	Clock pulse to Data pulse (Data = 1)	t3	55.5	62.5	69.5	µs
4	C	Pulses in a Burst	t4	17		33	#
5	C	FLP burst width	t5		2		ms
6	C	FLP burst to FLP burst	t6	8	16	24	ms

Typical values are at 25C.
1 BT = Bit Time = 100ns
These parameters are the minimum and maximum times as specified in section 24.6 of the IEEE 802.3u Standard

Figure A-7 A/N and Fast Link Pulse Timing



A.3.2 MII – 10Base-T Receive Timing

Table A-8 Auto Negotiation and Fast Link Pulse Timing

Num	C	Parameter	Sym	Min	Typ	Max	Units
1	C	Transmit FLNP width		1.25	1.5	1.75	µs
2	C	Receive FLNP width		1	1.5	2	µs
3	C	Clock/Data pulse width	t1		100		ns
4	C	Clock FLNP to Clock FLNP	t2	111	125	139	µs
5	C	Clock FLNP to Data FLNP (Data = 1)	t3	55.5	62.5	69.5	µs
6	C	Pulses in a Burst	t4	17		33	#
7	C	FLNP burst width	t5		2		ms
8	C	FLNP burst to FLNP burst	t6	8	16	24	ms

Typical values are at 25C.
1 BT = Bit Time = 100ns

Figure A-8 Fast Link Pulse Timing

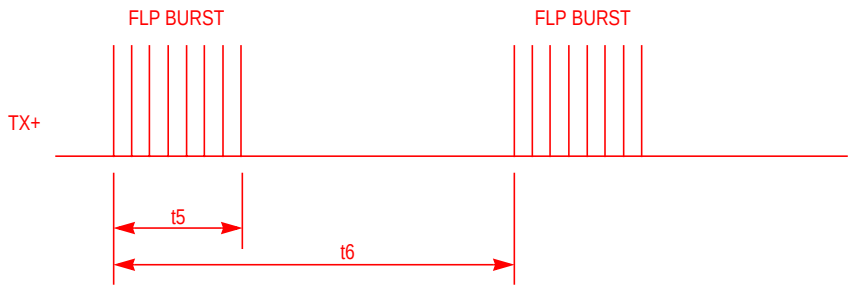


Figure A-9 AutoNegotiation Pulse Timing

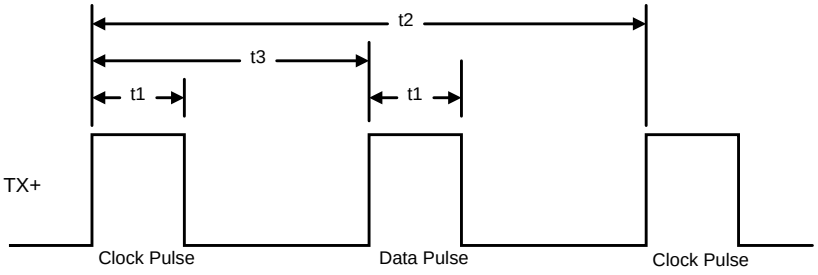
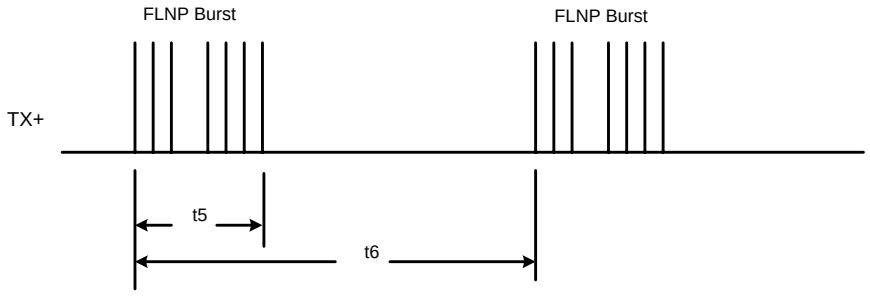


Figure A-10 Fast Link Pulse Timing



A.4 MII Timing

The following MII timing is based on IEEE Std 802.3.

A.4.1 MII Receive Signal Timing (RXD[3:0], RXDV, RXER, RXCLK)

NUM	Characteristic	MIN	MAX	UNIT
M1	RXD[3:0], RXDV, RXER setup to RXCLK rise	10	-	ns
M2	RXCLK rise to RXD[3:0], RXDV, RXER hold	10	-	ns
M3	RXCLK pulse width high	35%	65%	RXCLK period
M4	RXCLK pulse width low	35%	65%	RXCLK period

Table A-9 MII Receive Signal Timing

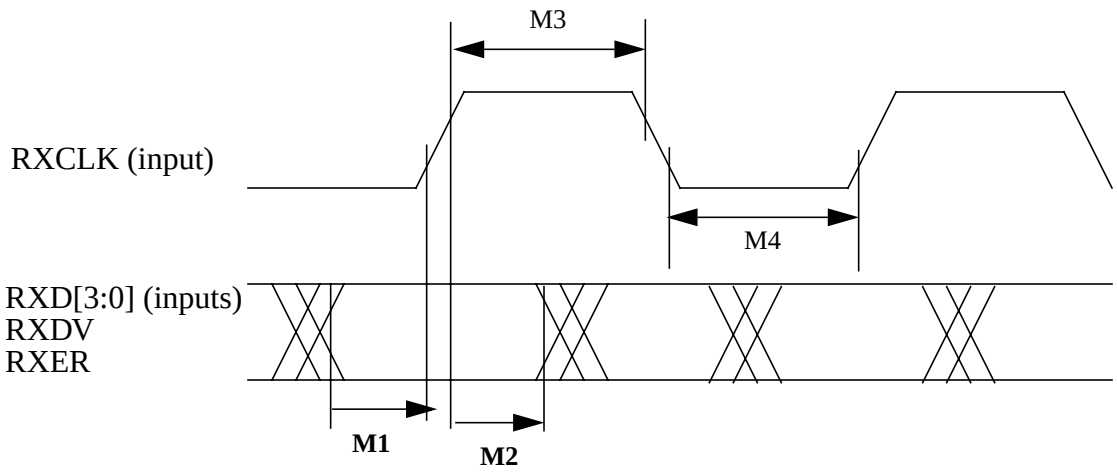


Figure A-11 MII Receive Signal Timing Diagram

A.4.2 MII Transmit Signal Timing (TXD[3:0], TXEN, TXER, TXCLK)

NUM	Characteristic	MIN	MAX	UNIT
M5	TXCLK rise to TXD[3:0], TXEN, TXER invalid	0	-	ns
M6	TXCLK rise to TXD[3:0], TXEN, TXER valid	-	25	ns
M7	TXCLK pulse width high	35%	65%	TXCLK period
M8	TXCLK pulse width low	35%	65%	TXCLK period

Table A-10 MII Transmit Signal Timing

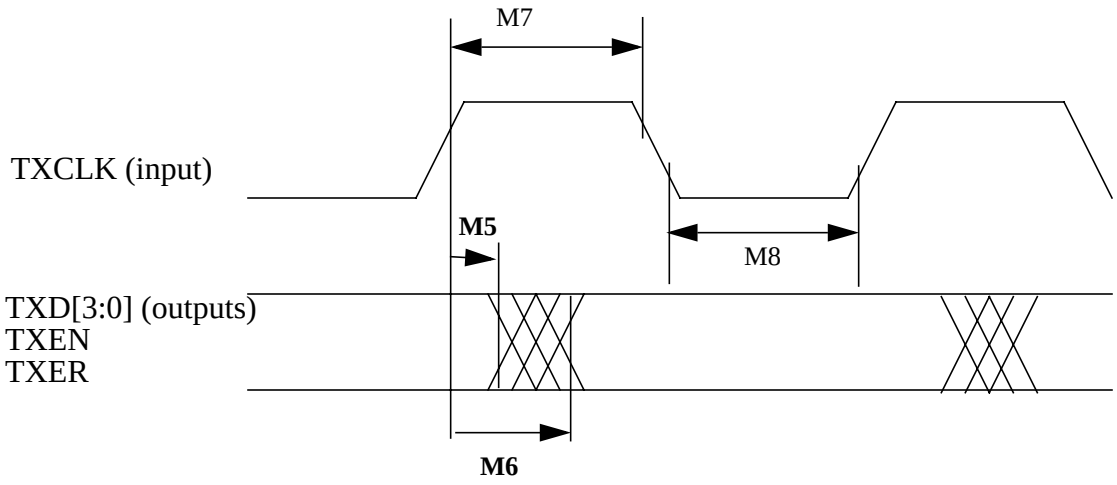


Figure A-12 MII Transmit Signal Timing Diagram

A.4.3 MII Asynchronous Inputs Signal Timing (CRS, COL)

NUM	Characteristic	MIN	MAX	UNIT
M9	CRS, COL minimum pulse width	1.5	-	TXCLK period

Table A-11 MII Transmit Signal Timing

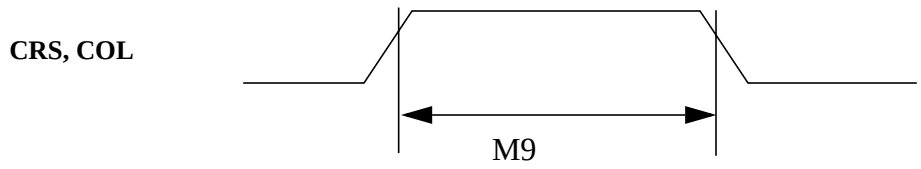


Figure A-13 MII Asynchronous Inputs Timing Diagram

A.4.4 MII Management Timing (MDIO,MDC)

NUM	Characteristic	MIN	MAX	UNIT
M10	MDC rise to MDIO (output) invalid	10	-	ns
M11	MDC rise to MDIO (output) valid	-	390	ns
M12	MDIO (input) setup to MDC rise	100	-	ns
M13	MDC rise to MDIO (input) hold	0	-	ns
M14	MDC pulse width high	40%	60%	MDC period
M15	MDC pulse width low	40%	60%	MDC period

Table A-12 MII Management Signal Timing

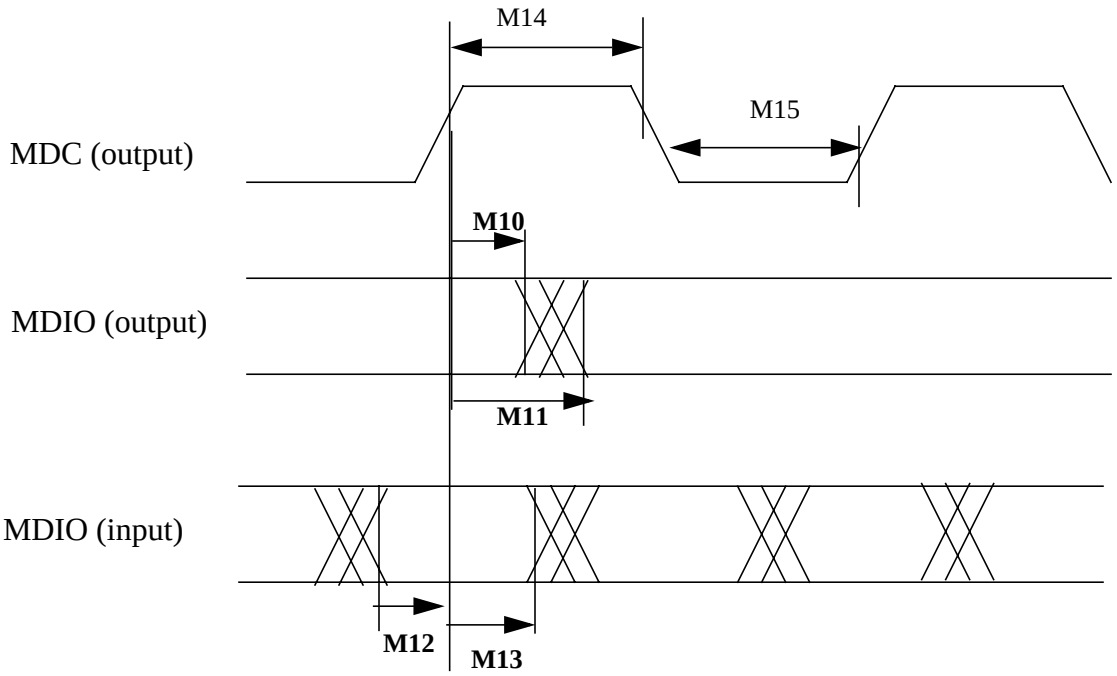


Figure A-14 MII Serial Management Channel Timing Diagram

A.5 Electrical Specifications

Table A-13 Recommended Operating Conditions

Num	C	Parameter	Sym	Min	Typ	Max	Units	Issues/comments
1	C	Power Supply	VDD	2.375	2.5	2.625	V	5% Tolerance
2	C	Power Supply Ripple Noise		-50	0	+50	mV	Spectrum < 160MHz
3	C	Power Supply (IO)	VDD3P3	3.135	3.3	3.465	V	5% Tolerance
4	C	Junction Temperature		0	55	135	C	
5	C	Power Supply Common Block	VDDA			25	mA	When both 10BT and 100BT modes simultaneously operating

Table A-14 10BaseT Transceiver Characteristics

Num	C	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	C	Peak Differential Output Voltage	VOP	2.2	2.5	2.8	V	With specified transformer and line replaced by 100ohm (+/-1%) load
2	C	Transmit Timing Jitter	-	0	2	11	ns	Using line model specified in the IEEE 802.3
3	C	Receive dc Input Impedance	Zin	-	10	-	kΩ	0.0 < Vin < 3.3V
4	C	Receive Differential Squelch Level	Vsquelch	300	400	585	mV	3.3MHz sine wave input

Table A-15 100BaseTX Transceiver Characteristics

Num	C	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
1	C	Transmit Peak Differential Output Voltage	VOP	0.95	1.00	1.05	V	With specified transformer and line replaced by 100ohm (+/-1%) load
2	C	Transmit Signal Amplitude Symmery	Vsym	98	100	102	%	With specified transformer and line replaced by 100ohm (+/-1%) load
3	C	Transmit Rise/Fall Time	Trf	3	4	5	ns	With specified transformer and line replaced by 100ohm (+/-1%) load
4	C	Transmit Rise/Fall Time Symmetry	Trfs	-0.5	0	+0.5	ns	See IEEE 802.3 for details
5	C	Transmit Overshoot/UnderShoot	Vosh	-	2.5	5	%	
6	C	Transmit Jitter	-	0	.6	1.4	ns	
7	C	Receive Common Mode Voltage	Vcm	-	1.6	-	V	VDDRX=2.5V
8	C	Receiver Maximum Input Voltage	Vmax	-	-	4.7	V	VDDRX=2.5V. Internal circuits protected by divider in shutdown

Block Guide End Sheet

FINAL PAGE OF
84
PAGES