# PB68HC12A4 Controller Module



# PB68HC12A4 - I/O Connectors

The Motorola M68HC12 Microcontroller is attached to four dual row 14 pin connectors (28 pins each) which are configured as follows:

P1						P2					
Vss	1	1	2	2	Vdd	D9/PC1	29	1	2	30	PC2/D10
PJ0	3	3	4	4	PJ1	D11/PC3	31	3	4	32	PC4/D12
PJ2	5	5	6	6	PJ3	D13/PC5	33	5	6	34	PC6/D14
PJ4	7	7	8	8	PJ5	D15/PC7	35	7	8	36	PE0/XIRQ
PJ6	9	9	10	10	PJ7	IRQ/PE1	37	9	10	38	PE2/R/W
A16/PG0	11	11	12	12	PG1/A17	LSTR/PE3	39	11	12	40	/RESET
A18/PG2	13	13	14	14	Vdd	Vss	41	13	14	42	Vdd
Vss	15	15	16	16	PG3/A19	Vddpll	43	15	16	44	XFC
A20/PG4	17	17	18	18	PG5/A21	Vsspll	45	17	18	46	EXTAL
BKGD	19	19	20	20	PD0/D0	XTAL	47	19	20	48	PE4/ECLK
D1/PD1	21	21	22	22	PD2/D2	MODA/PE5	49	21	22	50	PE6/MODB
D3/PD3	23	23	24	24	PD4/D4	ARST/PE7	51	23	24	52	PB0/A0
D5/PD5	25	25	26	26	PD6/D6	A1/PB1	53	25	26	54	PB2/A2
D7/PD7	27	27	28	28	PC0/D8	A3/PB3	55	27	28	56	PB4/A4
P3											
Λ <i>Ε/</i> DD <i>E</i>	ĺ		_	Ī	DDG/AG	V		_	24	٦	V
A5/PB5	57	1	2	58	PB6/A6	$V_{RH}$	85	1	2	86	$V_{RL}$
A7/PB7	59	1	2 4	60	PA0/A8	PAD0	87	1	2 4	88	PAD1
A7/PB7 A9/PA1	59 61	1 3 5	2 4 6	60 62	PA0/A8 PA2/A10	PAD0 PAD2	87 89	1 3 5	2 4 6	88 90	PAD1 PAD3
A7/PB7 A9/PA1 A11/PA3	59 61 63	1 3 5 7	2 4 6 8	60 62 64	PA0/A8 PA2/A10 PA4/A12	PAD0 PAD2 PAD4	87 89 91	1 3 5 7	2 4 6 8	88 90 92	PAD1 PAD3 PAD5
A7/PB7 A9/PA1 A11/PA3 A13/PA5	59 61 63 65	1 3 5 7 9	2 4 6 8 10	60 62 64 66	PA0/A8 PA2/A10 PA4/A12 PA6/A14	PAD0 PAD2 PAD4 PAD6	87 89 91 93	1 3 5 7 9	2 4 6 8 10	88 90 92 94	PAD1 PAD3 PAD5 PAD7
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7	59 61 63 65 67	1 3 5 7 9 11	2 4 6 8 10 12	60 62 64 66 68	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub>	87 89 91 93 95	1 3 5 7 9 11	2 4 6 8 10 12	88 90 92 94 96	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub>
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1	59 61 63 65 67 69	1 3 5 7 9 11 13	2 4 6 8 10 12 14	60 62 64 66 68 70	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0	87 89 91 93 95	1 3 5 7 9 11 13	2 4 6 8 10 12 14	88 90 92 94 96 98	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1 CS3/PF3	59 61 63 65 67 69 71	1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	60 62 64 66 68 70 72	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2 PF4/CSD	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0 RxD1/PS2	87 89 91 93 95 97	1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16	88 90 92 94 96 98 100	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0 PS3/TxD1
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1	59 61 63 65 67 69	1 3 5 7 9 11 13	2 4 6 8 10 12 14	60 62 64 66 68 70	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0 RxD1/PS2 SDI/PS4	87 89 91 93 95	1 3 5 7 9 11 13	2 4 6 8 10 12 14	88 90 92 94 96 98	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0 PS3/TxD1 PS5/SDO
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1 CS3/PF3 CSP0/PF5	59 61 63 65 67 69 71 73	1 5 7 9 11 13 15	2 4 6 8 10 12 14 16 18	60 62 64 66 68 70 72 74	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2 PF4/CSD PF6/CSP1	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0 RxD1/PS2	87 89 91 93 95 97 99	1 3 5 7 9 11 13 15	2 4 6 8 10 12 14 16 18	88 90 92 94 96 98 100	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0 PS3/TxD1 PS5/SDO PS7/SCK
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1 CS3/PF3 CSP0/PF5 PH0	59 61 63 65 67 69 71 73 75	1 3 5 7 9 11 13 15 17	2 4 6 8 10 12 14 16 18 20	60 62 64 66 68 70 72 74 76	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2 PF4/CSD PF6/CSP1 PH1	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0 RxD1/PS2 SDI/PS4 MOSI/PS6	87 89 91 93 95 97 99 101	1 3 5 7 9 11 13 15 17	2 4 6 8 10 12 14 16 18 20	88 90 92 94 96 98 100 102	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0 PS3/TxD1 PS5/SD0 PS7/SCK PT1
A7/PB7 A9/PA1 A11/PA3 A13/PA5 A15/PA7 CS1/PF1 CS3/PF3 CSP0/PF5 PH0 PH2	59 61 63 65 67 69 71 73 75	1 3 5 7 9 11 13 15 17 19 21	2 4 6 8 10 12 14 16 18 20 22	60 62 64 66 68 70 72 74 76 78	PA0/A8 PA2/A10 PA4/A12 PA6/A14 PF0/CS0 PF2/CS2 PF4/CSD PF6/CSP1 PH1 PH3	PAD0 PAD2 PAD4 PAD6 V <sub>DDA</sub> RxD0/PS0 RxD1/PS2 SDI/PS4 MOSI/PS6 PT0	87 89 91 93 95 97 99 101 103 105	1 3 5 7 9 11 13 15 17 19 21	2 4 6 8 10 12 14 16 18 20 22	88 90 92 94 96 98 100 102 104	PAD1 PAD3 PAD5 PAD7 V <sub>SSA</sub> PS1/TxD0 PS3/TxD1 PS5/SD0 PS7/SCK PT1 PT3

**Note** 1. Small number next to connector pin number is the MC68HC812A4 device pin number.

2. Designators next to pin numbers are MC68HC812A4 port designators.

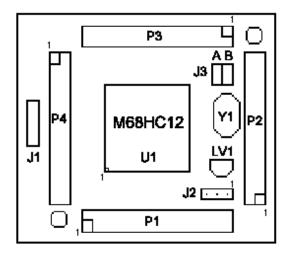
**J1 SCI0 Header** SCI 0 Serial Port Header.

Provides connection for +Vdd, Vss, RXD0 and TXD0.

**J2 Debug Header** Debug and Reset pin Connections.

J3 HC12 Mode A = MODA and B=MODB

# PB68HC12A4 - Jumper Options



### **J3 Mode Selection**

Jumper J3 selects the M68HC12 operating mode as follows:

Α	В	MODE
off	off	Expanded Wide Mode, 16 bit data bus
off	on	Expanded Narrow Mode, 8 bit data bus
on	off	Reserved, do not select.
on	on	Single Chip Mode, no external bus

### J1 SCI0 Header

The J1 header provides a means of easily connecting external power and communication access to the PB68HC12A4 board. Axiom provides an RS232 converter accessory module that can provide +5V and a DB9 connector for connection to a PC. This allows the use of the AX12 utility program for programming the M68HC12. Following are the J1 connections:

```
Pin 1 HC12 TxD0
Pin 2 HC12 RxD0
Pin 3 +Vdd (5 volts)
Pin 4 Vss (Ground)
```

# J2 Debug Header

The J2 header provides a means of easily connecting a background debug box. The header also provides for a means of applying RESET to the M68HC12 by jumpering pins 1 and 2 together. Following is the pinout of J2:

```
Pin 1 RESET active low
Pin 2 Vss Ground
Pin 3 BGND debug pin
```

# PB68HC12A4 - Operation

# Y1 Crystal Oscillator

Y1 is 16.00MHz standard. This provides a bus speed of 8mhz to the external system.

## **LV1 Reset Generator**

LV1 is a voltage detector that will generate an active low RESET state if Vdd is below +4.4 VDC. If the PB68HC12A4 is to be operated at 3.3VDC then LV1 should be removed. Contact the factory about low voltage options.

### **HC12 Bootloader Firmware**

The M68HC12 is pre-programmed with bootload firmware that operates in conjunction with the AX12 Utility software to provide a low cost debugging and programming environment for the M68HC12. The firmware is programmed into the second 64 byte block of the internal HC812A4 EEPROM and becomes operational when the HC812A4 is in Single Chip Mode.

### **Firmware Memory**

Single Chip Mode (normal) \$FF80 - \$FFBF and \$FFFE/FFFF = Reset Vector Expanded Modes (default) \$1F80 - \$1FBF and \$1FFE/1FFF = \$FF80

Caution should be used to assure the bootload firmware is not erased or corrupted by user software. The EEPROT Register (\$00F1 default) bits 0 and 1 should be set high during the initialization sequence to protect the bootload firmware. If the bootloader firmware is erased or corrupted it can be re-installed with the Monitor/Debugger BUF12 operating in the M68HC812 external memory (expanded mode).

# **Troubleshooting**

Checking to see if the PB68HC12A4 is functioning properly is very simple if the bootload firmware isn't erased or corrupted. An RS232 serial connection is required between the M68HC12 SCI0 port (J1 Header) and a PC or dumb terminal operating a serial COM port at 9600 baud, 8 data bits, 1 start, 1 stop, no parity.

- 1. Install J3 jumpers A and B to select M68HC12 Single Chip Mode.
- 2. Apply +5V DC to the PB68HC12A4 board (J1 pins 3 and 4).
- 3. Type characters on the PC operating a terminal program or dumb terminal keyboard.
- **4.** If the bootloader firmware is operating, typed characters will echo back to the screen. Do not type over 500 characters.