AT91RM9200-EK Evaluation Board

User Guide

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Section 1
Overview

1.1 Scope

The AT91RM9200-EK Evaluation Board enables real-time code development and evaluation. It supports the AT91RM9200 ARM9™-based 32-bit RISC microcontroller.

This guide focuses on the AT91RM9200-EK Evaluation Board as an evaluation and demonstration platform:

- Section 1 is this overview.
- Section 2 gives information on setting up the installation.
- Section 3 contains a description of the development board.
- Section 4 details the configuration straps.
- Section 5 shows board schematics.
- Section 6 contains errata.

1.2 Deliverables

The development kit is delivered with:

- One AC adapter 100 - 240V ~ 1.2A, 12V, 50 - 60 Hz with adapters
- One modem RS232 cable
- One RJ45 Ethernet crossed cable
- One A/B-type USB cable
- One AT91 DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.
- CD ROMs from third parties, providing solutions for operating system evaluation
- DataFlash® Cards to provide demonstrations of operating systems when inserted in the bootable slot

Note: To boot on a DataFlash Card:
- Ensure J15 (BMS) is set on position 1-2
- Insert the DataFlash Card in the J200 socket (bottom side)
- Reset the board

Further details are given on the AT91 DVD-ROM.

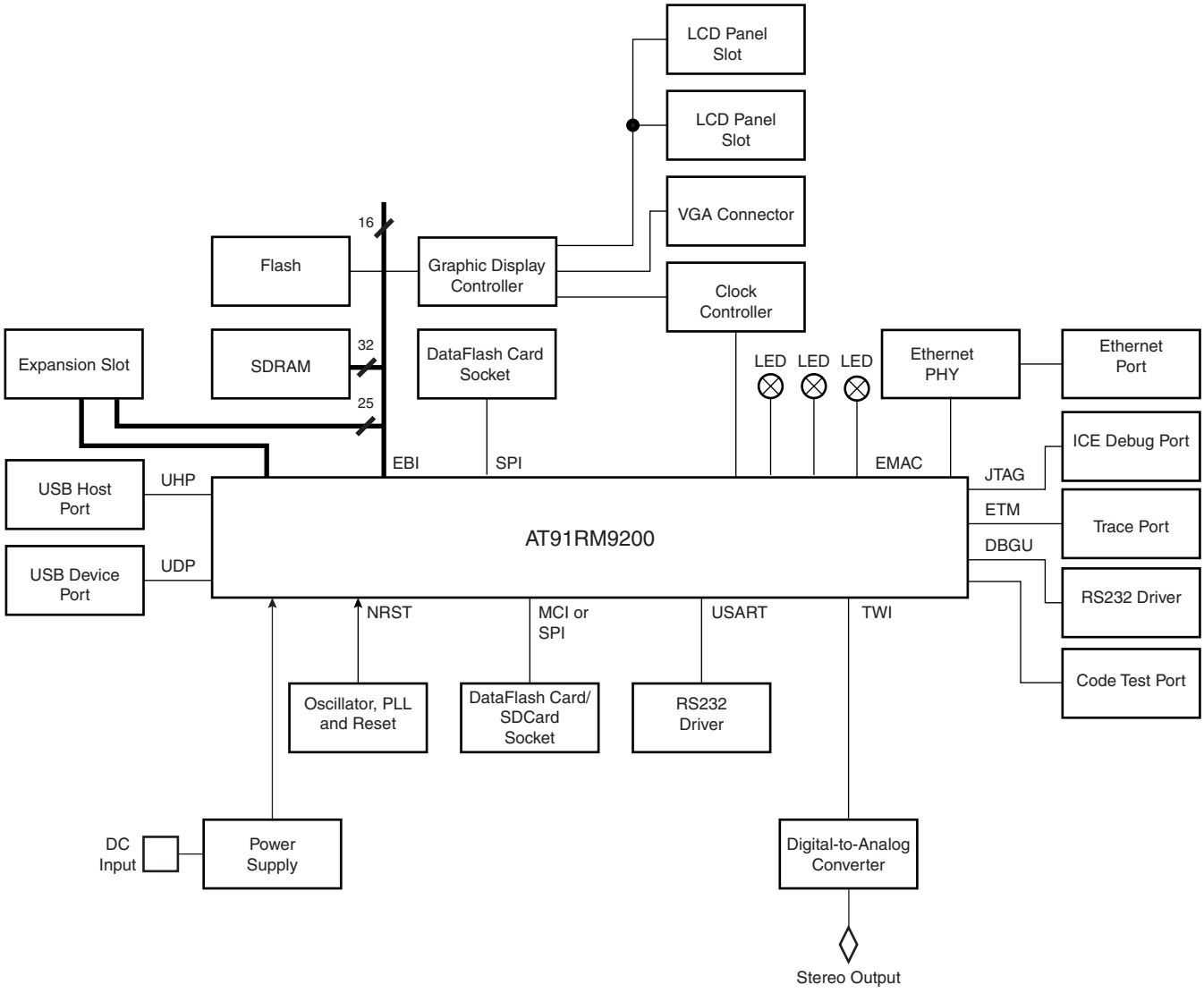
Note: These deliverables are subject to change without notice.

1.3 The AT91RM9200-EK Evaluation Board

The board consists of an AT91RM9200 together with the following:

- 8 Mbytes of parallel Flash memory
- Four banks of 2M x 32-bit SDRAM
- DataFlash® or SD/MMC memory expansion socket
- Additional DataFlash memory expansion socket
- Digital-to-Analog Converter (DAC) for a stereo audio signal
- Four communication ports (USB host and device, Ethernet, serial and DBGU)
- Graphic controller with output to a standard VGA monitor
- JTAG/ICE, ETM and code test port interface
- Expansion connector
- Onboard prototype area

Figure 1-1. AT91RM9200-EK Evaluation Board Block Diagram



Section 2

Setting Up the AT91RM9200-EK Evaluation Board

2.1 Electrostatic Warning

The AT91RM9200-EK Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to connect the AT91RM9200-EK Evaluation Board, the following element is required:

- The AT91RM9200-EK Evaluation Board itself

2.3 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1). The polarity of the power supply is not critical. The minimum voltage required is 7V.

The board has three voltage regulators providing 1.8V, 3.3V and 5V. The regulators allow the input voltage range to be from 7V to 12V.

2.4 Getting Started with the AT91RM9200

The AT91RM9200-EK Evaluation Board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/ for the most up-to-date information on getting started with the AT91RM9200.

Section 3

Board Description

3.1 AT91RM9200 Processor

- Incorporates the ARM920T™ ARM® Thumb® Processor
  - 200 MIPS at 180 MHz
  - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
  - Memory Management Unit
  - In-circuit Emulator including Debug Communication Channel
  - Mid-level Implementation Embedded Trace Macrocell™
- Additional Embedded Memories
  - 16K Bytes of SRAM and 128K Bytes of ROM
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia® and NAND Flash
- System Peripherals:
  - Enhanced Clock Generator and Power Management Controller
  - Two On-chip Oscillators with Two PLLs
  - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
  - System Timer Including Periodic Interrupt, Watchdog and Second Counter
  - Real-time Clock with Alarm Interrupt
  - Debug Unit, Two-wire UART and Support for Debug Communication Channel
  - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
  - Seven External Interrupt Sources and One Fast Interrupt Source
  - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
  - 20-channel Peripheral DMA Controller (PDC)
- Ethernet MAC 10/100 Base-T
- USB 2.0 Full Speed (12 M-bits per second) Host Double Port and Device Port

- MultiMedia Card Interface (MCI)
- Three Synchronous Serial Controllers (SSC)
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
- Master/Slave Serial Peripheral Interface (SPI)
- Two 3-channel, 16-bit Timer/Counters (TC)
- Two-wire Interface (TWI)
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins

3.2 Memory

- 8-Mbyte parallel Flash memory
- Four banks of 2M x 32-bit SDRAM

3.3 Memory Card

- SD Card/MMC
  - Supports MultiMedia and SD Card
  - Analog switches provide support for DataFlash® Card
- Additional DataFlash Card Socket

3.4 Clock Circuitry and Analog Functions

- 32.768 kHz standard crystal for the AT91RM9200
- 18.432 MHz standard crystal for the AT91RM9200
- 50 MHz CMOS oscillator for the Display Controller and Ethernet PHY

3.5 Reset Circuitry

- Reset Controller

3.6 Power Supply Circuitry

- 5V DC/DC converter
- 3.3V DC/DC converter
- 1.8V Linear regulator

3.7 Remote Communication

- Fast Ethernet Physical Layer Single Chip Transceiver
- Host Interface via RS-232 DB9 male socket
- Debug Port via RS-232 DB9 connector
- Host and Device USB socket

3.8 User Interface

- Graphic Display Controller
- TFT/SNT panel socket

- 15-pin standard socket for an external VGA monitor
- Three LEDs managed via general PIO lines
- Stereo Audio Jack connected to a DAC

3.9 Expansion Slot

- The expansion slot gives access to all the microcontroller's signals.

3.10 Debug Interface

- 38-pin trace Port socket (ETM)
- 38-pin Code Test port socket
- 20-pin JTAG ICE interface connector
- Serial Debug Unit

3.11 Wrapping User Area

- Onboard prototype area allowing the developer to fit additional components.

Section 4

Configuration Straps

4.1 Configuration Straps and Jumper Settings

Table 4-1 gives details on configuration straps and jumper settings on the AT91RM9200-EK Evaluation Board and their default settings.

Table 4-1. Configuration Straps and Jumper Settings

Designation	Default Setting	Feature
J13	Closed	Available for measuring VDDCORE current.
J15	1 - 2	The AT91RM9200 boots from internal ROM and can also boot from external SPI DataFlash® connected on NPCS0.
	2 - 3	The AT91RM9200 boots from Flash memory connected on NCS0.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Top View
- AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Bottom View
- Power Supply
- AT91RM9200 Chip
- Debug
- SDRAM and Flash
- RMII Ethernet
- Stereo Audio DAC
- Serial Interfaces
- VGA Display
- Expansion Connector

Figure 5-1. AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Top View

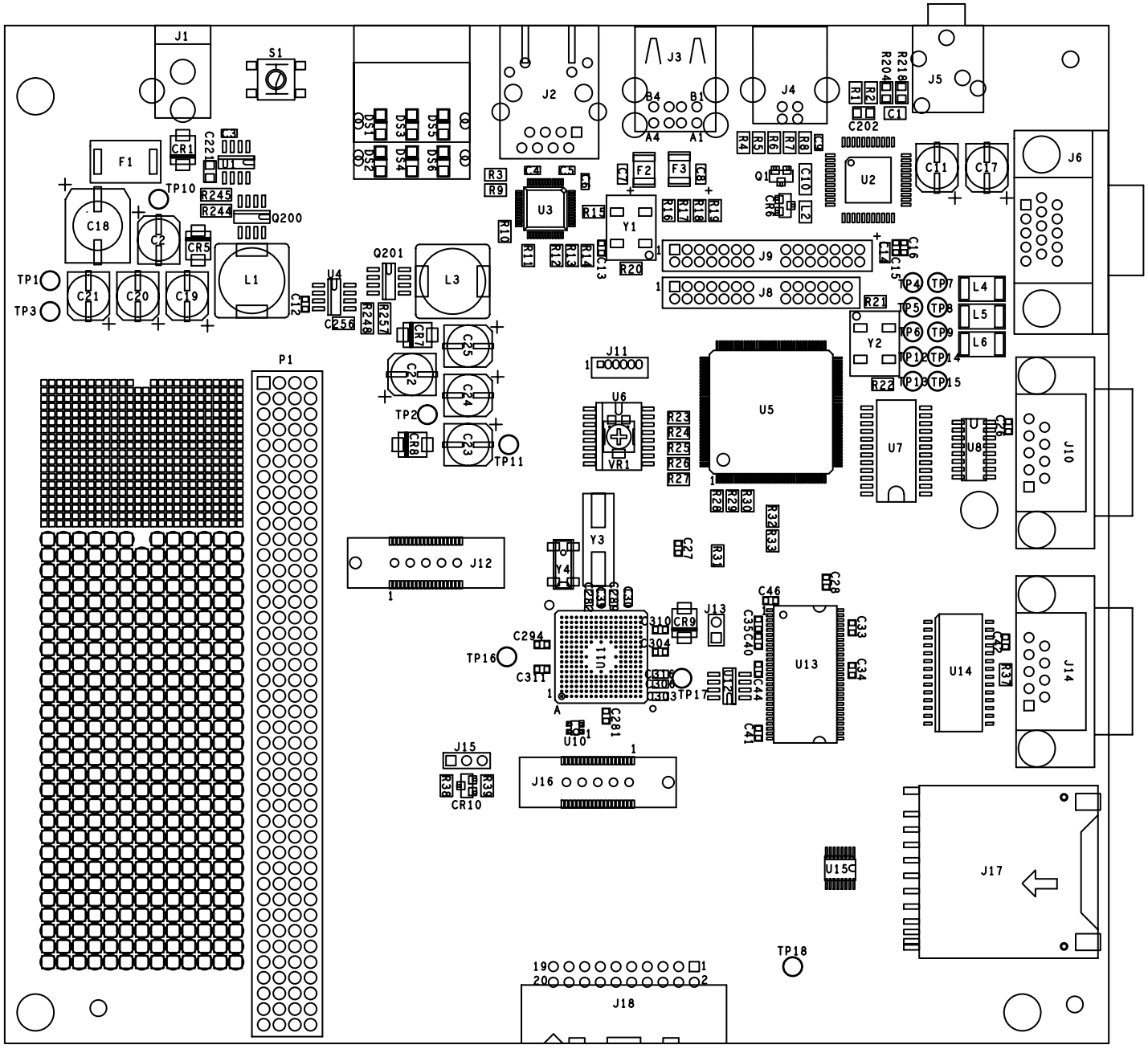
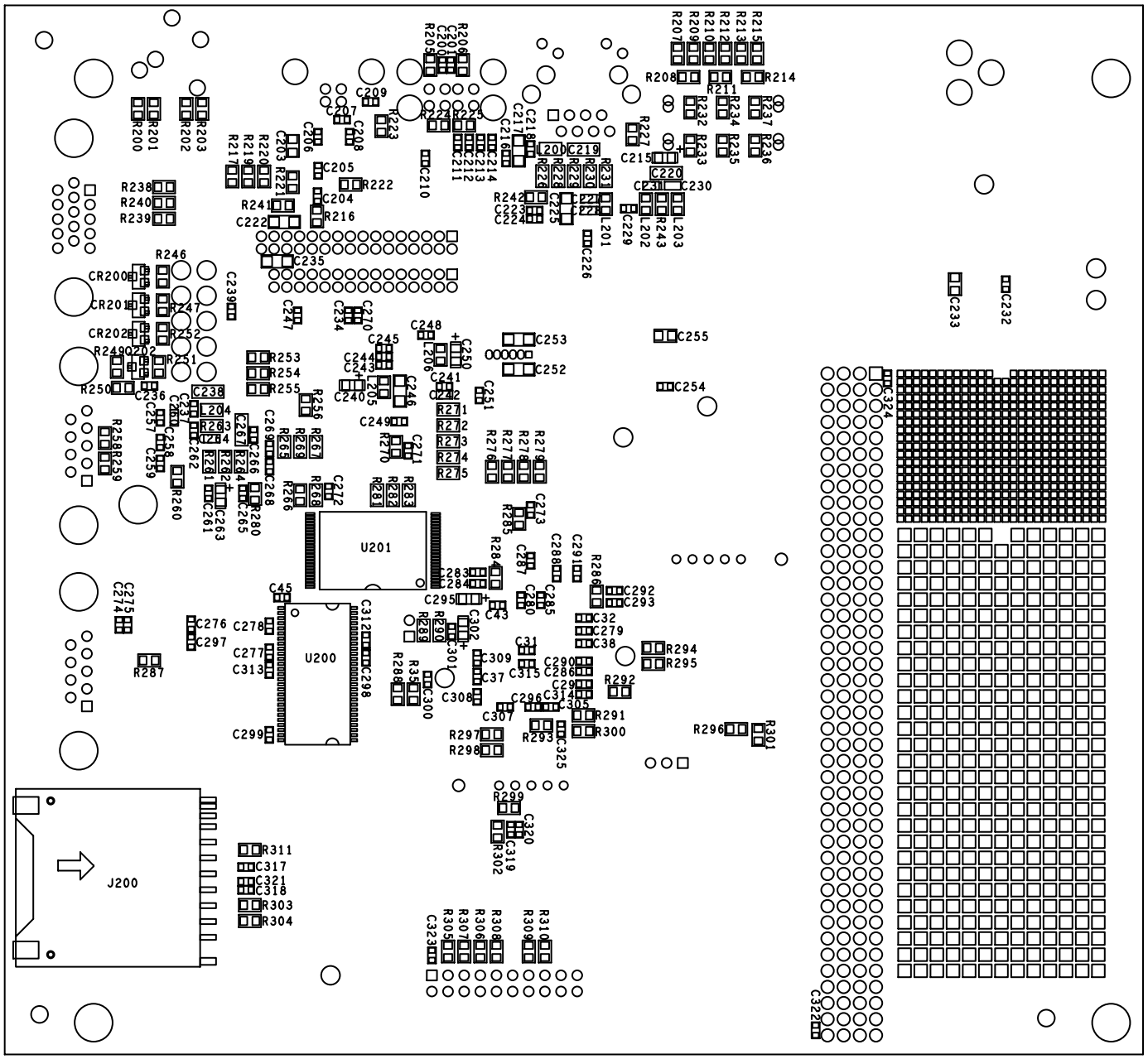


Figure 5-2. AT91RM9200-EK Board Layout, Rev. 63PC042262A01 - Bottom View



12V DC INPUT

J1
MP179_2.1mm

CR1
STPS340U

F1
2A

C18
470uF
25V

TP10

R248
0R100

R257
0R100

I limit = 0.1V / R ... about 2.9A

C256
2.2µF

C22
220uF
16V

U4
V+
SHDN
3/5
REF
GND
CS
EXT
OUT
MAX1626ESA

C12
100NF

Q201
IRF7425

L3
22uH
3.8A

CR7
STPS340U

3V3

TP11

C254
100NF

C25
220uF
16V

C24
220uF
16V

C255
2.2µF

C23
220uF
16V

CR8
3.3 V

1V8

TP17

U12
VIN
VIN
VOUT
VOUT
RES/PG
GND
EN
FB/NC
TPS77518D

C300
100NF

3V3

R35
1K
1%

NTRST

R288
4K7

R244
0R100

R245
0R100

I limit = 0.1V / R ... about 2.9A

C221
2.2µF

C2
220uF
16V

U1
V+
SHDN
3/5
REF
GND
CS
EXT
OUT
MAX1626ESA

C3
100NF

Q200
IRF7425

L1
22uH
3.8A

CR5
STPS340U

5V

TP3

C233
2.2µF

C232
100NF

C21
220uF
16V

C20
220uF
16V

C19
220uF
16V

Z3 - Z5 are mounting holes.
The Z reference designators
are not listed on the actual
board.

GUARD RING

Z4 TM
Z5 TM
Z3 TM
Z2 TM
Z1 TM

R227
0R

NORMALLY CLOSED

TP2
TP18
TP1
TP5

Z6 Z7 Z9 Z13
Z8 Z10
Z11
Z12

Wednesday, February 23, 2005

REV	MODIF.	DES.	DATE	VER.	DATE
B	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

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AT91RM9200-EK

POWER SUPPLY

SCALE 1/1

REV. A01

SHEET 1/9

63SC042261

AT91RM9200

U11

PB[0..29]
PA[0..31]
PD[0..27]
PC[0..15]
D[0..31]
A[0..25]

PD0 E17 PD0/ETX0
PD1 E15 PD1/ETX1
PD2 E14 PD2/ETX2
PD3 E16 PD3/ETX3
PD4 D17 PD4/ETXEN
PD5 C17 PD5/ETXER
PD6 D16 PD6/DTXD
PD7 D6 PD7/PCK0/TSYNC
PD8 A6 PD8/PCK1/TCLK
PD9 B6 PD9/PCK2/TPS0
PD10 C6 PD10/PCK3/TPS1
PD11 A5 PD11/TPS2
PD12 B5 PD12/TPK0
PD13 B2 PD13/TPK1
PD14 C3 PD14/TPK2
PD15 C2 PD15/TD0/TPK3
PD16 F1 PD16/TD1/TPK4
PD17 G2 PD17/TD2/TPK5
PD18 G5 PD18/NPCS1/TPK6
PD19 G1 PD19/NPCS2/TPK7
PD20 H2 PD20/NPCS3/TPK8
PD21 H4 PD21/RTS0/TPK9
PD22 H3 PD22/RTS1/TPK10
PD23 H1 PD23/RTS2/TPK11
PD24 J3 PD24/RTS3/TPK12
PD25 J1 PD25/DTR1/TPK13
PD26 J4 PD26/TPK14
PD27 J2 PD27/TPK15

DDP K5 DDP
DDM K2 DDM

HDPA K1 HDPA
HDMA K3 HDMA

HDPB L2 HDPB
HDMB L3 HDMB

TDI A1 TDI
TMS C1 TMS
TCK E5 TCK

TDO B1 TDO
NTRST E2 NTRST
A2 JTAGSEL

R292 0R

VDDPLL H13 VDDPLLB
C31 100NF
H15 GNDPLLB

C292 4.7NF
R286 1K96 1%
E17 PLLRCB
C293 470pF

C273 10PF
R285 0R
K17 XOUT
Y3 18.4320MHz
C287 10PF
J17 XIN

VDDOSC C280 100NF
J14 VDDOSC
J13 GNDOSC

C288 10PF
H17 XOUT32
Y4 32.768 kHz
C291 10PF
G17 XIN32

VDDPLL C285 100NF
J15 VDDPLLA
J16 GNDPLLA

C283 5.6NF
R284 1K27 1%
L17 PLLRCA
C284 680PF

1V8
J13
CR9 STPS1L30U
C302 10 uF 10V
C301 100NF
R290 0R VDDOSC
R289 0R VDDPLL

VDDCORE L16 C289 100NF
VDDCORE C14 C279 100NF
VDDCORE F6 C286 100NF
VDDCORE U1 C308 100NF
VDDCORE T2 C303 100NF
VDDCORE T10 C309 100NF

GND M12 P17 M16 J12 H16 C15 A14 C11 D11 B7 E8 E6 D4 E3 F2 G3 L1 L5 M2 R1 U2 R2 M7 U5 T9 N12 T13

VDDIOM P16 C30 100NF
VDDIOM R17 C43 100NF
VDDIOM K16 C39 100NF
VDDIOM M1 C307 100NF
VDDIOM P4 C306 100NF
VDDIOM R6 C37 100NF
VDDIOM T5 C316 100NF
VDDIOM R10 C304 100NF
VDDIOM R14 C310 100NF
VDDIOM H14 C282 100NF
VDDIOP A16 C32 100NF
VDDIOP A11 C294 100NF
VDDIOP B11 C38 100NF
VDDIOP D8 C290 100NF
VDDIOP A7 C311 100NF
VDDIOP D5 C29 100NF
VDDIOP D2 C305 100NF
VDDIOP D3 C314 100NF
VDDIOP H5 C315 100NF
VDDIOP K4 C281 100NF
VDDIOP L6 C296 100NF
3V3
C295 10 uF 10V

PA31 A10 RTS2/DTXD/PA31
PA30 E11 CTS2/DRXD/PA30
PA29 E11 TCLK5/MCDA0/PA29
PA28 E12 TCLK4/MCCDA/PA28
PA27 G12 TCLK3/MCCK/PA27
PA26 E12 IRQ1/TWCK/PA26
PA25 E13 IRQ2/TWD/PA25
PA24 B12 PCK1/SCK2/PA24
PA23 A12 IRQ3/TXD2/PA23
PA22 D12 TIOB2/RXD2/PA22
PA21 D13 TIOA2/RTS0/PA21
PA20 C12 TIOB1/CTS0/PA20
PA19 A13 TIOA1/SCK0/PA19
PA18 C13 TIOB0/RXD0/PA18
PA17 B13 TIOA0/TXD0/PA17
PA16 D14 IRQ6/EMDIO/PA16
PA15 B14 TCLK2/EMDC/PA15
PA14 A15 TCLK1/ERXER/PA14
PA13 A17 TCLK0/ERX1/PA13
PA12 B16 MCDB3/ERX0/PA12
PA11 B15 MCDB2/ERXDV/PA11
PA10 D15 MCDB1/ETX1/PA10
PA9 E14 MCDB0/ETX0/PA9
PA8 C16 MCCDB/ETXEN/PA8
PA7 B17 EXTCK/PCK2/PA7
PA6 E15 RXD3/NPCS3/PA6
PA5 E16 TXD3/NPCS2/PA5
PA4 F13 PCK1/NPCS1/PA4
PA3 G16 IRQ5/NPCS0/PA3
PA2 G15 IRQ4/SPCK/PA2
PA1 G14 PCK0/MOSI/PA1
PA0 G13 PCK3/MISO/PA0

PB29 J6 IRQ0/PB29
PB28 J5 FIQ/PB28
PB27 G6 PCK0/PB27
PB26 G4 RTS1/PB26
PB25 E4 EF100/DSR1/PB25
PB24 E5 CTS1/PB24
PB23 F3 DCD1/PB23
PB22 C4 SCK1/PB22
PB21 B4 RXD1/PB21
PB20 A3 TXD1/PB20
PB19 C5 RXCK/DTR1/PB19
PB18 B3 ECOL/RI1/PB18
PB17 A4 ERXDV/RF2/PB17
PB16 F7 ERX3/RK2/PB16
PB15 E7 ERX2/RD2/PB15
PB14 D7 ETXER/TD2/PB14
PB13 C7 ETX3/TK2/PB13
PB12 C8 ETX2/TF2/PB12
PB11 F9 TIOB5/RF1/PB11
PB10 B8 TIOA5/RK1/PB10
PB9 A8 TIOB4/RD1/PB9
PB8 D9 TIOA4/TD1/PB8
PB7 E9 TIOB3/TK1/PB7
PB6 C9 TIOA3/TF1/PB6
PB5 B9 MCDA3/RF0/PB5
PB4 A9 MCDA2/RK0/PB4
PB3 E10 MCDA1/RD0/PB3
PB2 D10 SCK3/TD0/PB2
PB1 C10 CTS3/TK0/PB1
PB0 B10 RTS3/TF0/PB0

PC15 L13 HOLDA/PC15
PC14 M17 HOLD/PC14
PC13 M13 NCS7/PC13
PC12 N17 CFCE2/NCS6/PC12
PC11 N16 CFCE1/NCS5/PC11
PC10 L12 CFCS/NCS4/PC10
PC6 K15 NWAIT/PC6
PC5 K13 BFWE/PC5
PC4 K14 BFOE/PC4
PC3 L15 SMWE/BFBAA/PC3
PC2 L14 BFAVD/PC2
PC1 M14 SMOE/BFRDY/PC1
PC0 M15 BFCK/PC0

D0 R9 D0
D1 P10 D1
D2 N11 D2
D3 U9 D3
D4 M11 D4
D5 P11 D5
D6 U10 D6
D7 U11 D7
D8 R11 D8
D9 T11 D9
D10 P12 D10
D11 U12 D11
D12 T12 D12
D13 R12 D13
D14 U13 D14
D15 P13 D15
PC16/D16 U14 D16
PC17/D17 R13 D17
PC18/D18 U15 D18
PC19/D19 T14 D19
PC20/D20 U16 D20
PC21/D21 T15 D21
PC22/D22 U17 D22
PC23/D23 T16 D23
PC24/D24 R15 D24
PC25/D25 T17 D25
PC26/D26 P14 D26
PC27/D27 P15 D27
PC28/D28 N13 D28
PC29/D29 R16 D29
PC30/D30 N15 D30
PC31/D31 N14 D31

NBS0/A0 N1 A0
NWR2/NBS2/A1 M4 A1
A2 M6 A2
A3 M3 A3
A4 N4 A4
A5 N2 A5
A6 L4 A6
A7 P1 A7
A8 N7 A8
A9 N3 A9
A10 M5 A10
A11 P5 A11
A12 P3 A12
A13 P2 A13
A14 N5 A14
A15 T1 A15
BA0/A16 U3 A16
BA1/A17 T3 A17
A18 R3 A18
A19 U4 A19
A20 R4 A20
A21 N8 A21
A22 P6 A22
PC7/A23 T4 A23
PC8/A24 R5 A24
CFRNW/PC9/A25 P7 A25

RAS N10 RAS
CAS U8 CAS

SDWE T8 SDWE
SDA10 N6 SDA10
SDCKE P9 SDCKE
SDCK U7 SDCK

BFCS/NCS0 U6 BFCS_NCS0
SDCS/NCS1 M9 SDCS
NCS2 T6 NCS2
SMCS/NCS3 R7 SMCS_NCS3
CFOE/NOE/NRD N9 CFOE_NOE_NRD

CFWE/NWE/NWR0 P8 CFWE_NWE_NWR0
CFIOR/NBS1/NWR1 T7 CFIOR_NBS1_NWR1
CFIOW/NBS3/NWR3 R8 CFIOW_NBS3_NWR3

NRST E1
TST1 D1 R300 1K 1%
TST0 E4 1K 1% R291

3V3
R38 47K
PA31 2 J15
R39 470R
CR10 BAT54-7 3 NRST

BOOT MODE SELECT
1-2: BMS=Hight=Internal Boot
1-3: BMS=Low=External Boot from NCS0

C325 100NF
U10 GND VCC RESET MR MAX6390XS29D4-T
RESET
S1
R293 1K 1%

Monday, March 21, 2005

REV					
A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05
REV	MODIF.	DES.	DATE	VER.	DATE

AT91RM9200-EK
AT91RM9200
SCALE 1/1
REV. A01
63SC042261
SHEET 2/9

D[0..31]

D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

A[0..25]

A1
A2
A3
A4

PD[0..27]

PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
PD16
PD17
PD18
PD19
PD20
PD21
PD22
PD23
PD24
PD25
PD26
PD27

PC[0..15]

PC13

R294
0R

CODETEST PORT

J12

D0	38	37	D16
D1	36	35	D17
D2	34	33	D18
D3	32	31	D19
D4	30	29	D20
D5	28	27	D21
D6	26	25	D22
D7	24	23	D23
D8	22	21	D24
D9	20	19	D25
D10	18	17	D26
D11	16	15	D27
D12	14	13	D28
D13	12	11	D29
D14	10	9	D30
D15	8	7	D31
NCS7	6	5	CT_CLK
A1	4	3	A2
A3	2	1	A4

G1 G2 G3 G4 G5

CT_CLK — R295 0R — PD8

3V3
10K
R309
10K
R305 R306 R307 R308

J18

C323
100NF

NTRST
TDI
TMS
TCK
TDO
NRST

R310
0R

ICE INTERFACE

ETM TRACE PORT

J16

PD9	PIPESTAT[0]	38	37	TRACEPKT[8]	PD20
PD10	PIPESTAT[1]	36	35	TRACEPKT[9]	PD21
PD11	PIPESTAT[2]	34	33	TRACEPKT[10]	PD22
PD7	TRACESYNC	32	31	TRACEPKT[11]	PD23
PD12	TRACEPKT[0]	30	29	TRACEPKT[12]	PD24
PD13	TRACEPKT[1]	28	27	TRACEPKT[13]	PD25
PD14	TRACEPKT[2]	26	25	TRACEPKT[14]	PD26
PD15	TRACEPKT[3]	24	23	TRACEPKT[15]	PD27
PD16	TRACEPKT[4]	22	21	NTRST	
PD17	TRACEPKT[5]	20	19	TDI	
PD18	TRACEPKT[6]	18	17	TMS	
PD19	TRACEPKT[7]	16	15	TCK	
	VSUPPLY	14	13		
	EXTTRIG	12	11	TDO	
	TRACECLK	10	9	NSRST	
		8	7	DBGRQ	
		6	5	GND	
		4	3		
		2	1		

G1 G2 G3 G4 G5

3V3
R302
10K

3V3

PD8 R299 0R

C320
100NF

C319
100NF

SYSTEM RESET

R297 0R NRST

R298
10K

Monday, March 21, 2005

ATMEL ROUSSET

AT91RM9200-EK

ETM - ICE - TEST

REV	MODIF.	DES.	DATE	VER.	DATE
A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

SCALE 1/1

REV. A01

63SC042261

SHEET 3/9

EBI SDRAM INTERFACE

A[0..25]
D[0..31]
RAS
CAS
SDWE
SDA10
SDCKE
SDCK
CFIOR_NBS1_NWR1
CFIOW_NBS3_NWR3
SDCS

U13 — MT48LC8M16A2 — 128 Mbits

A2	23	A0	
A3	24	A1	
A4	25	A2	
A5	26	A3	
A6	29	A4	
A7	30	A5	
A8	31	A6	
A9	32	A7	
A10	33	A8	
A11	34	A9	
SDA10	22	A10	
A13	35	A11	
A16	BA0	20	BA0
A17	BA1	21	BA1
A14	36	N.C	
	40	N.C	
SDCKE	37	CKE	
SDCK	38	CLK	
A0	NBS0	15	DQML
CFIOR_NBS1_NWR1		39	DQMH
CAS	17	CAS	
RAS	18	RAS	
SDWE	16	WE	
	19	CS	

DQ0	2	D0	
DQ1	4	D1	
DQ2	5	D2	
DQ3	7	D3	
DQ4	8	D4	
DQ5	10	D5	
DQ6	11	D6	
DQ7	13	D7	
DQ8	42	D8	
DQ9	44	D9	
DQ10	45	D10	
DQ11	47	D11	
DQ12	48	D12	
DQ13	50	D13	
DQ14	51	D14	
DQ15	53	D15	
VDD	1	3V3	
VDD	14		
VDD	27		
VDDQ	3		
VDDQ	9		
VDDQ	43		
VDDQ	49		
VSS	28		
VSS	41		
VSS	54		
VSSQ	6		
VSSQ	12		
VSSQ	46		
VSSQ	52		

C40 100NF, C35 100NF, C41 100NF, C44 100NF, C46 100NF, C33 100NF, C34 100NF

U200 — MT48LC8M16A2 — 128 Mbits

A2	23	A0	
A3	24	A1	
A4	25	A2	
A5	26	A3	
A6	29	A4	
A7	30	A5	
A8	31	A6	
A9	32	A7	
A10	33	A8	
A11	34	A9	
SDA10	22	A10	
A13	35	A11	
A16	BA0	20	BA0
A17	BA1	21	BA1
A14	36	N.C	
	40	N.C	
SDCKE	37	CKE	
SDCK	38	CLK	
A1	NBS2	15	DQML
CFIOW_NBS3_NWR3		39	DQMH
CAS	17	CAS	
RAS	18	RAS	
SDWE	16	WE	
	19	CS	

DQ0	2	D16	
DQ1	4	D17	
DQ2	5	D18	
DQ3	7	D19	
DQ4	8	D20	
DQ5	10	D21	
DQ6	11	D22	
DQ7	13	D23	
DQ8	42	D24	
DQ9	44	D25	
DQ10	45	D26	
DQ11	47	D27	
DQ12	48	D28	
DQ13	50	D29	
DQ14	51	D30	
DQ15	53	D31	
VDD	1	3V3	
VDD	14		
VDD	27		
VDDQ	3		
VDDQ	9		
VDDQ	43		
VDDQ	49		
VSS	28		
VSS	41		
VSS	54		
VSSQ	6		
VSSQ	12		
VSSQ	46		
VSSQ	52		

C277 100NF, C278 100NF, C299 100NF, C313 100NF, C45 100NF, C312 100NF, C298 100NF

D[0..31]
A[0..25]

U201 — AT49BV6416-70TI

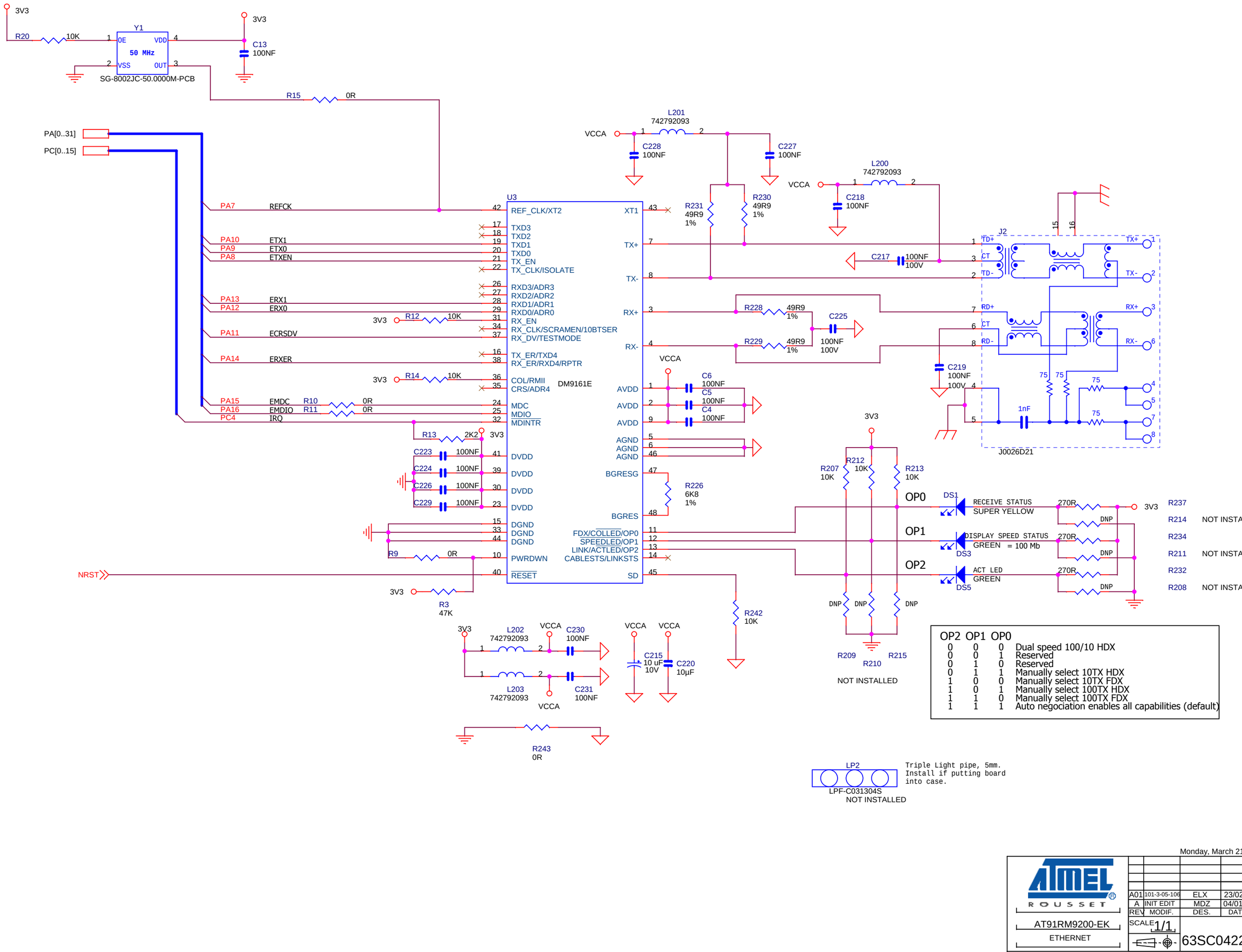
A1	25	A0	
A2	24	A1	
A3	23	A2	
A4	22	A3	
A5	21	A4	
A6	20	A5	
A7	19	A6	
A8	18	A7	
A9	8	A8	
A10	7	A9	
A11	6	A10	
A12	5	A11	
A13	4	A12	
A14	3	A13	
A15	2	A14	
A16	1	A15	
A17	48	A16	
A18	17	A17	
A19	16	A18	
A20	15	A19	
A21	10	A20	
A22	9	A21	
NRST	12	RESET	
CFWE_NWE_NWR0	11	WE	
3V3	13	VPP	
3V3	14	WP	
BFCS_NCS0	26	CE	
CFOE_NOE_NRD	28	OE	
	47	VCCQ	
	37	VCC	
	46	GND	
	27	GND	

3V3, R32 47K, R33 0R, R31 10K, C28 100NF, C27 100NF

Monday, March 21, 2005

REV	MODIF.	DES.	DATE	VER.	DATE
A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05

AT91RM9200-EK
SDRAM & FLASH
SCALE 1/1
63SC042261**A01**
REV.
SHEET 4/9


3V3
R20
10K
Y1
OE
VDD
50 MHz
VSS
OUT
SG-8002JC-50.0000M-PCB
C13
100NF
R15
0R
PA[0..31]
PC[0..15]
U3
REF_CLK/XT2
TXD3
TXD2
TXD1
TXD0
TX_EN
TX_CLK/ISOLATE
RXD3/ADR3
RXD2/ADR2
RXD1/ADR1
RXD0/ADR0
RX_EN
RX_CLK/SCRAMEN/10BTSER
RX_DV/TESTMODE
TX_ER/TXD4
RX_ER/RXD4/RPTR
COL/RMII
CRS/ADR4
DM9161E
MDC
MDIO
MDINTR
DVDD
DGND
PWRDWN
RESET
XT1
TX+
TX-
RX+
RX-
AVDD
AGND
BGRESG
BGRES
FDX/COLLED/OP0
SPEEDLED/OP1
LINK/ACTLED/OP2
CABLESTS/LINKSTS
SD
PA7
REFCK
PA10
ETX1
PA9
ETX0
PA8
ETXEN
PA13
ERX1
PA12
ERX0
PA11
ECRSDV
PA14
ERXER
PA15
EMDC
PA16
EMDIO
PC4
IRQ
R10
R11
R12
R13
2K2
R14
R9
R3
47K
NRST
C223
C224
C226
C229
C6
C5
C4
R226
6K8
1%
R242
10K
L201
742792093
L200
742792093
L202
742792093
L203
742792093
C228
C227
C218
C230
C231
C215
10 uF
10V
C220
10µF
R243
0R
R231
R230
R228
R229
C225
C217
C219
J2
TD+
CT
TD-
RD+
RD-
J0026D21
1nF
75
R207
R212
R213
R209
R210
R215
OP0
OP1
OP2
DS1
DS3
DS5
RECEIVE STATUS
SUPER YELLOW
DISPLAY SPEED STATUS
GREEN = 100 Mb
ACT LED
GREEN
270R
DNP
R237
R214
R234
R211
R232
R208
NOT INSTALLED
OP2 OP1 OP0
0 0 0 Dual speed 100/10 HDX
0 0 1 Reserved
0 1 0 Reserved
0 1 1 Manually select 10TX HDX
1 0 0 Manually select 10TX FDX
1 0 1 Manually select 100TX HDX
1 1 0 Manually select 100TX FDX
1 1 1 Auto negociation enables all capabilities (default)
LP2
LPF-C031304S
Triple Light pipe, 5mm.
Install if putting board
into case.
Monday, March 21, 2005
ATMEL ROUSSET
AT91RM9200-EK
ETHERNET
A01 101-3-05-106 ELX 23/02/05 JPG 23/02/05
A INIT EDIT MDZ 04/01/05 JPG 06/01/05
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
63SC042261 A01
SHEET 5/9
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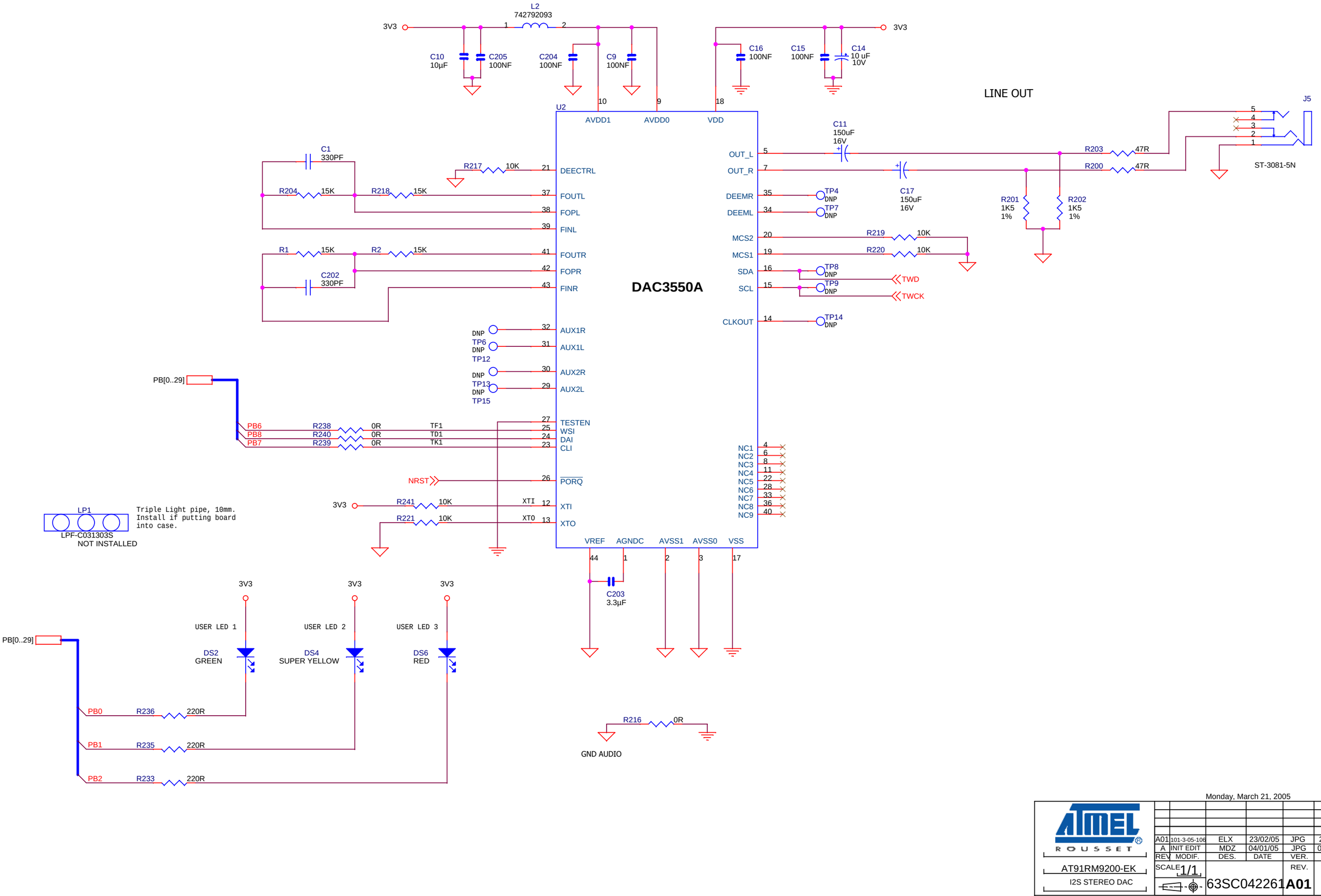


Monday, March 21, 2005

A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05
REV	MODIF.	DES.	DATE	VER.	DATE

ATMEL ROUSSET

AT91RM9200-EK

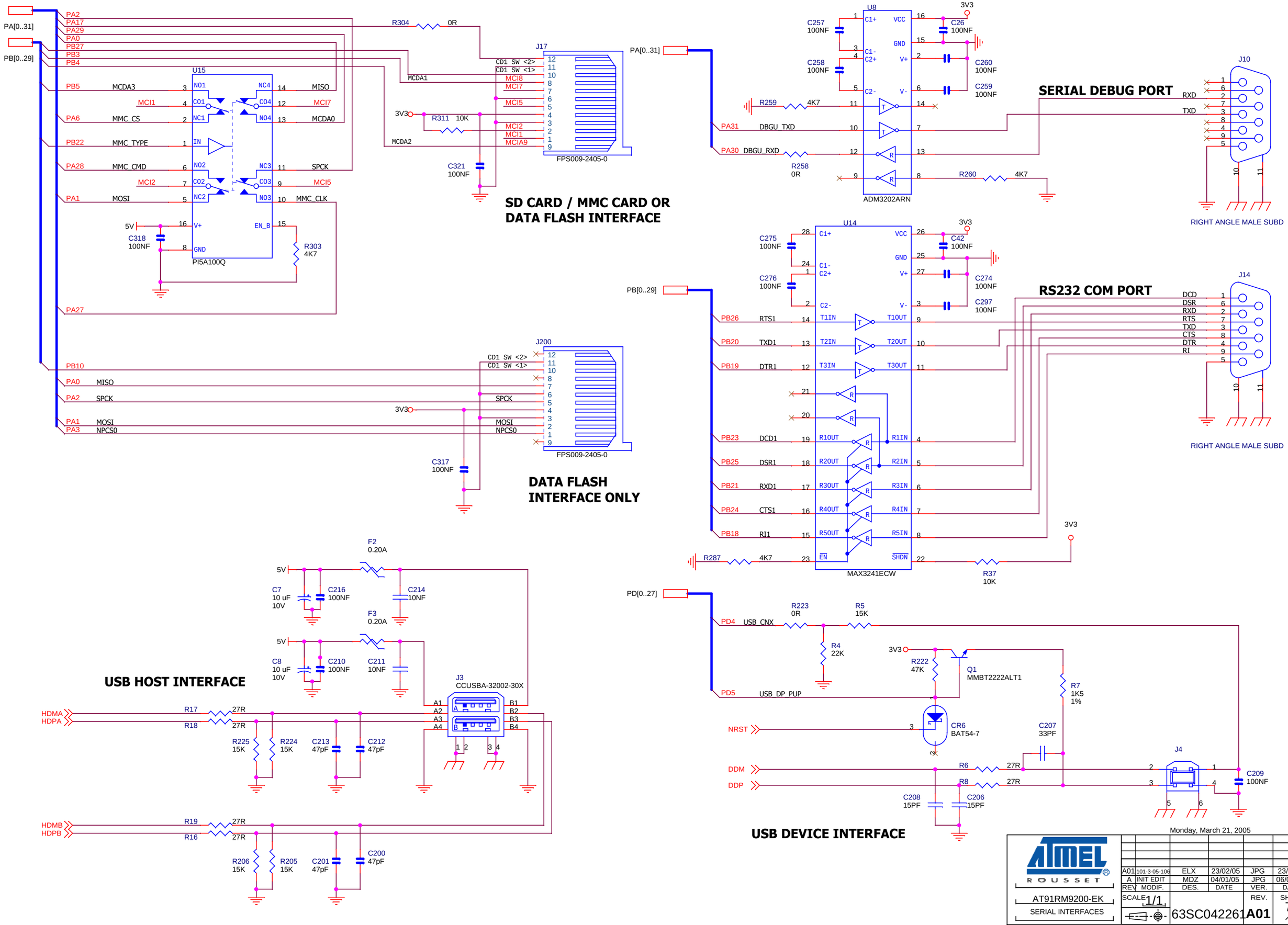
I2S STEREO DAC

SCALE 1/1

REV. A01

63SC042261

SHEET 6/9


SD CARD / MMC CARD OR
DATA FLASH INTERFACE
DATA FLASH
INTERFACE ONLY
SERIAL DEBUG PORT
RS232 COM PORT
USB HOST INTERFACE
USB DEVICE INTERFACE
RIGHT ANGLE MALE SUBD
RIGHT ANGLE MALE SUBD
ADM3202ARN
MAX3241ECW
FPS009-2405-0
FPS009-2405-0
PI5A100Q
CCUSBA-32002-30X
MMBT2222ALT1
BAT54-7
PA[0..31]
PB[0..29]
PD[0..27]
3V3
5V
MCDA1
MCDA2
MCDA3
MMC_CS
MMC_TYPE
MMC_CMD
MMC_CLK
MISO
SPCK
MOSI
NPCS0
DBGU_TXD
DBGU_RXD
RTS1
TXD1
DTR1
DCD1
DSR1
RXD1
CTS1
RI1
USB_CNX
USB_DP_PUP
HDMA
HDPA
HDMB
HDPB
NRST
DDM
DDP
Monday, March 21, 2005
AT91RM9200-EK
SERIAL INTERFACES
63SC042261A01
7/9

S1D13806
DISPLAY CONTROLLER

U5

LUMINANCE 20% ..100%

Generic Little Indian
(Default)

4.6mA

ICS1523

SG-8002JC-50.0000M-PCB

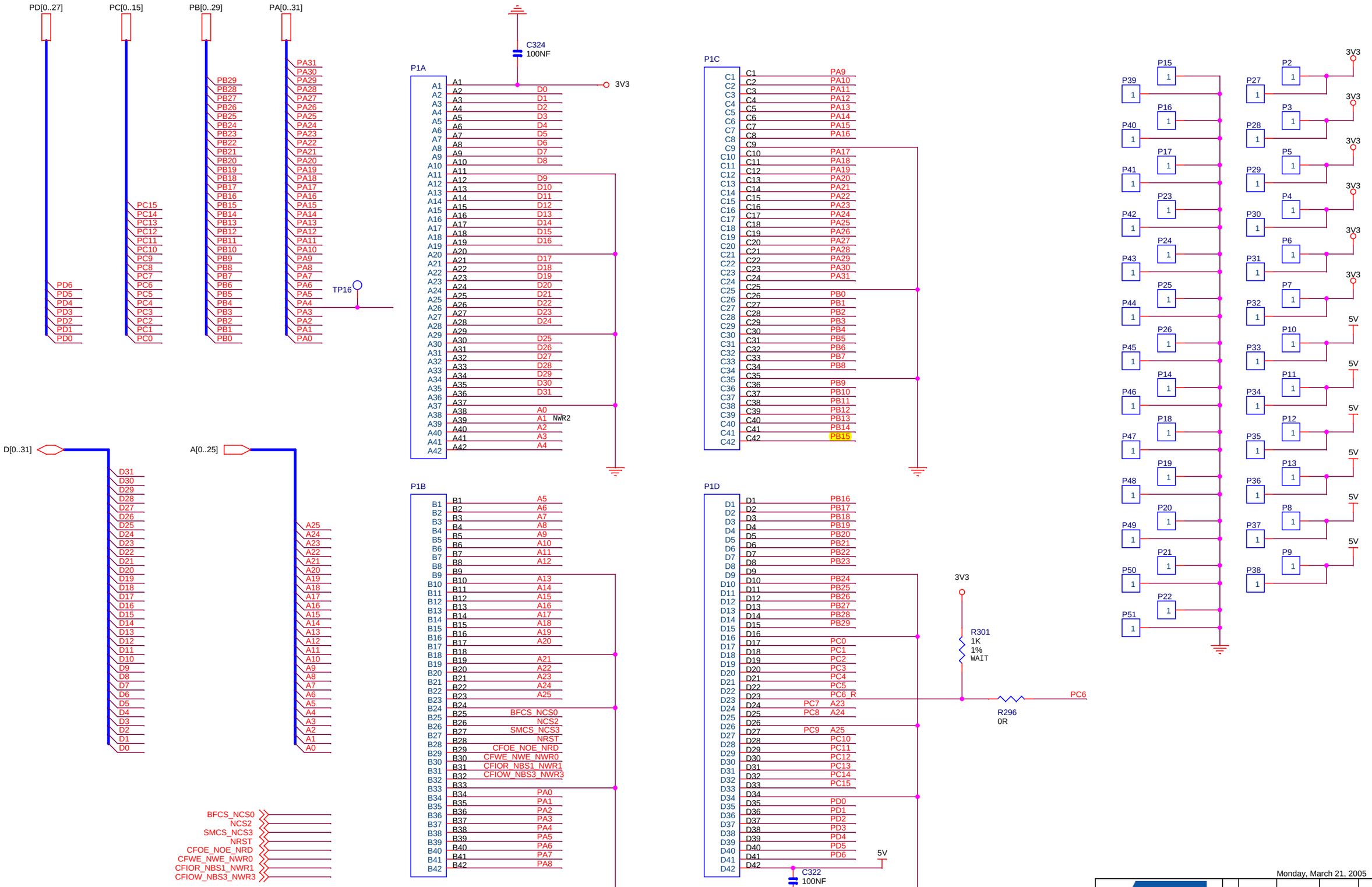
Monday, March 21, 2005

A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05
REV	MODIF.	DES.	DATE	VER.	DATE

AT91RM9200-EK
VGA TFT/CRT DISPLAY

SCALE 1/1 | REV. | SHEET

63SC042261 **A01** | 8/9



Monday, March 21, 2005

A01	101-3-05-106	ELX	23/02/05	JPG	23/02/05
A	INIT EDIT	MDZ	04/01/05	JPG	06/01/05
REV	MODIF.	DES.	DATE	VER.	DATE

AT91RM9200-EK

EXPANSION CONNECTORS

SCALE 1/1

63SC042261

REV. A01

SHEET 9/9

Section 6

Errata

6.1 Errata

6.1.1 SD/MMC Card Slot Communication Problem

On the AT91RM9200-EK Board, revision 700-20226 REV X5, a communication problem may occur on the SD/MMC interface.

This issue has been corrected on all boards of revision 63PC042262A by adding a 10 kOhm pull-up resistor between the pin connectors J17-2 and J17-4.

Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6103A	24-Sep-04	First issue.	
6103B	02-Mar-05 19-Jul-05	Section 1.2, “Deliverables” on page 2; List simplified Table 4-1, Boot information modified New schematics added in Section 5.	CSR 04-361, CSR 05-028, CSR 05-246
6103C	07-Nov-05	Added Section 6, Errata.	CSR 05-478

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Fax: (33) 2-40-18-19-60

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Zone Industrielle
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6103C–ATARM–05-Jan-06