# 2015年计算机组成研讨班

## 多周期CPU形式建模综合方法

# 多周期控制器

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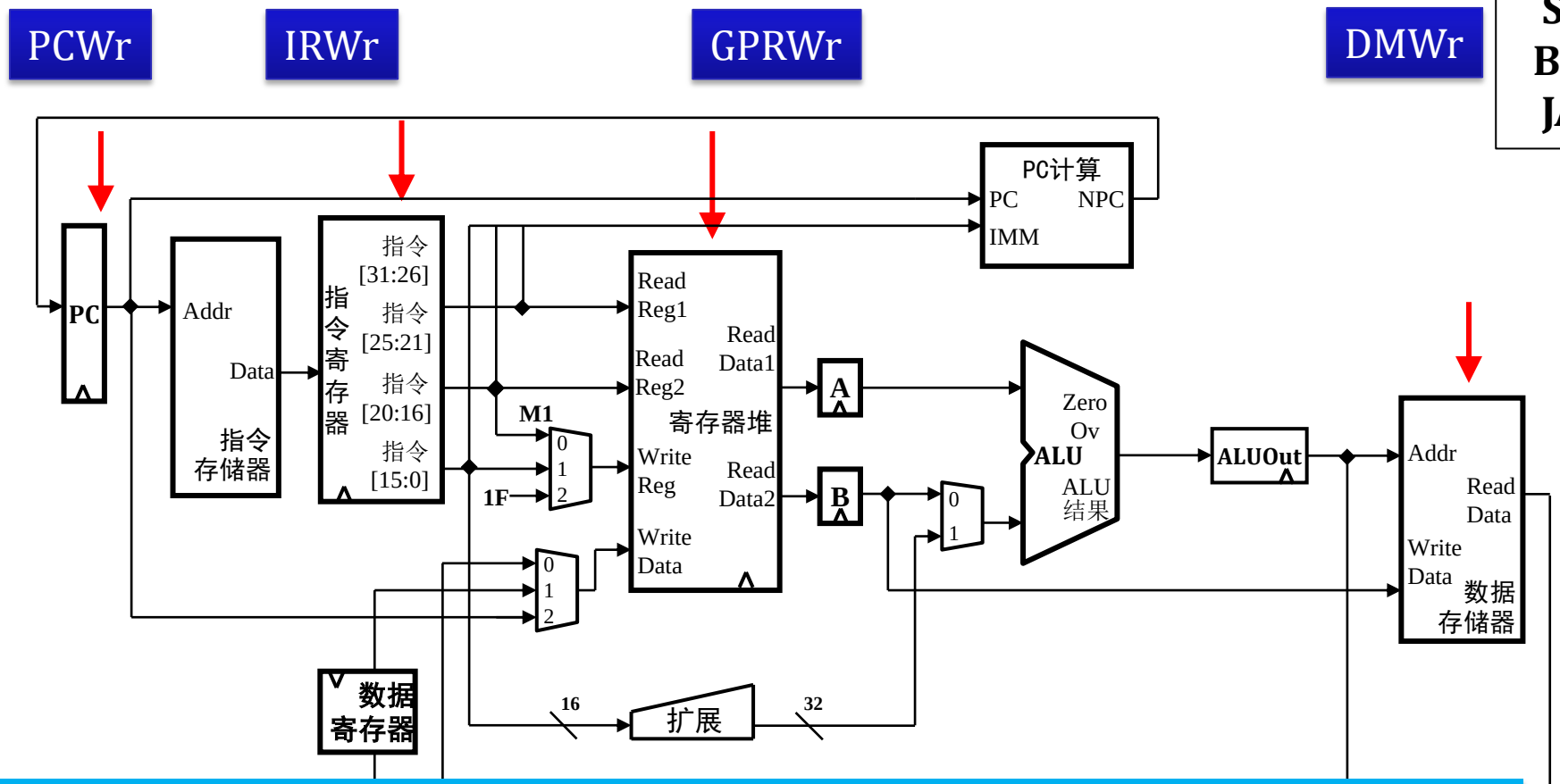
北京航空航天大学计算机学院
2015年7月

# 提纲

- 内容主要取材
  - 数字设计和计算机体系结构（第3章，第7章）
- 多周期数据通路控制信号分析
- 多周期控制器状态机构造
- 多周期性能分析

# 多周期数据通路控制信号：寄存器写使能

LW
ADDU
SUBU
ORI
LUI
SW
BEQ
JAL

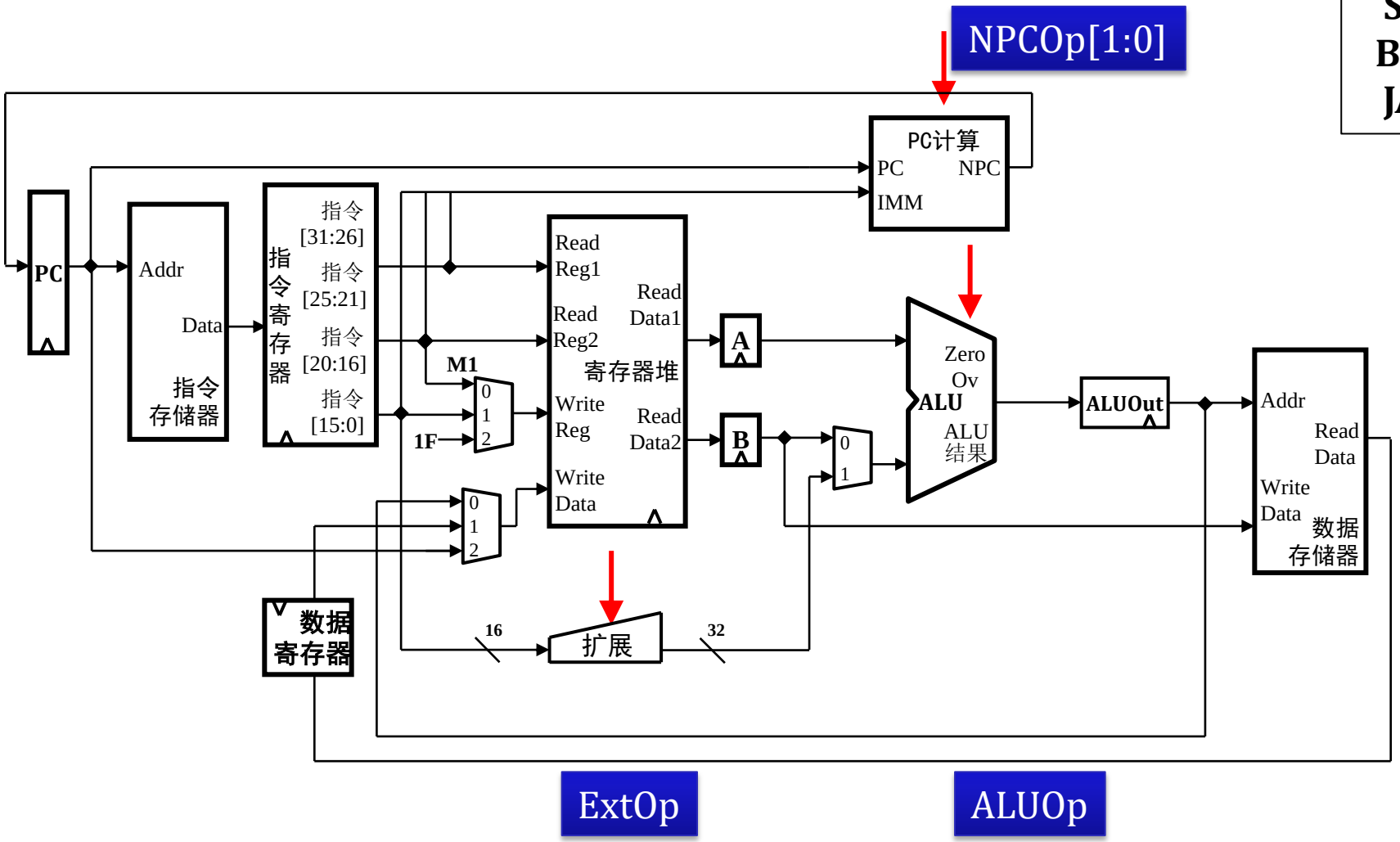



写使能信号

1：允许写入；0：禁止写入

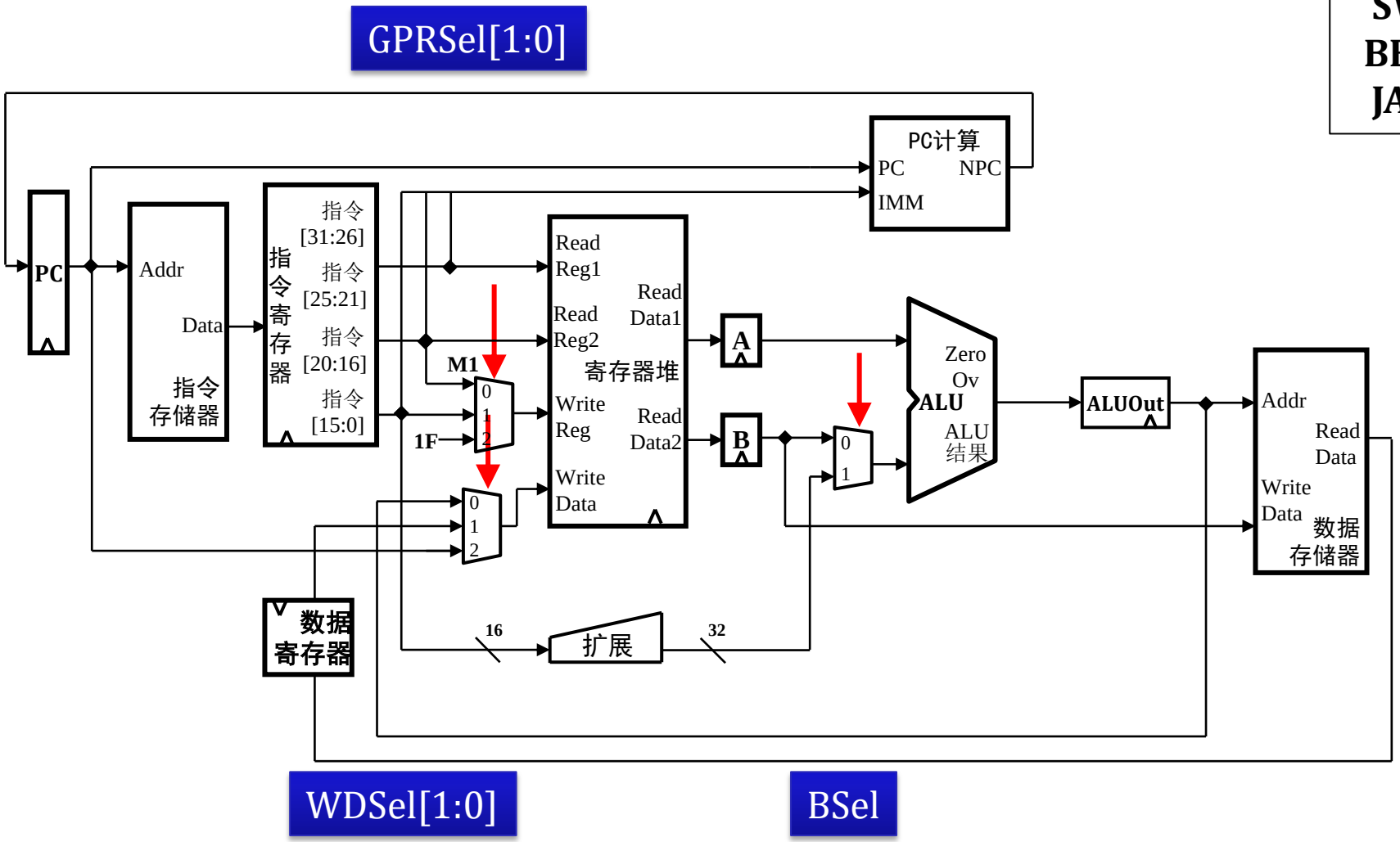
# 多周期数据通路控制信号：操作选择

LW
ADDU
SUBU
ORI
LUI
SW
BEQ
JAL



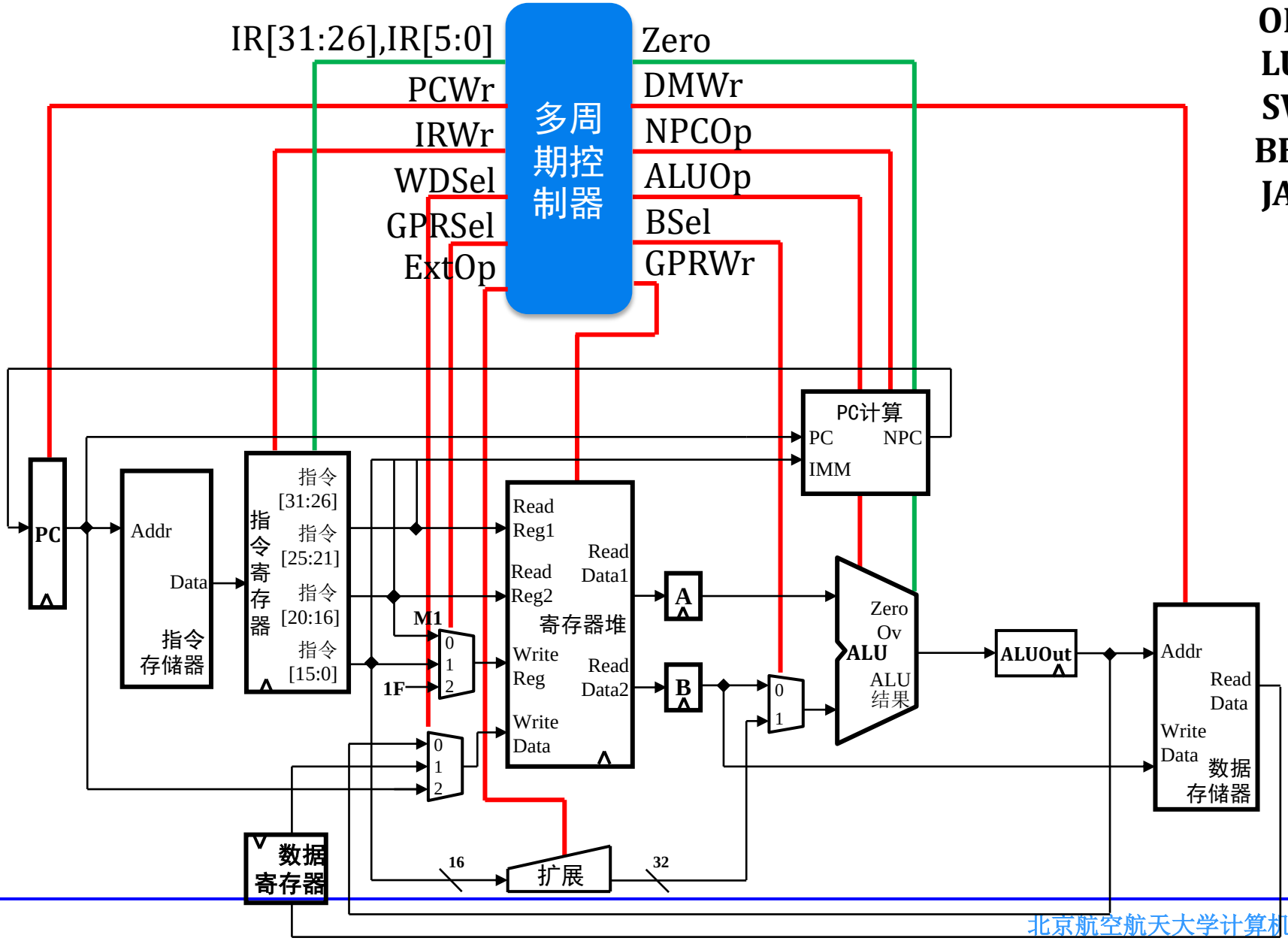
# 多周期数据通路控制信号：多路选择

LW
ADDU
SUBU
ORI
LUI
SW
BEQ
JAL



# 多周期数据通路及控制器

LW
ADDU
SUBU
ORI
LUI
SW
BEQ
JAL



# 提纲

- 内容主要取材
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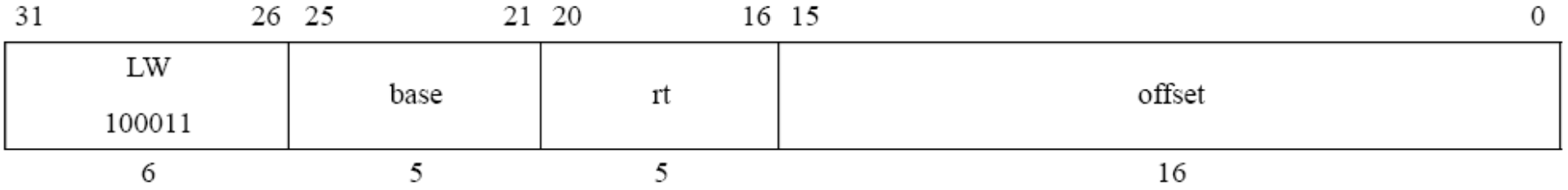
- 多周期数据通路控制信号分析
- 多周期控制器状态机构造
- 多周期性能分析

# 多周期控制器设计

- 数据通路：5阶段(IF、DCD/RF、EXE、MEM、WB)
  - 特点：每条指令由若3～5个时钟周期完成
- 控制器：FSM＋输出逻辑
  - FSM至少应包括5个状态：分别对应数据通路的5个阶段
- FSM输入
  - Op/Funct：Instr[31:26]/Instr[5:0]
  - Zero
  - Reset，Clk
- 输出逻辑
  - 各个控制信号：*f* (输入信号，状态机)

# FSM构造过程

- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL




```
Addr ← sign_extend(offset) + GPR[base]
memword ← Memory[Addr]
GPR[rt] ← memword
PC ← PC + 4
```

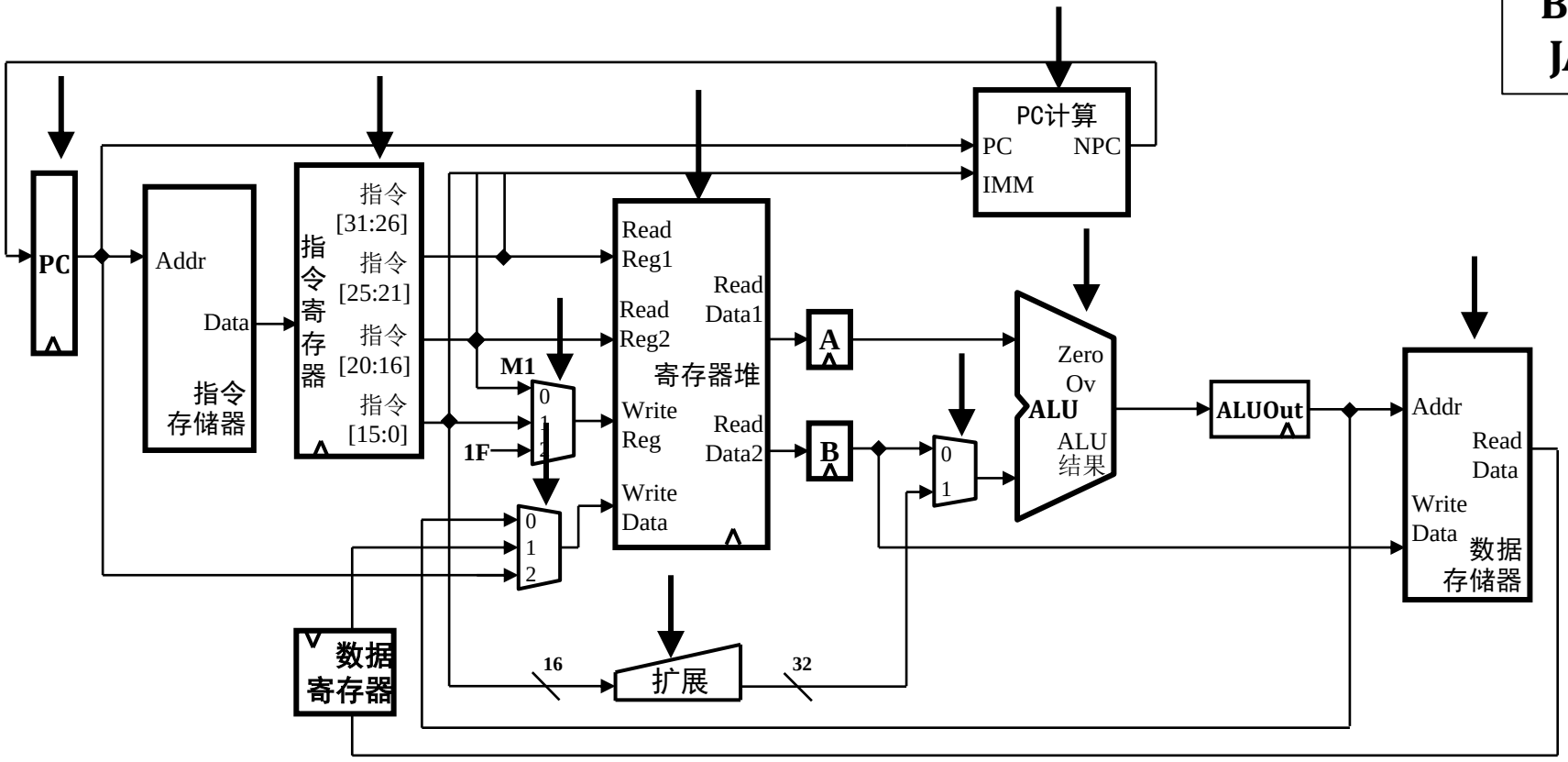
RTL

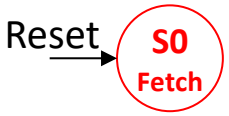
R[rt]←MEM[R[rs]+sign_ext(imm16)]

PC←PC+4

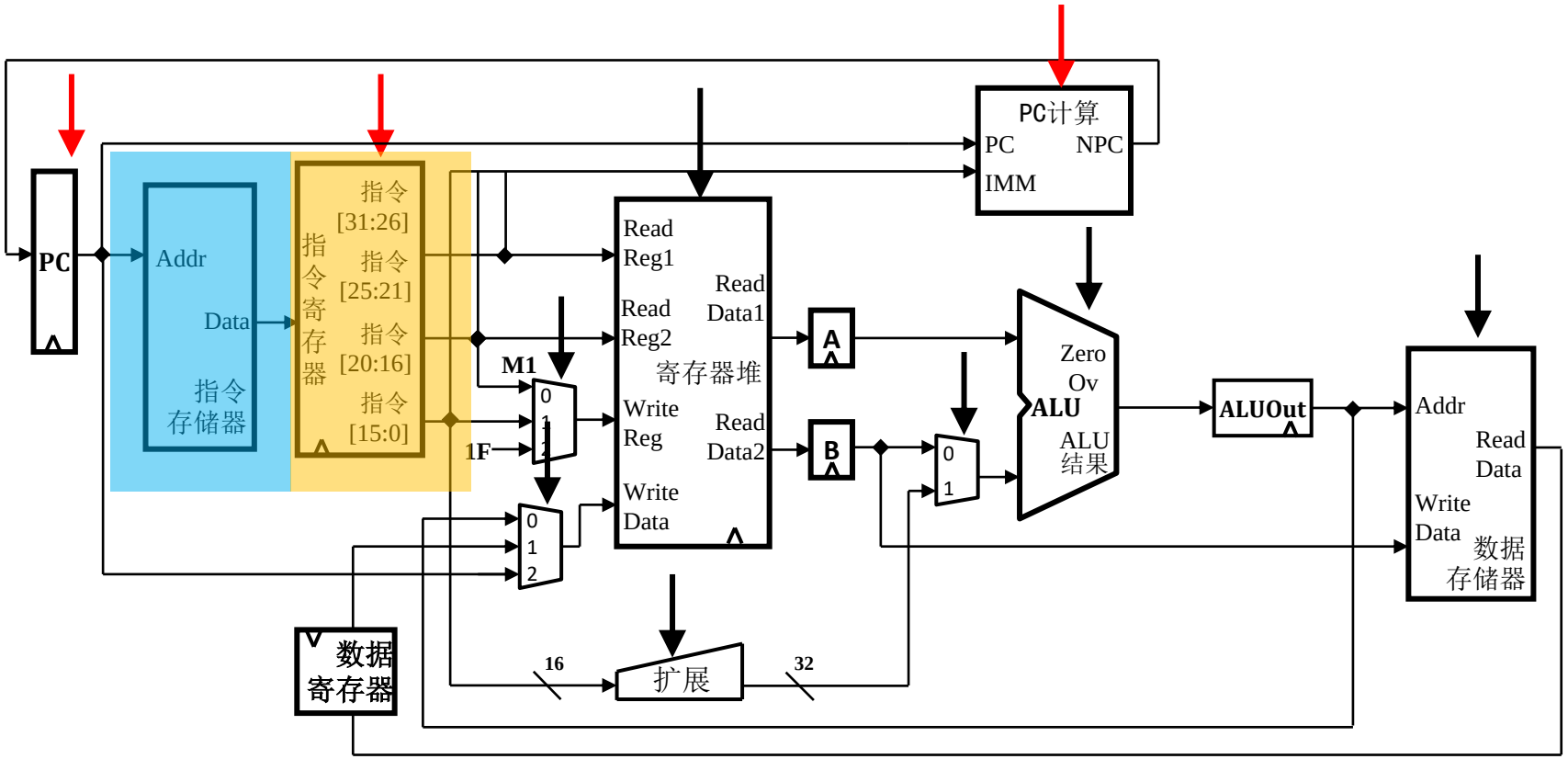
# 多周期数据通路控制信号：寄存器写使能

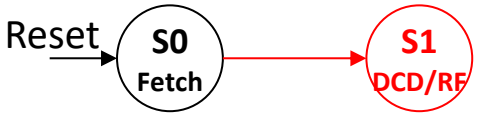
LW
ADDU
SUBU
ORI
LUI
SW
BEQ
JAL






| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | | | | | | | | | |
| NPCOp | PC+4 | | | | | | | | | |
| IRWr | 1 | | | | | | | | | |
| GPRWr | 0 | | | | | | | | | |
| DMWr | 0 | | | | | | | | | |
| ALUOp | X | | | | | | | | | |
| GPRSel | X | | | | | | | | | |
| WDSel | X | | | | | | | | | |
| ExtOp | X | | | | | | | | | |
| BSel | X | | | | | | | | | |

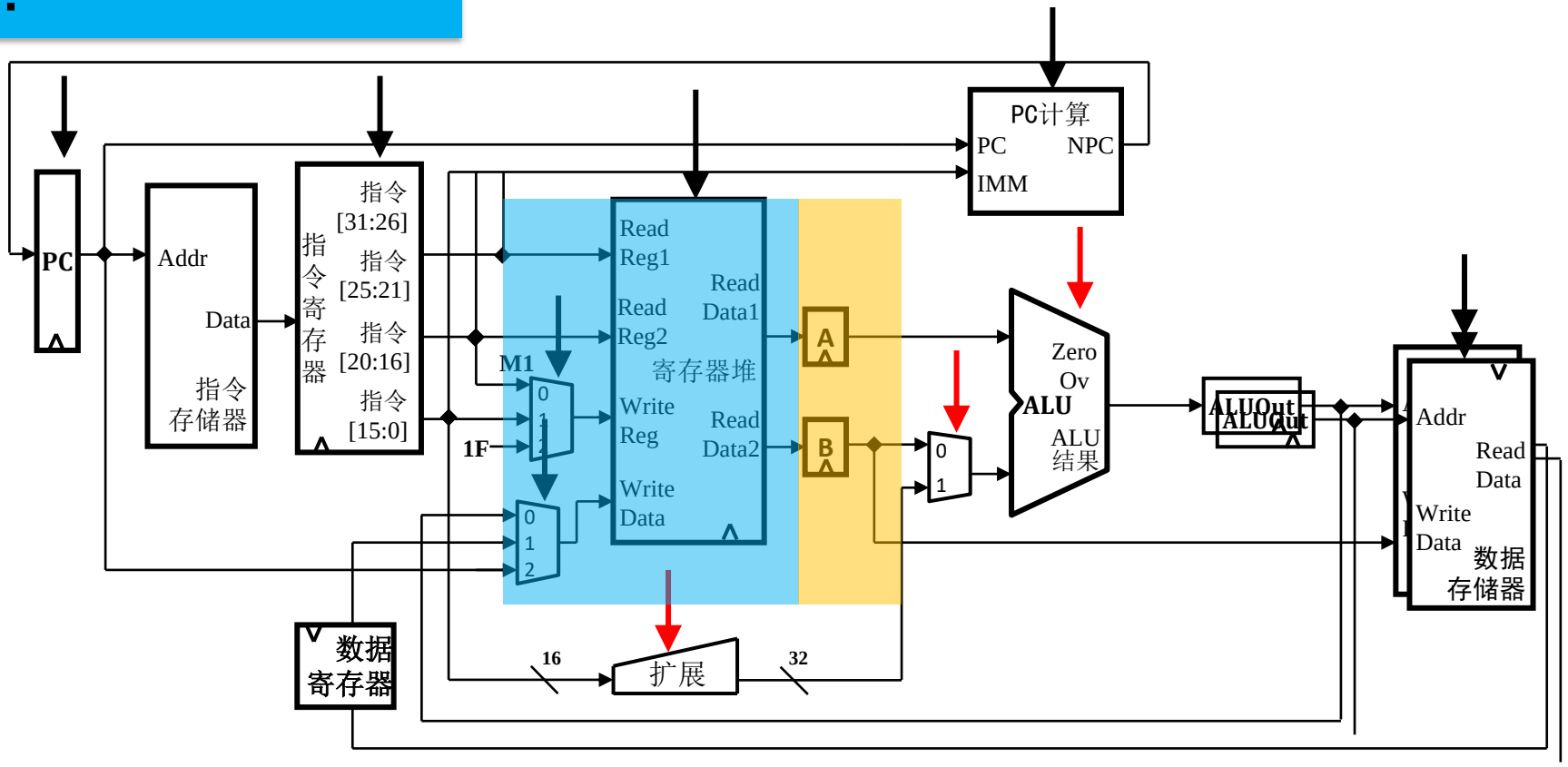


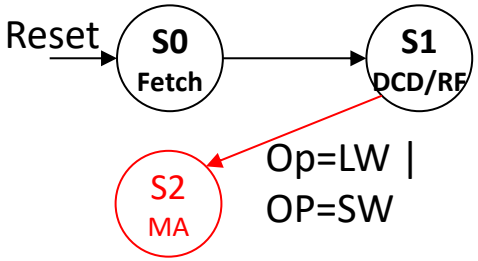



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | | | | |
| NPCOp | PC+4 | X | | | | | | | | |
| IRWr | 1 | 0 | | | | | | | | |
| GPRWr | 0 | 0 | | | | | | | | |
| DMWr | 0 | 0 | | | | | | | | |
| ALUOp | X | add | | | | | | | | |
| GPRSel | X | 00 | | | | | | | | |
| WDSel | X | 01 | | | | | | | | |
| ExtOp | X | SE | | | | | | | | |
| BSel | X | 1 | | | | | | | | |

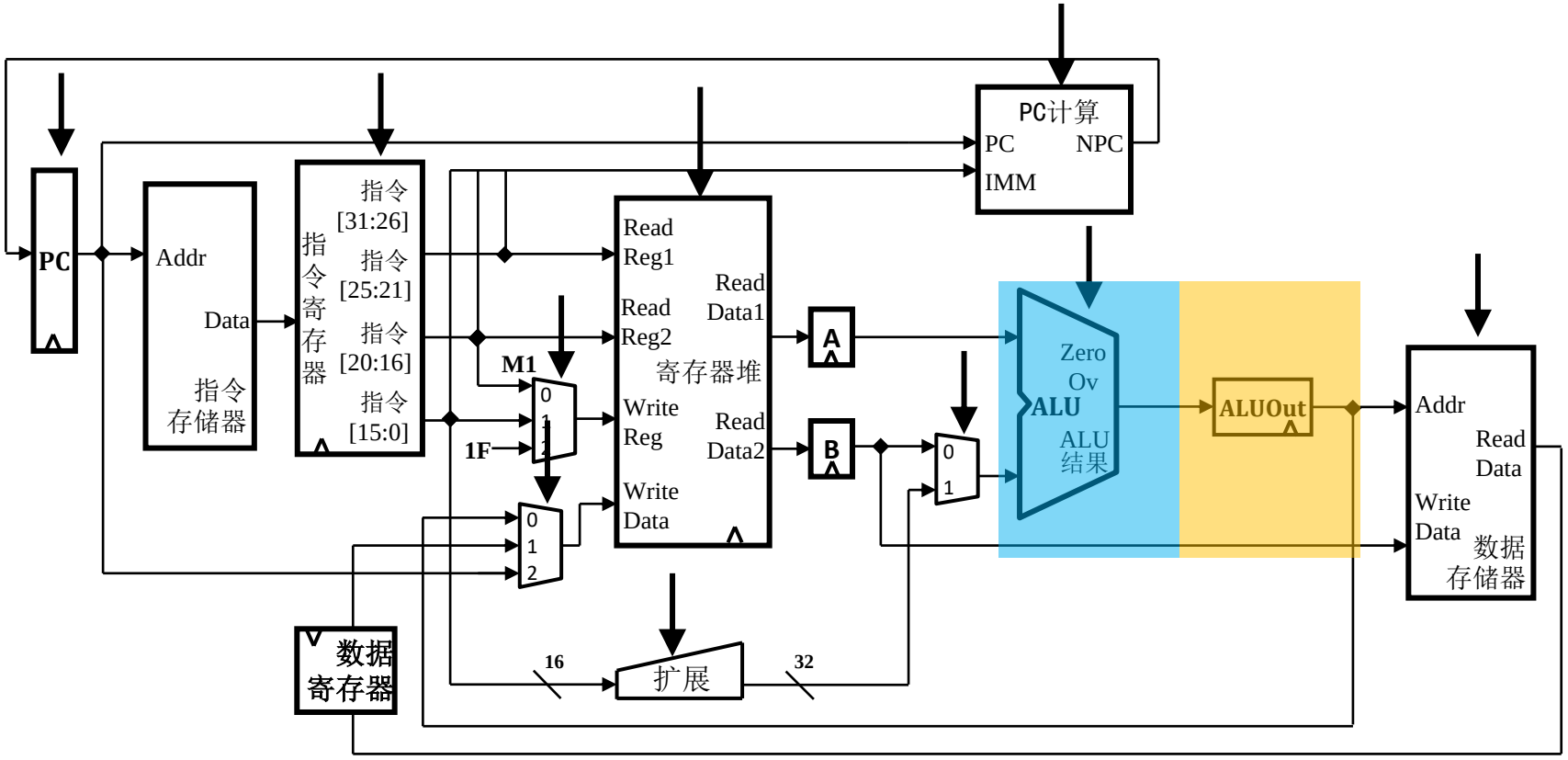
ALUOp/GPRSel/WDSel/EXTOp/BSel

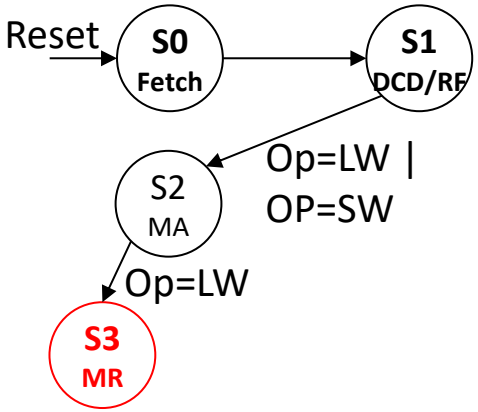
**需要这么早有效吗？**



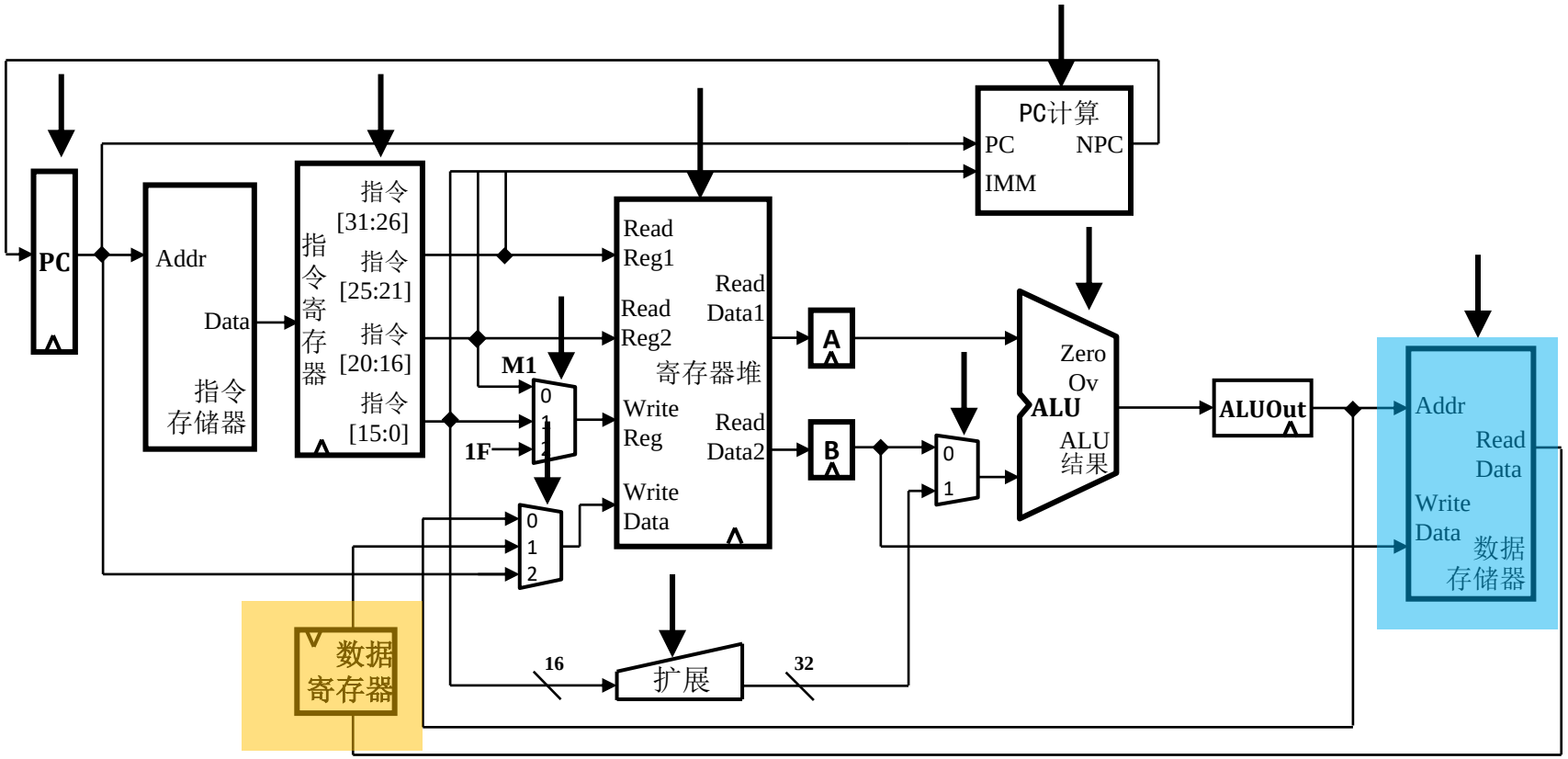


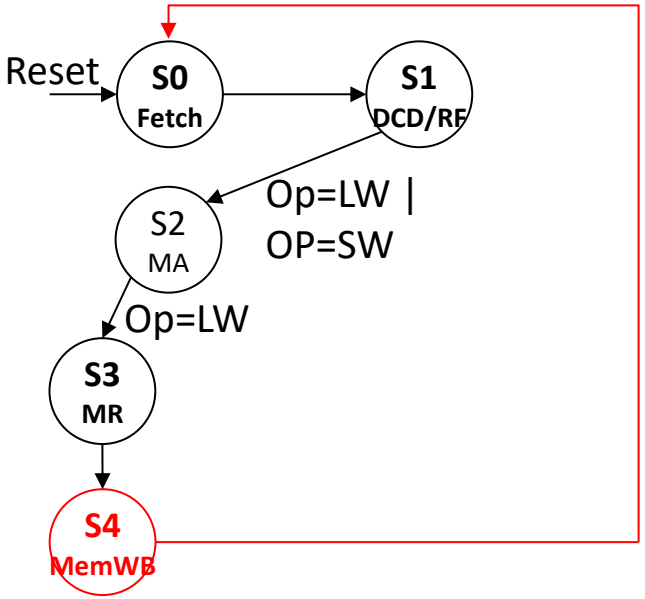

| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | 0 | | | | | | | |
| NPCOp | PC+4 | X | X | | | | | | | |
| IRWr | 1 | 0 | 0 | | | | | | | |
| GPRWr | 0 | 0 | 0 | | | | | | | |
| DMWr | 0 | 0 | 0 | | | | | | | |
| ALUOp | X | add | add | | | | | | | |
| GPRSel | X | 00 | 00 | | | | | | | |
| WDSel | X | 01 | 01 | | | | | | | |
| ExtOp | X | SE | SE | | | | | | | |
| BSel | X | 1 | 1 | | | | | | | |



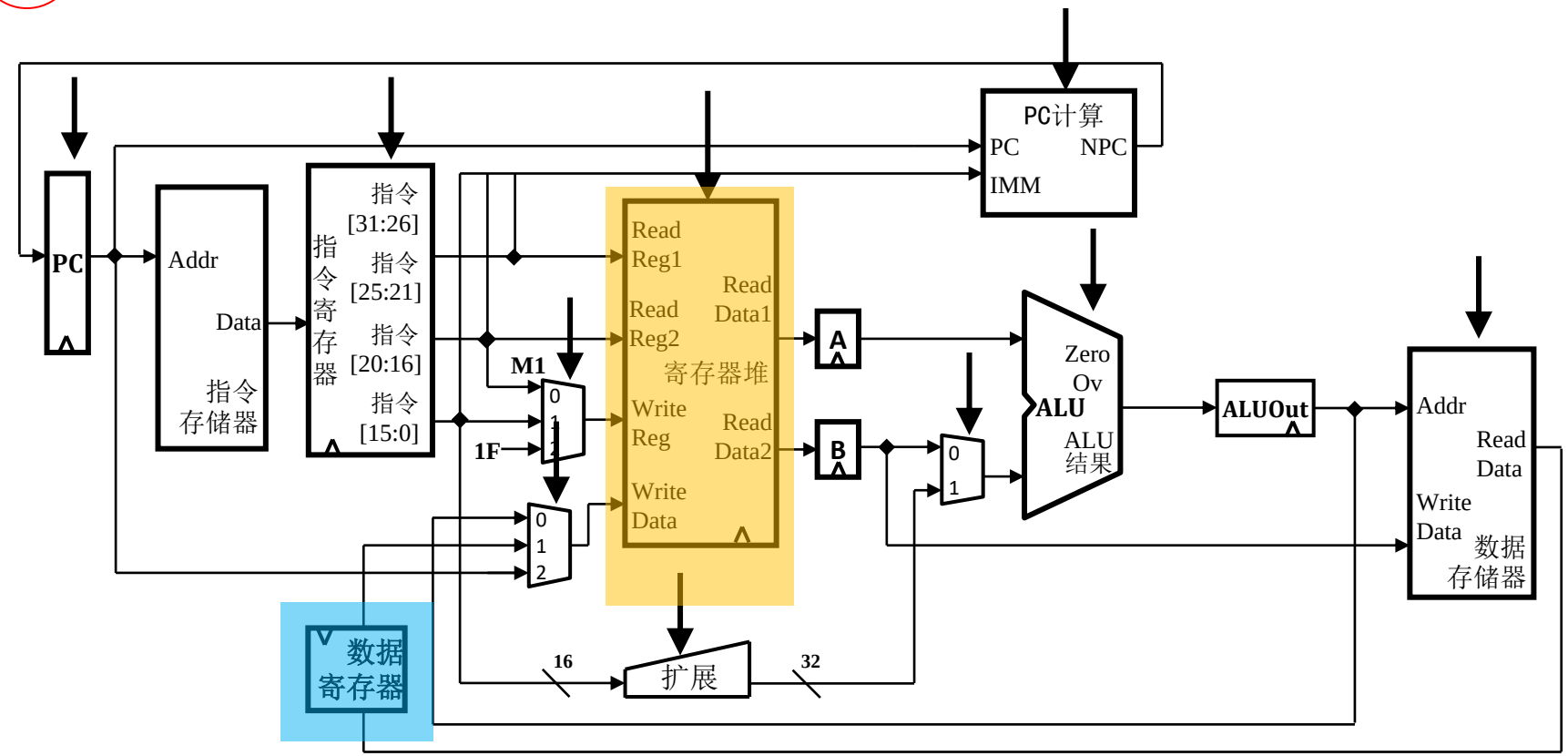



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | 0 | 0 | | | | | | |
| NPCOp | PC+4 | X | X | X | | | | | | |
| IRWr | 1 | 0 | 0 | 0 | | | | | | |
| GPRWr | 0 | 0 | 0 | 0 | | | | | | |
| DMWr | 0 | 0 | 0 | 0 | | | | | | |
| ALUOp | X | add | add | add | | | | | | |
| GPRSel | X | 00 | 00 | 00 | | | | | | |
| WDSel | X | 01 | 01 | 01 | | | | | | |
| ExtOp | X | SE | SE | SE | | | | | | |
| BSel | X | 1 | 1 | 1 | | | | | | |



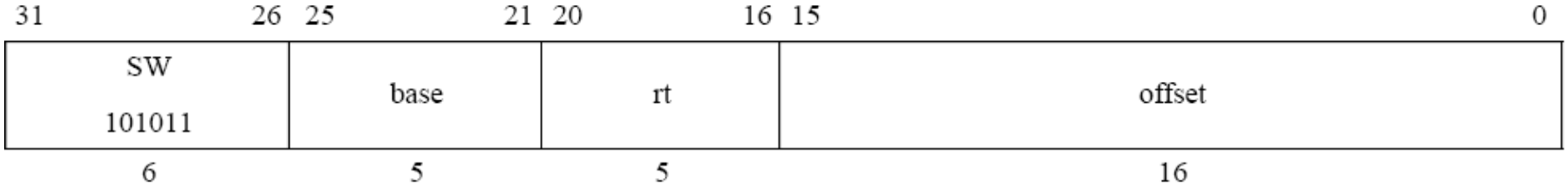



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | 0 | 0 | 0 | | | | | |
| NPCOp | PC+4 | X | X | X | X | | | | | |
| IRWr | 1 | 0 | 0 | 0 | 0 | | | | | |
| GPRWr | 0 | 0 | 0 | 0 | 1 | | | | | |
| DMWr | 0 | 0 | 0 | 0 | 0 | | | | | |
| ALUOp | X | add | add | add | add | | | | | |
| GPRSel | X | 00 | 00 | 00 | 00 | | | | | |
| WDSel | X | 01 | 01 | 01 | 01 | | | | | |
| ExtOp | X | SE | SE | SE | SE | | | | | |
| BSel | X | 1 | 1 | 1 | 1 | | | | | |



# FSM构造过程

- LW, SW, ADDU, SUBU, ORI, LUI, BEQ, JAL

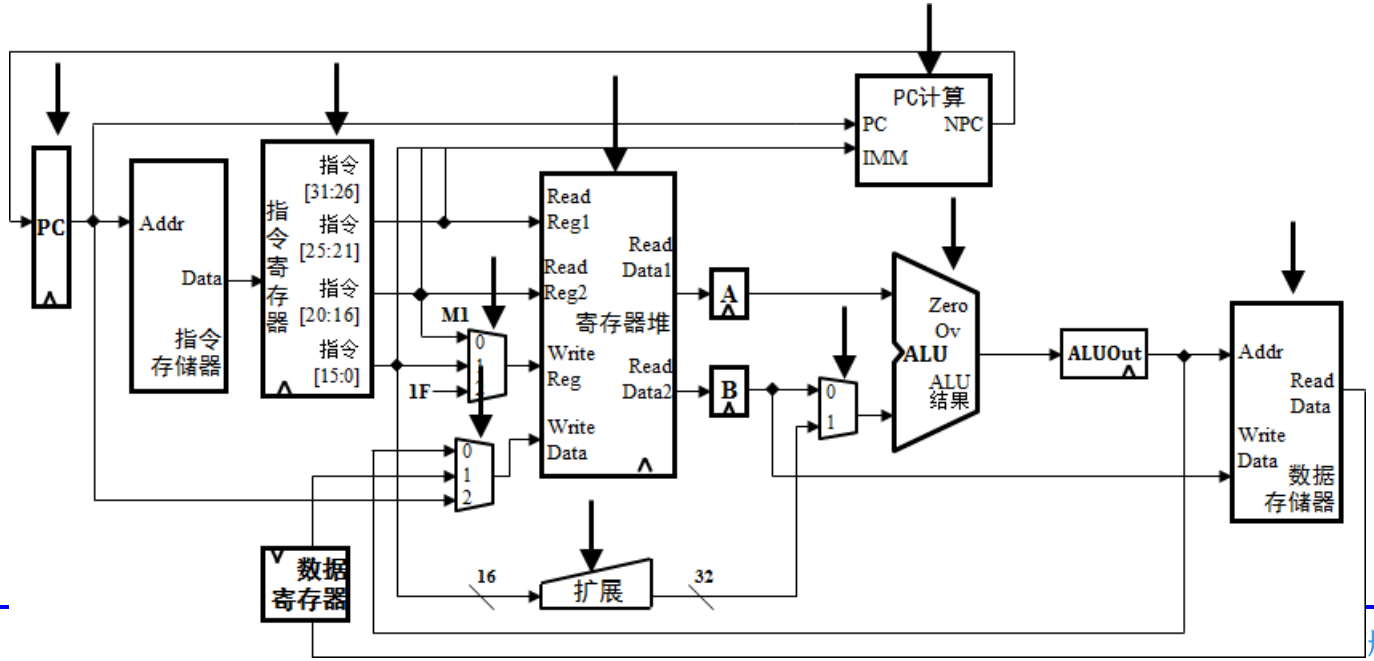


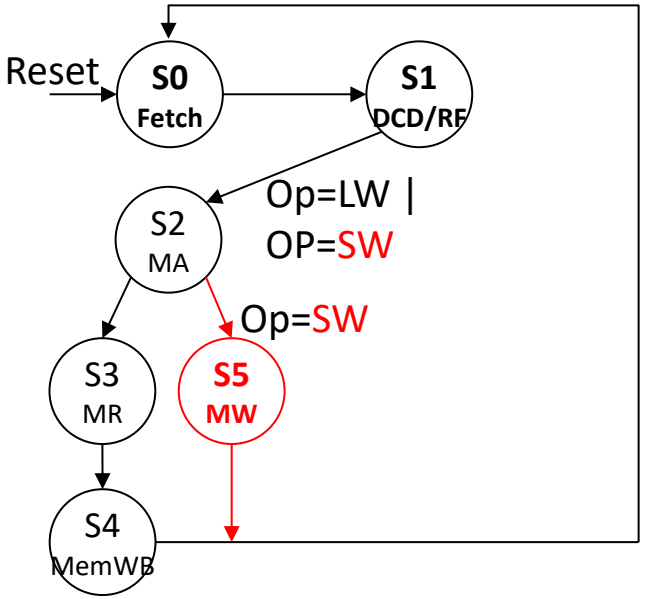

```
Addr ← sign_extend(offset) + GPR[base]
memword ← Memory[Addr]
GPR[rt] ← memword
PC ← PC + 4
```

RTL描述

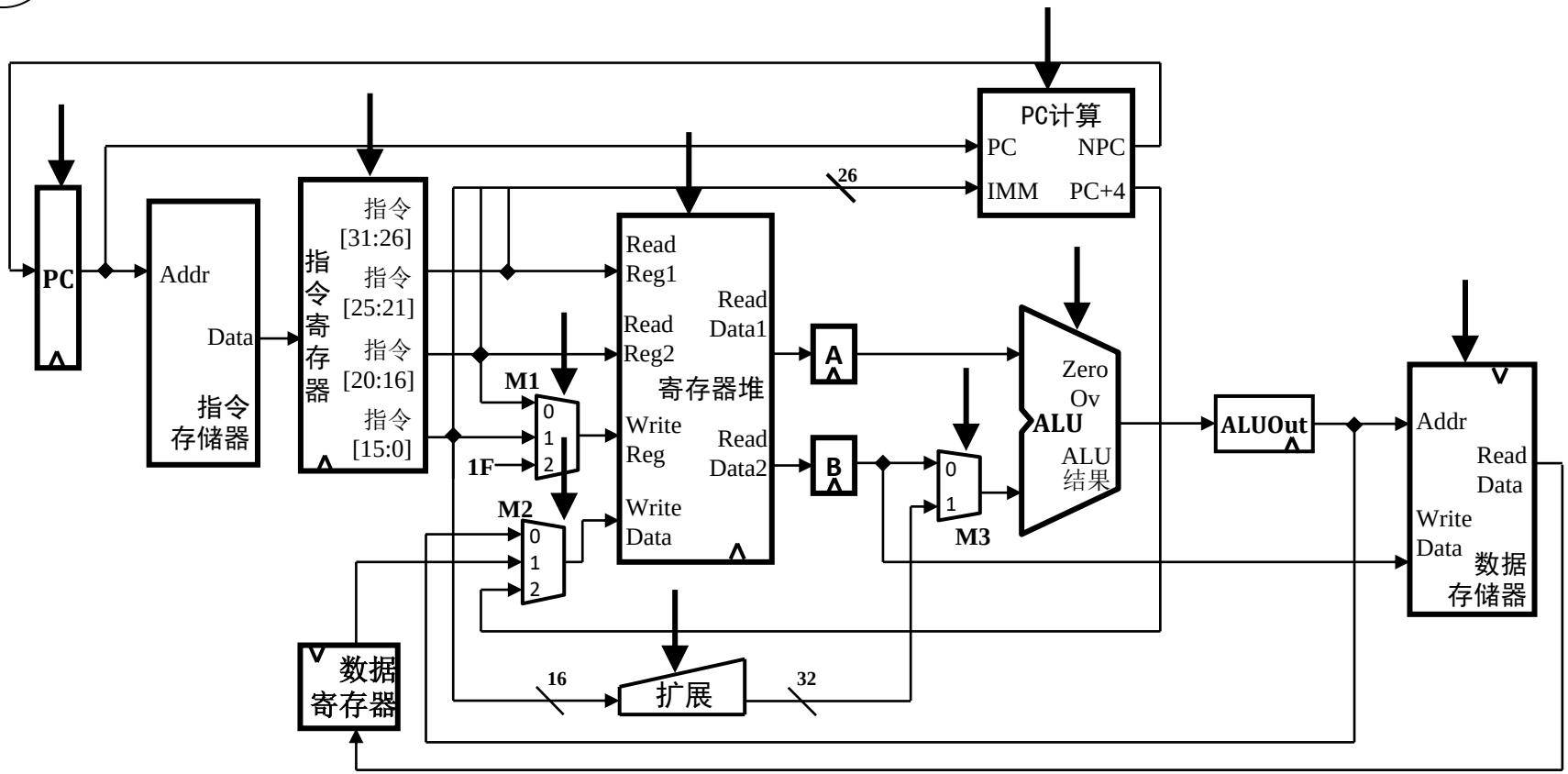
MEM[R[rs]+sign_ext(imm16)] ←R[rt]

PC←PC+4






| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | 0 | | | 0 | | | | |
| NPCOp | PC+4 | X | X | | | X | | | | |
| IRWr | 1 | 0 | 0 | | | 0 | | | | |
| GPRWr | 0 | 0 | 0 | | | 0 | | | | |
| DMWr | 0 | 0 | 0 | | | 1 | | | | |
| ALUOp | X | add | add | | | add | | | | |
| GPRSel | X | 00 | 00 | | | 00 | | | | |
| WDSel | X | 01 | 01 | | | 01 | | | | |
| ExtOp | X | SE | SE | | | SE | | | | |
| BSel | X | 1 | 1 | | | 1 | | | | |



# FSM构造过程

- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL

| 31–26 | 25–21 | 20–16 | 15–11 | 10–6 | 5–0 |
|---|---|---|---|---|---|
| SPECIAL<br>000000 | rs | rt | rd | 0<br>00000 | ADDU<br>100001 |
| 6 | 5 | 5 | 5 | 5 | 6 |

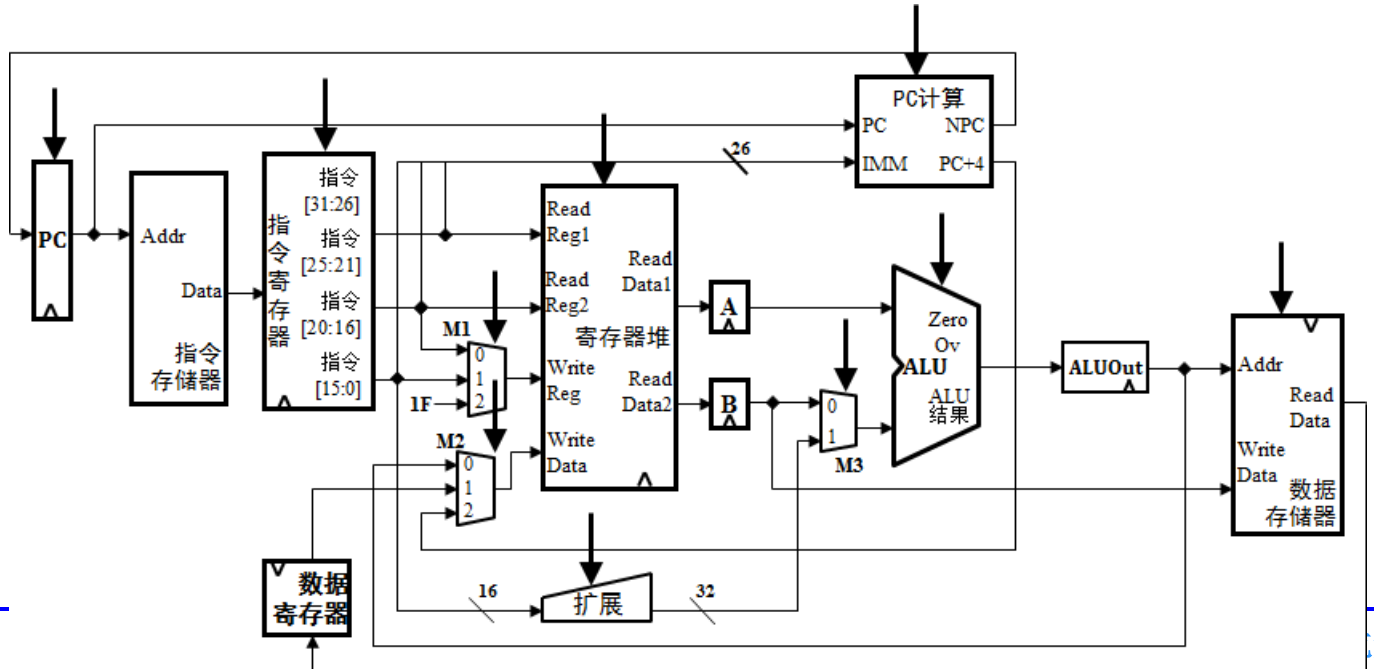
**Operation:**

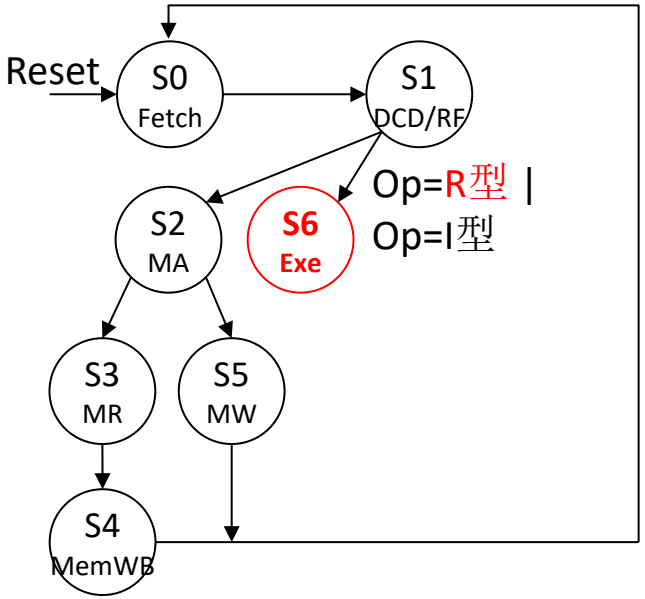
```
temp ← GPR[rs] + GPR[rt]
GPR[rd] ← temp
```

RTL

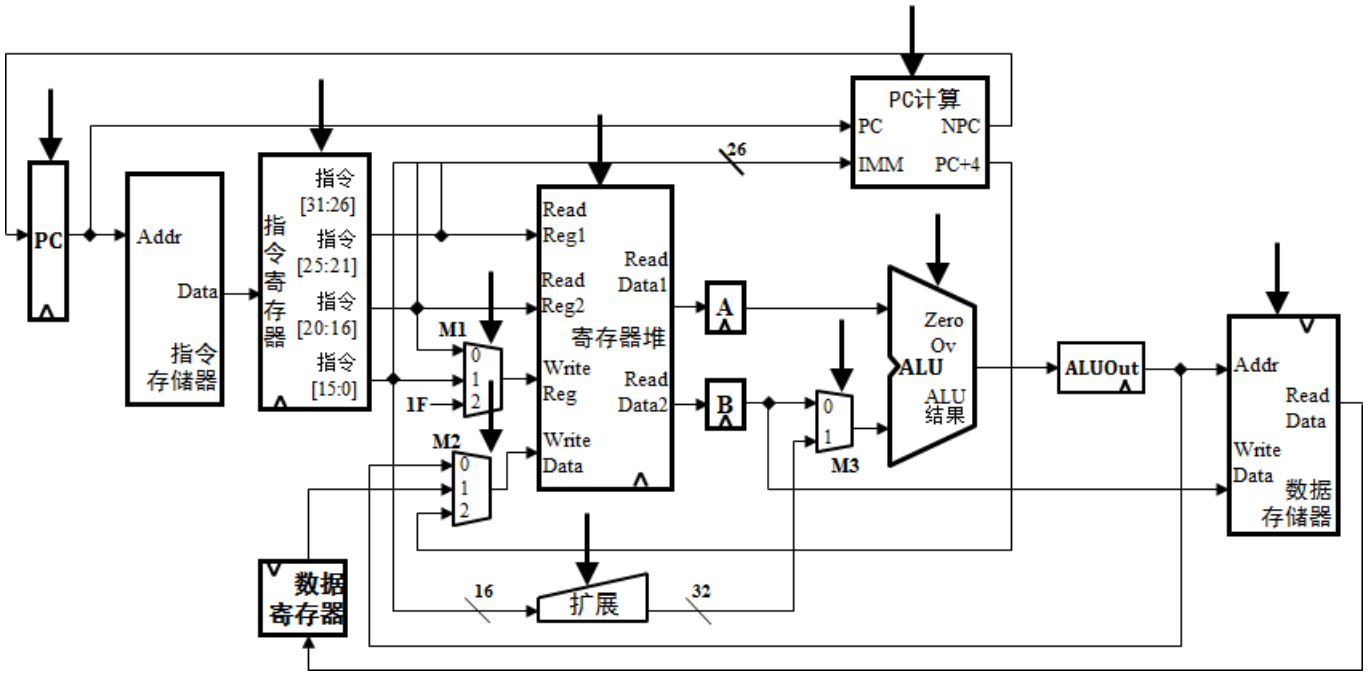
R[rd]←R[rs]+R[rt]

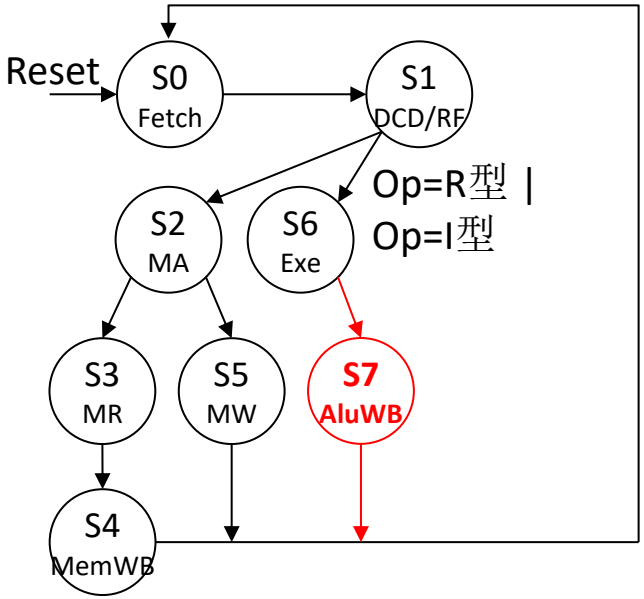
PC←PC+4



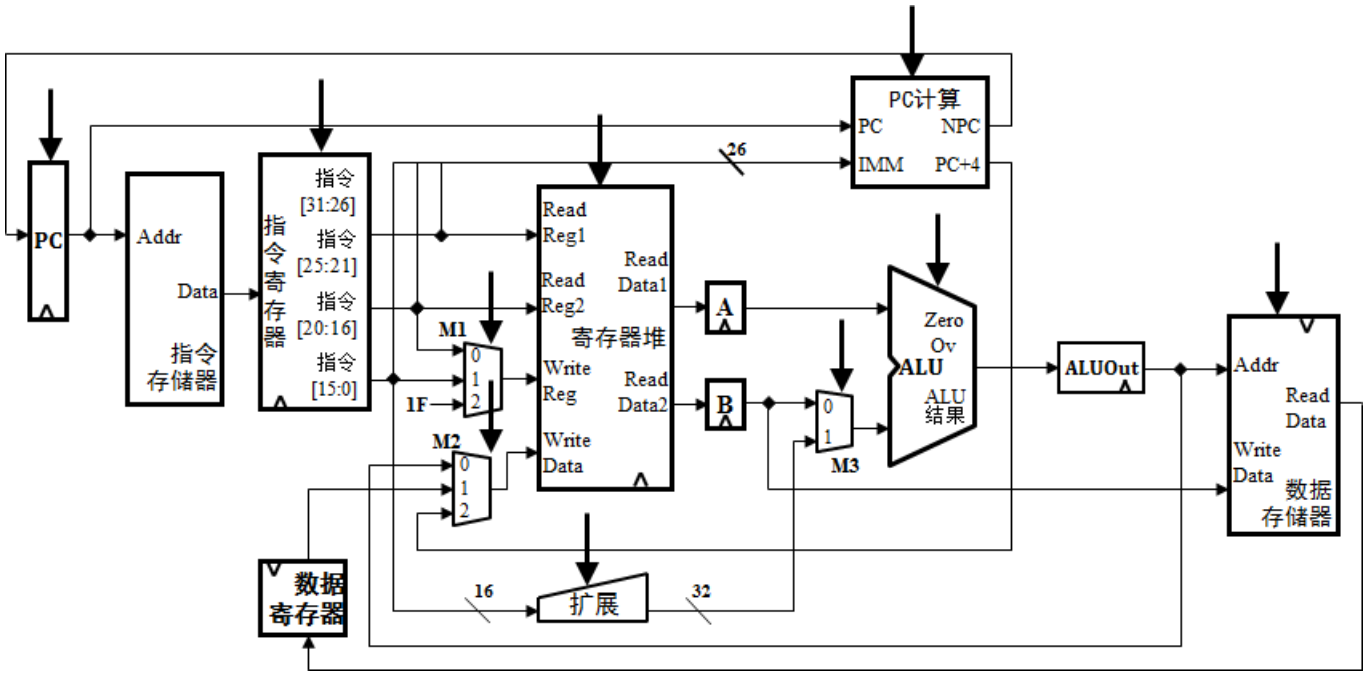



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | 0 | | | |
| NPCOp | PC+4 | X | | | | | X | | | |
| IRWr | 1 | 0 | | | | | 0 | | | |
| GPRWr | 0 | 0 | | | | | 0 | | | |
| DMWr | 0 | 0 | | | | | 0 | | | |
| ALUOp | X | add | | | | | add | | | |
| GPRSel | X | 01 | | | | | 01 | | | |
| WDSel | X | 00 | | | | | 00 | | | |
| ExtOp | X | X | | | | | X | | | |
| BSel | X | 0 | | | | | 0 | | | |



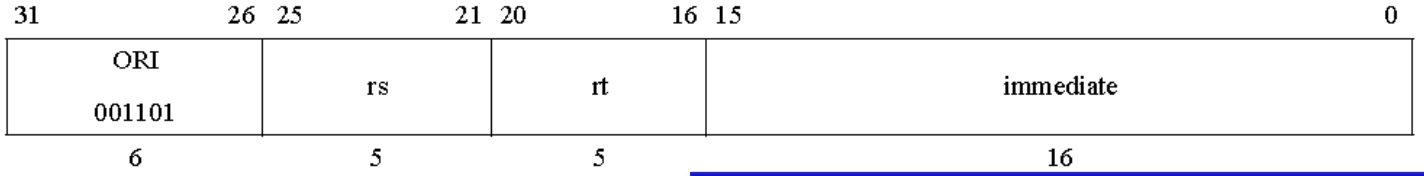



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | 0 | 0 | | |
| NPCOp | PC+4 | X | | | | | X | X | | |
| IRWr | 1 | 0 | | | | | 0 | 0 | | |
| GPRWr | 0 | 0 | | | | | 0 | 1 | | |
| DMWr | 0 | 0 | | | | | 0 | 0 | | |
| ALUOp | X | add | | | | | add | add | | |
| GPRSel | X | 01 | | | | | 01 | 01 | | |
| WDSel | X | 00 | | | | | 00 | 00 | | |
| ExtOp | X | X | | | | | X | X | | |
| BSel | X | 0 | | | | | 0 | 0 | | |



# FSM构造过程

- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL



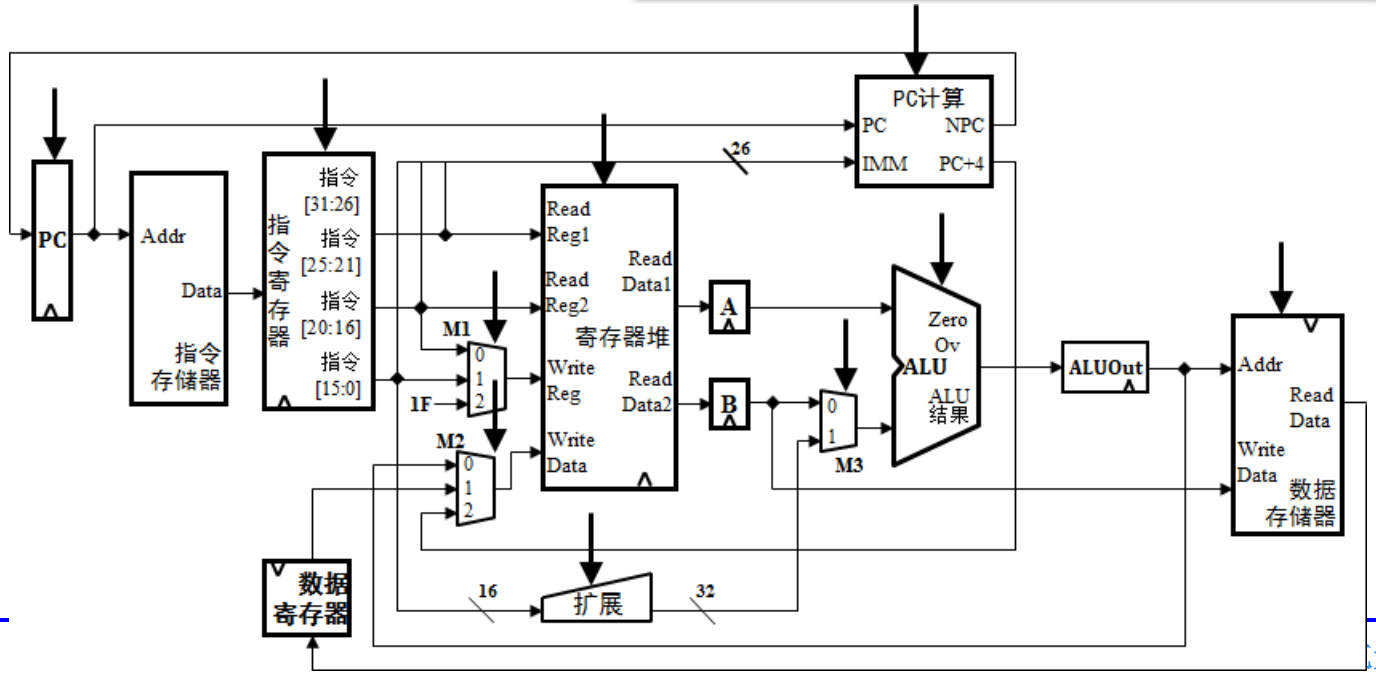

**Operation:**

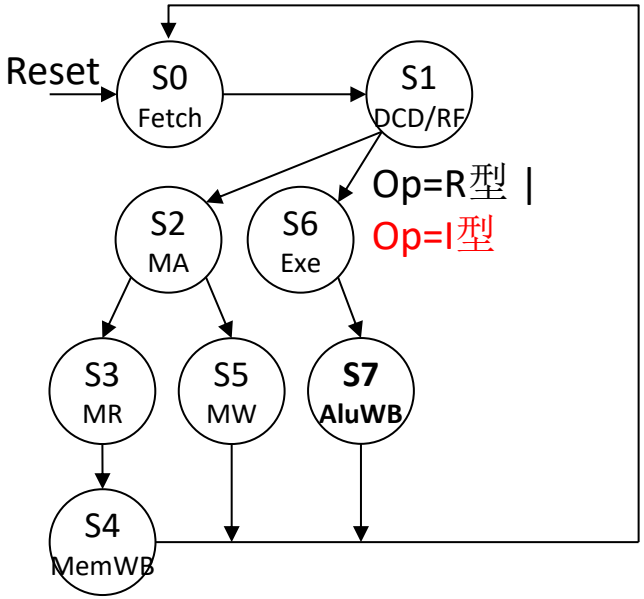
```
GPR[rt] ← GPR[rs] or zero_extend(imm
```

RTL

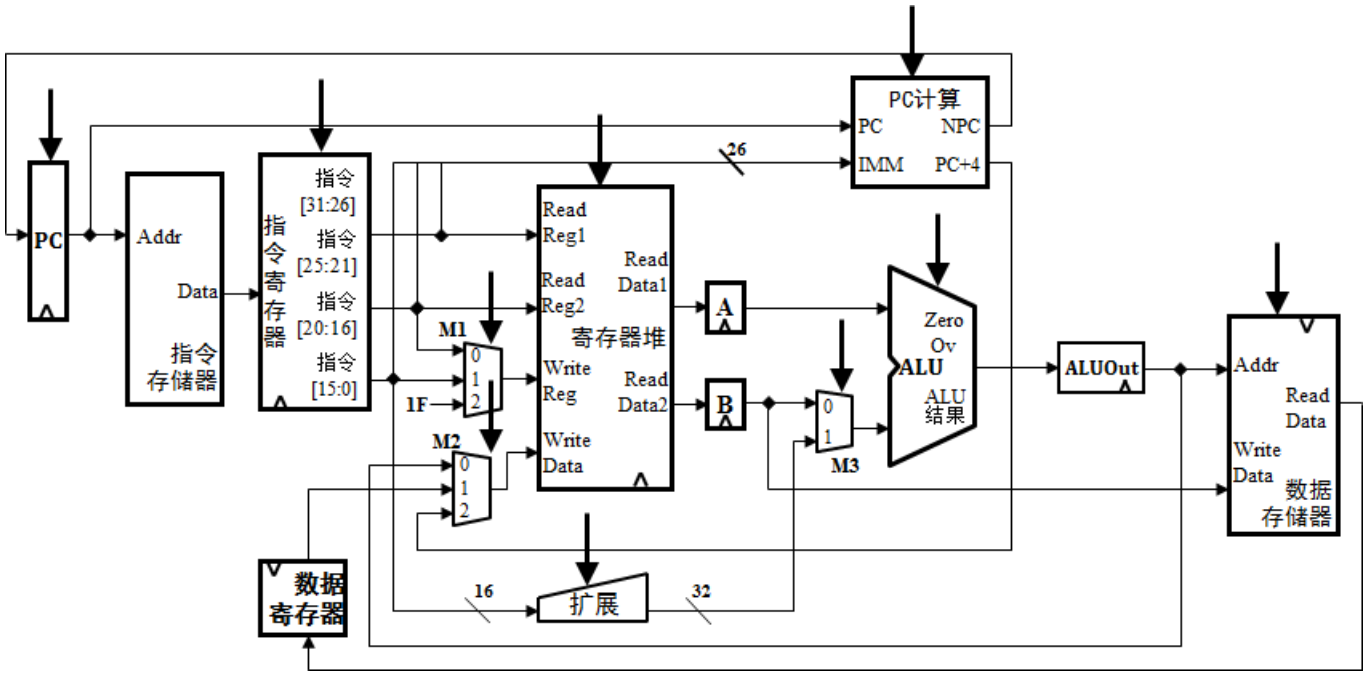
R[rd]←R[rs] | zero_extend(imm16)

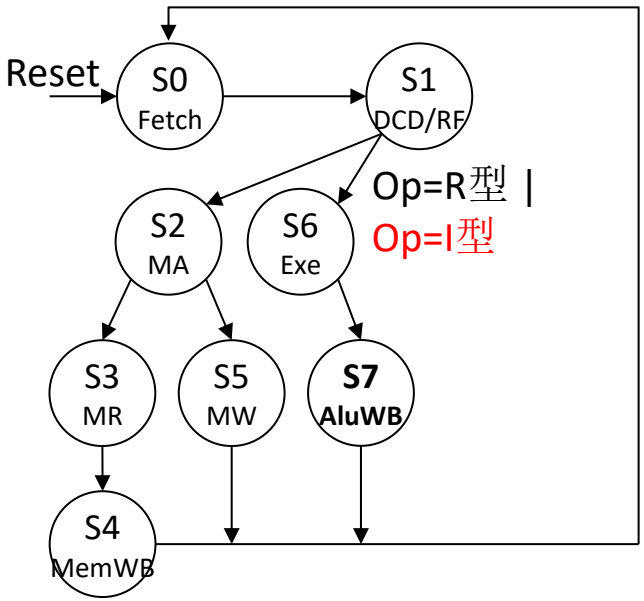
PC←PC+4






| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | 0 | 0 | | |
| NPCOp | PC+4 | X | | | | | X | X | | |
| IRWr | 1 | 0 | | | | | 0 | 0 | | |
| GPRWr | 0 | 0 | | | | | 0 | 1 | | |
| DMWr | 0 | 0 | | | | | 0 | 0 | | |
| ALUOp | X | OR | | | | | OR | OR | | |
| GPRSel | X | 00 | | | | | 00 | 00 | | |
| WDSel | X | 00 | | | | | 00 | 00 | | |
| ExtOp | X | ZE | | | | | ZE | ZE | | |
| BSel | X | 1 | | | | | 1 | 1 | | |

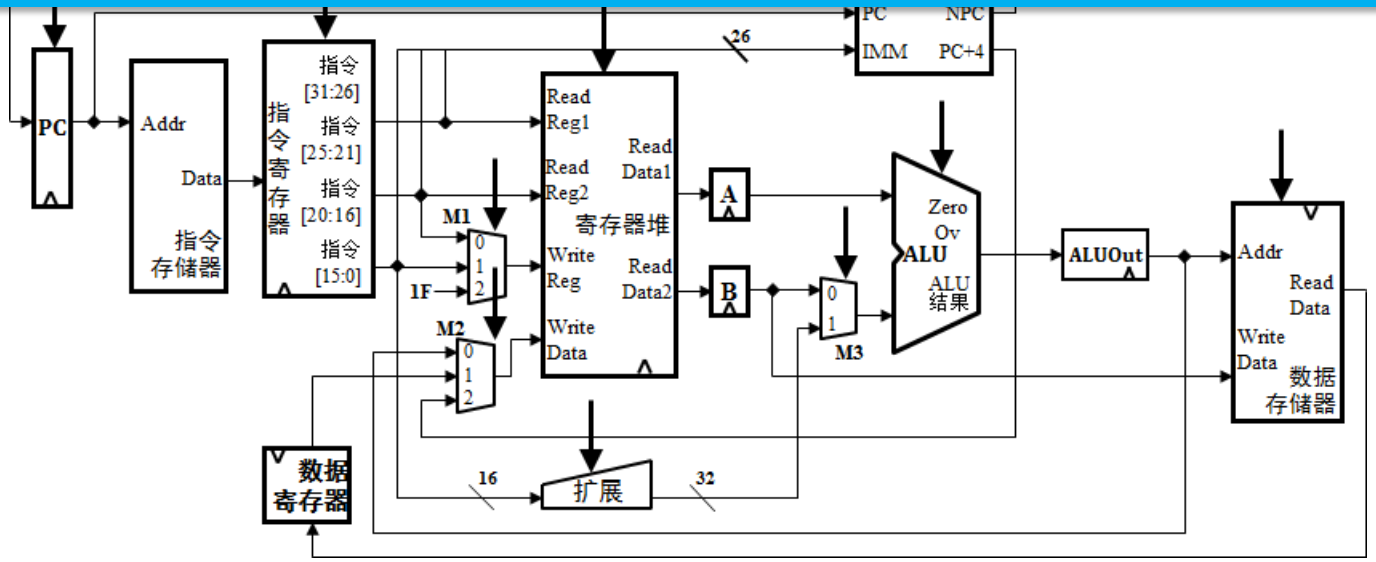





| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | 0 | 0 | | |
| NPCOp | PC+4 | X | | | | | X | X | | |
| IRWr | 1 | 0 | | | | | 0 | 0 | | |
| GPRWr | 0 | 0 | | | | | 0 | 1 | | |
| DMWr | 0 | 0 | | | | | 0 | 0 | | |
| ALUOp | X | OR | | | | | OR | OR | | |
| GPRSel | X | 00 | | | | | 00 | 00 | | |
| WDSel | X | 00 | | | | | 00 | 00 | | |
| ExtOp | X | ZE | | | | | ZE | ZE | | |
| BSel | X | 1 | | | | | 1 | 1 | | |

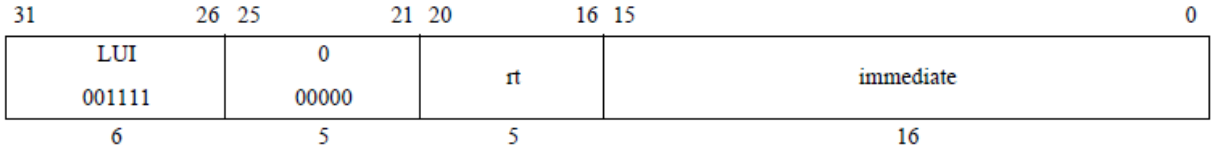
# I型与R型没有实质差别！区别仅在于：

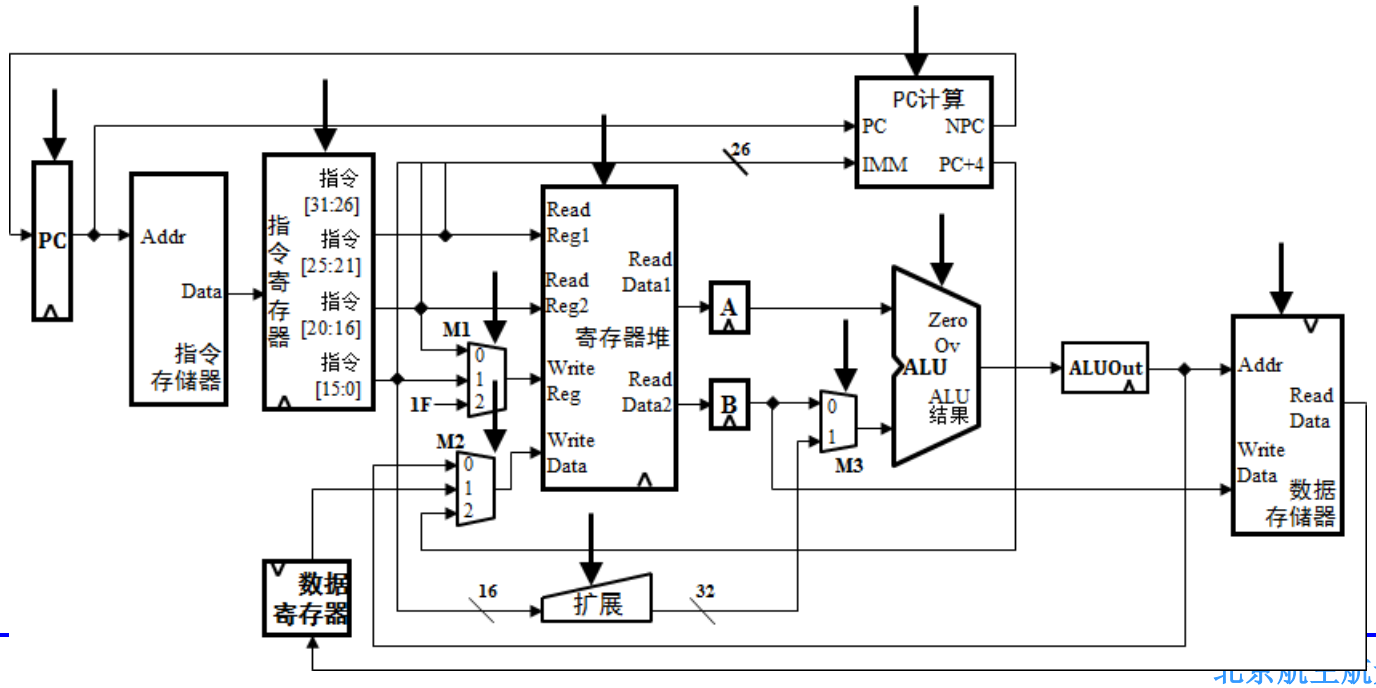
- ALU的B通道的控制

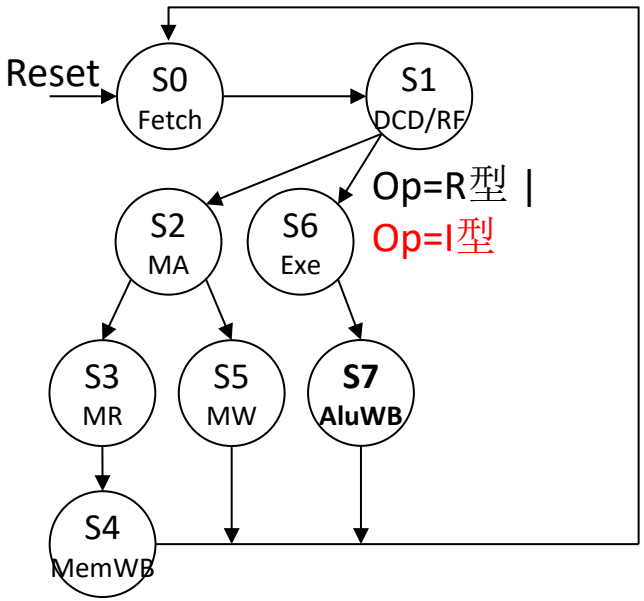


# FSM构造过程

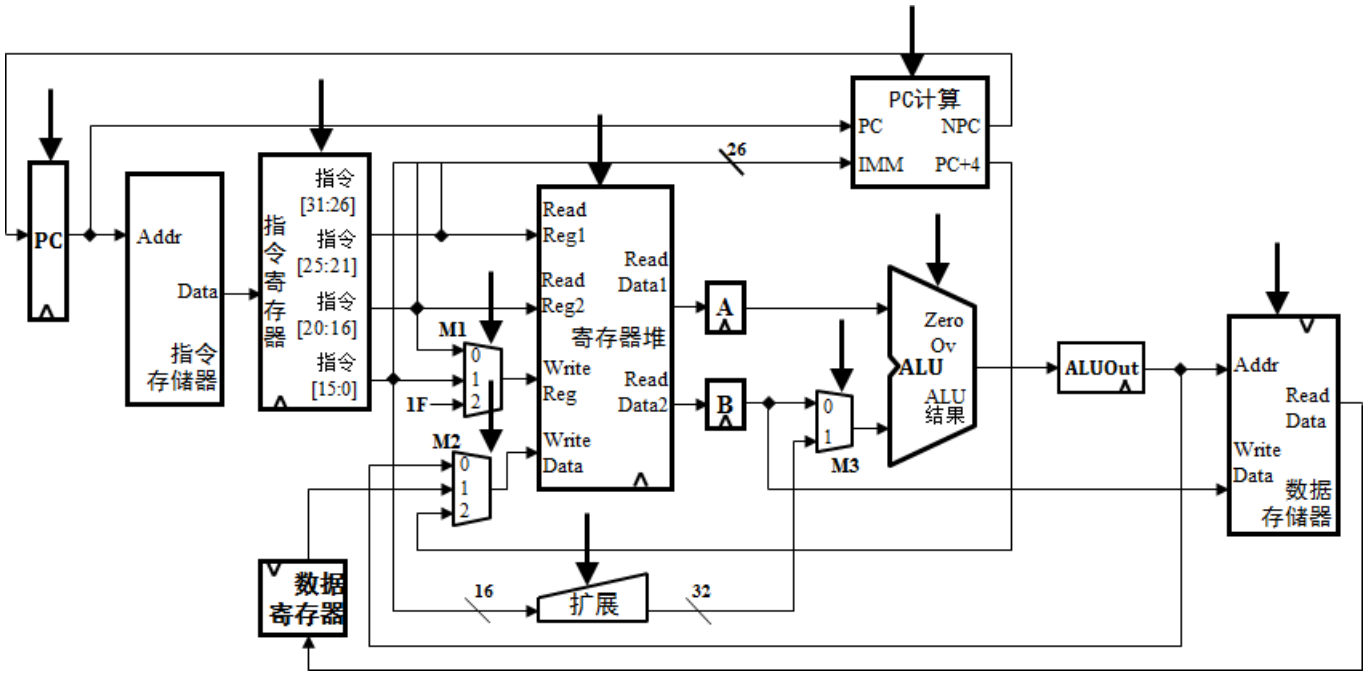
- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL
- LUI怎么执行？
  - GPR[rt] ← imm16 || $0^{16}$

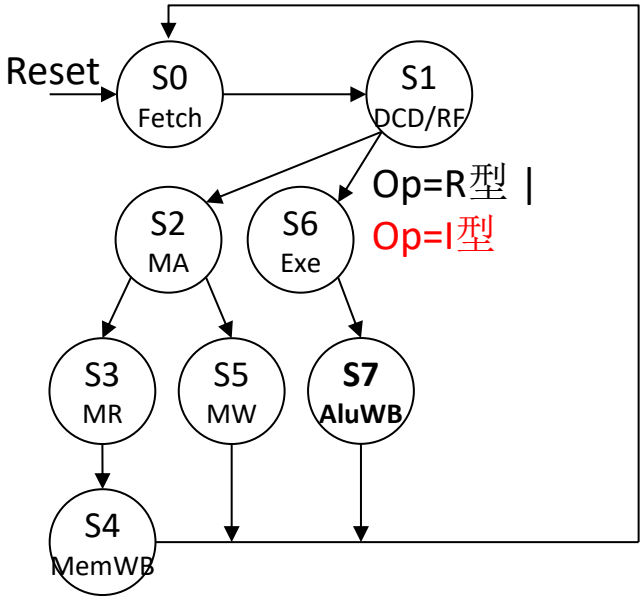




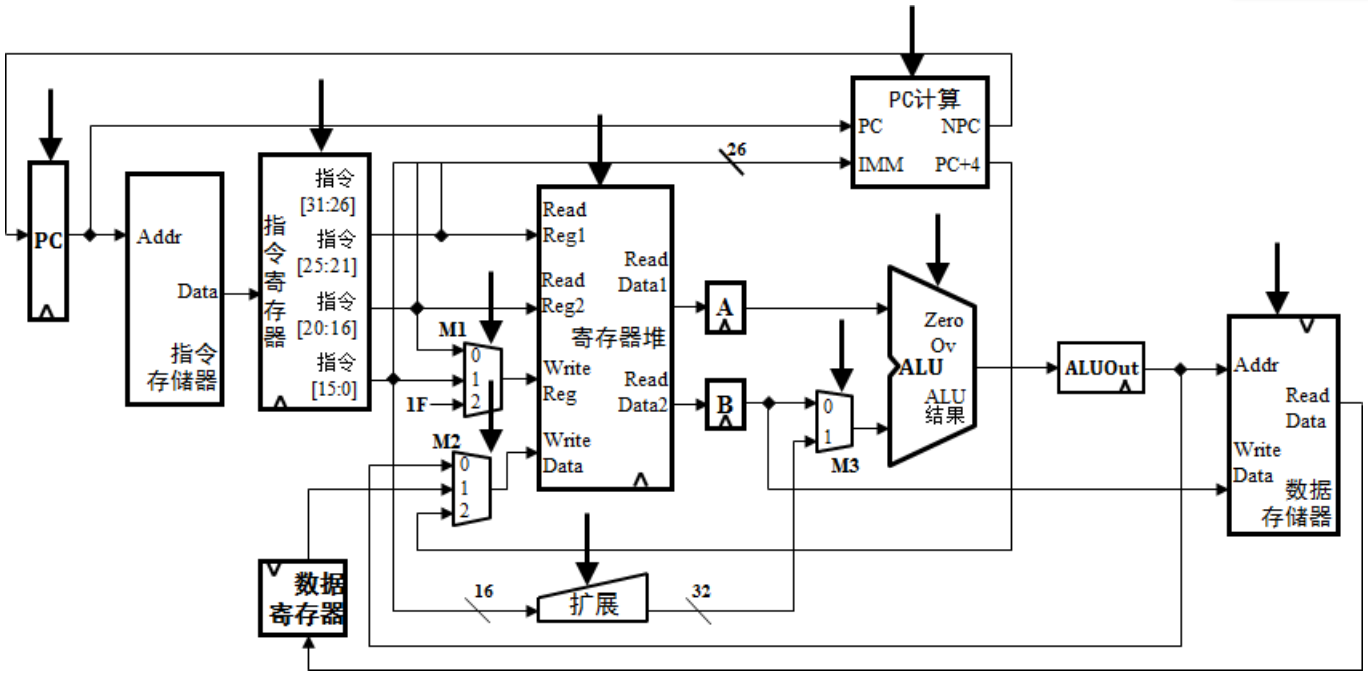

| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | | | | |
| NPCOp | PC+4 | X | | | | | | | | |
| IRWr | 1 | 0 | | | | | | | | |
| GPRWr | 0 | 0 | | | | | | | | |
| DMWr | 0 | 0 | | | | | | | | |
| ALUOp | X | | | | | | | | | |
| GPRSel | X | 00 | | | | | | | | |
| WDSel | X | 00 | | | | | | | | |
| ExtOp | X | | | | | | | | | |
| BSel | X | 1 | | | | | | | | |






| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | 0 | 0 | | |
| NPCOp | PC+4 | X | | | | | X | X | | |
| IRWr | 1 | 0 | | | | | 0 | 0 | | |
| GPRWr | 0 | 0 | | | | | 0 | 1 | | |
| DMWr | 0 | 0 | | | | | 0 | 0 | | |
| ALUOp | X | OR | | | | | OR | OR | | |
| GPRSel | X | 00 | | | | | 00 | 00 | | |
| WDSel | X | 00 | | | | | 00 | 00 | | |
| ExtOp | X | HC | | | | | HC | HC | | |
| BSel | X | 1 | | | | | 1 | 1 | | |

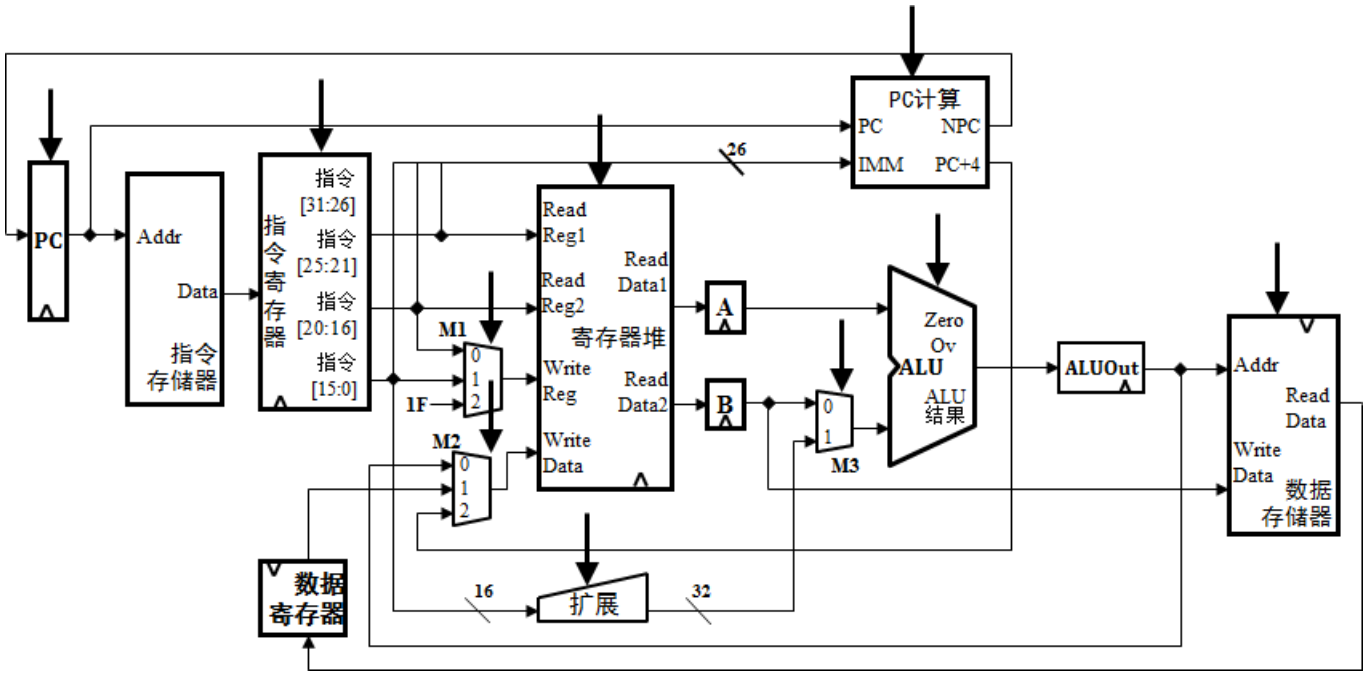
HC：高位复制

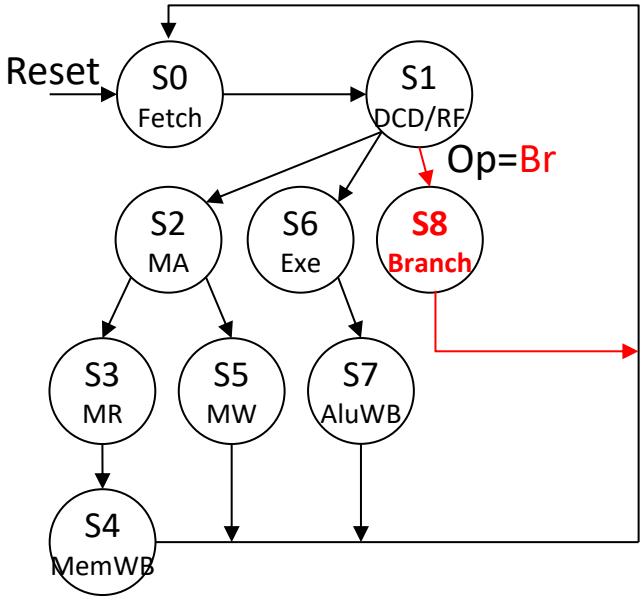


# FSM构造过程

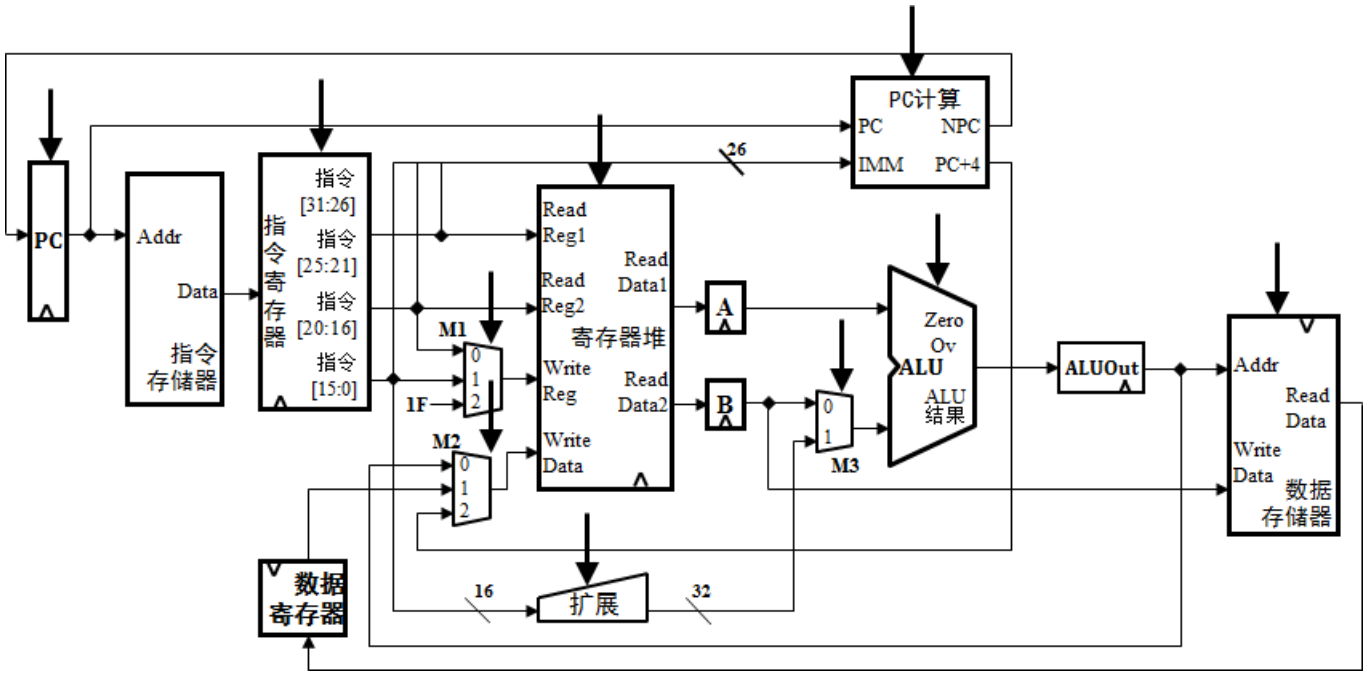
- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL

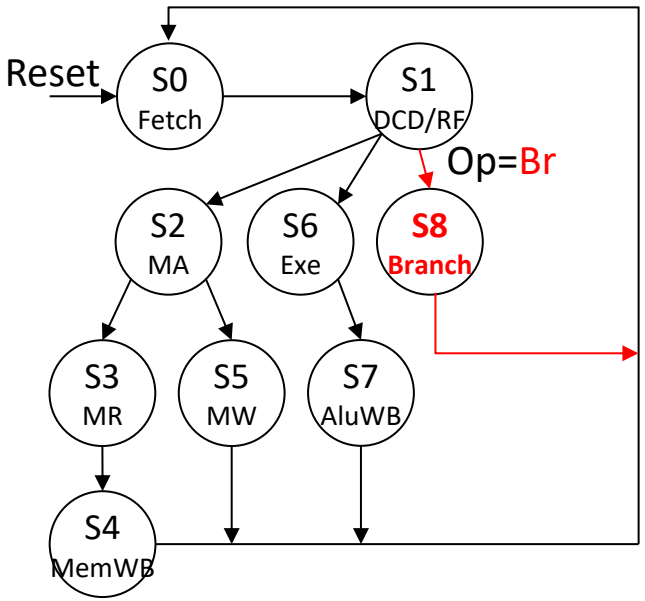
```
beq     if(R[rs]==R[rt])
           then PC←PC+4+[sign_ext(imm16)||00]
           else PC←PC+4
```



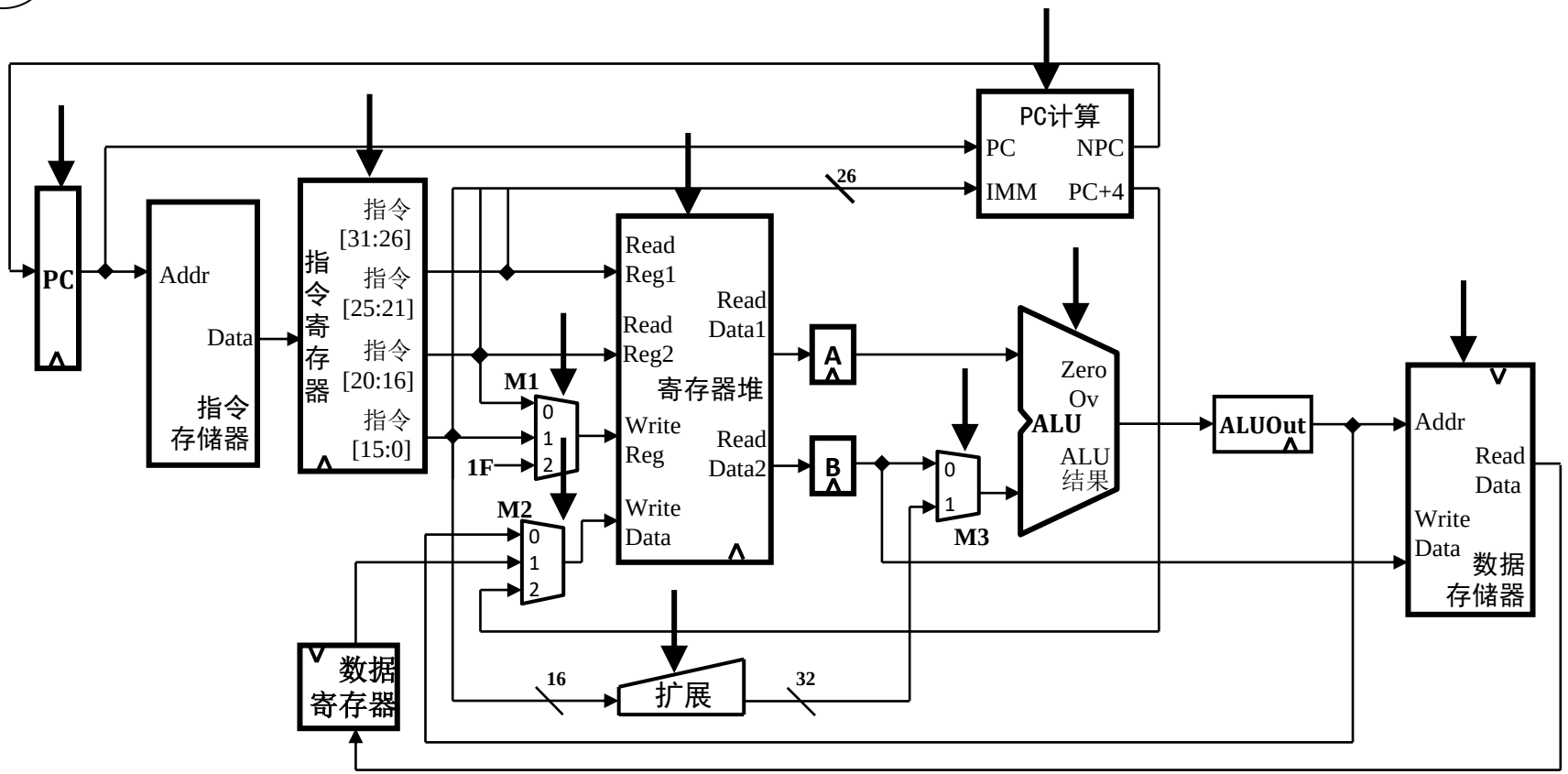



| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | | | Zero | |
| NPCOp | PC+4 | BEQ | | | | | | | | |
| IRWr | 1 | 0 | | | | | | | | |
| GPRWr | 0 | 0 | | | | | | | | |
| DMWr | 0 | 0 | | | | | | | | |
| ALUOp | X | SUB | | | | | | | SUB | |
| GPRSel | X | X | | | | | | | X | |
| WDSel | X | X | | | | | | | X | |
| ExtOp | X | X | | | | | | | X | |
| BSel | X | 0 | | | | | | | 0 | |





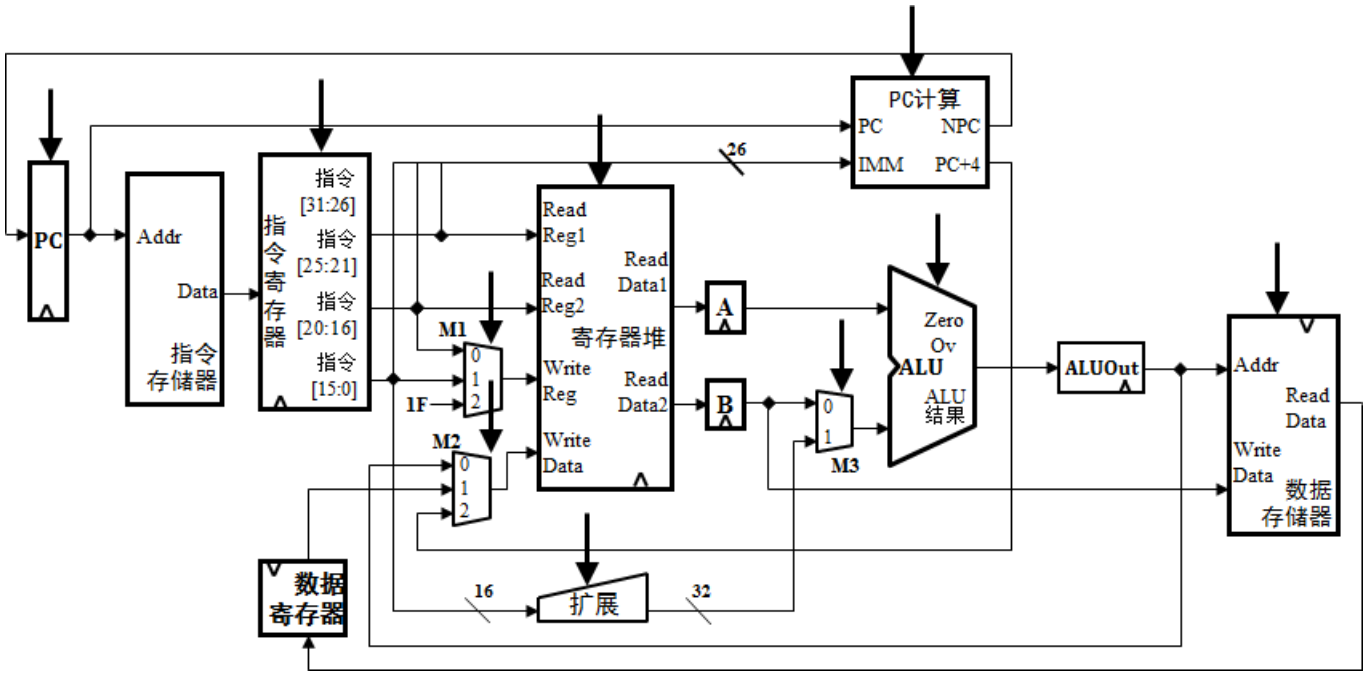

| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | | | Zero | |
| NPCOp | PC+4 | BEQ | | | | | | | | |
| IRWr | 1 | 0 | | | | | | | | |
| GPRWr | 0 | 0 | | | | | | | | |
| DMWr | 0 | 0 | | | | | | | | |
| ALUOp | X | SUB | | | | | | | SUB | |
| GPRSel | X | X | | | | | | | X | |
| WDSel | X | X | | | | | | | X | |
| ExtOp | X | X | | | | | | | X | |
| BSel | X | 0 | | | | | | | 0 | |

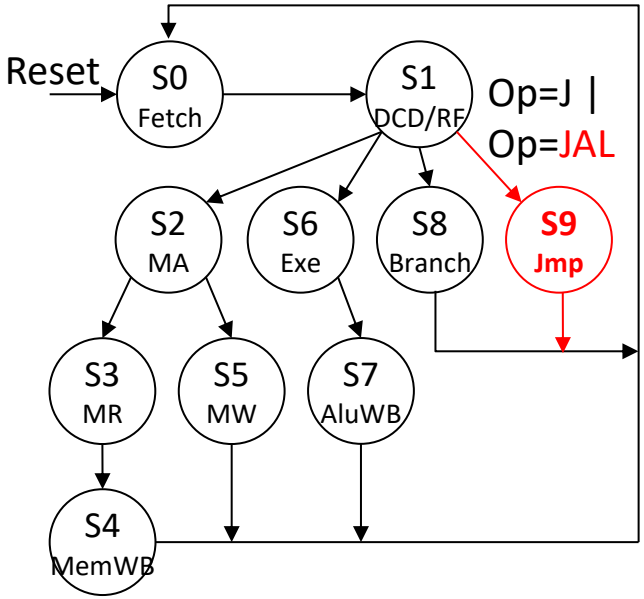


# FSM构造过程

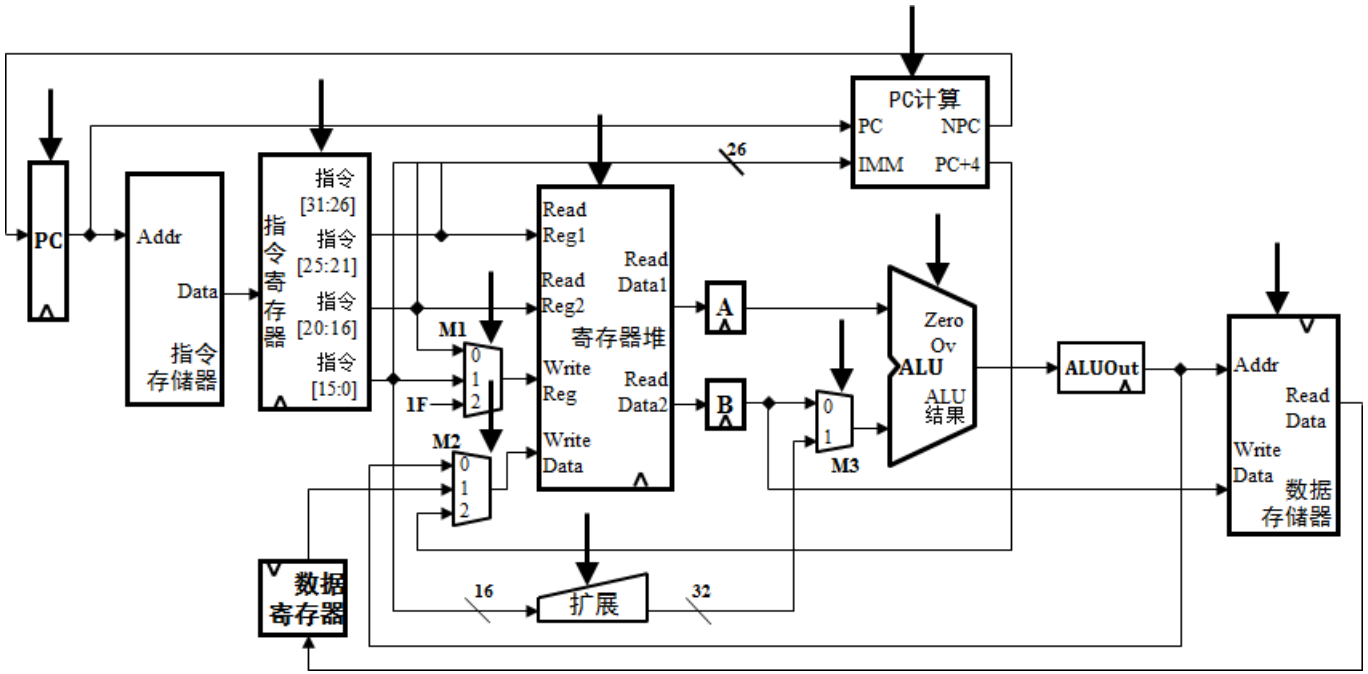
- LW，SW，ADDU，SUBU，ORI，LUI，BEQ，JAL

```
I:   GPR[31]← PC + 4
I+1:PC      ← PC_GPRLEN-1..28 || instr_index || 0^2
```






| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | 1 | 0 | | | | | | | | 1 |
| NPCOp | PC+4 | BEQ | | | | | | | | JAL |
| IRWr | 1 | 0 | | | | | | | | 0 |
| GPRWr | 0 | 0 | | | | | | | | 1 |
| DMWr | 0 | 0 | | | | | | | | 0 |
| ALUOp | X | X | | | | | | | | X |
| GPRSel | X | 10 | | | | | | | | 10 |
| WDSel | X | 10 | | | | | | | | 10 |
| ExtOp | X | X | | | | | | | | X |
| BSel | X | X | | | | | | | | X |



# 综合信号：第1步

- 用变量表达所有指令

```
beq = op[5]'·op[4]'·op[3]'·op[2]·op[1]'·op[0]'

。。。

Rtype = op[5]'·op[4]'·op[3]'·op[2]'·op[1]'·op[0]'

addu = Rtype·funct[5] ·funct[4]'·funct[3]'·
                funct[2]'·funct[1]'·funct[0]
```

| | Op | Funct |
|---|---|---|
| LW | 100011 | |
| SW | 101011 | |
| ADDU | 000000 | 100001 |
| SUBU | 000000 | 100011 |
| ORI | 001101 | |
| LUI | 001111 | |
| BEQ | 000100 | |
| JAL | 000011 | |

# 综合信号：第2步

- 给状态机分配寄存器
  - S0～S9：4个寄存器，fsm[3:0]
- 定义状态编号
- 用变量表达状态

```
S0 = fsm[3]'·fsm[2]'·fsm[1]'·fsm[0]'
S1 = fsm[3]'·fsm[2]'·fsm[1]'·fsm[0]
S2 = fsm[3]'·fsm[2]'·fsm[1] ·fsm[0]'
…
S8 = fsm[3] ·fsm[2]'·fsm[1]'·fsm[0]'
S9 = fsm[3] ·fsm[2]'·fsm[1]'·fsm[0]
```

| 状态名 | 编号 |
|---|---|
| S0 | 0000 |
| S1 | 0001 |
| S2 | 0010 |
| S3 | 0011 |
| S4 | 0100 |
| S5 | 0101 |
| S6 | 0110 |
| S7 | 0111 |
| S8 | 1000 |
| S9 | 1001 |

# 综合信号：第3步(以PCWr为例)

| | Op | Funct | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LW | 100011 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SW | 101011 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ADDU | 000000 | 100001 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SUBU | 000000 | 100011 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ORI | 001101 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| LUI | 001111 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BEQ | 000100 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | zero | 0 |
| JAL | 000011 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

PCWr = (lw+sw+addu+subu+ori+lui+beq+jal)·S0 +

(beq·zero)·S8 +

jal·S9

由于S0是所有指令的公共状态，可以优化为

PCWr = S0 +

(beq·zero)·S8 +

jal·S9

# 合并

- 构造出N类表
  - N << 56!
- 示例：PCWr
  - 抽取：N张表分别抽取PCWr的所有真值
  - 真值：形成PCWr的真值表
  - 方程：真值表化简

**注意：**

⇨ 某些信号(ALUOp)可能需要二次真值表

ADD

| | Op | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | | 1 | 0 | | | | | 0 | 0 | | |

SW

| | Op | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | | 1 | 0 | 0 | | | 0 | | | | |

LW

| | Op | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCWr | | 1 | 0 | 0 | 0 | 0 | | | | | |
| IRWr | | 1 | 0 | 0 | 0 | 0 | | | | | |
| RFDataSrc | 01 | | | | | | | | | | |
| RegDst | 00 | | | | | | | | | | |
| ExtOp | S | | | | | | | | | | |
| RegWr | | 0 | 0 | 0 | 0 | 1 | | | | | |
| ALUSrcA | | 00 | X | 1 | X | X | | | | | |
| ALUSrcB | | 01 | X | 10 | XX | XX | | | | | |
| ALUOp | | 00 | X | 00 | XX | XX | | | | | |
| PCSrc | | 00 | X | XX | XX | XX | | | | | |
| MemWr | | 0 | 0 | 0 | 0 | 0 | | | | | |