

计算机学院专业基础课

---

# 计算机组成

## MIPS单周期数据通路

高小鹏

北京航空航天大学计算机学院  
系统结构研究所

# 提纲

- 内容主要取材
  - ▣ CS617的20讲
- 处理器设计
- 数据通路概述
- 组装数据通路
- 控制介绍

# Great Idea #1: Levels of Representation/Interpretation

Higher-Level Language  
Program (e.g. C)

*Compiler*

Assembly Language  
Program (e.g. MIPS)

*Assembler*

Machine Language  
Program (MIPS)

```
temp = v[k];  
v[k] = v[k+1];  
v[k+1] = temp;
```

```
lw    $t0, 0($2)  
lw    $t1, 4($2)  
sw    $t1, 0($2)  
sw    $t0, 4($2)
```

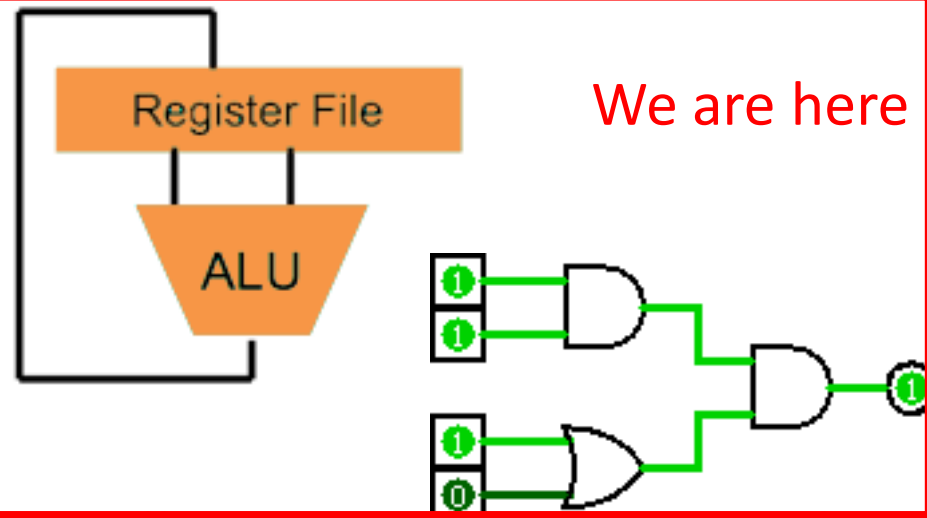
```
0000 1001 1100 0110 1010 1111 0101 1000  
1010 1111 0101 1000 0000 1001 1100 0110  
1100 0110 1010 1111 0101 1000 0000 1001  
0101 1000 0000 1001 1100 0110 1010 1111
```

*Machine  
Interpretation*

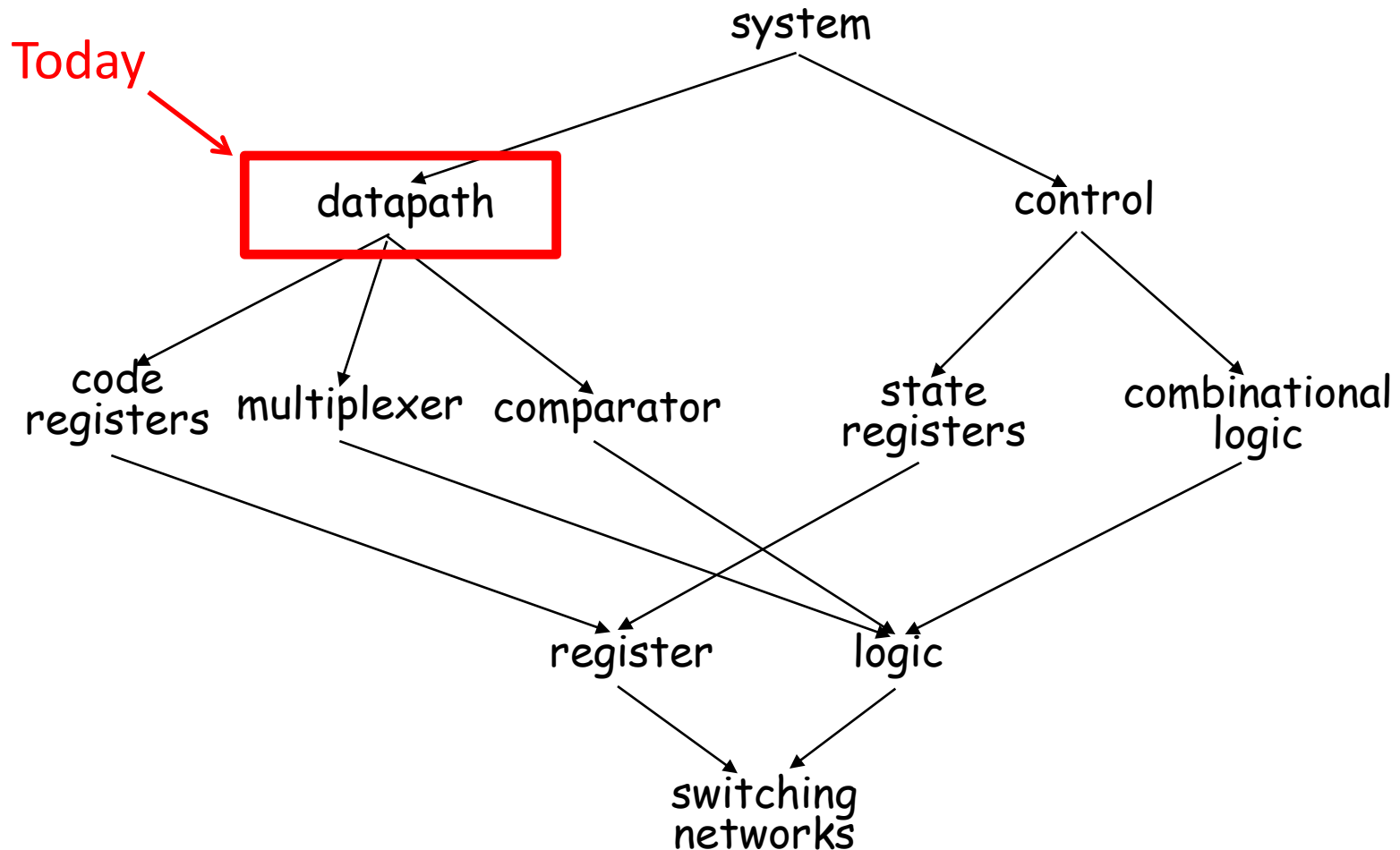
Hardware Architecture Description  
(e.g. block diagrams)

*Architecture  
Implementation*

Logic Circuit Description  
(Circuit Schematic Diagrams)



# Hardware Design Hierarchy

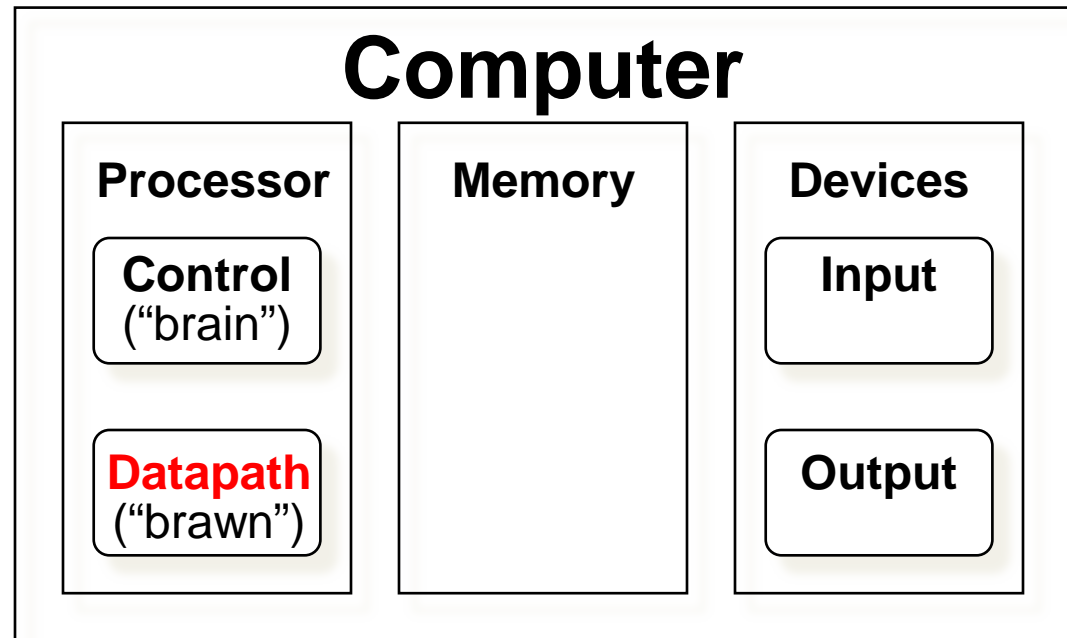


# 提纲

- 内容主要取材
  - ▣ CS617的20讲
- 处理器设计
- 数据通路概述
- 组装数据通路
- 控制介绍

# Five Components of a Computer

- Components a computer needs to work
  - Control
  - Datapath
  - Memory
  - Input
  - Output

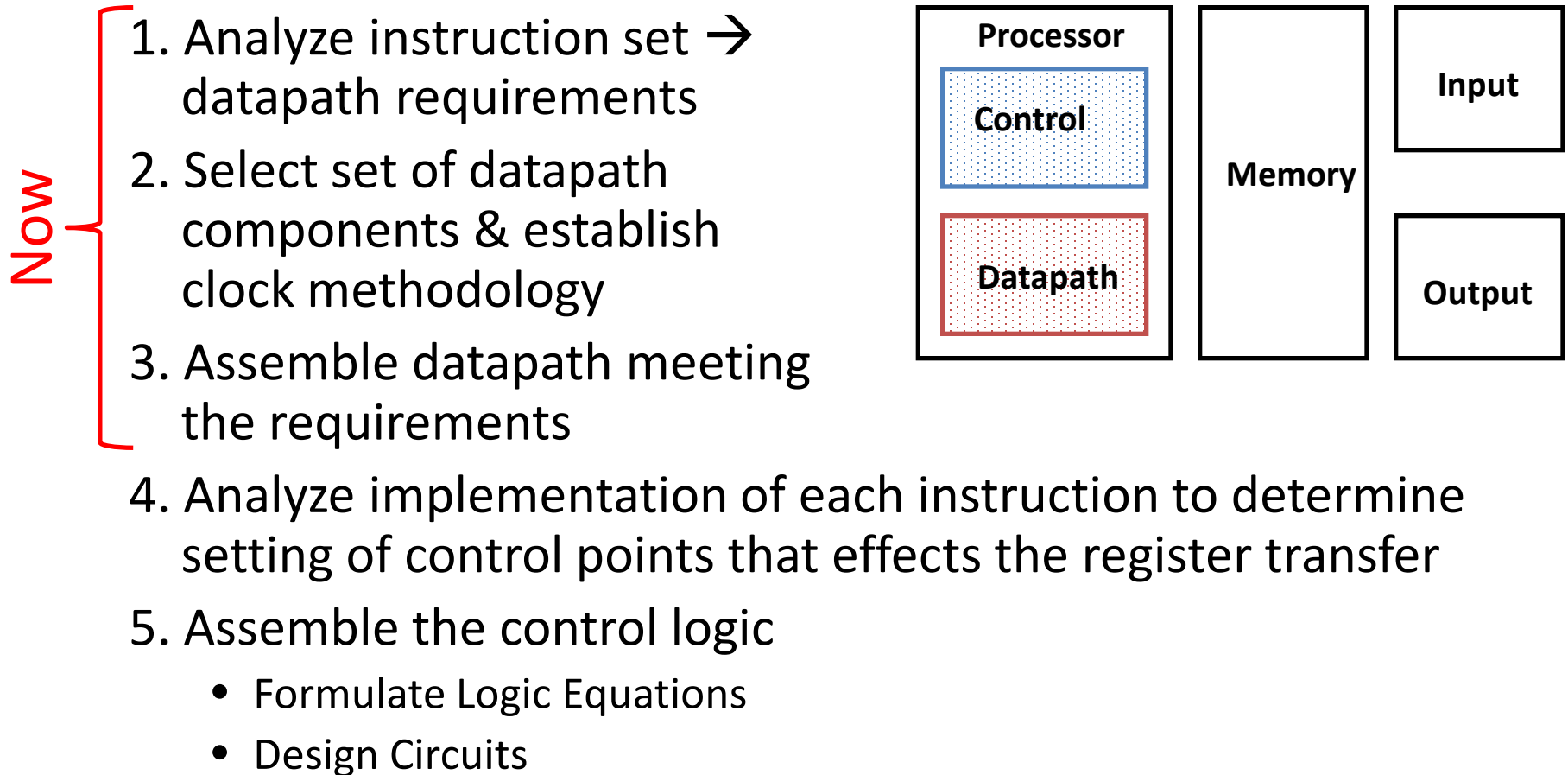


# The Processor

- **Processor (CPU):** Implements the instructions of the Instruction Set Architecture (ISA)
  - **Datapath:** part of the processor that contains the hardware necessary to perform operations required by the processor (“the brawn”)
  - **Control:** part of the processor (also in hardware) which tells the datapath what needs to be done (“the brain”)

# Processor Design Process

- Five steps to design a processor:

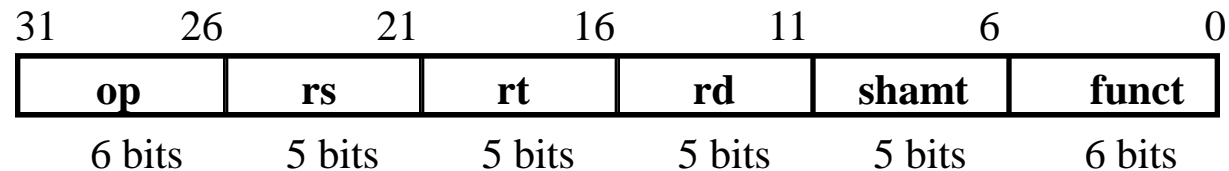




# The MIPS-lite Instruction Subset

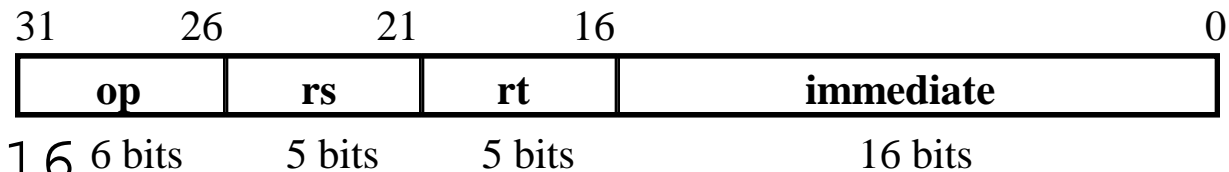
- ADDU and SUBU

- `addu rd,rs,rt`
- `subu rd,rs,rt`



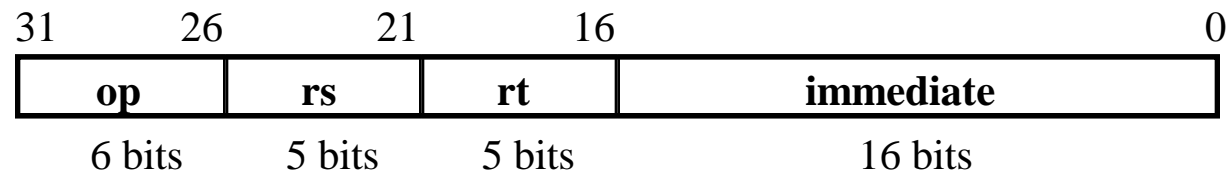
- OR Immediate:

- `ori rt,rs,imm16`



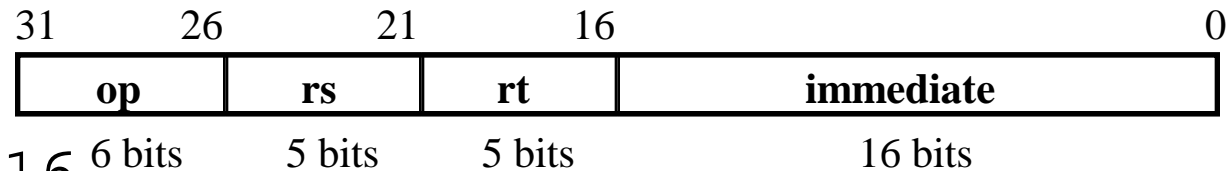
- LOAD and  
STORE Word

- `lw rt,rs,imm16`
- `sw rt,rs,imm16`



- BRANCH:

- `beq rs,rt,imm16`



# Register Transfer Language (RTL)

- All start by *fetching* the instruction:

R-format:  $\{op, rs, rt, rd, shamt, funct\} \leftarrow \text{MEM}[PC]$

I-format:  $\{op, rs, rt, imm16\} \leftarrow \text{MEM}[PC]$

- RTL gives the meaning of the instructions:

## **Inst    Register Transfers**

ADDU     $R[rd] \leftarrow R[rs] + R[rt]; \quad PC \leftarrow PC + 4$

SUBU     $R[rd] \leftarrow R[rs] - R[rt]; \quad PC \leftarrow PC + 4$

ORI     $R[rt] \leftarrow R[rs] \mid \text{zero\_ext}(imm16); \quad PC \leftarrow PC + 4$

LOAD     $R[rt] \leftarrow \text{MEM}[R[rs] + \text{sign\_ext}(imm16)]; \quad PC \leftarrow PC + 4$

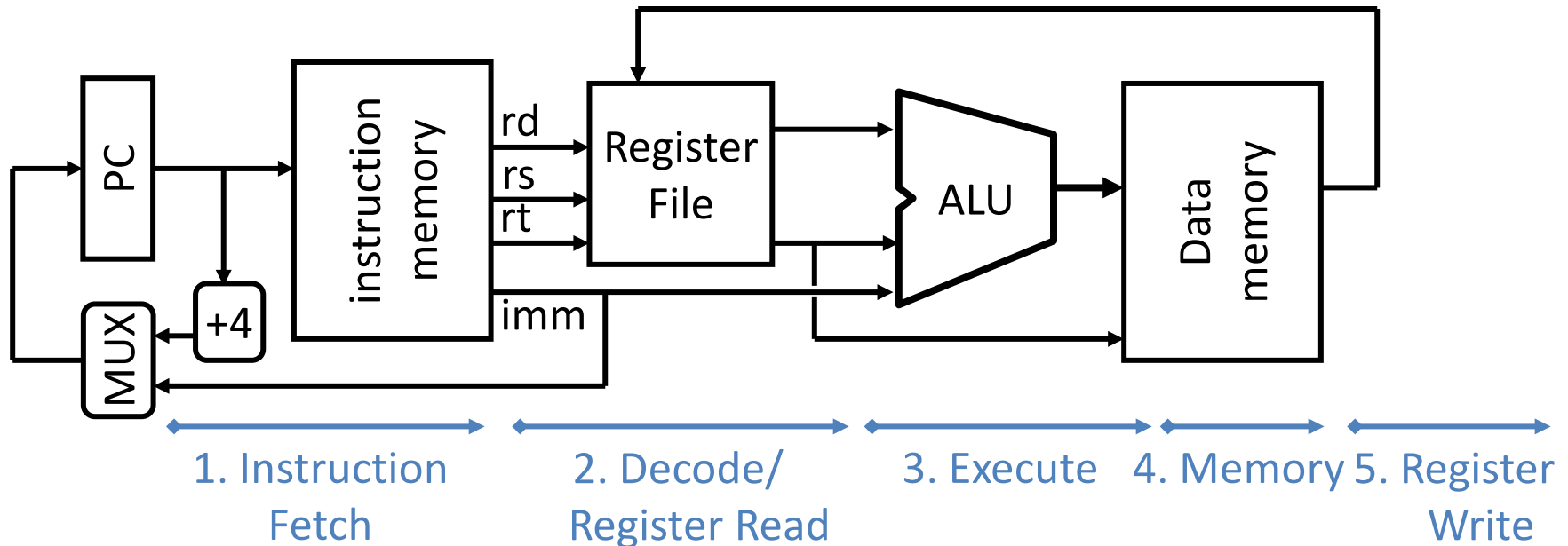
STORE     $\text{MEM}[R[rs] + \text{sign\_ext}(imm16)] \leftarrow R[rt]; \quad PC \leftarrow PC + 4$

BEQ     $\text{if } (R[rs] == R[rt])$   
          then  $PC \leftarrow PC + 4 + (\text{sign\_ext}(imm16) \mid \mid 00)$   
          else  $PC \leftarrow PC + 4$

# Step 1: Requirements of the Instruction Set

- Memory (MEM)
  - Instructions & data (separate: in reality just caches)
  - Load from and store to
- Registers (32 32-bit regs)
  - Read *rs* and *rt*
  - Write *rt* or *rd*
- PC
  - Add 4 (+ maybe extended immediate)
- Extender (sign/zero extend)
- Add/Sub/OR unit for operation on register(s) or extended immediate
  - Compare if registers equal?

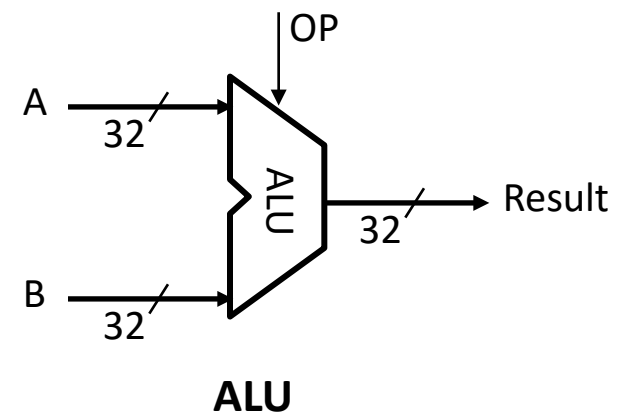
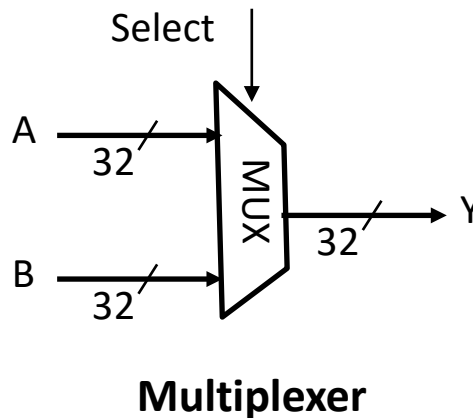
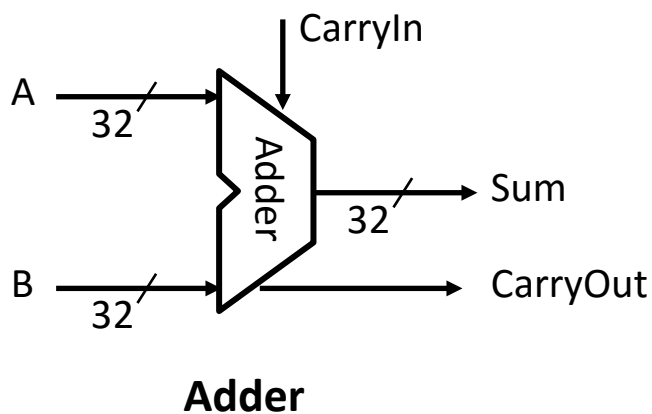
# Generic Datapath Layout



- Break up the process of “executing an instruction”
  - Smaller phases easier to design and modify independently
- ~~Proj1 had 3 phases: Fetch, Decode, Execute~~
  - ~~Now expand Execute~~

## Step 2: Components of the Datapath

- Combinational Elements
  - Gates and wires
- State Elements + Clock
- Building Blocks:



# ALU Requirements

- MIPS-lite: add, sub, OR, equality

ADDU         $R[rd] = R[rs] + R[rt]; \dots$

SUBU         $R[rd] = R[rs] - R[rt]; \dots$

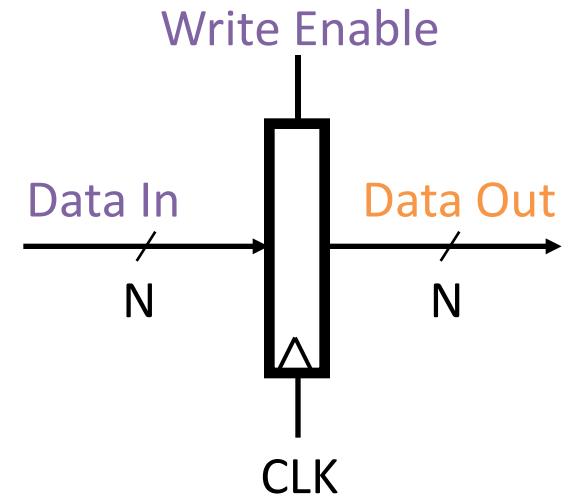
ORI          $R[rt] = R[rs] \mid \text{zero\_ext}(\text{Imm16}) \dots$

BEQ          $\text{if } (R[rs] == R[rt]) \dots$

- Equality test: Use subtraction and implement output to indicate if result is 0
- P&H also adds AND, Set Less Than (1 if  $A < B$ , 0 otherwise)
- Can see ALU from P&H C.5 (on CD)

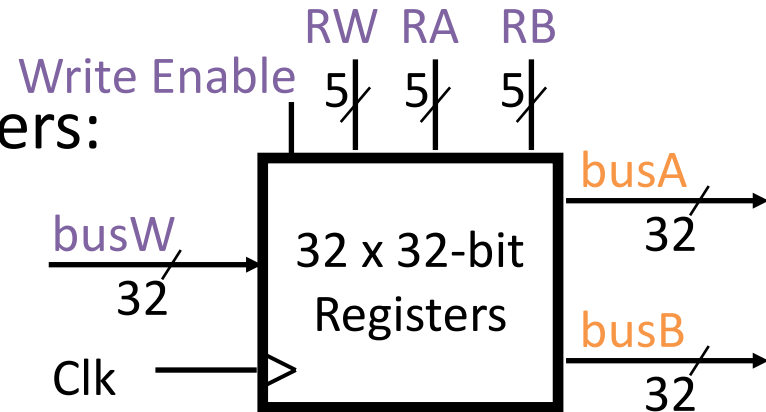
# Storage Element: Register

- As seen in Logisim intro
  - N-bit input and output buses
  - Write Enable input
- Write Enable:
  - De-asserted (0): Data Out will not change
  - Asserted (1): Data In value placed onto Data Out on the rising edge of CLK



# Storage Element: Register File

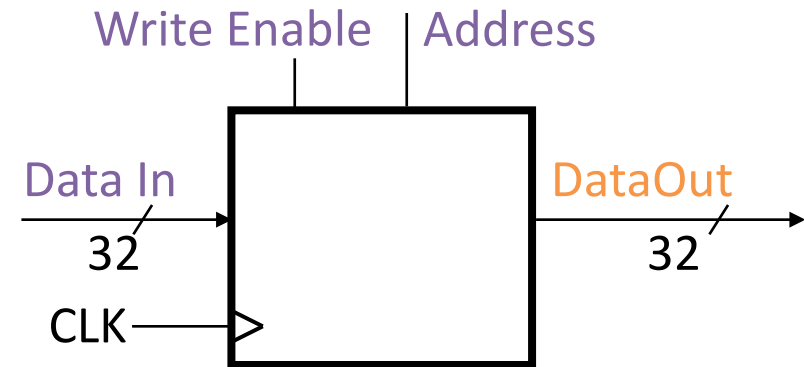
- **Register File** consists of 32 registers:
  - Output buses **busA** and **busB**
  - Input bus **busW**
- Register selection
  - Place data of register **RA** (number) onto **busA**
  - Place data of register **RB** (number) onto **busB**
  - Store data on **busW** into register **RW** (number) when **Write Enable** is 1
- Clock input (CLK)
  - CLK input is a factor ONLY during write operation
  - During read, behaves as a combinational logic block:  
**RA** or **RB** valid → **busA** or **busB** valid after “access time”





# Storage Element: Idealized Memory

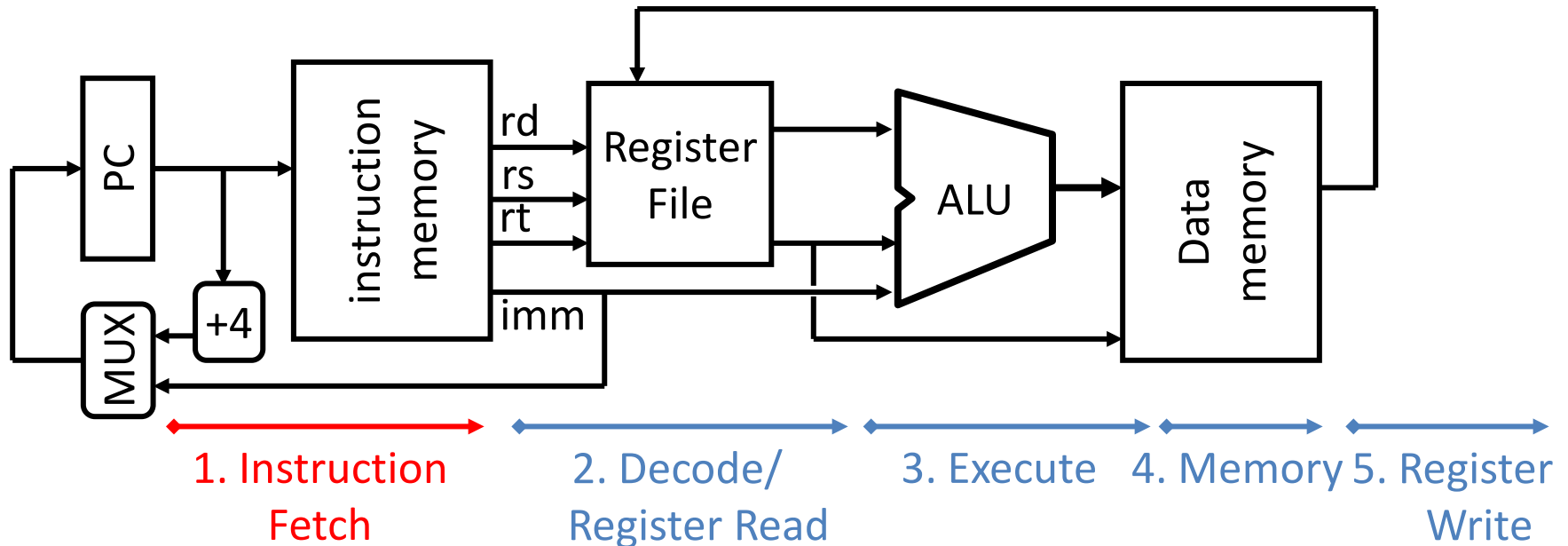
- Memory (idealized)
  - One input bus: Data In
  - One output bus: Data Out
- Memory access:
  - Read: Write Enable = 0, data at Address is placed on Data Out
  - Write: Write Enable = 1, Data In written to Address
- Clock input (CLK)
  - CLK input is a factor ONLY during write operation
  - During read, behaves as a combinational logic block: Address valid → Data Out valid after “access time”



# 提纲

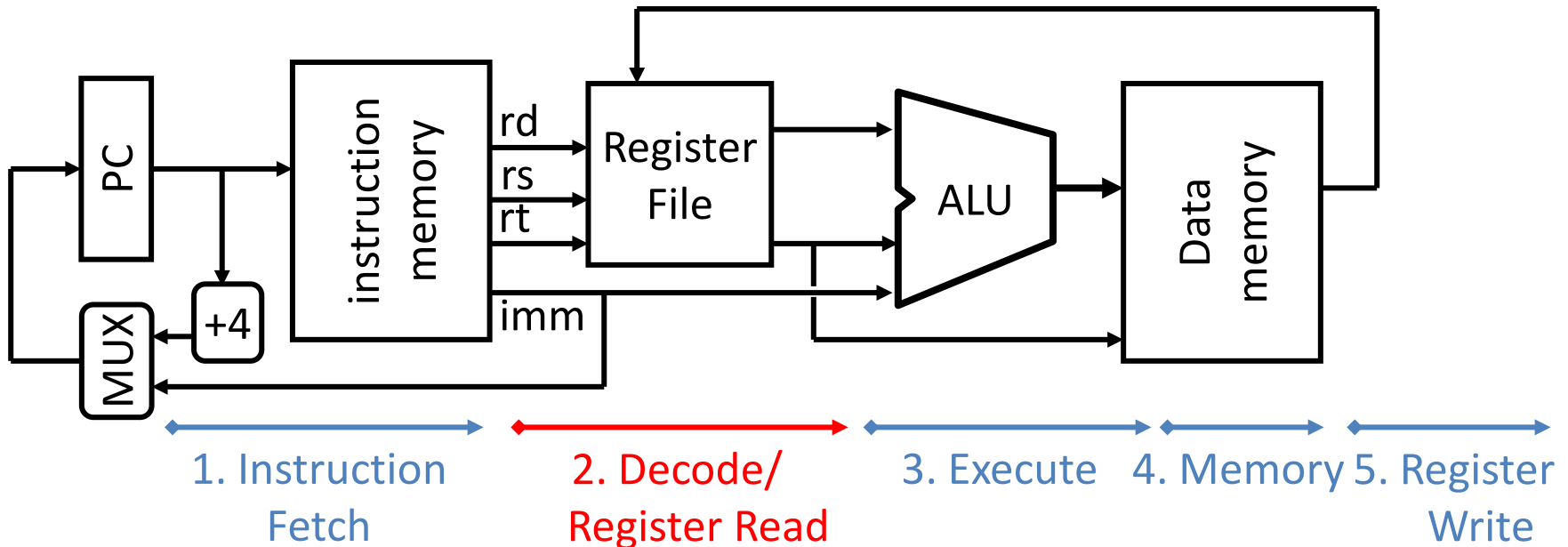
- 内容主要取材
  - ▣ CS617的20讲
- 处理器设计
- 数据通路概述
- 组装数据通路
- 控制介绍

# Datapath Overview (1/5)



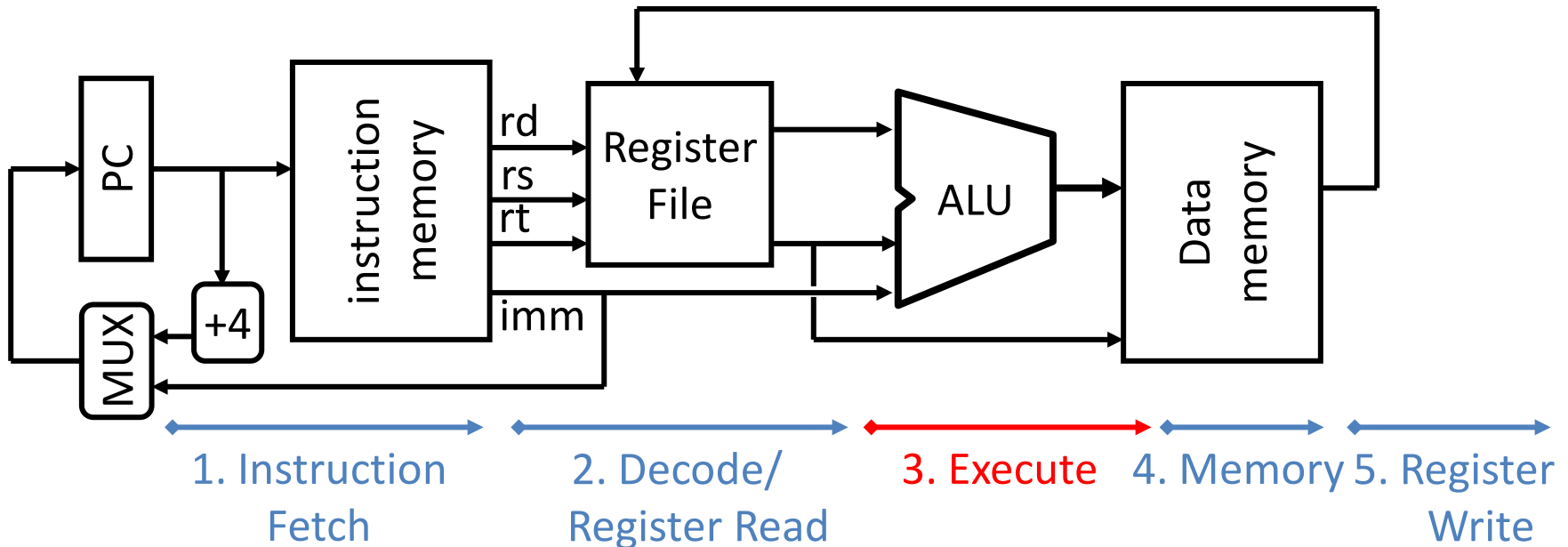
- Phase 1: *Instruction Fetch* (IF)
  - Fetch 32-bit instruction from memory
  - Increment PC ( $PC = PC + 4$ )

# Datapath Overview (2/5)



- Phase 2: *Instruction Decode* (ID)
  - Read the opcode and appropriate fields from the instruction
  - Gather all necessary registers values from Register File

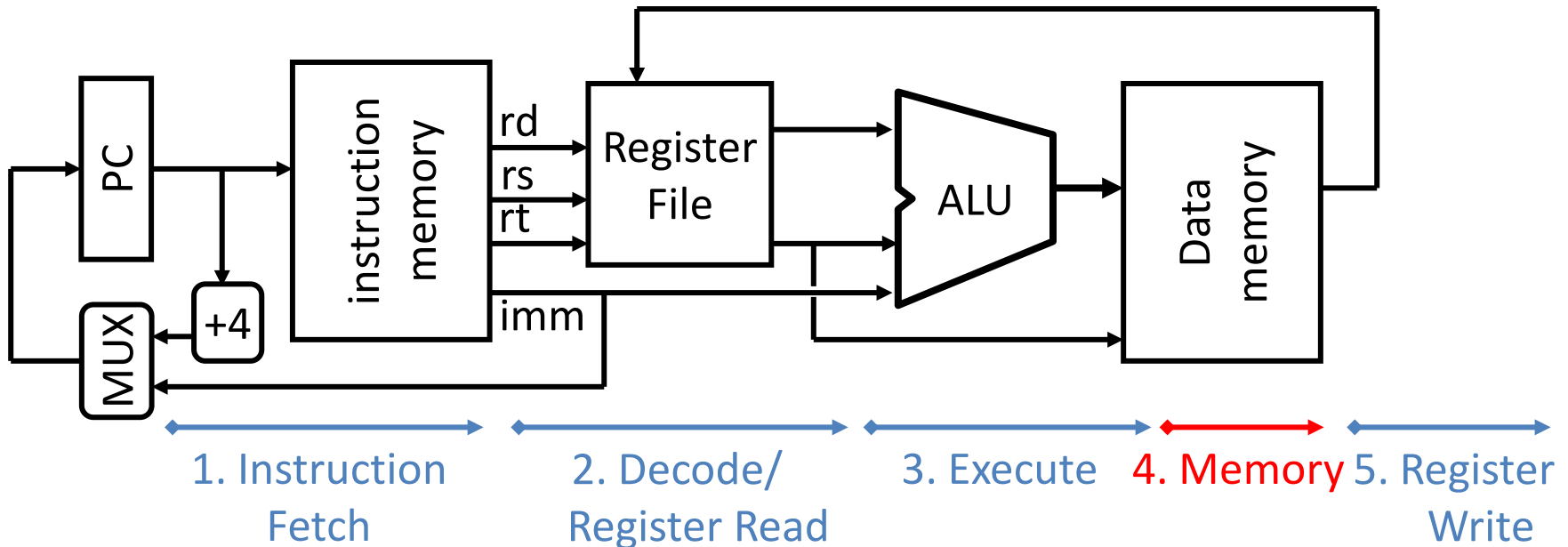
# Datapath Overview (3/5)



- Phase 3: *Execute* (EX)

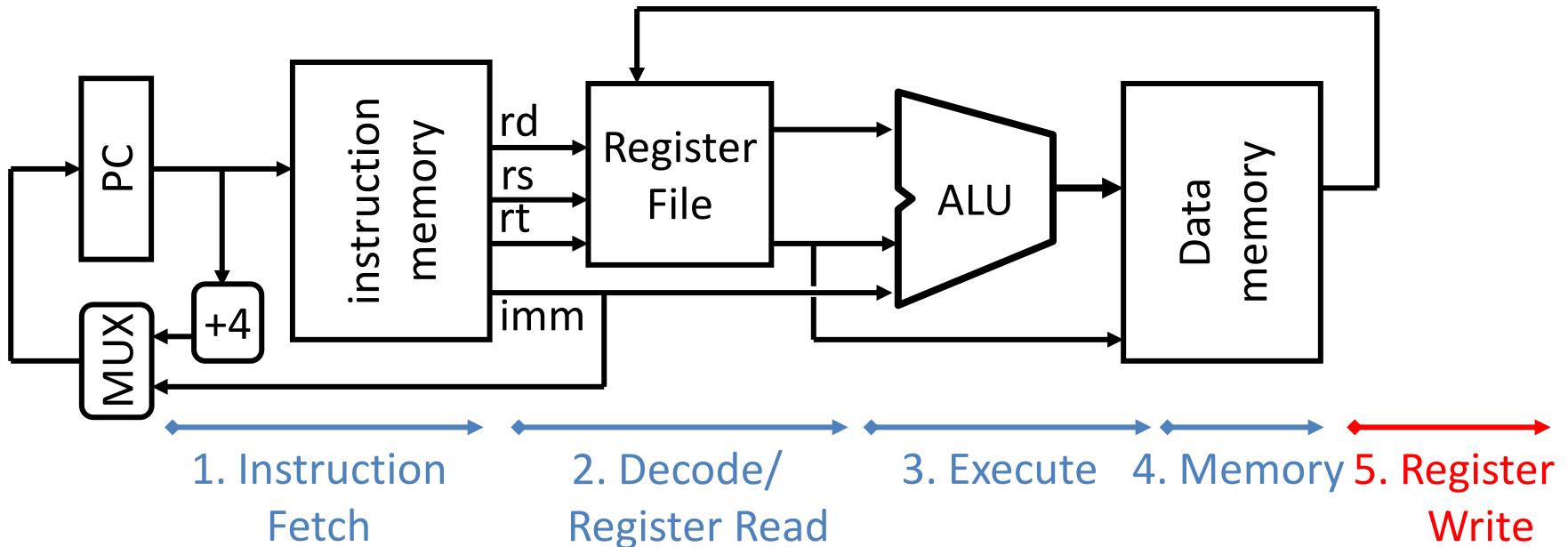
- ALU performs operations: arithmetic (+, -, \*, /), shifting, logical (&, |), comparisons (slt, ==)
- Also calculates addresses for loads and stores

# Datapath Overview (4/5)



- Phase 4: *Memory Access* (MEM)
  - Only load and store instructions do anything during this phase; the others remain idle or skip this phase
  - Should be fast due to caches

# Datapath Overview (5/5)



- Phase 5: *Register Write* (WB for “write back”)
  - Write the instruction result back into the Register File
  - Those that don’t (e.g. `sw`, `j`, `beq`) remain idle or skip this phase

# Why Five Stages?

- Could we have a different number of stages?
  - Yes, and other architectures do
- So why does MIPS have five if instructions tend to idle for at least one stage?
  - The five stages are the union of all the operations needed by all the instructions
  - There is one instruction that uses all five stages:  
*load* (1w/1b)



# 提纲

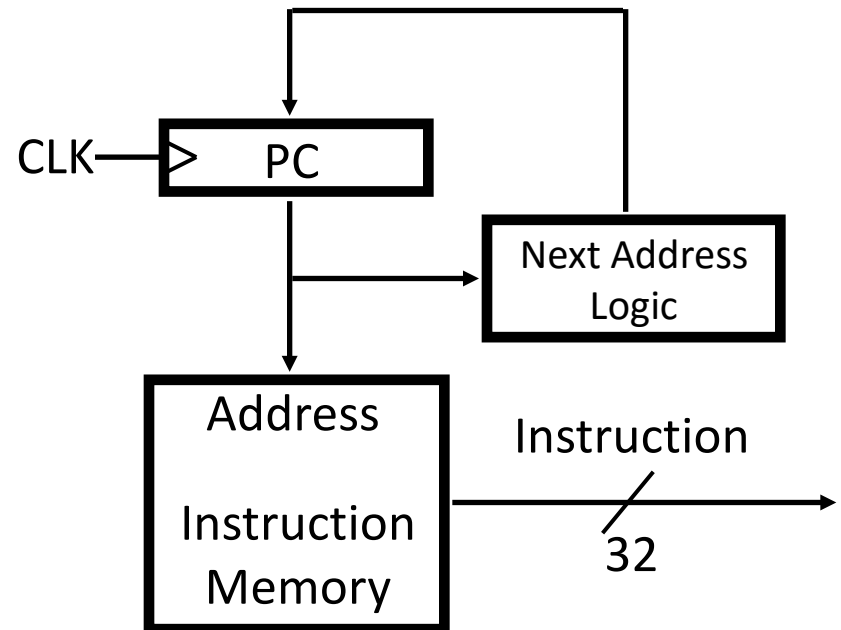
- 内容主要取材
  - ▣ CS617的20讲
- 处理器设计
- 数据通路概述
- 组装数据通路
- 控制介绍

# Step 3: Assembling the Datapath

- Assemble datapath to meet RTL requirements
  - Exact requirements will change based on ISA
  - Here we will examine *each instruction* of MIPS-lite
- The datapath is all of the hardware components and wiring necessary to carry out all of the different instructions
  - Make sure all components (e.g. RegFile, ALU) have access to all necessary signals and buses
  - Control will make sure instructions are properly executed (the decision making)

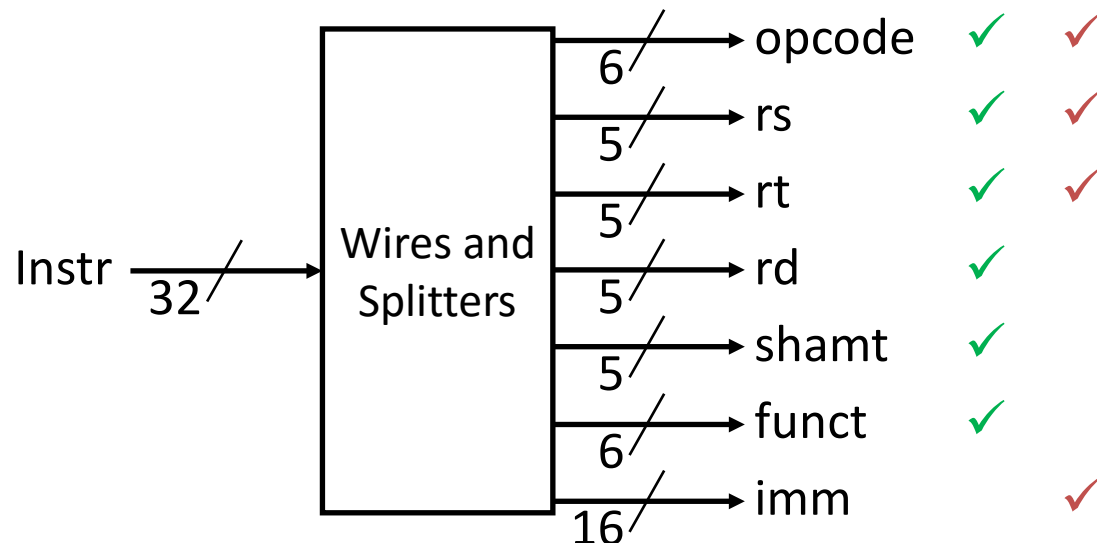
# Datapath by Instruction

- All instructions: *Instruction Fetch (IF)*
  - Fetch the Instruction:  $\text{mem}[\text{PC}]$
  - Update the program counter:
    - Sequential Code:  
 $\text{PC} \leftarrow \text{PC} + 4$
    - Branch and Jump:  
 $\text{PC} \leftarrow \text{“something else”}$



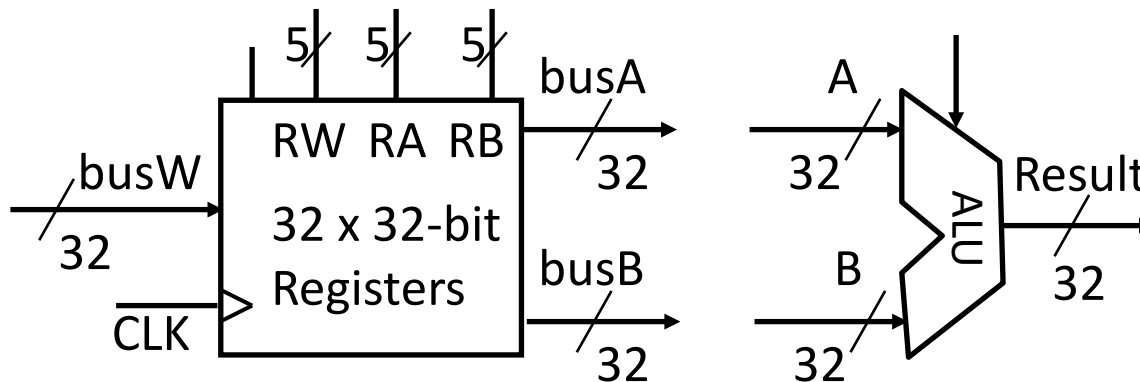
# Datapath by Instruction

- All instructions: *Instruction Decode (ID)*
  - Pull off all relevant fields from instruction to make available to other parts of datapath
    - MIPS-lite only has **R-format** and **I-format**
    - Control will sort out the proper routing (discussed later)



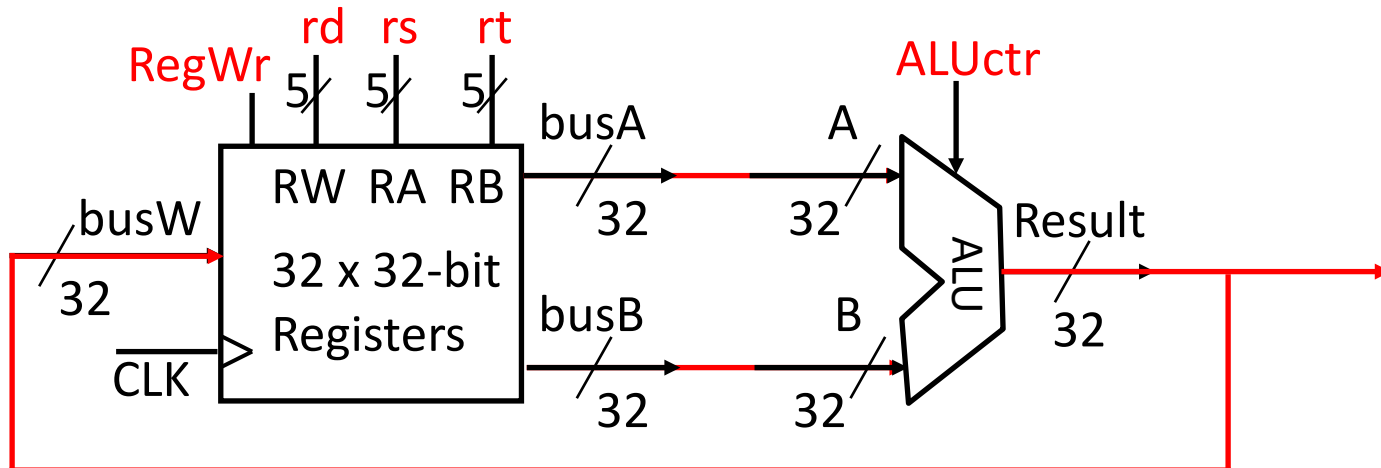
# Step 3: Add & Subtract

- $\text{ADDU } R[\text{rd}] \leftarrow R[\text{rs}] + R[\text{rt}] ;$
- Hardware needed:
  - Instruction Mem and PC (already shown)
  - Register File (RegFile) for read and write
  - ALU for add/subtract



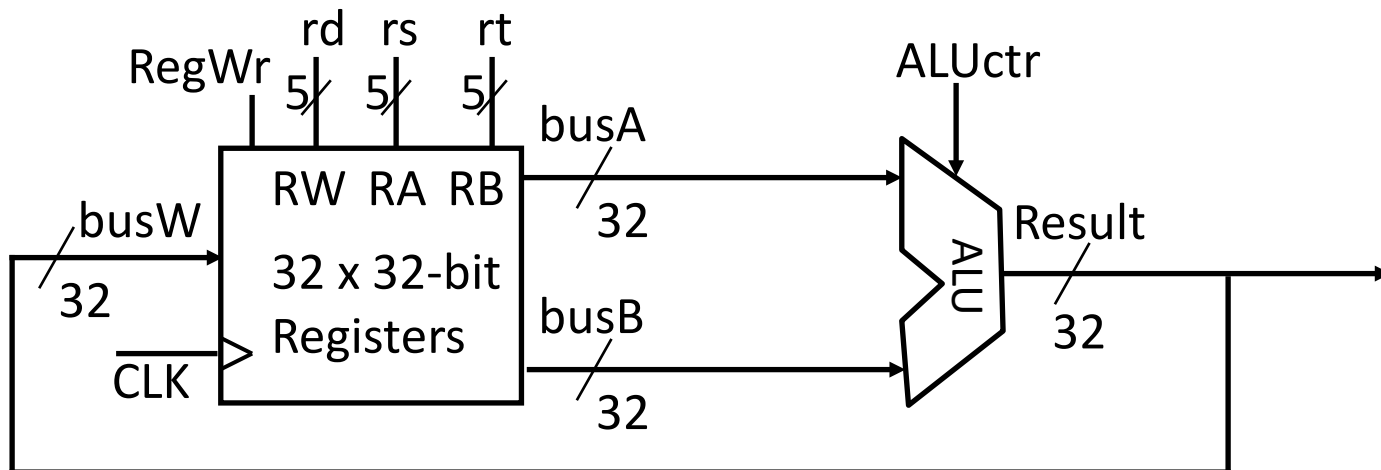
# Step 3: Add & Subtract

- $\text{ADDU } R[\text{rd}] \leftarrow R[\text{rs}] + R[\text{rt}] ;$
- Connections:
  - RegFile and ALU Inputs
  - Connect RegFile and ALU
  - RegWr (1) and ALUctr (ADD/SUB) set by control in **ID**



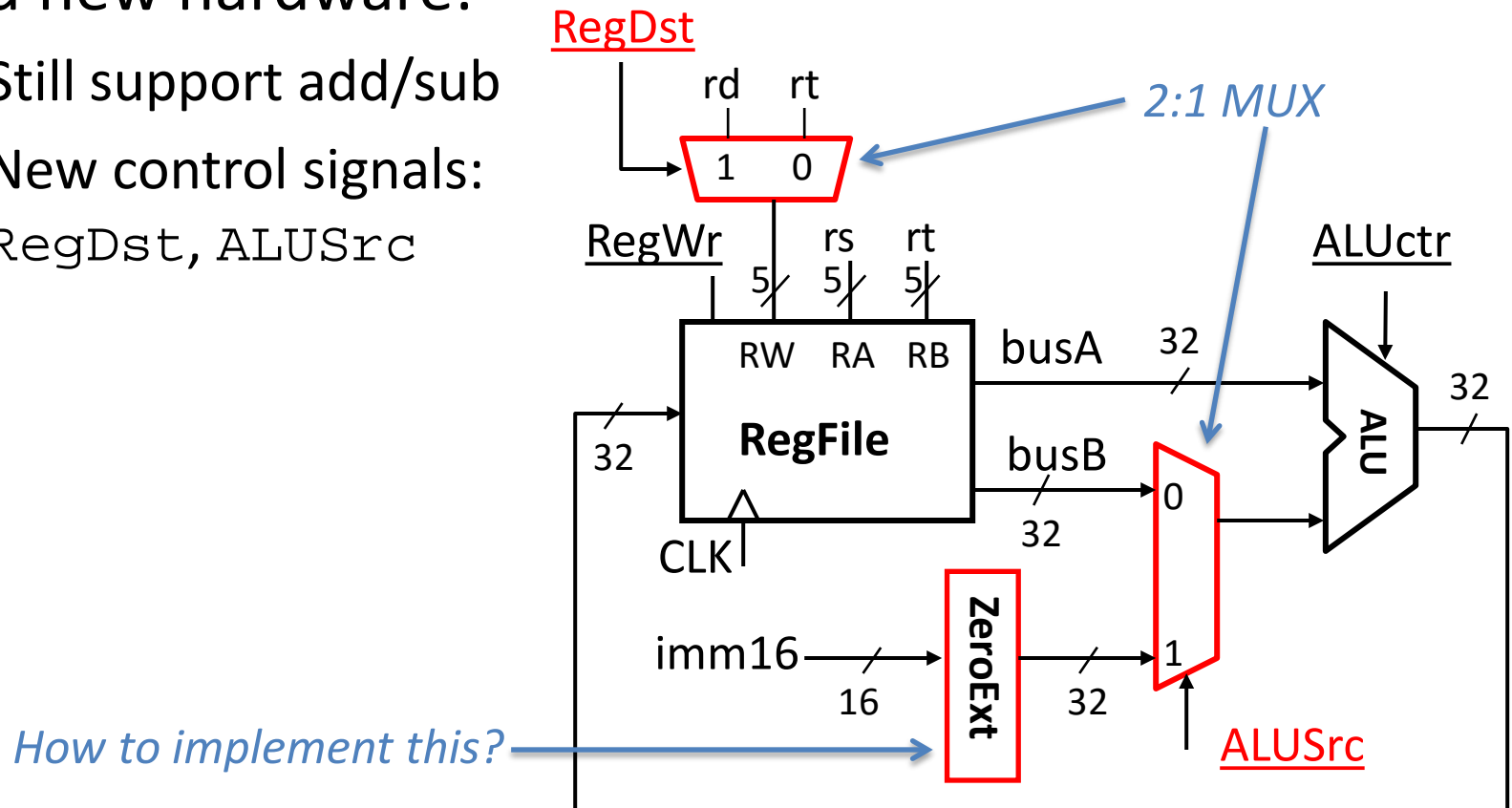
# Step 3: Or Immediate

- `ORI R[rt] ← R[rs] | zero_ext(Imm16) ;`
- Is the hardware below sufficient?
  - Zero extend `imm16`?
  - Pass `imm16` to input of ALU?
  - Write result to `rt`?



# Step 3: Or Immediate

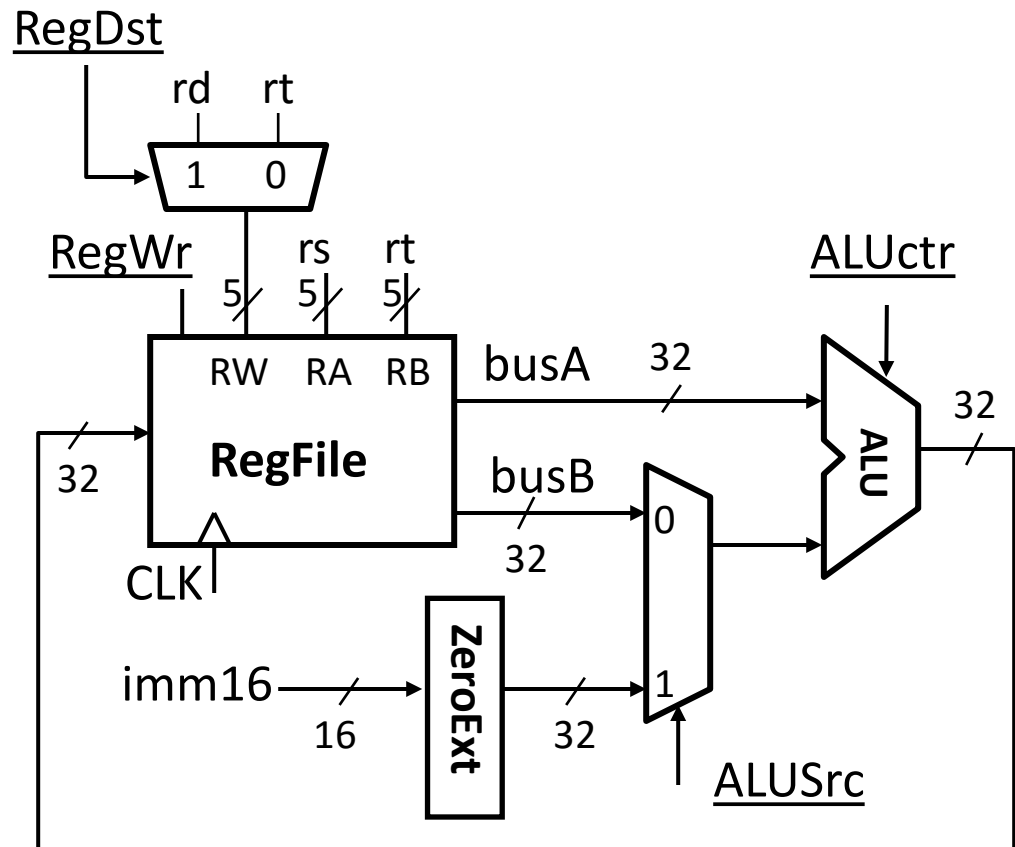
- $\text{ORI } R[\text{rt}] \leftarrow R[\text{rs}] \mid \text{zero\_ext}(\text{Imm16}) ;$
- Add new hardware:
  - Still support add/sub
  - New control signals:  
RegDst, ALUSrc





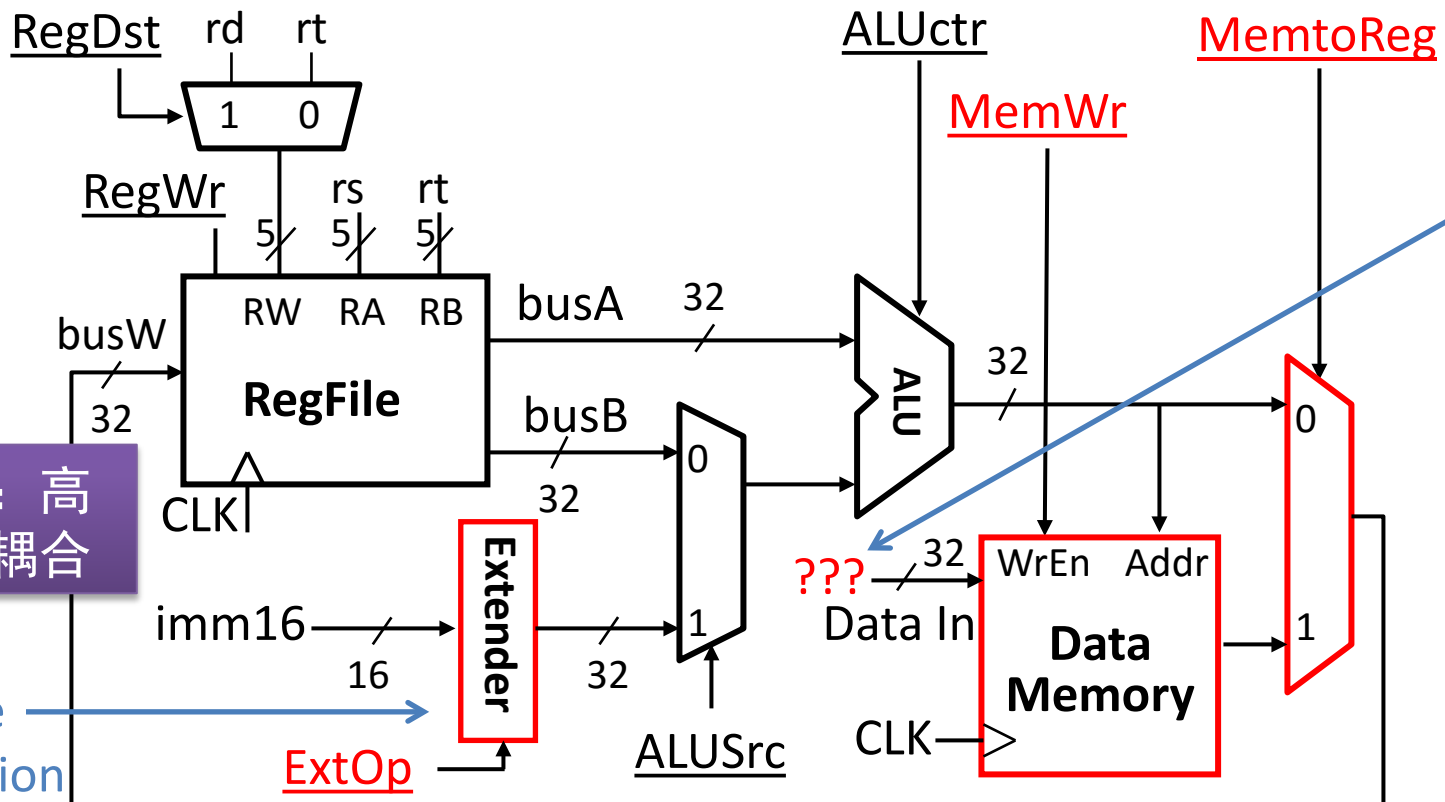
# Step 3: Load

- $\text{LOAD } R[rt] \leftarrow \text{MEM}[R[rs] + \text{sign\_ext}(\text{Imm16})];$
- Hardware sufficient?
  - Sign extend imm16?
  - Where's MEM?



## Step 3: Load

- `LOAD R[rt] ← MEM[R[rs] + sign_ext(Imm16)];`
- **New control signals:** `ExtOp`, `MemWr`, `MemtoReg`



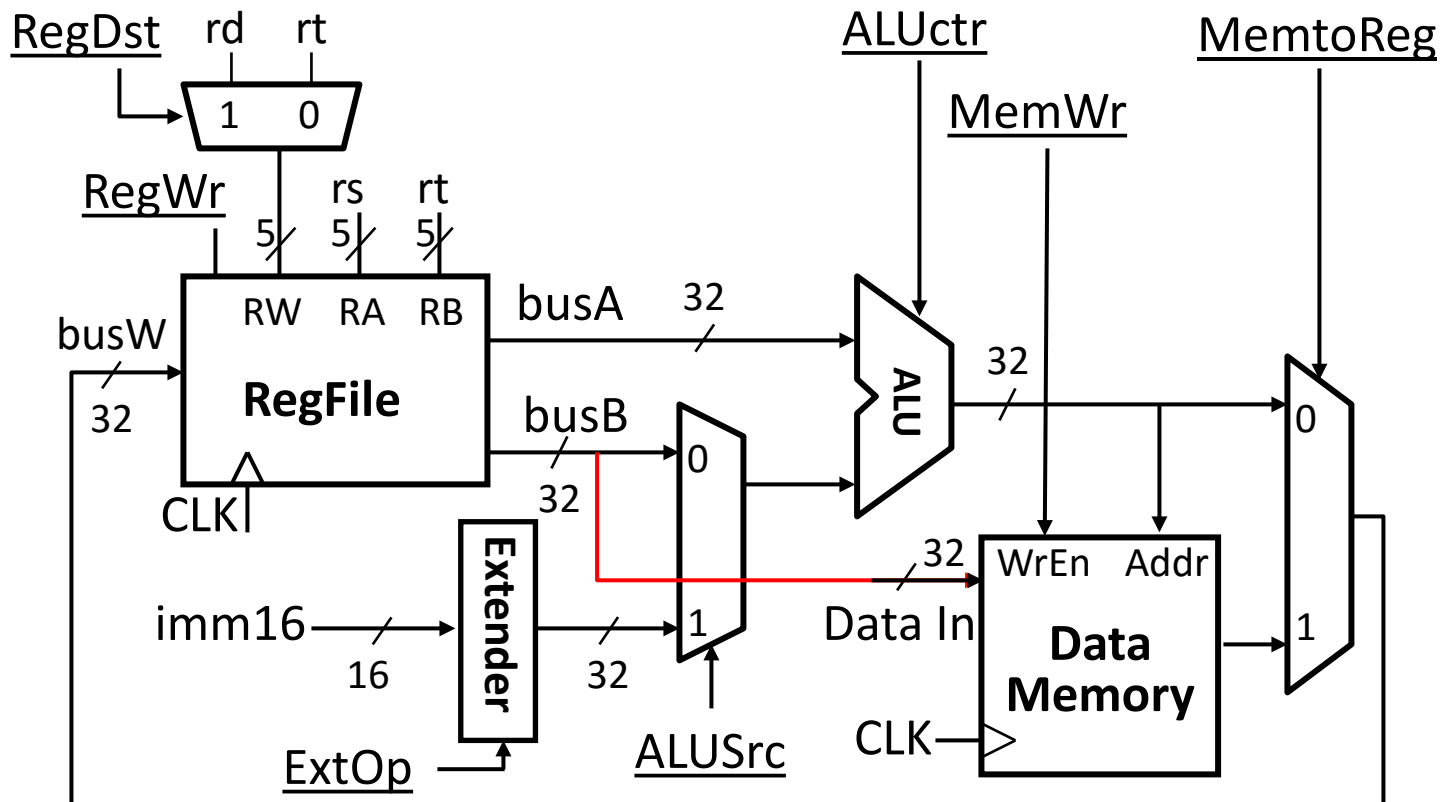
What goes here during a store?

## 设计原则：高内聚，低耦合

Must now  
also handle —  
sign extension

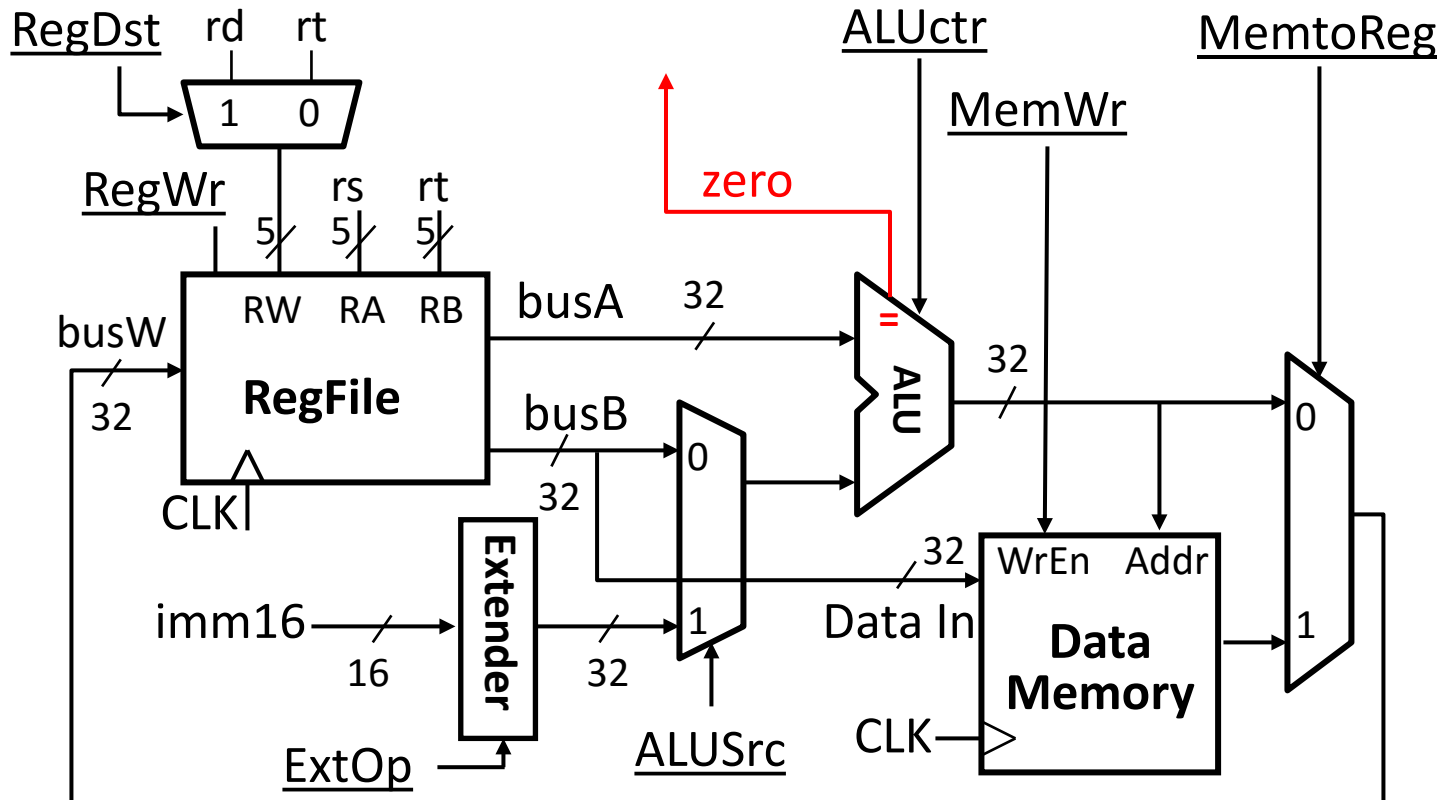
# Step 3: Store

- $\text{STORE MEM}[R[rs] + \text{sign\_ext}(\text{Imm16})] \leftarrow R[rt];$
- Connect busB to Data In (no extra control needed!)



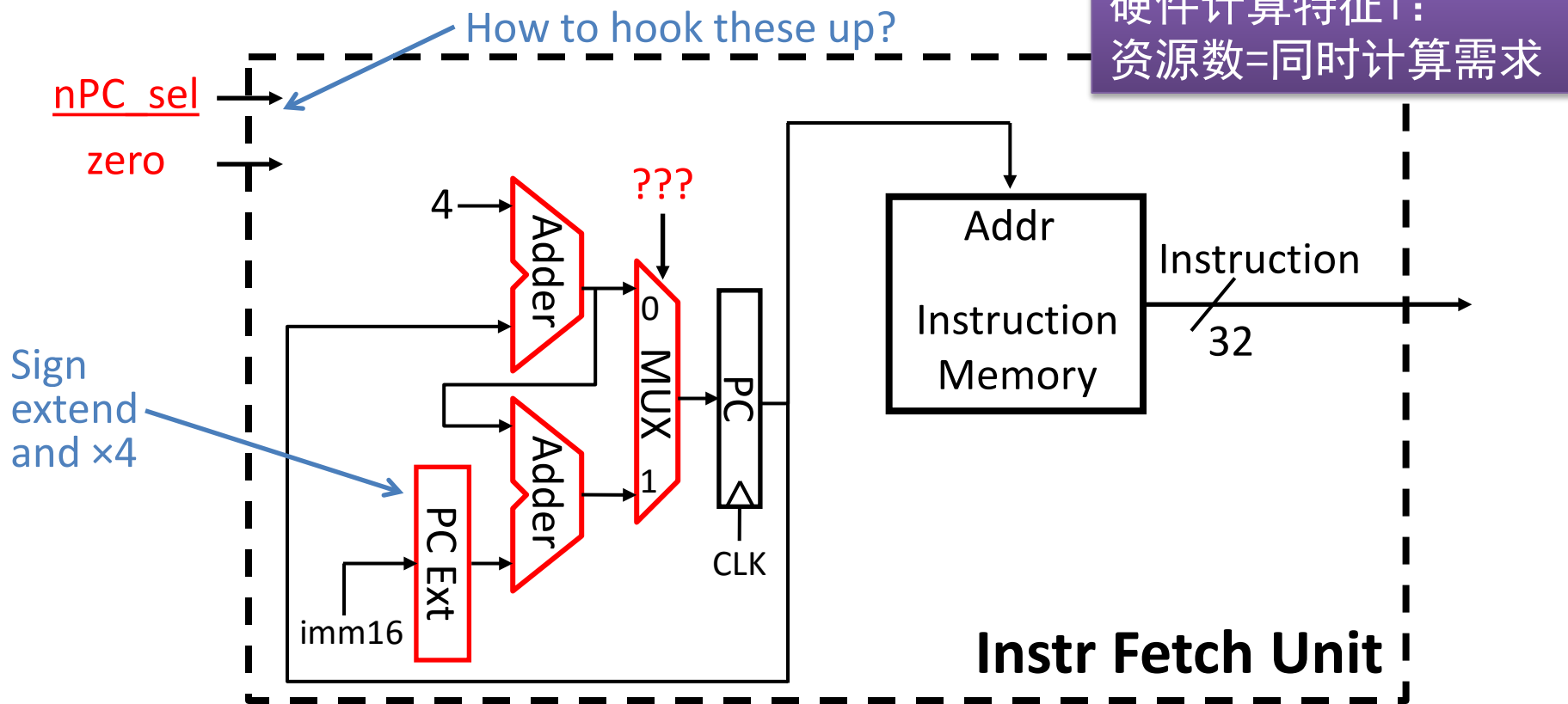
# Step 3: Branch If Equal

- $\text{BEQ if}(R[\text{rs}] == R[\text{rt}]) \text{ then } \text{PC} \leftarrow \text{PC} + 4 + (\text{sign\_ext}(\text{Imm16}) \parallel 00)$
- Need comparison output from ALU



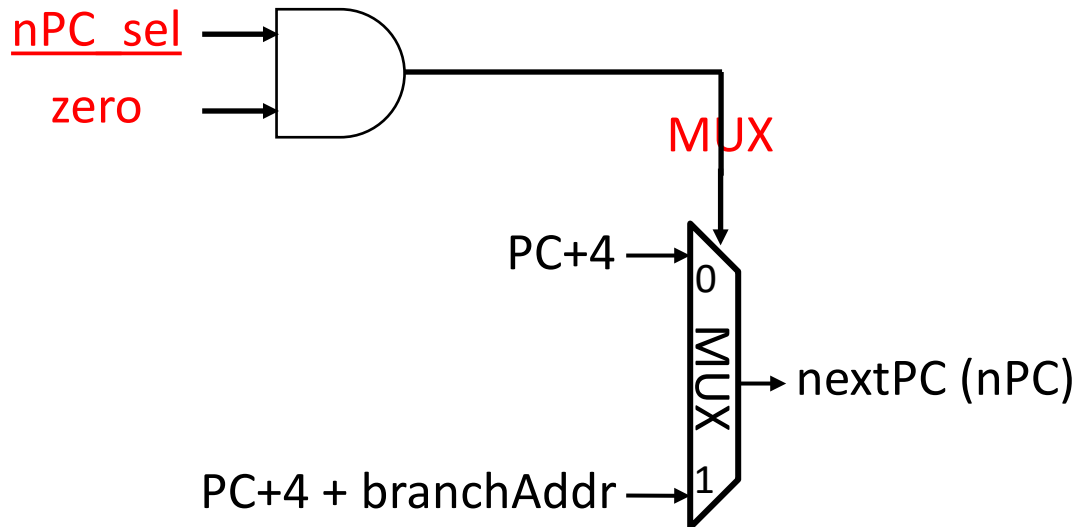
# Step 3: Branch If Equal

- $\text{BEQ if}(R[\text{rs}]==R[\text{rt}]) \text{ then } \text{PC} \leftarrow \text{PC}+4 + (\text{sign\_ext}(\text{Imm16}) \parallel 00)$
- Revisit “next address logic”:



# Step 3: Branch If Equal

- BEQ if( $R[rs] == R[rt]$ ) then  $PC \leftarrow PC+4 + (\text{sign\_ext}(\text{Imm16}) \parallel 00)$
- Revisit “next address logic”:
  - nPC\_sel should be 1 if branch, 0 otherwise

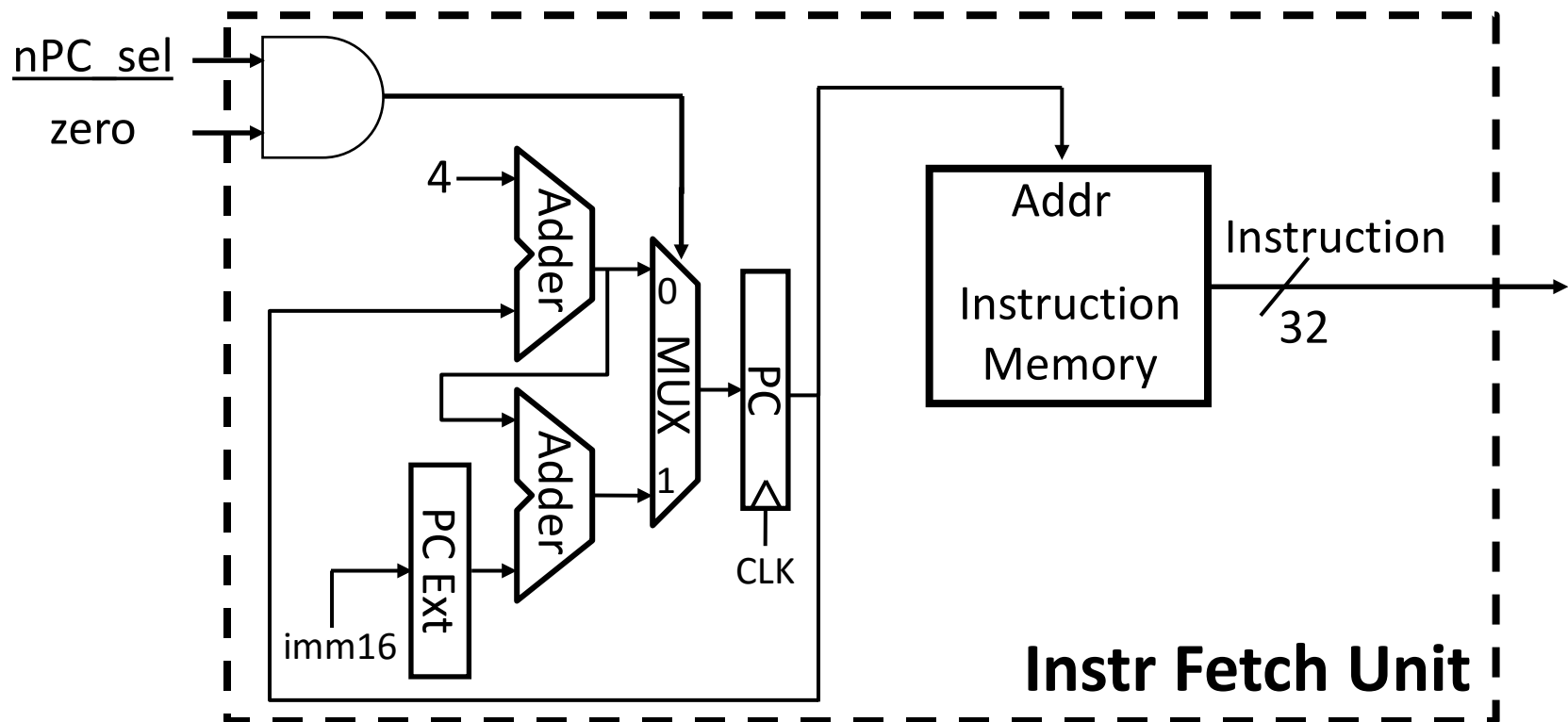


nPC_sel	zero	MUX
0	0	0
0	1	0
1	0	0
1	1	1

*How does this change  
if we add bne?*

# Step 3: Branch If Equal

- BEQ if( $R[rs] == R[rt]$ ) then  $PC \leftarrow PC + 4 + (\text{sign\_ext}(\text{Imm16}) \ll 00)$
- Revisit “next address logic”:



# 提纲

- 内容主要取材
  - ▣ CS617的20讲
- 处理器设计
- 数据通路概述
- 组装数据通路
- 控制介绍

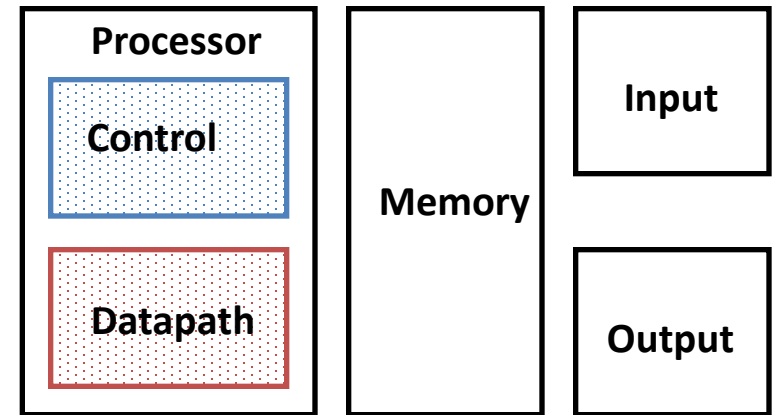


# Processor Design Process

- Five steps to design a processor:

1. Analyze instruction set → datapath requirements
2. Select set of datapath components & establish clock methodology
3. Assemble datapath meeting the requirements

- Now** {
4. Analyze implementation of each instruction to determine setting of control points that effects the register transfer
  5. Assemble the control logic
    - Formulate Logic Equations
    - Design Circuits

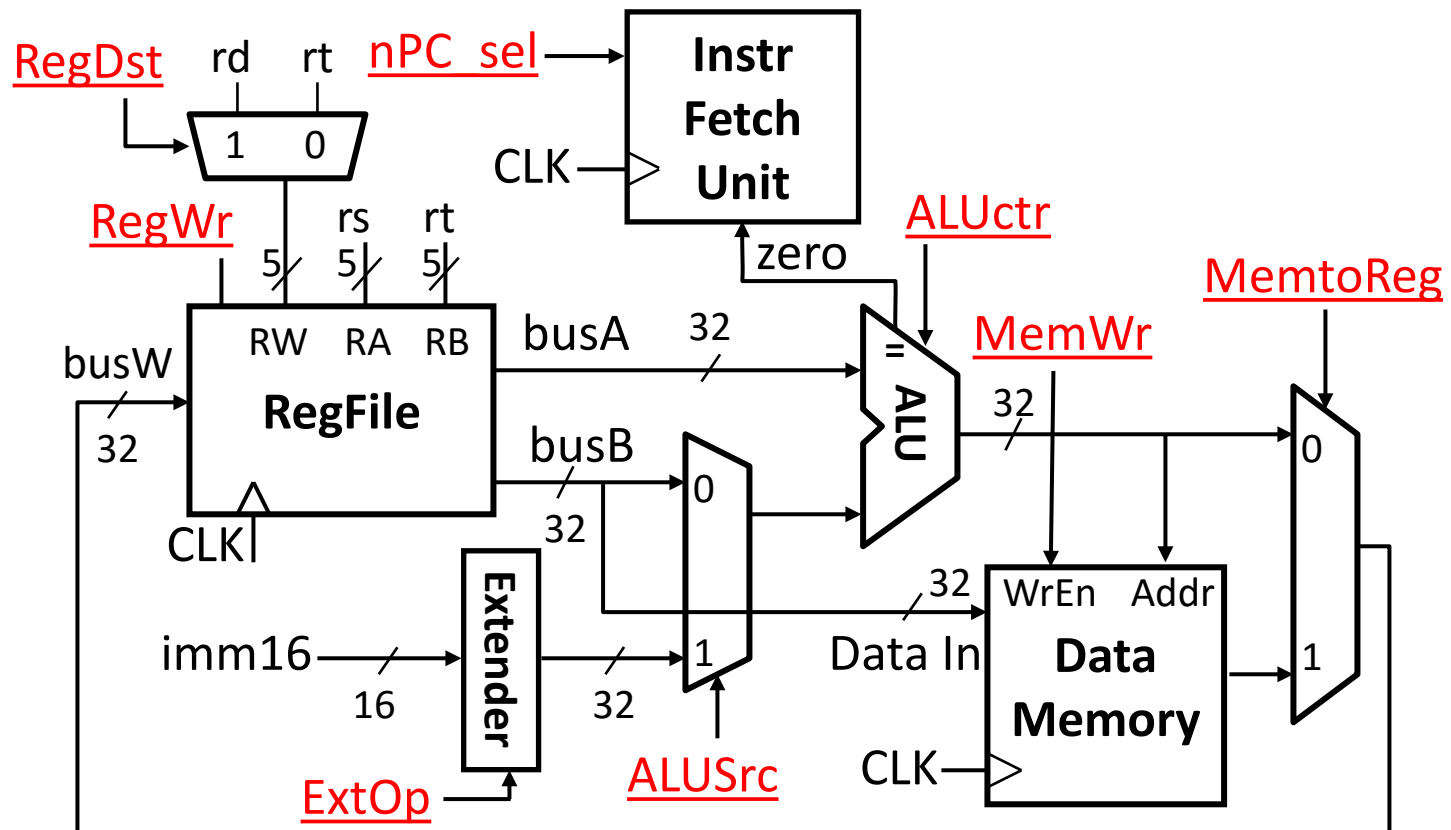


# Control

- Need to make sure that correct parts of the datapath are being used for each instruction
  - Have seen *control signals* in datapath used to select inputs and operations
  - For now, focus on what value each control signal should be for each instruction in the ISA
  - Next lecture, we will see how to implement the proper combinational logic to implement the control

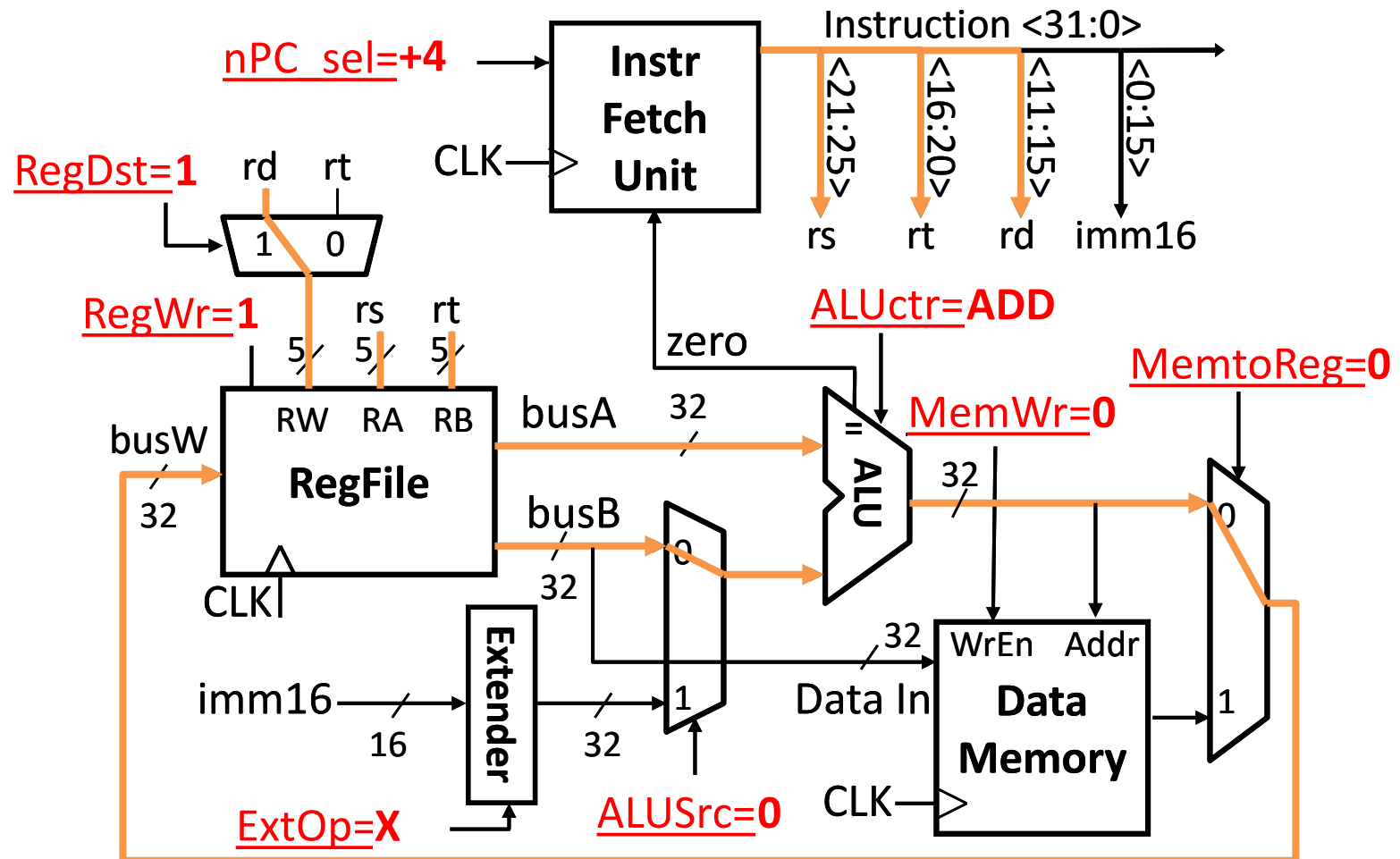
# MIPS-lite Datapath Control Signals

- **ExtOp:** 0 → “zero”; 1 → “sign”
- **ALUsrc:** 0 → busB; 1 → imm16
- **ALUctr:** “ADD”, “SUB”, “OR”
- **nPC\_sel:** 0 → +4; 1 → branch
- **MemWr:** 1 → write memory
- **MemtoReg:** 0 → ALU; 1 → Mem
- **RegDst:** 0 → “rt”; 1 → “rd”
- **RegWr:** 1 → write register



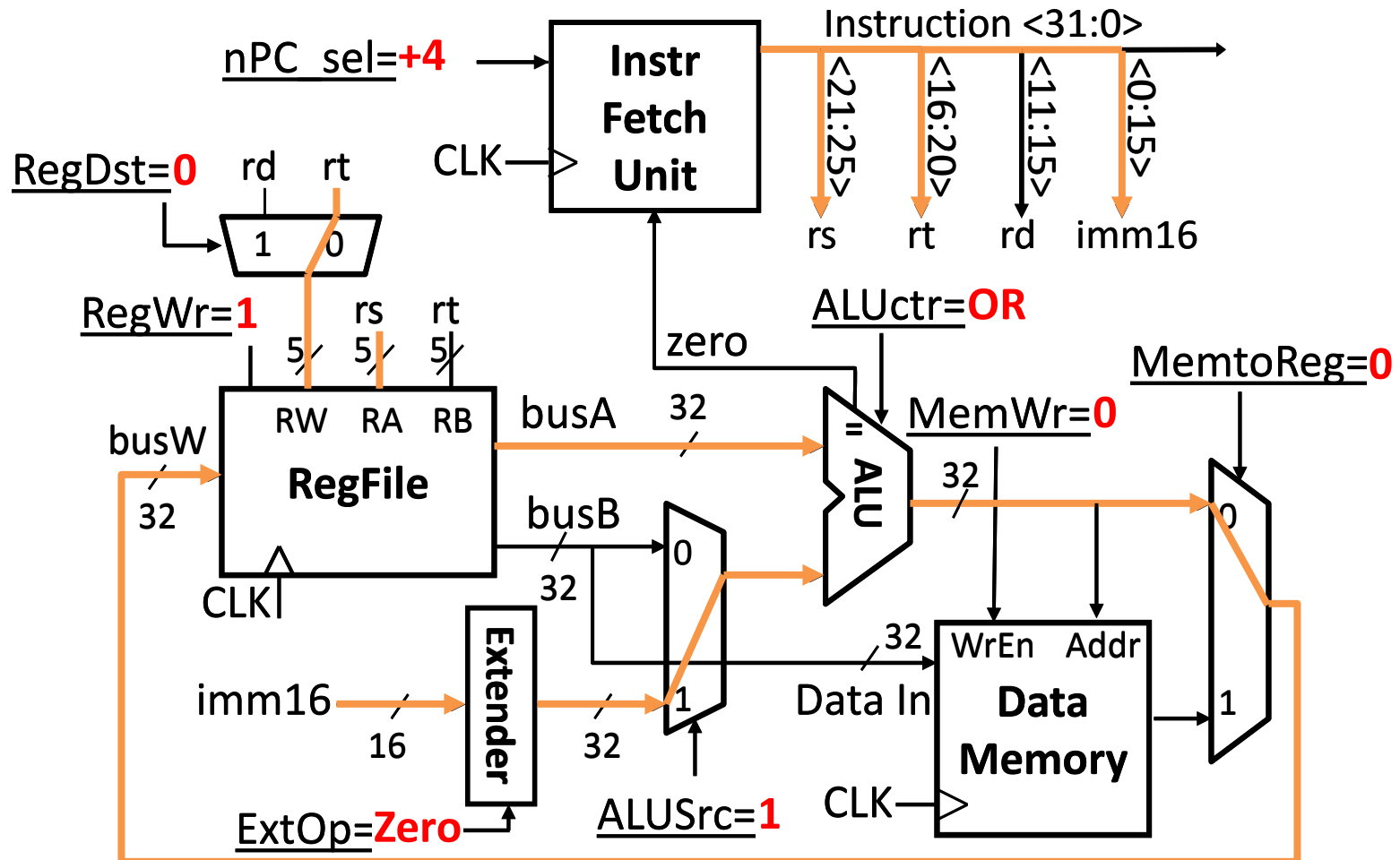
# Desired Datapath For addu

- $R[rd] \leftarrow R[rs] + R[rt];$



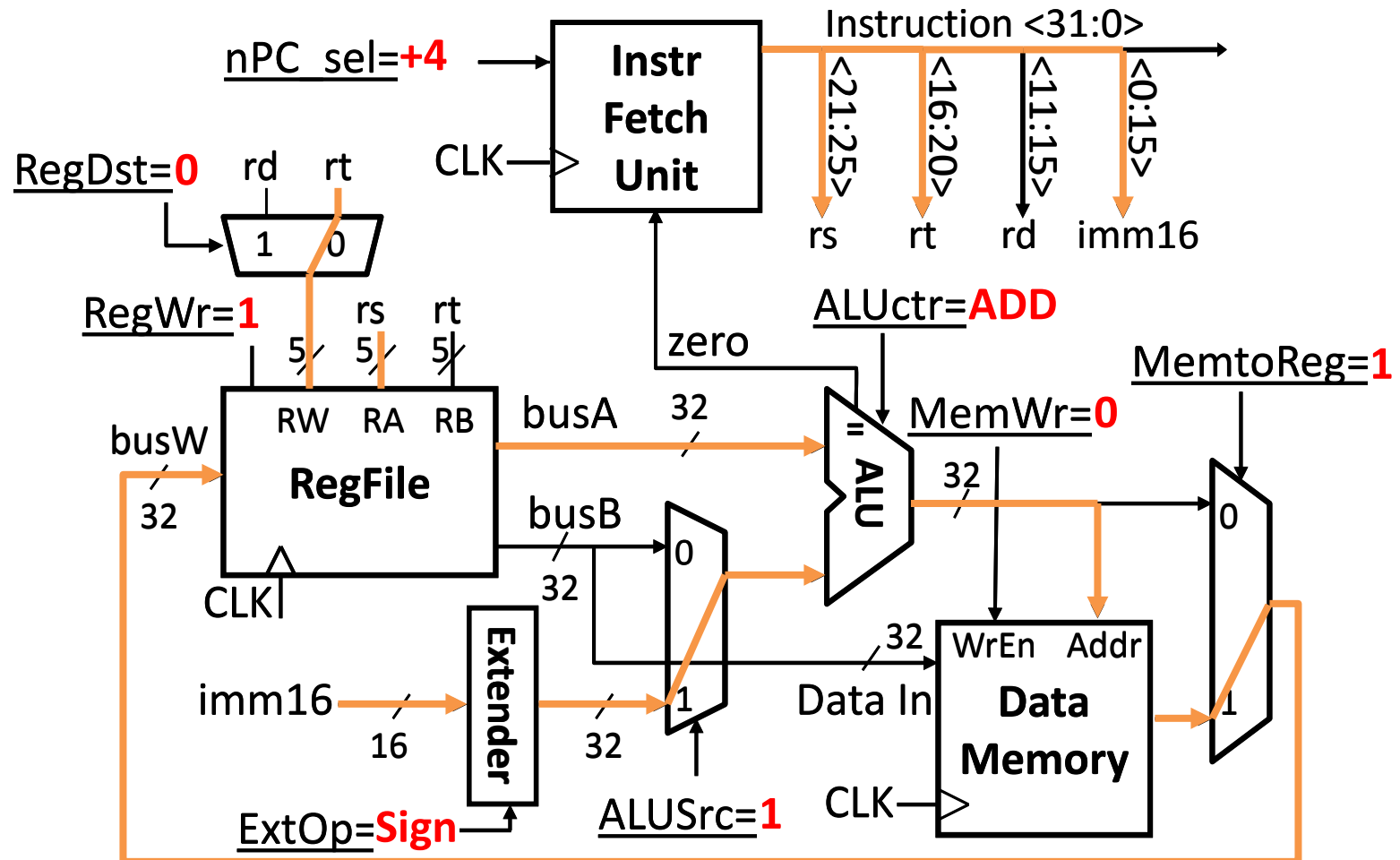
# Desired Datapath For ori

- $R[rt] \leftarrow R[rs] \mid \text{ZeroExt}(\text{imm16})$ ;



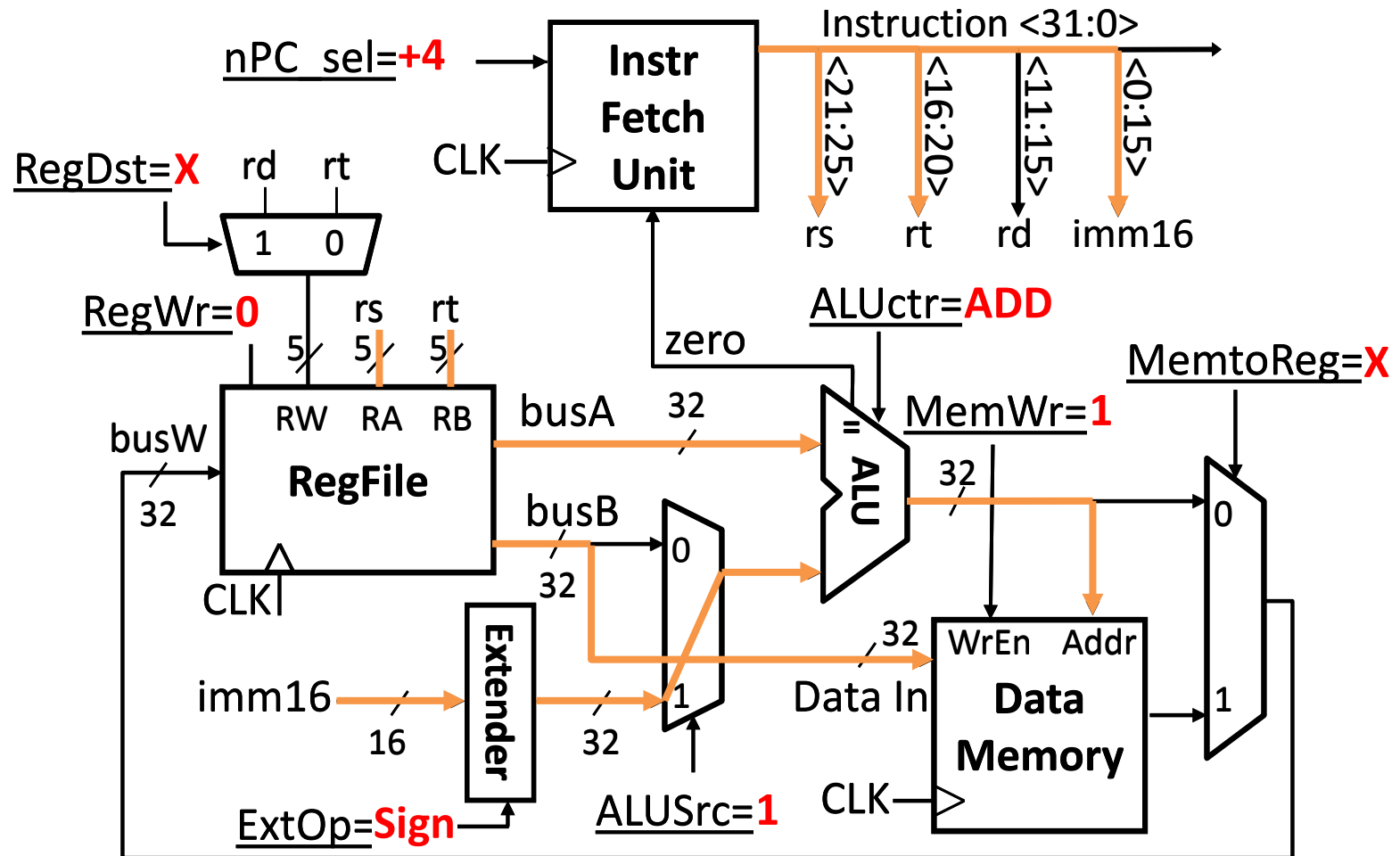
# Desired Datapath For Load

- $R[rt] \leftarrow \text{MEM}\{R[rs] + \text{SignExt}[imm16]\};$



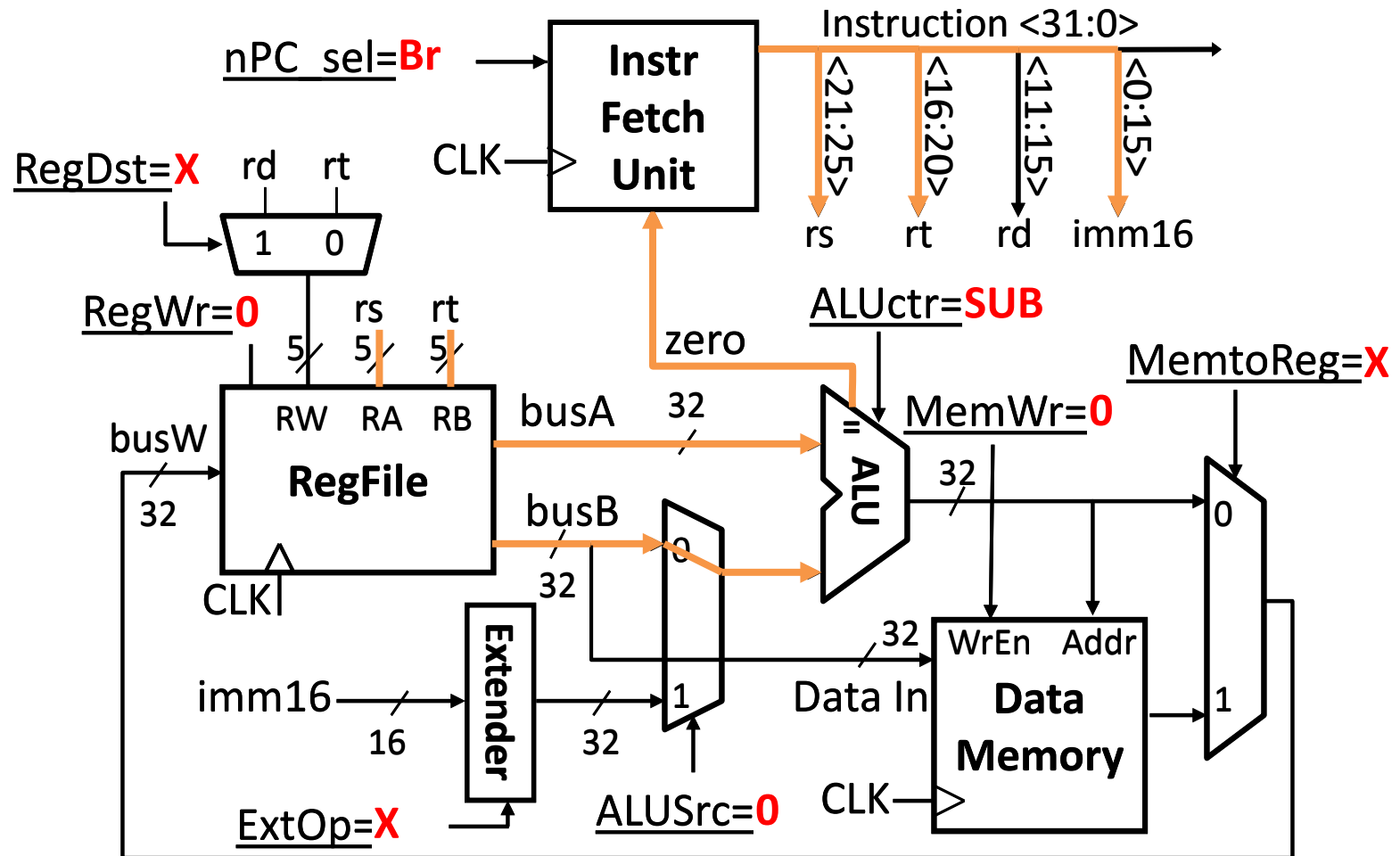
# Desired Datapath For store

- $\text{MEM}\{R[\text{rs}] + \text{SignExt}[\text{imm16}]\} \leftarrow R[\text{rt}] ;$



# Desired Datapath For beq

- BEQ if( $R[rs] == R[rt]$ ) then  $PC \leftarrow PC + 4 + (\text{sign\_ext}(\text{Imm16}) \ll 00)$

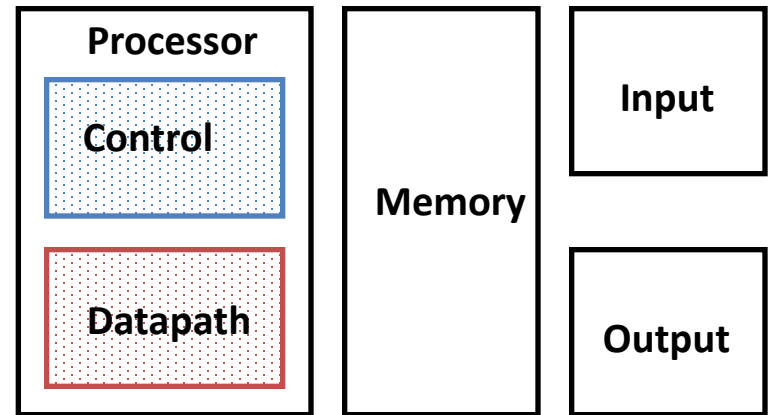




# Summary (1/2)

- Five steps to design a processor:

- 1) Analyze instruction set → datapath requirements
- 2) Select set of datapath components & establish clock methodology
- 3) Assemble datapath meeting the requirements



- 4) Analyze implementation of each instruction to determine setting of control points that effects the register transfer
- 5) Assemble the control logic
  - Formulate Logic Equations
  - Design Circuits

# Summary (2/2)

- Determining control signals
  - Any time a datapath element has an input that changes behavior, it requires a control signal (e.g. ALU operation, read/write)
  - Any time you need to pass a different input based on the instruction, add a MUX with a control signal as the selector (e.g. next PC, ALU input, register to write to)
- Your datapath and control signals will change based on your ISA

# 作业1

《计算机组成与设计》	Logisim	WORD
4.1		✓(4.1.3暂不作)
4.2		✓(只要求4.2.1和4.2.2)
4.9		✓

# 作业2

## ■ Logisim

- 学习1：学习使用Built-in Library中的各电路，特别是
  - ◆ Wiring：Splitter、Clock
  - ◆ Memory：Register、RAM、ROM
  - ◆ 注意：学会设置电路的Attributes
- 学习2：使用Add Circuit功能和Library功能
  - ◆ 将所有开发的部件都部署在一个设计文件或多个设计文件中
  - ◆ 一个文件：应注意每个电路部件的命名要有意义
  - ◆ 多个文件：应注意文件命名尽可能体现电路特性

