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Lab 7: Creative Project

For the creative portion of the project, a NES controller was connected to the FPGA board and used to control the motion of the tank and the firing of the tank bullet. In order to use the controller, additional hardware was created so that commands from the controller could be recognized by the board. A new hardware was created wherein new vhdl files were created and the logic was implemented so that when buttons were pressed on the controller, the vhdl code would recognize the buttons presses and store the data in a register corresponding to which buttons were pressed. The vhdl code that was added was similar to the vhdl code that was added for the implementation of the PIT timer from the last lab. Corresponding changes to the .ucf file and all other necessary changes to the hardware were made so that the vhdl implementing the controller could be usable.

Once the hardware was correctly implemented so the NES controller could communicate with the board, software was added to the C code in the existing project workspace. The additional C code was simple to implement as all that was required to read the registers created from the vhdl hardware. These registers stored the values corresponding to button pushes. After the register was read, the left and right buttons were used to control lateral motion of the tank, and the A button was used to fire the tank bullet.

Many bugs were encountered during implementation of this project. The most difficult problems occurred while trying to create the hardware and vhdl code. The logic of the vhdl code proved to be very difficult and confusing to implement. The use of the three signals between the NES controller and board: latch, data, and pulse, were confusing to understand as far as timing requirements were concerned. The most difficult problem was encountered when the logic for these signals was implemented correctly in the vhdl and an accurate simulation of waveforms was given, but the FPGA board could still not recognize signals from the controller. This was frustrating and required much debugging while adjusting the .ucf and other signals created during instantiation of the hardware. Multiple, time consuming, hardware exports were required and eventually the project came together.