Processor Design

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December 19, 2018

1 Introduction

2 Modules

2.1 Adder

The adder used in this processor is a simple 32 bit ripple-carry adder. The 32 bit adder is created using a series of smaller adder modules including:

- Half Adder
- Full Adder
- 2 Bit Adder
- 4 Bit Adder
- 16 Bit Adder
- 32 Bit Adder

2.1.1 Half Adder

2.1.1.1 Inputs

- Operand A - 1 bit
- Operand B - 1 bit

2.1.1.2 Outputs

- Sum - 1 bit
- Carry - 1 bit

2.1.1.3 Functionality

Takes two single bit operands and produces the single bit sum and the carry bit.

2.1.1.4 Diagrams

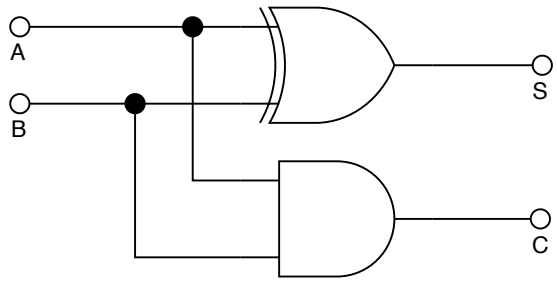

Figure 1: Logic diagram of the half adder

2.1.1.5 Testing

All possible inputs for the half adder are stimulated by the test bench and are compared to the expected outputs according to the following table:

A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

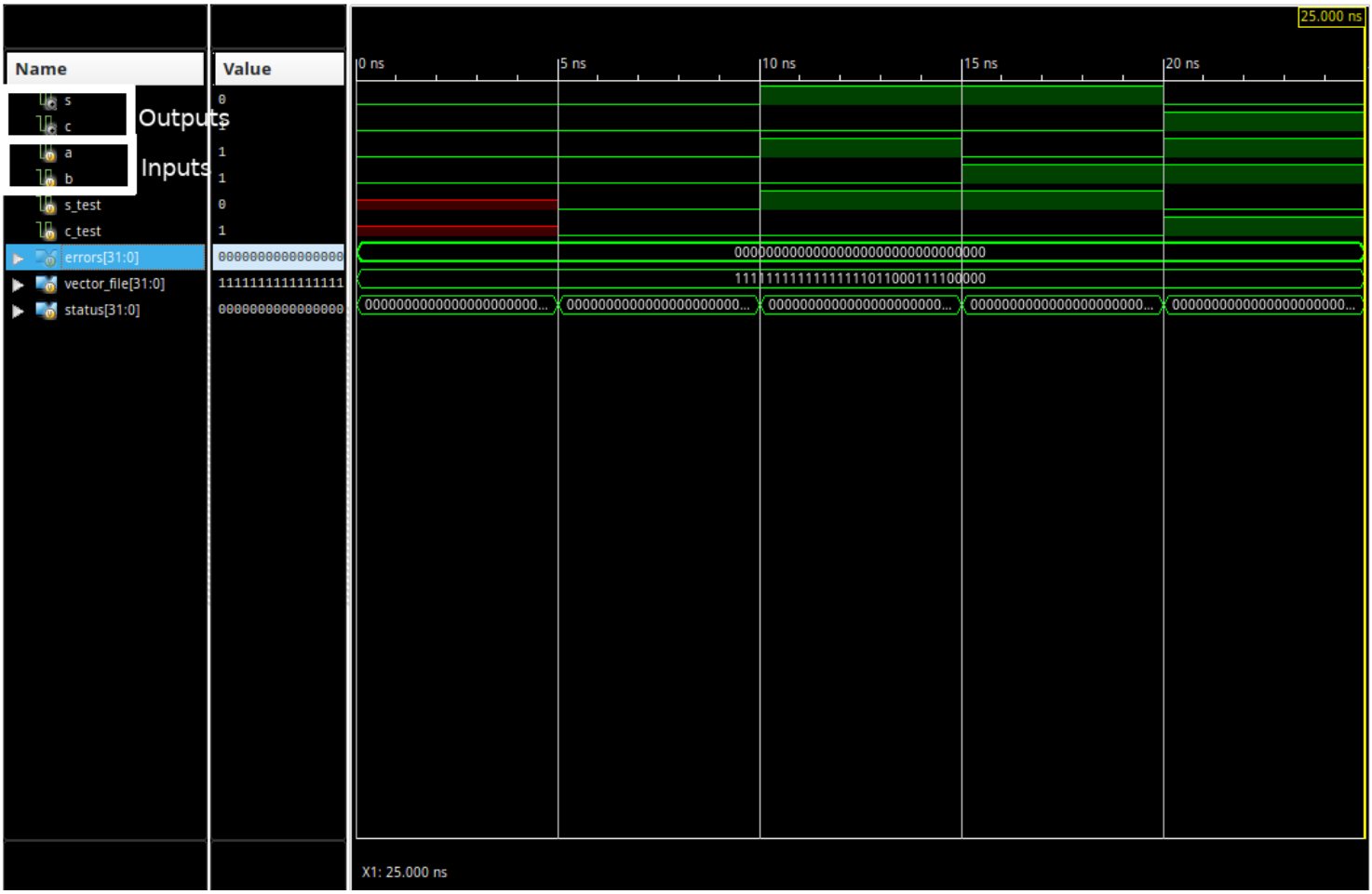

Figure 2: Simulation output of half adder

2.1.2 Full Adder

2.1.2.1 Inputs

- Operand A - 1 bit
- Operand B - 1 bit
- Carry In - 1 bit

2.1.2.2 Outputs

- Sum - 1 bit
- Carry Out - 1 bit

2.1.2.3 Functionality

Takes three single bit operands and produces the single bit sum and the carry bit.

2.1.2.4 Diagrams

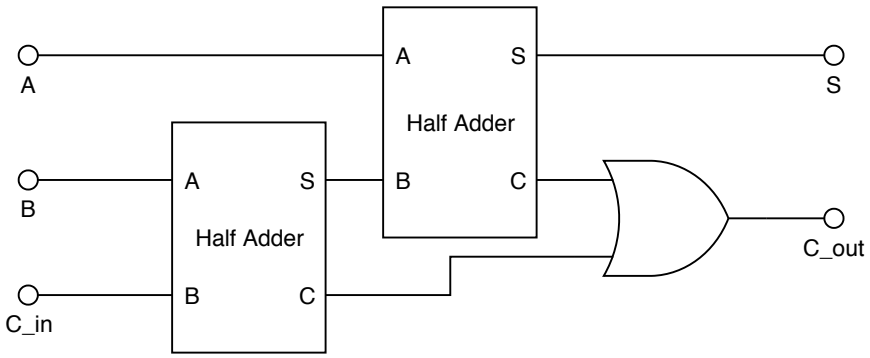

Figure 3: Logic diagram of the full adder

2.1.2.5 Testing

All possible inputs for the full adder are stimulated by the test bench and are compared to the expected outputs according to the following table:

A	B	Carry In	S	Carry Out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Figure 4: Simulation output of full adder

2.1.3 2 Bit Adder

2.1.3.1 Inputs

- Operand A - 2 bit
- Operand B - 2 bit
- Carry In - 1 bit

2.1.3.2 Outputs

- Sum - 2 bit
- Carry Out - 1 bit

2.1.3.3 Functionality

Takes two 2 bit operands and a third single bit operand and produces the 2 bit sum and the carry bit.

2.1.3.4 Diagrams

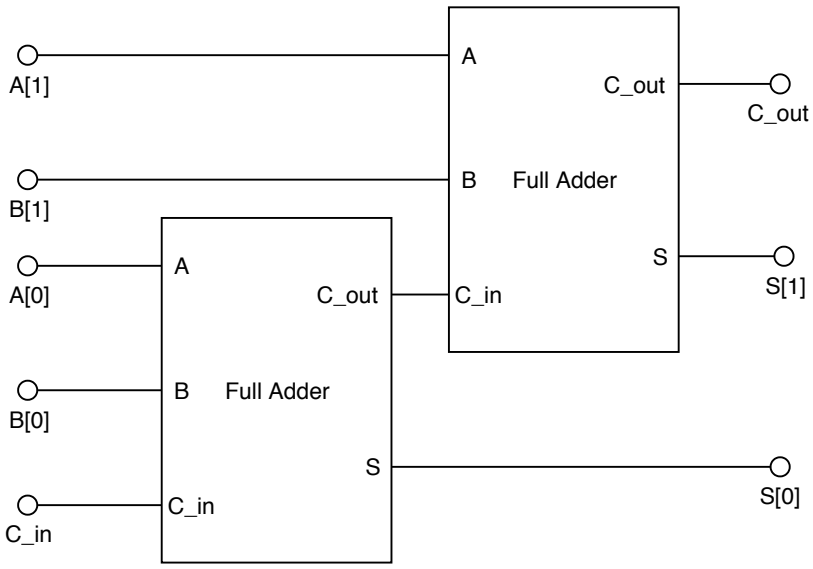

Figure 5: Logic diagram of the 2 bit adder

2.1.3.5 Testing

Due to the larger range of possible inputs, inputs are selected to include several base cases, as well as the maximum input value case and minimum input value case. The inputs and expected outputs are as follows:

A	B	Carry In	S	Carry Out
3	3	0	2	1
3	1	0	0	1
3	3	1	3	1
0	0	0	0	0

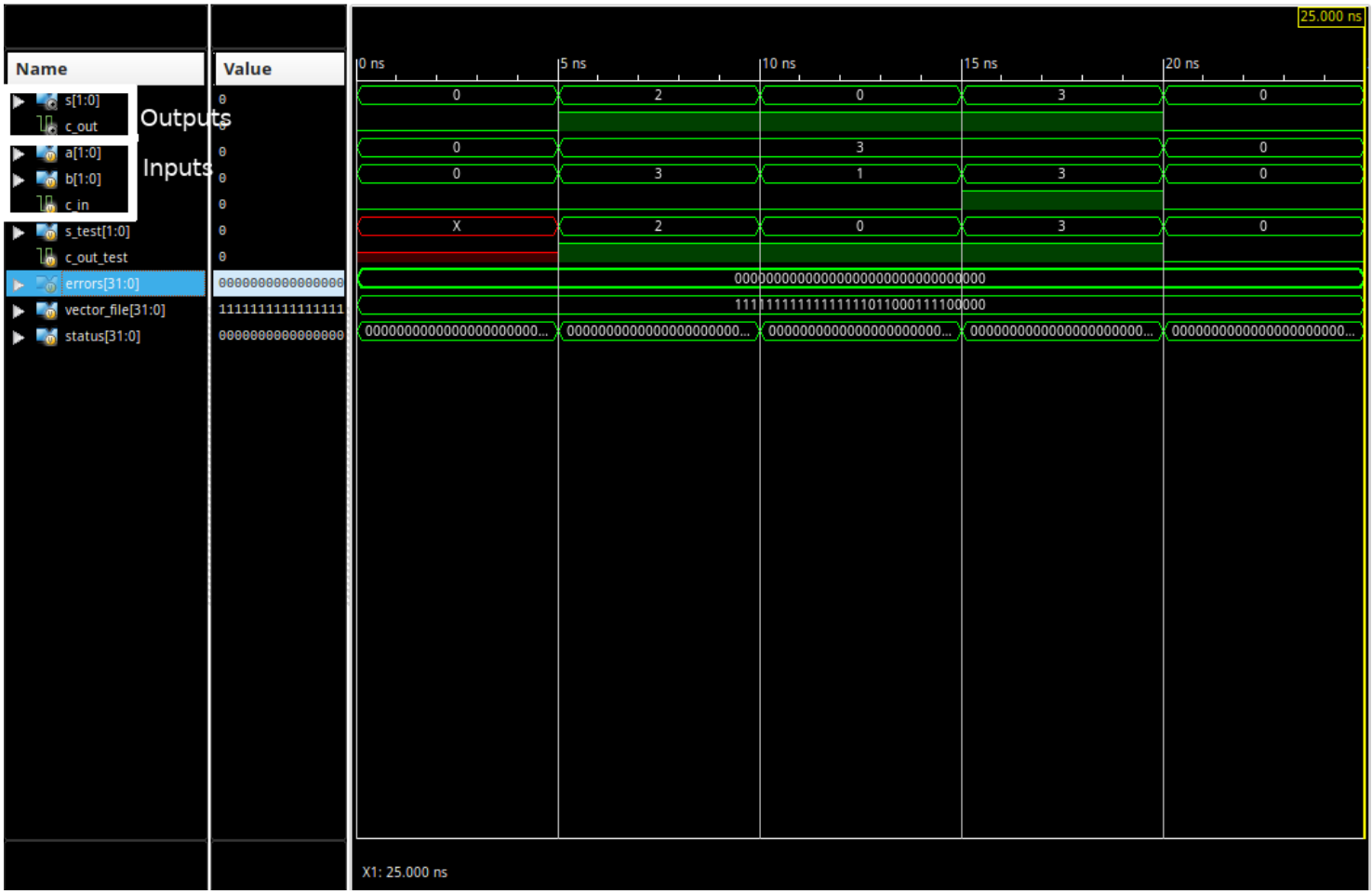

Figure 6: Simulation output of 2 bit adder

2.1.4 4 Bit Adder

2.1.4.1 Inputs

- Operand A - 4 bit
- Operand B - 4 bit
- Carry In - 1 bit

2.1.4.2 Outputs

- Sum - 4 bit
- Carry Out - 4 bit

2.1.4.3 Functionality

Takes two 4 bit operands and a third single bit operand and produces the 4 bit sum and the carry bit.

2.1.4.4 Diagrams

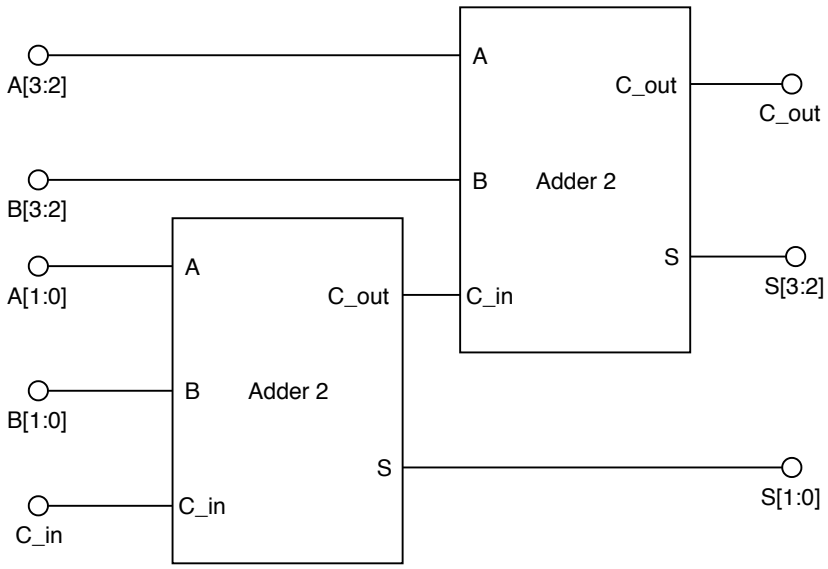

Figure 7: Logic diagram of the 4 bit adder

2.1.4.5 Testing

As this module follows a nearly identical functionality as the 2 bit adder, and nearly identical Verilog code, testing was ommitted. This module's test is included within the 32 bit adder test, as the 32 bit adder will only function correctly if this module functions correctly.

2.1.5 8 Bit Adder

2.1.5.1 Inputs

- Operand A - 8 bit
- Operand B - 8 bit
- Carry In - 1 bit

2.1.5.2 Outputs

- Sum - 8 bit
- Carry Out - 8 bit

2.1.5.3 Functionality

Takes two 8 bit operands and a third single bit operand and produces the 8 bit sum and the carry bit.

2.1.5.4 Diagrams

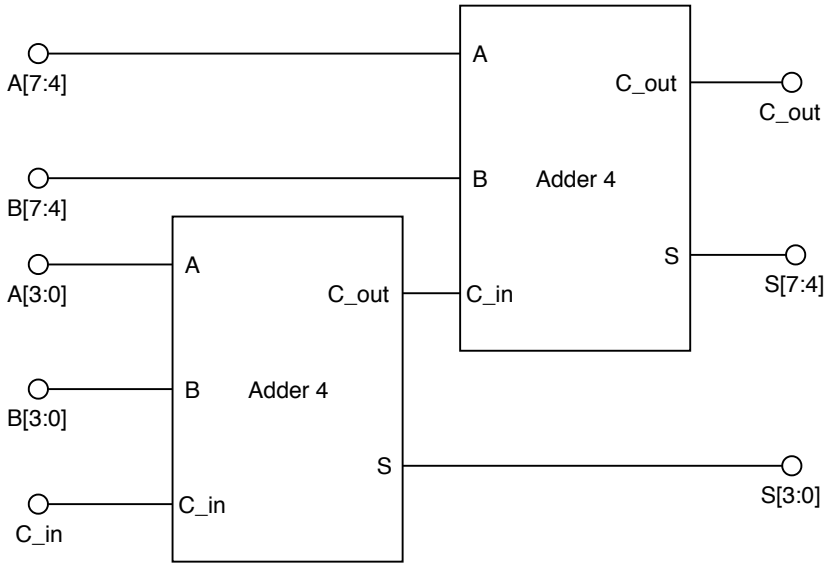

Figure 8: Logic diagram of the 8 bit adder

2.1.5.5 Testing

As this module follows a nearly identical functionality as the 2 bit adder, and nearly identical Verilog code, testing was ommitted. This module's test is included within the 32 bit adder test, as the 32 bit adder will only function correctly if this module functions correctly.

2.1.6 16 Bit Adder

2.1.6.1 Inputs

- Operand A - 16 bit
- Operand B - 16 bit
- Carry In - 1 bit

2.1.6.2 Outputs

- Sum - 16 bit
- Carry Out - 16 bit

2.1.6.3 Functionality

Takes two 16 bit operands and a third single bit operand and produces the 16 bit sum and the carry bit.

2.1.6.4 Diagrams

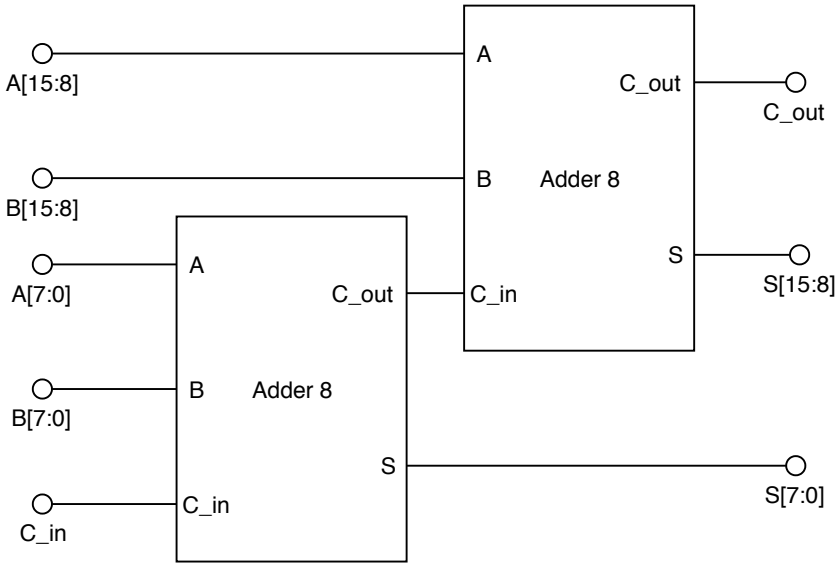

Figure 9: Logic diagram of the 16 bit adder

2.1.6.5 Testing

As this module follows a nearly identical functionality as the 2 bit adder, and nearly identical Verilog code, testing was ommitted. This module's test is included within the 32 bit adder test, as the 32 bit adder will only function correctly if this module functions correctly.

2.1.7 32 Bit Adder

2.1.7.1 Inputs

- Operand A - 32 bit
- Operand B - 32 bit
- Carry In - 1 bit

2.1.7.2 Outputs

- Sum - 32 bit
- Carry Out - 32 bit

2.1.7.3 Functionality

Takes two 32 bit operands and a third single bit operand and produces the 32 bit sum and the carry bit.

2.1.7.4 Diagrams

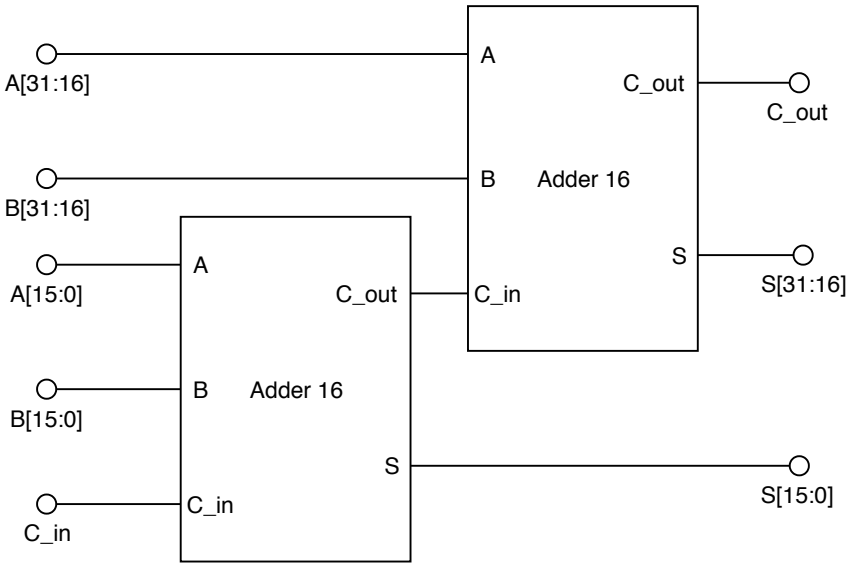

Figure 10: Logic diagram of the 32 bit adder

2.1.7.5 Testing

Due to the larger range of possible inputs, inputs are selected to include several base cases, as well as the maximum input value case. The inputs and expected outputs are as follows:

A	B	Carry In	S	Carry Output
10	10	1	21	0
1	0	1	2	0
4294967295	0	1	0	1
4294967295	4294967295	1	4294967295	1

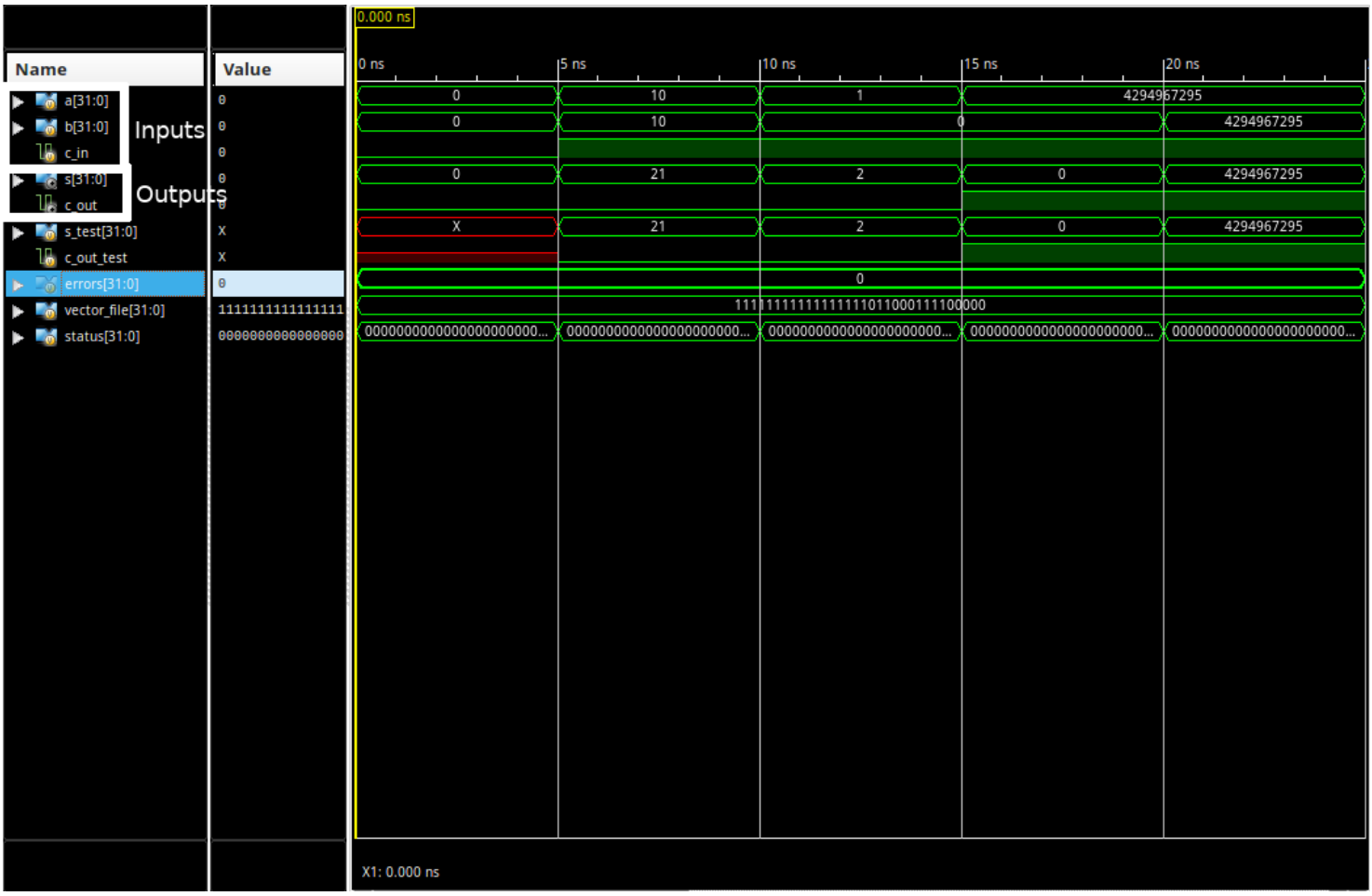

Figure 11: Simulation output of 32 bit adder