

# KamLAND frontend analog electronics



## MoGURA2 design document

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The frontend analog electronics take the AC coupled signal from the PMT, amplify and condition the signal such that they can be digitized by the **Zynq UltraScale+ RFSoC RF-ADC**. The following describes a reference design that is capable of providing the correct amplification for a low gain and high gain channel, over the desired bandwidth. This design introduces a design for the digital baseline recovery (DBRL) — a correction applied to the waveform via a DAC to compensate for droop/overshoot introduced by the AC coupling.

This document will first give an overview and the requirements of the FEA, then go through the amplification stages one at a time — presenting simulations and design requirements. The end of the document will show the full circuit design along with a full simulation illustrating the expected noise, frequency response, and an example transient waveform.

The simulation is performed using Texas Instruments TINA TI.  
The circuit design and layout were performed using KiCAD.

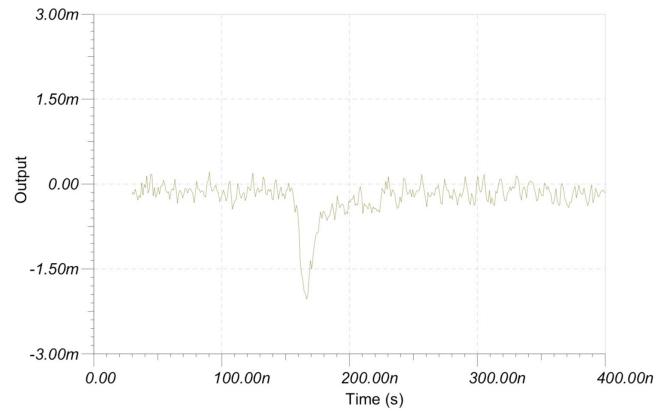
A GitHub repository contains the design files, located here:

### References:

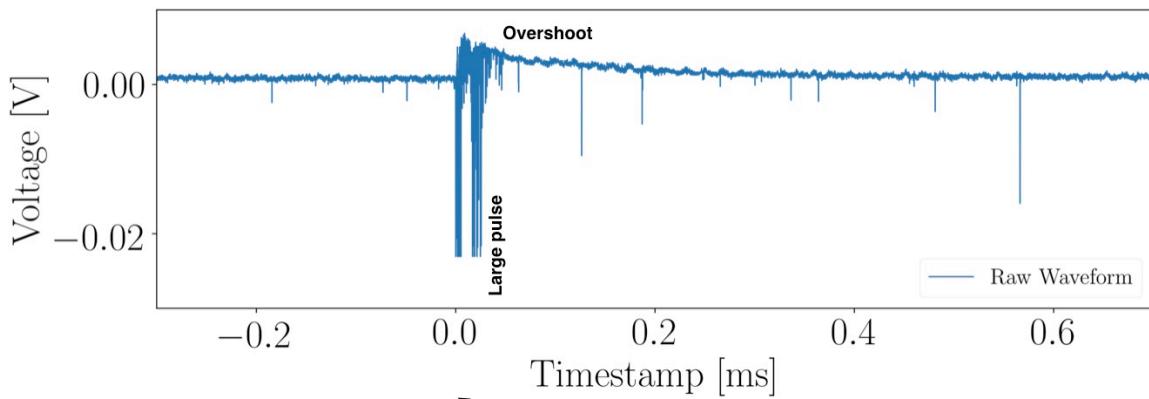
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## Requirements

The photomultipliers (PMT) are AC coupled to the front end electronics via a large capacitor. The uni-directional AC coupled signals are assumed to produce signals ranging from 0 to -8V. **Large signals** are rare — order Hz, and tend to be order microseconds in length. These originate from cosmic ray muons passing through the KamLAND detector. **Small signals**, originating from single photoelectrons, are expected to be between 0.1 and 6mV. These are much more frequent — order 20kHz. The primary frequency component of the small signals are  $\sim$ 10-100MHz, and are only  $\sim$ 10s of nanoseconds in length. An example of a few small signals (single photoelectron) is shown on the right.



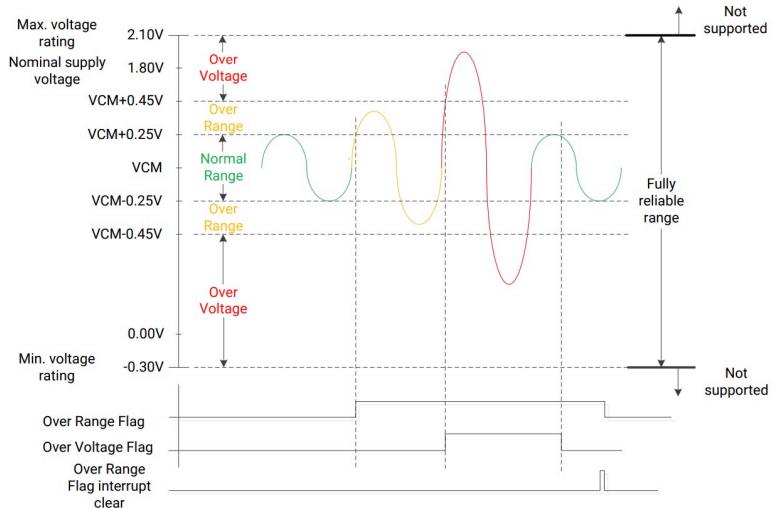
The large signals produce two issues. First, since they contain a large amount of charge, the droop/overshoot introduced by the AC coupling can be substantial. The overshoot time constant is several microseconds (adjustable design), and we **must** be able to extract small pulses that “ride” on the overshoot. We aim to accomplish this with a *Digital Baseline Recovery System*, which compensates for the overshoot using a digital to analog converter. An example of overshoot from the KamLAND detector is shown below.



The second issue produced by large signals is due to saturation of the electronics. Once saturated, we can no longer calculate the required baseline correction. Therefore, there must be ample room in the output voltage range to accommodate this.

We aim to have two digitizers. The high-gain digitization (**HGain**) is part of the RFSOC and digitizes the small signals at 1 GSPS (RF-ADC). This means that we require the front-end analog (FEA) electronics to have a bandwidth of ~400-500MHz (First Nyquist zone). This channel should have a gain of approximately 6dB (voltage gain of 2). However, the gain from the PMTs has been observed to decrease overtime, therefore, the gain on the FEA should be able to accommodate a change of another 6dB with minimal impact on the performance. The RF-ADC on the RFSOC operates at a common mode voltage of 1.2V, with a range of +/- 0.25V. It has an effective resolution of 12-bits, corresponding to a discrete step size of 0.13mV. The RMS noise on the HGain channel should not be more than this. Also note, that this channel must be protected against the large signals.

**Figure 10: Threshold, Over Range, and Over Voltage Levels**



The low-gain (**LGain**) channel will likely be digitized by a 250MSPS digitizer. My guess is that it will also be single ended input, differential output. We require that it is able to accept input pulses with a peak voltage >8V. The following describes the reference design which instead uses a separate channel from the RF-ADC, which means the signal has to be attenuated by -24dB. However, the design allows for the a rather large change in the gain by simply changing the values of the voltage divider prior to amplifier.

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## **Requirements Summary:**

### **HGain FEA:**

- 400-500MHz bandwith. Digitization at 1GSPS.
- Capable of 6-12dB gain.
- 0.13mV RMS noise (max). Peak-to-Peak noise at 10-100MHz above 0.13mV is also unacceptable.
- Single-ended input, differential output, operating between 1.2V +/-0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection against large signals.

### **LGain FEA:**

- 100-200MHz bandwith. Digitization at 250MSPS.
- Capable of -24dB attenuation.
- Noise is less crucial here.
- Single-ended input, differential output? operating between 1.2V +/-0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection against large signals.

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## Reference design, full circuit.

The following is the circuit diagram for the FEA. Following that, there is a description of each component accompanied by the simulation.

## Inverting buffer (1st stage)

The inverting buffer (perhaps providing some small amplification) is the first stage of the FEA. We impedance match the 50Ω (Av = -6dB), AC coupled, PMT connection near the inverting terminal of a high speed op amp (currently chosen to be the LMH6703 or LMH6702). The inverting configuration is more stable than the non-inverting configurations near unity gain. This configuration also allows us to connect the high input impedance, non-inverting terminal to the RF-DAC to allow for a DBLR.

The SOT-23 version (lower H2 and H3 distortion) of the LMH6702 operates at +/- 5.5V rails with ultra-low distortion (-100/-96 dBc) current feedback amplifier. With also low noise (1.83 nV/√Hz), and a high slew-rate (3100 V/μs). The output range of the amplifier is 1.2V within the rails (output between -4.3V and 4.3V).

Link: <https://www.ti.com/lit/ds/symlink/lmh6702.pdf?ts=1591103993527>

We protect the input of the inverting buffer with clamping diodes. These limit the input range to -5.1V to 400mV (assuming a voltage drop of 400mV). A slight amount of amplification is allowed (up to a gain of Av = 1.3), but beyond this and a -8V signal will saturate the output.

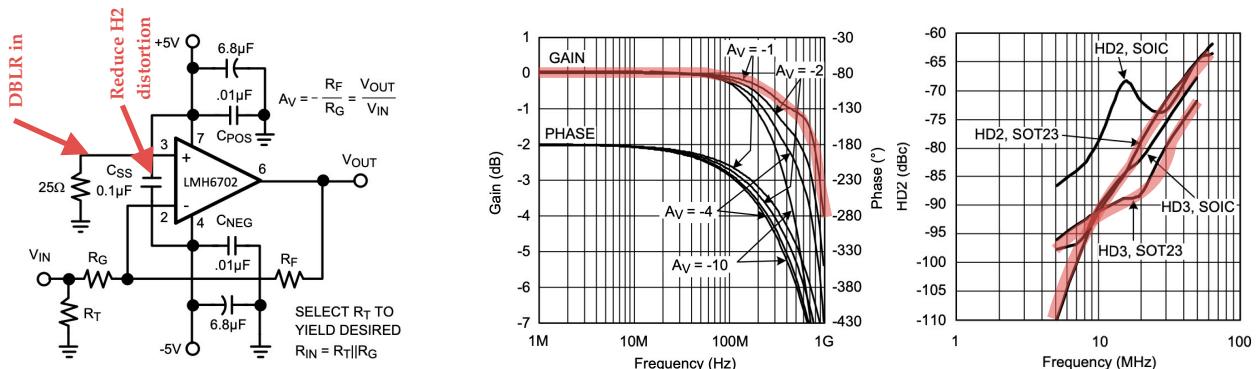


Figure 25. Recommended Inverting Gain Circuit

### Disadvantages of Inverting buffer design:

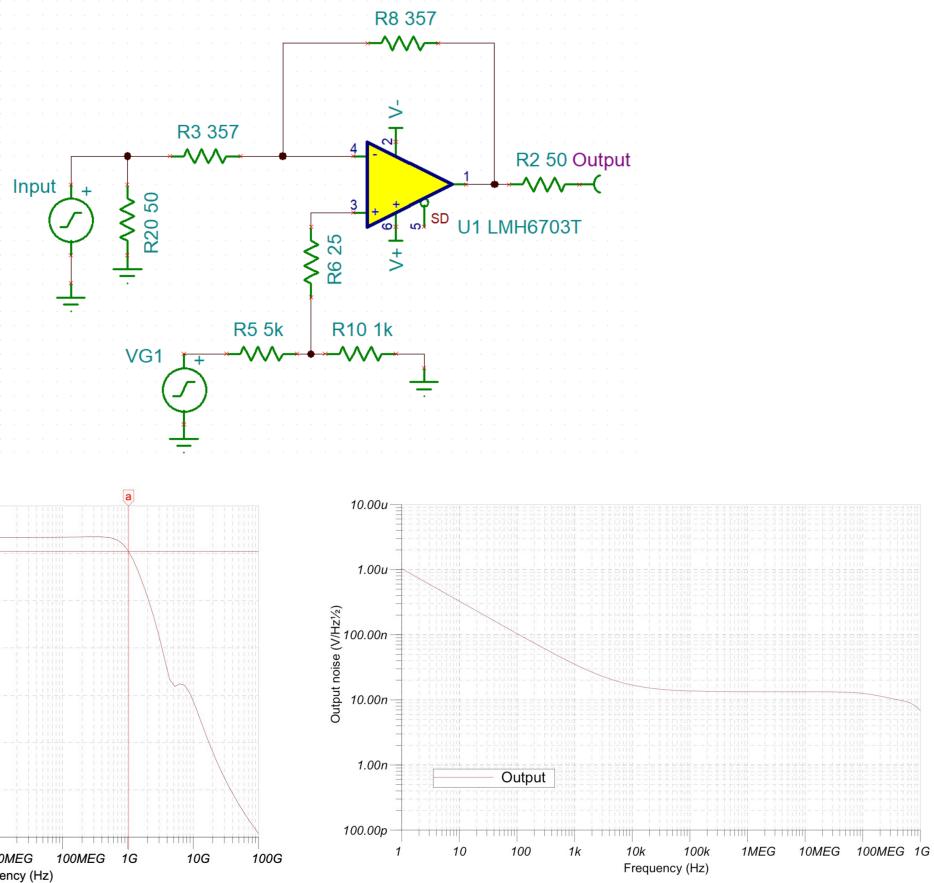
1. We introduce a DBLR level shifting signal to the non-inverting terminal via the RF-DAC. The noise from the RF-DAC is amplified by 1+R<sub>2</sub>/R<sub>1</sub>, whereas the signal is only amplified by R<sub>2</sub>/R<sub>1</sub>. We need to perform the DBLR at the first stage since the correction needs to be applied to both the HGain and LGain channels, using a single DAC.

## TINA TI simulation of inverting buffer:

Unity gain. Inverting configuration is more stable than the non-inverting amp at unity gain. Gain =  $R_8 / R_3$ .  $R_{20}$  is used to terminate the 50Ω input.  $R_2$  isolates the output of the amplifier.  $VG1$  is used to inject waveforms, that is, this is the DAC. The voltage divider formed by  $R_5$  and  $R_{10}$ , reduce the full range of the DAC from 2.5V to 500mV.  $R_6$  should be equal to the parallel resistance ...

RMS noise  $\sim 11\text{nV}/\sqrt{\text{Hz}}$  at a bandwidth of 100MHz is 0.11mV. Noise of the DAC, however is amplified by  $1+R_8/R_3$ , which is larger than that of the signal. Care must be taken to ensure that the noise from the DAC is sufficiently small.

The determined 3dB frequency rolloff happens as 1.02GHz.



# HGain Non-Inverting amplifier

The non-inverting amplifier is the second stage for the HGain channel. This amplifier is used to provide the necessary gain for this channel. RG can be used to change the gain of the amplifier. We use the same op amp as the buffer (LMH6702 or LMH6703).

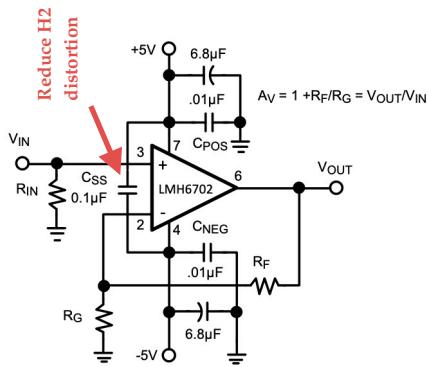
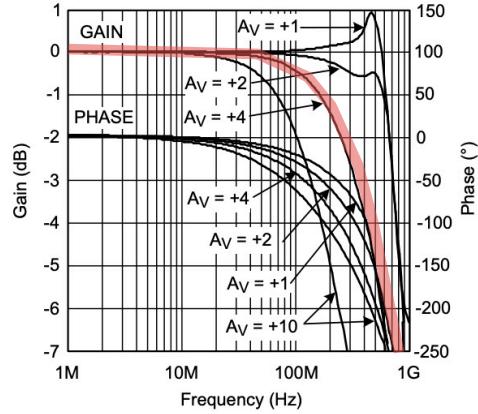


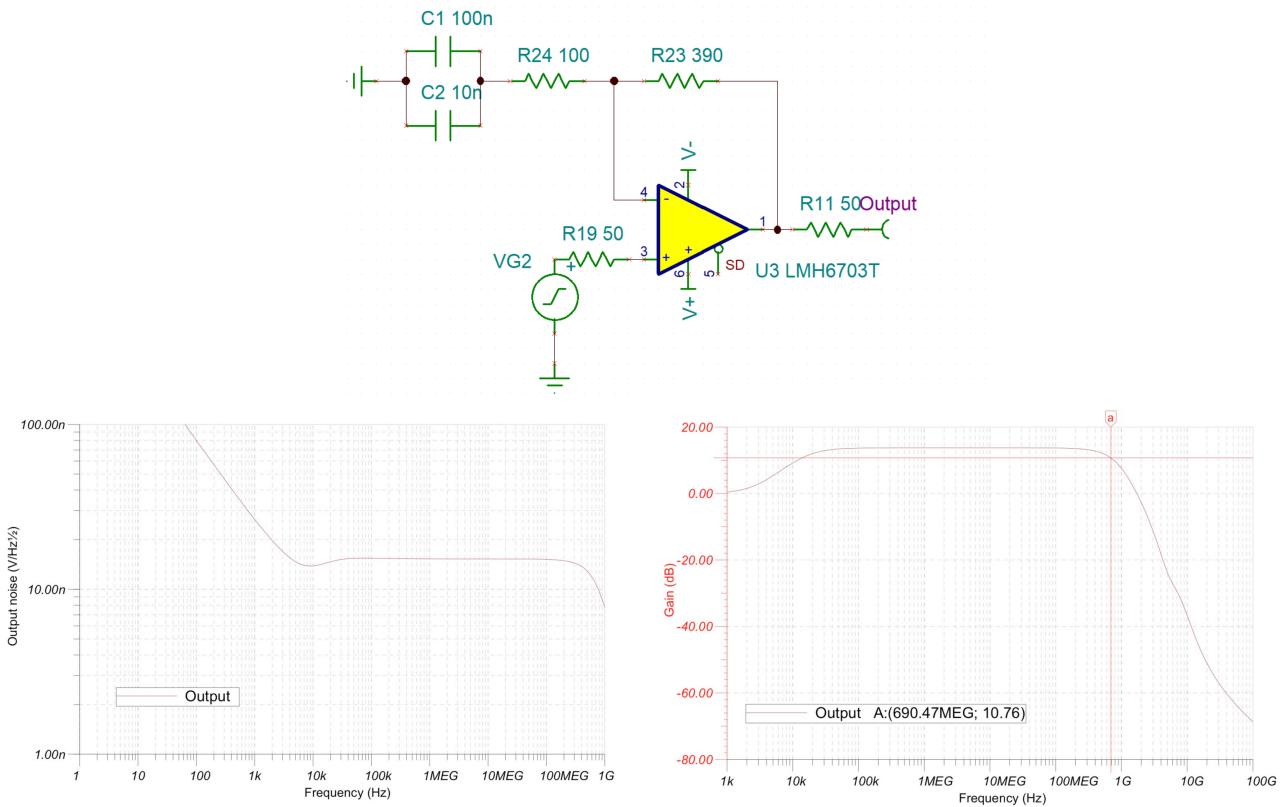
Figure 24. Recommended Non-Inverting Gain Circuit



The non-inverting terminal is connected to the ground via a capacitor. The capacitor reduces the amplification of low frequencies to unity. You can see this in the simulated frequency response below.

## TINA TI simulation:

Non-inverting configuration. Gain =  $1+R_{23}/R_{24}$ .  $R_{19}$  might not be needed. It is used to isolate the non-inverting input to the op amp from capacitive loading, should be placed as close as possible to the input, same side of PCB, small SMT component. Same goes for  $R_{11}$ . If the signal traces are short enough, these may be neglected.  $C_1$  and  $C_2$  looks like the ground connection for high frequencies, however at low frequencies (<10KHz), there is significant impedance and the amplification goes to unity gain. This reduces low frequency baseline shifts from being amplified.



## HGain Differential Amplifier

We now take the output of the non-inverting amplifier and differentiate the signal. This is accomplished using the 1.5GHz GBP TI LMH6552. It also allows for amplification up to  $A_v = 4$  (however we'll keep this at unity gain), and has a similar slew rate to the LMH6702 (3800-V/ $\mu$ s at unity gain. Current feedback amplifier). This differential op amp also has an integrated output common mode control to connect to the common mode of the RFADC ( $V_{cm} = 1.2V$ ).

Feedback resistor should be 270-390Ohms. This and RG need to be precision resistors (0.1%). Bypass  $V_{cm}$  with a 0.1uF capacitor.

The final version should have the WSON LMH6552 package rather than the SOIC package since it has better thermal properties.

We also need this amplifier to level shift the uni-directional signal such that we maximize the dynamic range of the RF-ADC. This is accomplished by level shifting the signal by biasing the non-inverting terminal using a precision voltage regulator. However, the downside to this is that

We protect the input of the differential amplifier using clamping diodes. These limit the input range to -400mV to 400mV. At unity gain, the output voltage should be incapable of damaging the RFADC.

The series resistors on the output isolate the capacitive loading from the RF-ADC (unknown value). They may need to be modified from 25-1k.

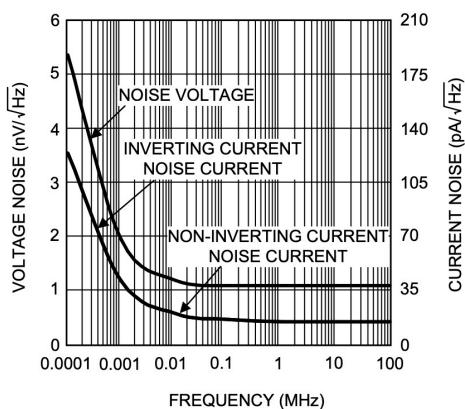


Figure 33. Input Noise vs Frequency

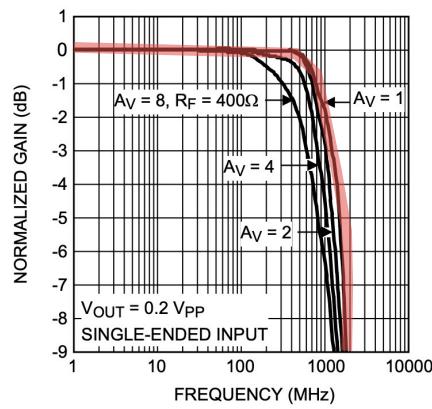


Figure 2. Frequency Response vs Gain

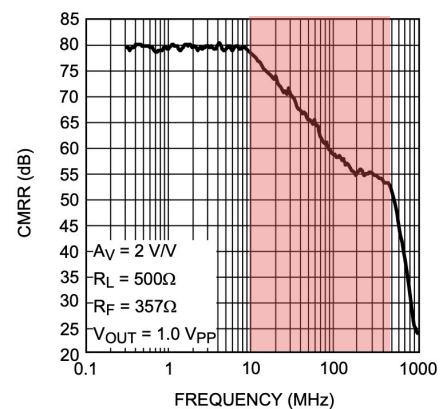


Figure 29. CMRR

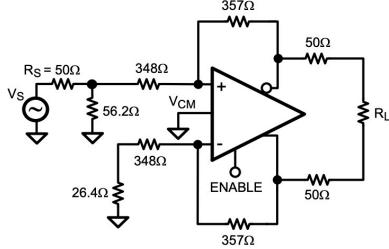


Figure 41. Single Ended Input S-Parameter Test Circuit (50Ω System)

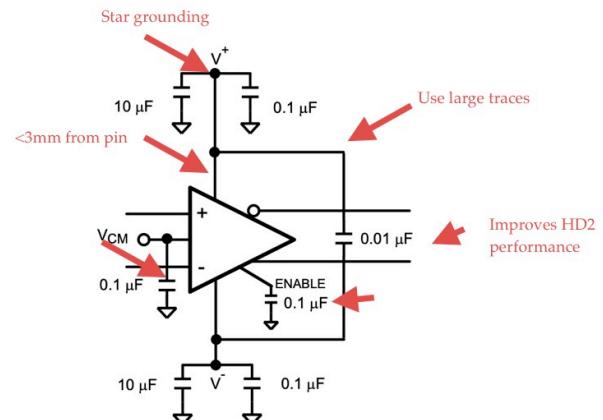
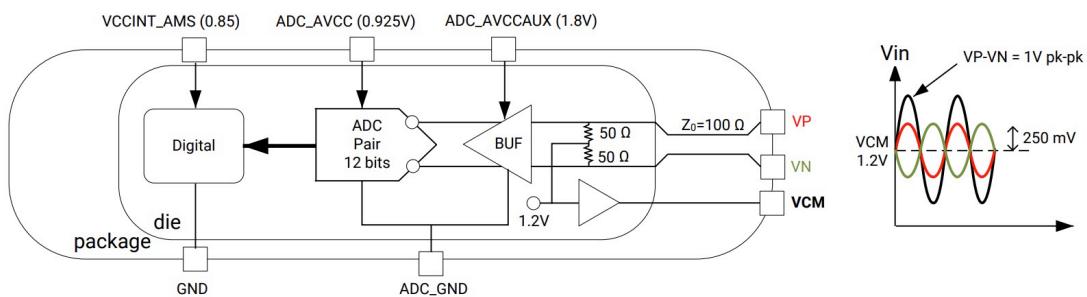


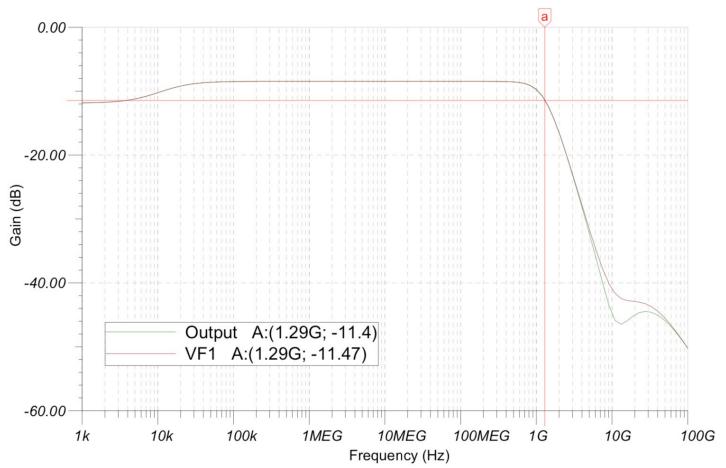
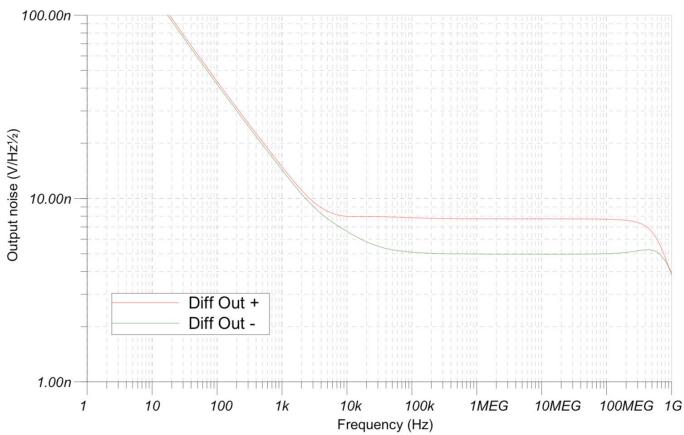
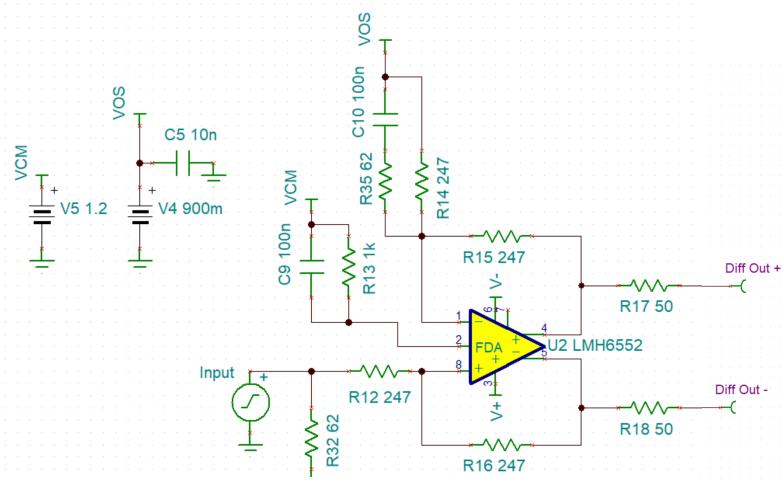
Figure 53. Split Supply Bypassing Capacitors

### TINA TI simulation:

$V_{CM}$  connects to the common mode of the RF-ADC. As shown in the image below,  $V_{CM}$  is feed by a voltage follower at 1.2V. The LMH6552 op amp recommends using a 0.1uF cap on  $V_{CM}$ .  $V_{OS}$  supplies the level shifting that maximizes the dynamic range of the ADC.  $R_{17}$  and  $R_{18}$  are used to isolate the op amp from capacitive loading from the RF-ADC input. This op amp can provide amplification, however the current configuration uses it at unity gain.  $R_{32}$  is the termination resistor. The cutoff frequency is 1.3GHz. And the noise density is lower than 10nV/sqrt(Hz) in our bandwidth of interest.

Figure 8: RF-ADC Analog Input





# Transient simulation

