

KamLAND analog frontend electronics



MoGURA2 design document

Dr. Spencer N. G. Axani - June 2, 2020

The frontend analog electronics take the AC coupled signal from a single photomultiplier tube (PMT), amplify and condition the signal such that they can be digitized by the **Zynq UltraScale+ RFSoC RF-ADC**. The following describes a reference design that is capable of providing the correct amplification for a low gain (LGain) and high gain (HGain) channel, over the desired bandwidth. This design introduces a design for the digital baseline recovery (DBRL) — a correction applied to the waveform via a DAC to compensate for droop/overshoot introduced by the AC coupling.

This document will first give an overview and the requirements of the FEA, then go through the amplification stages one at a time — presenting simulations and design requirements. Near the end of the document will show the full circuit design along with a full simulation illustrating the expected noise, frequency response, and an example transient waveform. Finally, a description of the differential to single-ended DAC circuit is presented.

The simulation is performed using Texas Instruments **TINA TI**.
The circuit design and layout were performed using **KiCAD**.

A GitHub repository contains the design files, located here:

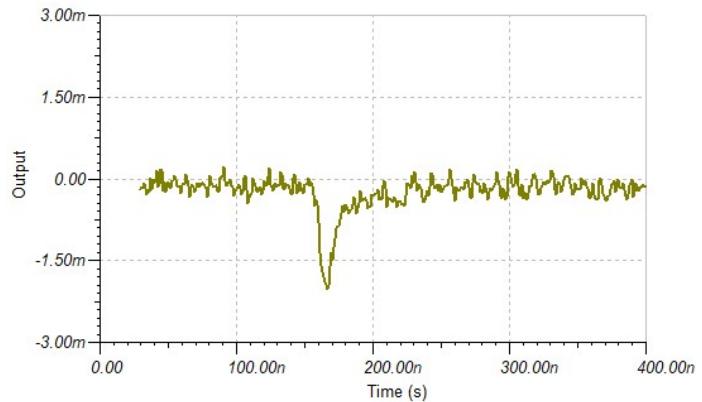
<https://github.com/spenceraxani/KamLAND-FEA>

References:

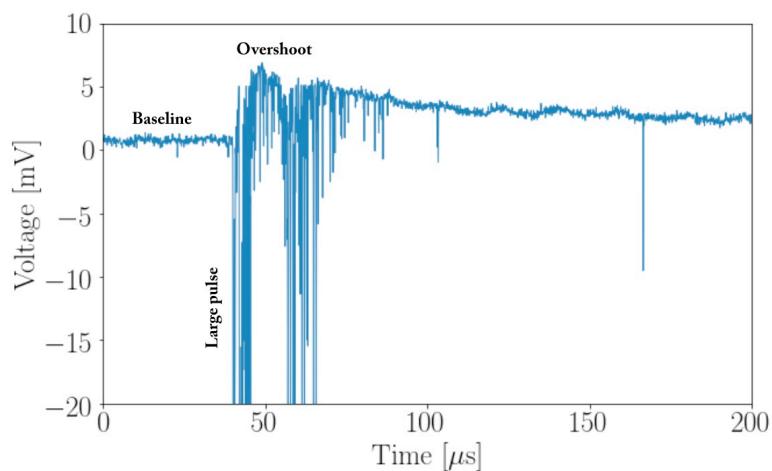
Xilinx: https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_0/pg269-rf-data-converter.pdf

Requirements

The photomultipliers (PMT) are AC coupled to the front end electronics via a large capacitor. The uni-directional AC coupled signals (negative) are assumed to produce signals ranging from 100mV to -8V. **Large signals** are rare — order Hz — and tend to be order microseconds in length. These originate from cosmic ray muons passing through the KamLAND detector. **Small signals**, originating from single photoelectrons, are expected to be between 0.1 and 6mV. These are much more frequent — order 20kHz. The primary frequency component of the small signals are \sim 10-100MHz, and are only \sim 20s of nanoseconds in length . An example small signal (single photoelectron) is shown on the right.



The large signals produce two issues. First, since they contain a large amount of charge, the droop/overshoot introduced by the AC coupling can be substantial and cause issues with the data acquisition system. The overshoot time constant is several 100 microseconds (adjustable design), and we **must** be able to extract small pulses that “ride” on the overshoot. We aim to accomplish this with a *Digital Baseline Recovery System*, which compensates for the overshoot using a digital to analog converter (RF-DAC). An example of overshoot from the KamLAND detector is shown below.

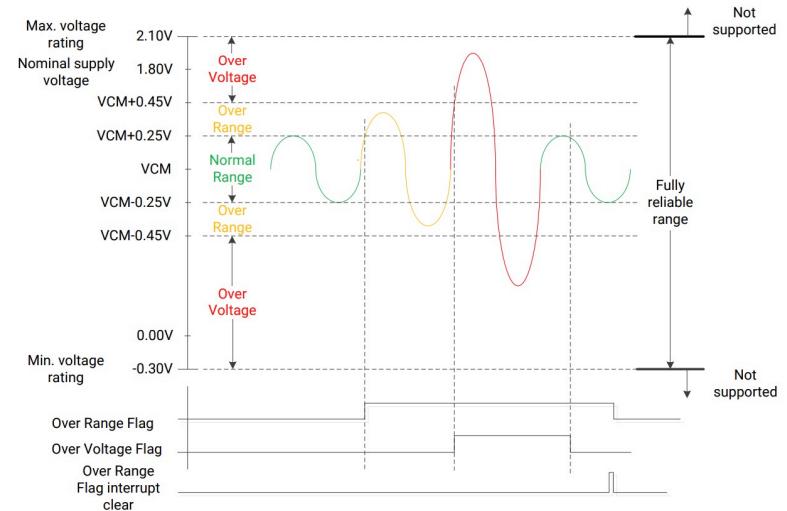


The second issue produced by large signals is due to saturation of the electronics. Once saturated, we can no longer calculate the required baseline correction. Therefore, there must be ample room in the output voltage range to accommodate this. The last part of this document describes the current DAC electronics.

We aim to have two digitizers. The high-gain digitization (**HGain**) is part of the RFSOC and digitizes the small signals at 1GSPS (RF-ADC, 12-bit). This means that we desire the front-end analog (FEA) electronics to have a bandwidth below 500MHz (First Nyquist zone). This channel should have a gain of approximately 6dB (voltage gain of 2). However, the gain from the PMTs has been observed to decrease overtime, therefore, the gain on the FEA should be able to accommodate a change of another 6dB with minimal impact on the performance.

The RF-ADC on the RFSOC operates at a common mode voltage of 1.2V, with a range of ± 0.25 V (right). It has an effective resolution of 12-bits, corresponding to a discrete step size of 0.13mV. The RMS noise on the HGain channel should not be more than this. Also note, that this channel must be protected against the large signals.

Figure 10: Threshold, Over Range, and Over Voltage Levels



The low-gain (**LGain**) channel will likely be digitized by a 250MSPS digitizer. My guess is that it will also be single ended input, differential output. We require that it is able to accept input pulses with a peak voltage $> 8V$. The following describes the reference design which instead uses a separate channel from the RF-ADC, which means the signal has to be attenuated by -24dB. However, the design allows for a rather large change in the gain by simply changing the values of the voltage divider prior to amplifier.

Requirements Summary:

HGain FEA:

- 500MHz bandwidth. Digitization at 1GSPS.
- Capable of Av = 6-12dB. This gives this channel an effective range from ~0-100PE, assuming the average PE peak voltage is ~2.5mV, with a resolution of 0.1mV.
- 0.13mV RMS noise (max).
- Single-ended input, differential output, operating between 1.2V +/- 0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection for op amps and ADC against large signals.

LGain FEA:**

The LGAIN channel needs to be able to digitize input pulses from the PMT ranging from 0 to -8V.

- 100-200MHz bandwidth. Digitization at 250MSPS.
- Capable of -24dB attenuation.
- Noise is less crucial here.
- Single-ended input, differential output? operating between 1.2V +/- 0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection against large signals.

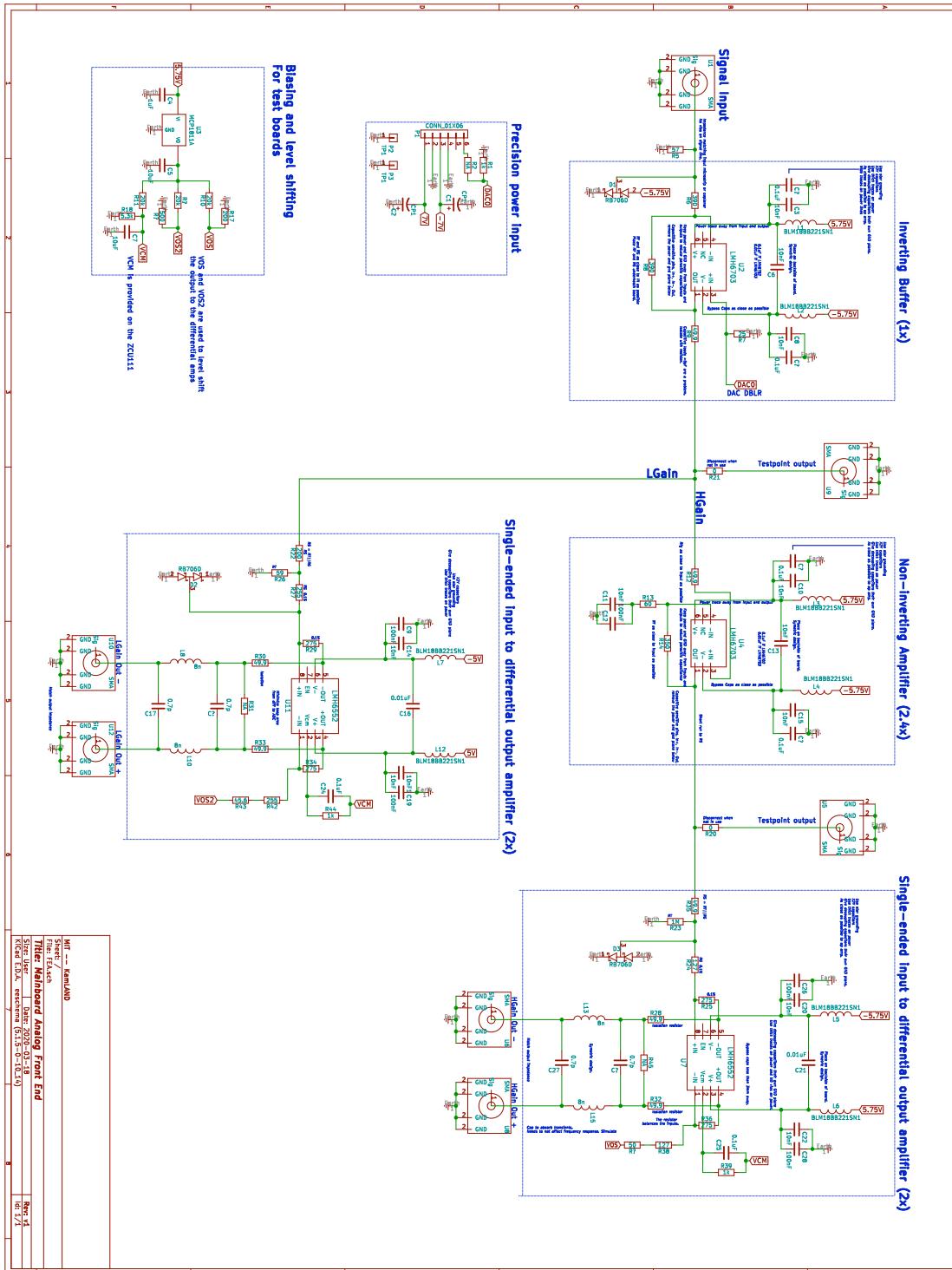
DAC (digital baseline correction):

- 10-100MHz-capable correction
- positive voltage correction, 0-50mV dynamic range after attenuator.
- >8-bit resolution

** Note: more work has gone into designing the HGain channel. The LGain channel has a bandwidth of 500MHz, therefore we could think about redesigning it with a different op amp.

Reference design, ADC full circuit (vectorized).

The following is the circuit diagram for the FEA. Notes regarding layout can be found next to the components.



Inverting buffer (1st stage)

The inverting buffer (perhaps providing some small amplification) is the first stage of the FEA. We impedance match the 50Ω (Av = -6dB), AC coupled, PMT connection near the inverting terminal of a high speed op amp (currently chosen to be the LMH6703 or LMH6702). The inverting configuration is more stable than the non-inverting configurations near unity gain. This configuration also allows us to connect the high input impedance, non-inverting terminal to the RF-DAC to allow for a DBLR.

The SOT-23 version (lower H2 and H3 distortion) of the LMH6702 operates at +/- 5.75V rails with ultra-low distortion (-100/-96 dBc) current feedback amplifier. With also low noise (1.83 nV/√Hz), and a high slew-rate (3100 V/μs). The output range of the amplifier is 1.2V within the rails (output between -4.5V and 4.5V).

Link: <https://www.ti.com/lit/ds/symlink/lmh6702.pdf?ts=1591103993527>

We protect the input of the inverting buffer with clamping diodes. These limit the input range to -5.1V to 400mV (assuming a voltage drop of 400mV). A slight amount of amplification is allowed (up to a gain of Av = 1.3), but beyond this and a -8V signal will saturate the output.

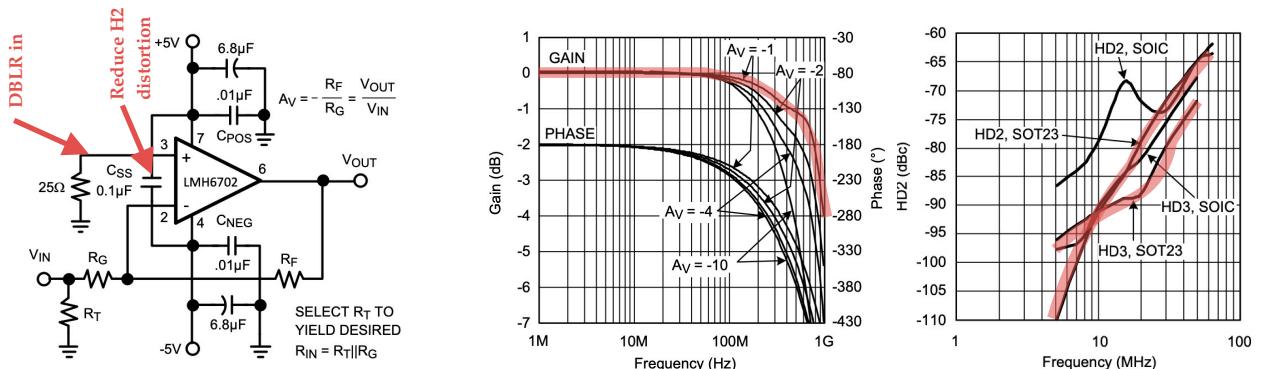


Figure 25. Recommended Inverting Gain Circuit

Disadvantages of Inverting buffer design:

1. We introduce a DBLR level shifting signal to the non-inverting terminal via the RF-DAC. The noise from the RF-DAC is amplified by $1+R_2/R_1$, whereas the signal is only amplified by R_2/R_1 . We need to perform the DBLR at the first stage since the correction needs to be applied to both the HGain and LGain channels, using a single DAC.

TINA TI simulation of inverting buffer:

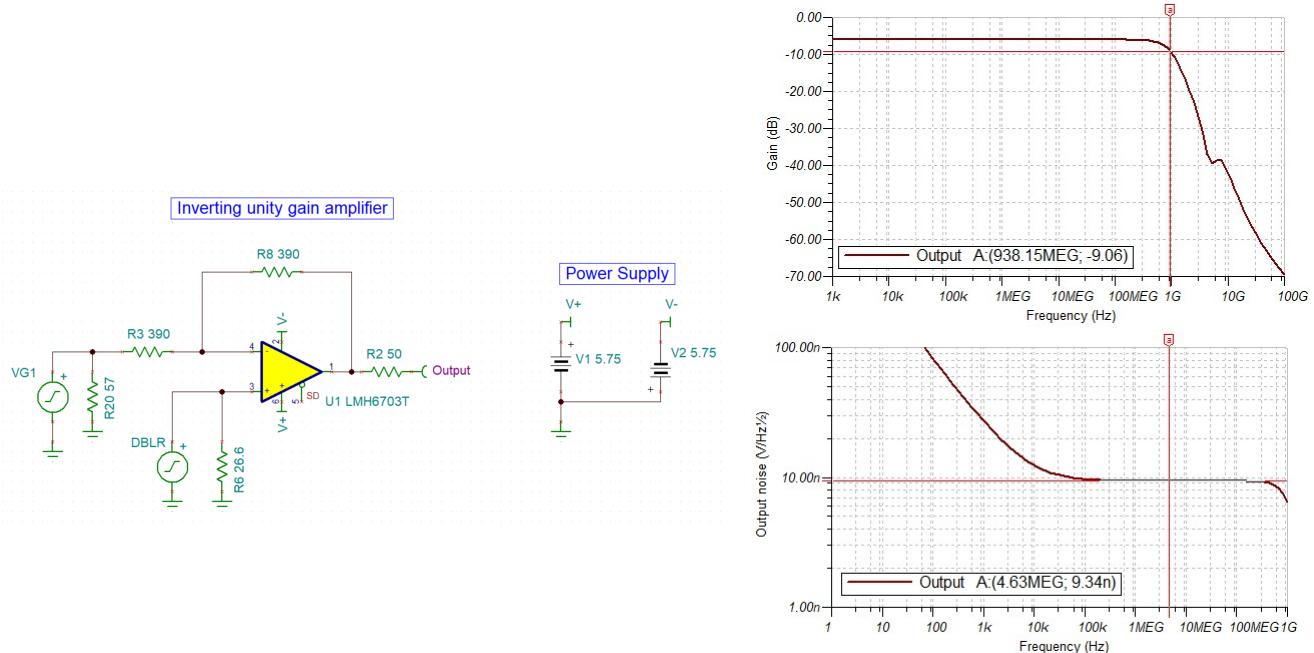
Unity gain. Inverting configuration is more stable than the non-inverting amp at unity gain. Gain = R_8 / R_3 . R_{20} is used to terminate the 50Ohm input, thus providing a -6dB loss. The op amp is powered with $\pm 5.75V$, with an output range from $\pm 4.5V$, or an input from $\pm 9V$.

The output resistor R_2 isolates the output of the amplifier. VG_1 is used to inject waveforms, that is, this is the DAC that is used for the digital baseline restoration (DBLR). The voltage divider formed by R_5 and R_{10} , reduce the full range of the DAC from 2.5V to 500mV (at 14-bit). The DBLR is on the first stage since we want it to correct the waveform prior to dividing the signal into the LGain and HGain channels. The downside of this is, though, that the correction will be delayed by the subsequent stages, digitization, and DAC output.

R_6 should be equal to the parallel resistance ... R_3 and R_8 for the LMH6703 is optimized to be 390Ohms. The terminating resistor R_{20} , should be equal to $1/(1/50-1/R_3)$ for the 50Ohm input. The data sheet recommends $R_6 = 25\Omega$.

RMS noise $\sim 11nV/\sqrt{Hz}$ at a bandwidth of 100MHz is 0.11mV. Noise of the DAC, however is amplified by $1+R_8/R_3$, which is larger than that of the signal. Care must be taken to ensure that the noise from the DAC is sufficiently small.

The frequency response is shown in the simulation. The -3db from the flat region is marked. Here is found to be at 938MHz.



HGain Non-Inverting amplifier

The non-inverting amplifier is the second stage for the HGain channel. This amplifier is used to provide the necessary gain for this channel. RG can be used to change the gain of the amplifier. We use the same op amp as the buffer (LMH6702 or LMH6703).

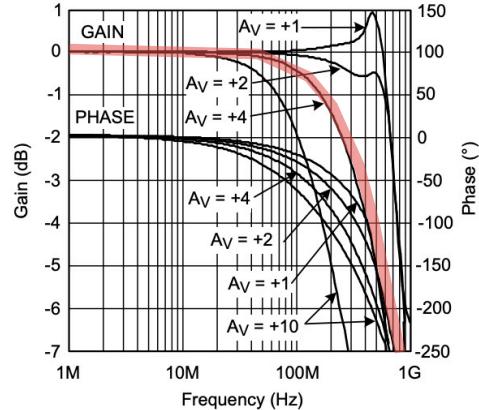
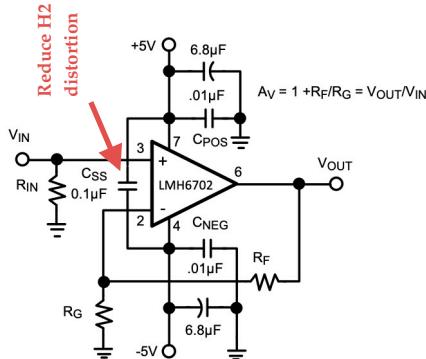


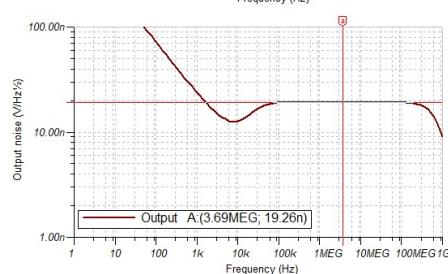
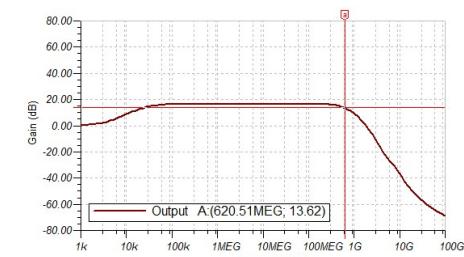
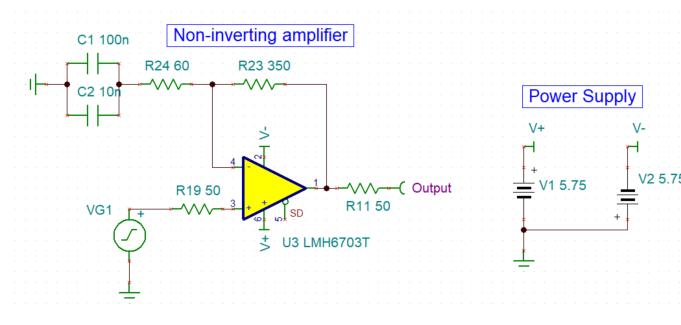
Figure 24. Recommended Non-Inverting Gain Circuit

The non-inverting terminal is connected to the ground via a capacitor. The capacitor reduces the amplification of low frequencies to unity. You can see this in the simulated frequency response below.

TINA TI simulation (see images below):

Non-inverting configuration. Gain = $1+R_{23}/R_{24}$. R19 might not be needed. It is used to isolate the non-inverting input to the op amp from capacitive loading, should be placed as close as possible to the input, same side of PCB, small SMT component. Same goes for R11. If the signal traces are short enough <5mm, these can be neglected. Another option is to remove the power and ground plane below this trace. C1 and C2 limit the low frequency gain (<10KHz) to unity.

The determined 3dB frequency rolloff happens as 621MHz.



HGain Differential Amplifier

We now take the output of the non-inverting amplifier and differentiate the signal. This is accomplished using the 1.5GHz GBP TI LMH6552 (or the LMH6550). It also allows for amplification up to $A_v = 4$ (however we'll keep this at unity gain), and has a similar slew rate to the LMH6702 (3800-V/ μ s at unity gain. Current feedback amplifier). This differential op amp also has an integrated output common mode control to connect to the common mode of the RF-ADC ($V_{cm} = 1.2V$).

The feedback resistors should be 270-390Ohms with 0.1% value uncertainty. Similarly to R_G . Bypass V_{cm} with a 0.1uF capacitor. The design needs to be symmetric.

The final version should have the WSON LMH6552 package rather than the SOIC package since it has better thermal properties.

We also need this amplifier to level shift the uni-directional signal such that we maximize the range of the RF-ADC. This is accomplished by level shifting the signal by biasing the non-inverting terminal using a precision voltage source. However, if the gain changes in the future, the level shifting voltage will also need to be changed. For this, I suggest using a voltage divider on the 1.8V line provided by the Xilinx board.

We protect the input of the differential amplifier using clamping diodes. These limit the input range to -400mV to 400mV. The optimal range is +/-250mV, however, the RF-ADC can safely handle up to +/-1V. The diodes are not included in the simulation.

The series resistors on the output isolate the capacitive loading from the RF-ADC (unknown value). They may need to be modified from 25-1k.

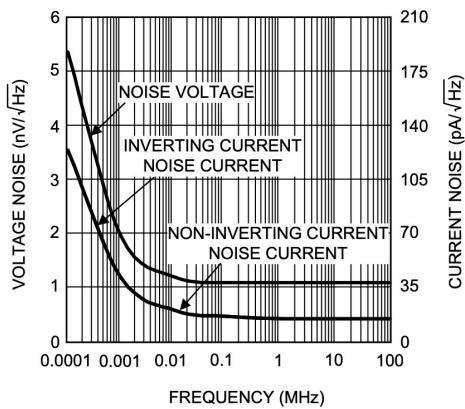


Figure 33. Input Noise vs Frequency

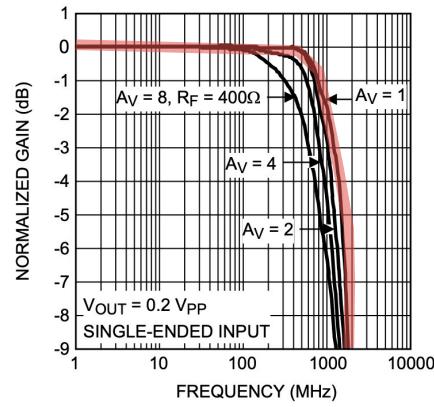


Figure 2. Frequency Response vs Gain

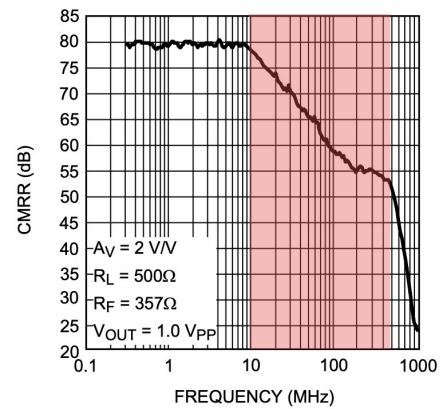


Figure 29. CMRR

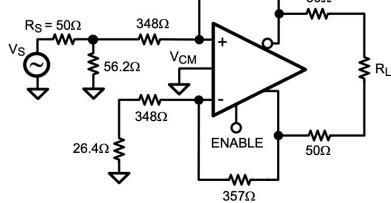


Figure 41. Single Ended Input S-Parameter Test Circuit (50Ω System)

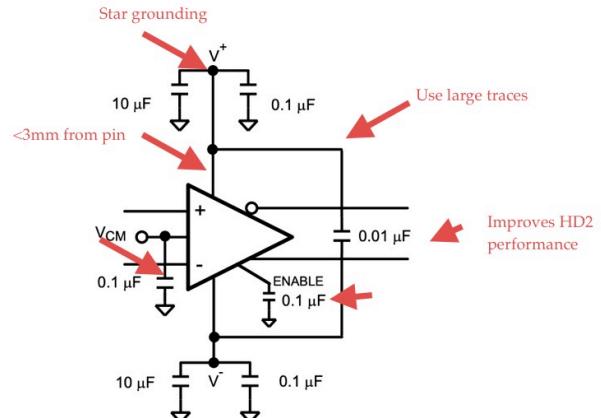
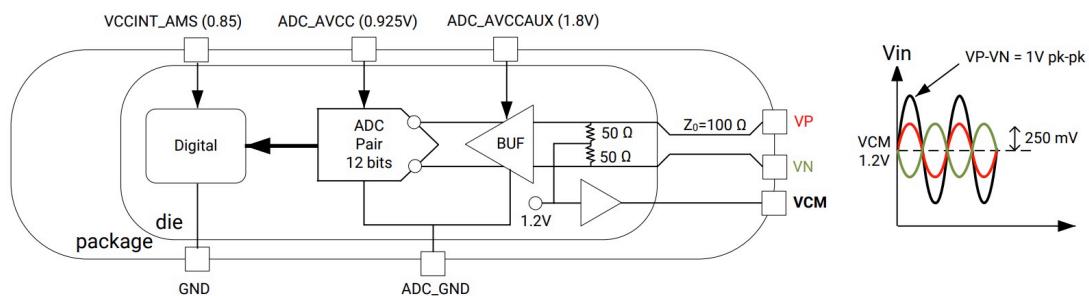


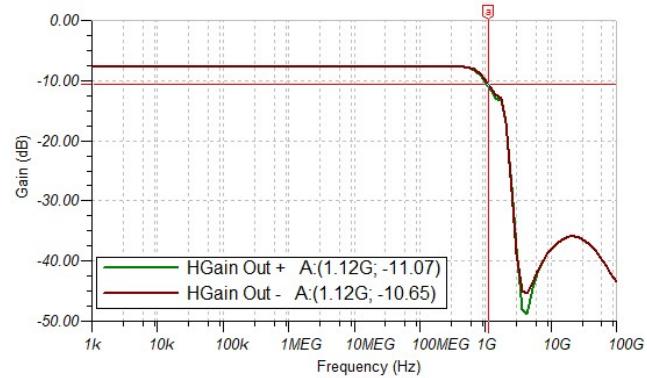
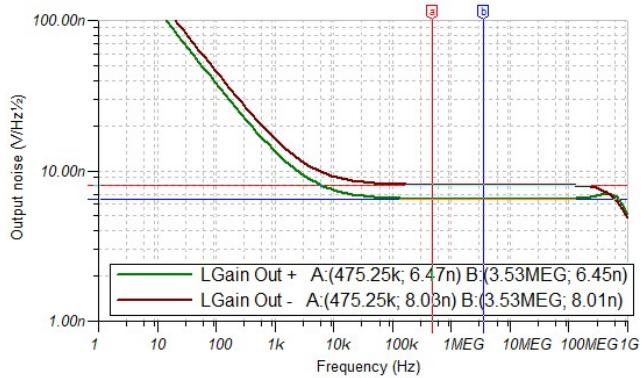
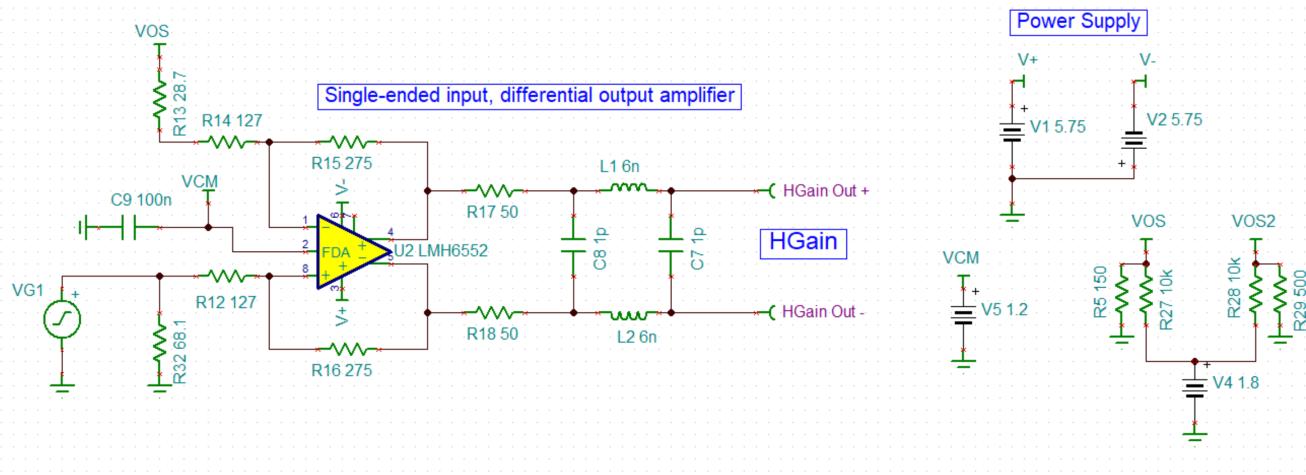
Figure 53. Split Supply Bypassing Capacitors

TINA TI simulation:

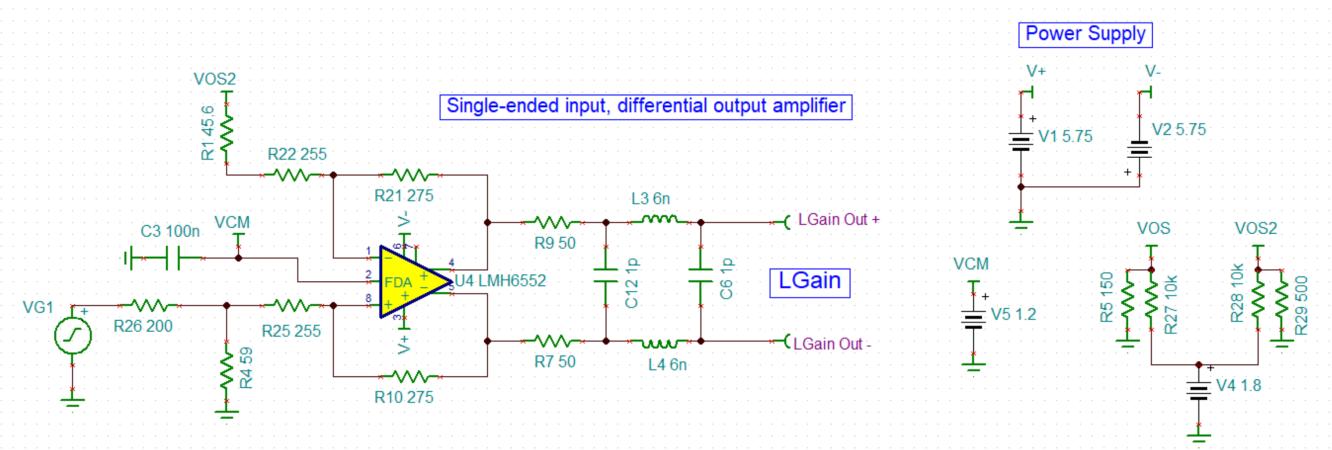
V_{cm} of the differential amplifier connects to the common mode of the RF-ADC. As shown in the image below, V_{CM} is feed by a voltage follower at 1.2V. The LMH6552 op amp recommends using a 0.1uF cap on V_{CM}. V_{os} supplies the level shifting used to maximizes the useable range of the ADC. R₁₇ and R₁₈ are used to isolate the op amp from capacitive loading from the RF-ADC input. This op amp can provide amplification, however the current configuration uses it at unity gain. R₃₂ is the termination resistor. The cutoff frequency is 1.3GHz. And the noise density is lower than 10nV / sqrt(Hz) in our bandwidth of interest.

Figure 8: RF-ADC Analog Input





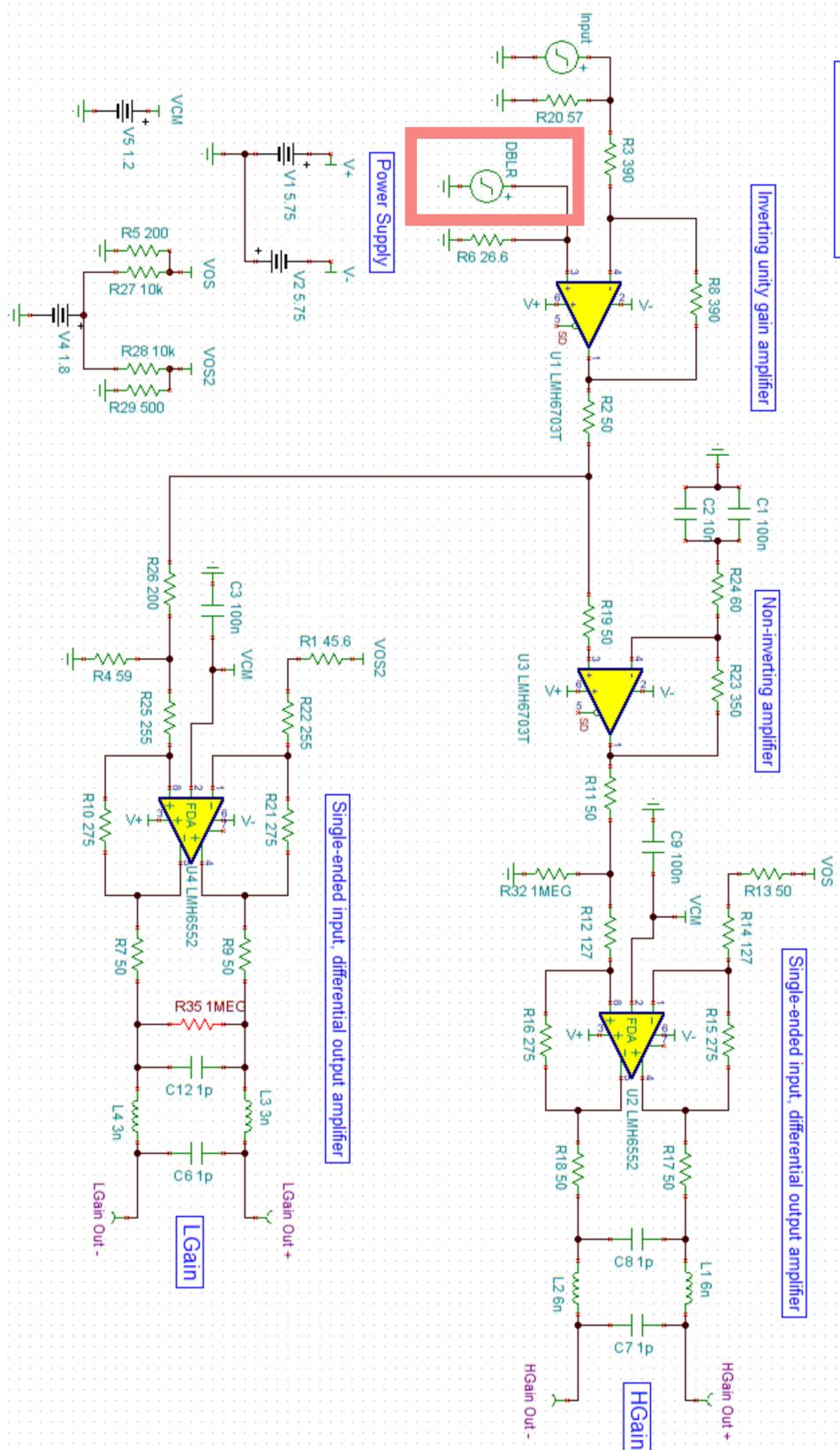
The LGain differential channel uses a very similar setup to the HGAIN differential amp, although for an attenuator before the amp. Below, I show the circuit, and then in the next section, you can see all the circuit stages together.



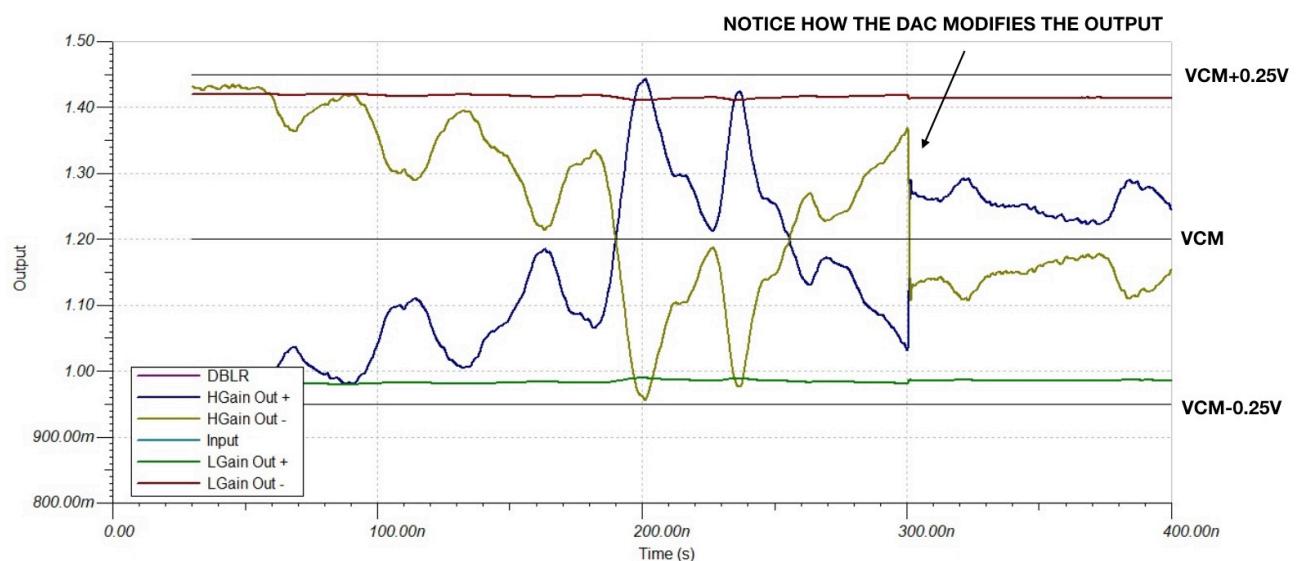
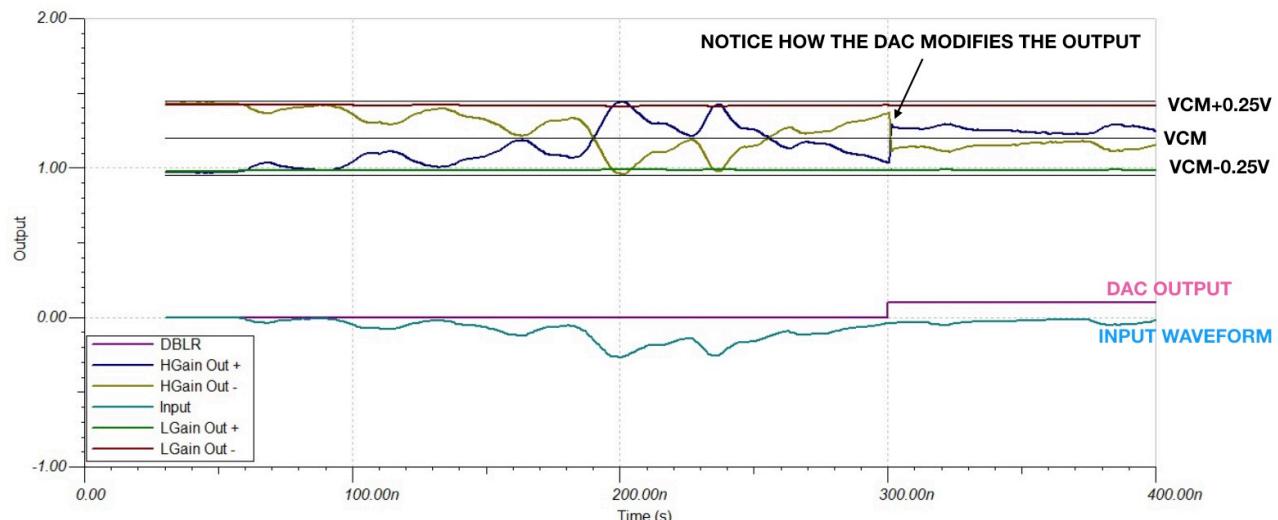
HGain Full simulation

Analog Front End, MOGURA2

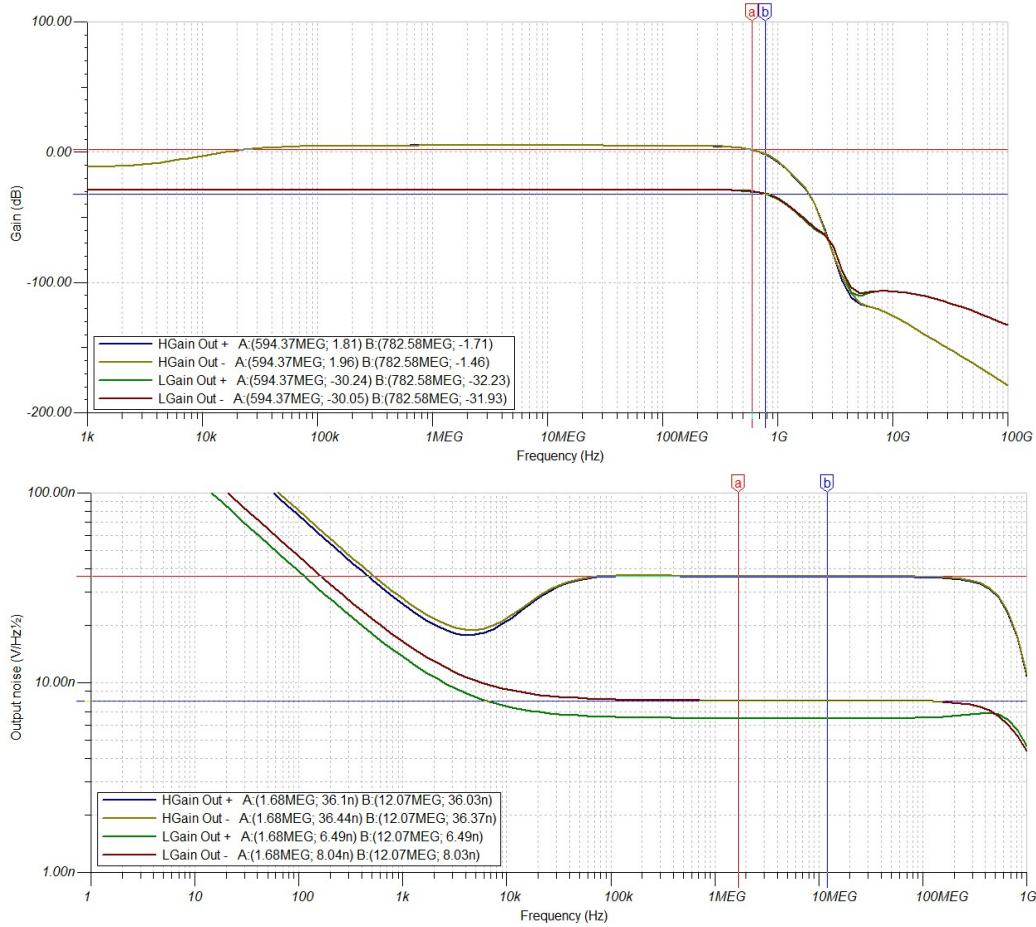
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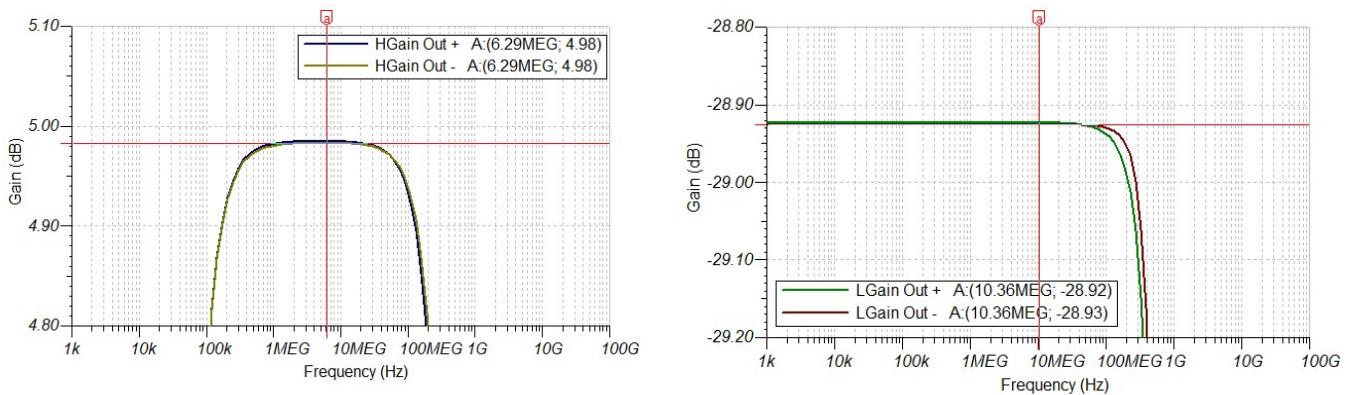
Transient simulation using a waveform with a range from 0 to -300mV:



The following two figures show the gain and noise density for the differential outputs on HGAIN and LGAIN.



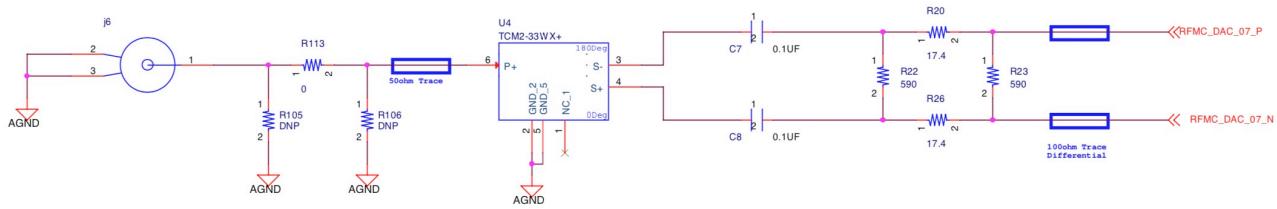
The following figures show the linearity of the HGAIN (left) and LGAIN (right) channels:



DAC requirements

The RF-DAC will be used to provide the digital baseline recovery. The RF-DAC appears to operate between 0 and 2.5V, with 14-bits of resolution. While the RF-DAC can operate at 6GSPS, we actually only need it for adding ~MHz frequency corrections (see overshoot waveform in the second figure of this document). The differential output from the DAC is first passed through a differential to single-ended op amp attenuator (unless there are better ways to perform the differential to single-ended conversion). The Xilinx method is to use a transformer, specifically, for their DAC conversion they use the TCM2-33WX+ transformer, which appears as though the frequency response is from 10MHz to 3GHz, making it unsuitable for the MHz signals that are of interest. The Xilinx converter schematic is shown below.

0-1GHz Channels Minicircuit Balun [LF]



We expect the overshoot to introduce order 10mV of distortion to the baseline. Therefore, the DAC output is attenuated from 0-2.5V to 0-50mV, through a 50x voltage divider.

An untested requirement is that the RF-DAC correction is applied very shortly after the waveform digitization. There will be approximately 10ns of added delay simply from the analog electronics as well. The delay from digitization to correction application (either made through the FPGA or CPU) is unknown but will be tested shortly once the labs are open.

TINA TI Simulation:

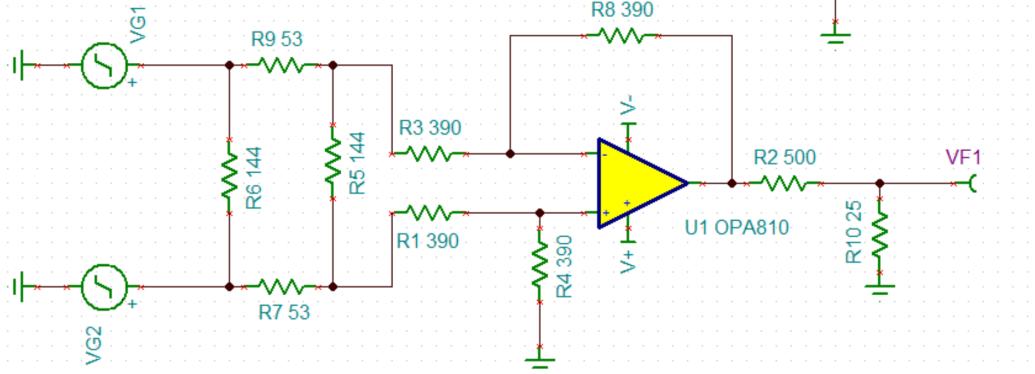
The simulation below shows the input of a 1MHz sine wave, and the output at VF1. The corresponding voltage drop is ~50x. It is desirable to have an op amp with a low total response time, as well as 10-100MHz gain band-width product. The Pi-attenuator at the input from VG1 and VG2 attenuates the signal prior to the op amp, and the voltage divider at the output of the op amp further attenuates the signal. The total attenuation for this circuit should be capable of -34dB.

If you look back at the section **HGain Full simulation**, the output of the circuit below connects to the non-inverting terminal of the first stage amplifier (labelled there as DBLR, in a red box). That is the correction from the DAC is inserted into the first stage such that it modifies both the LGain and HGain channels.

DAC, MOGURA2

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Diff to single-ended



Power Supply

