

# KamLAND analog frontend electronics



## MoGURA2 design document

Dr. Spencer N. G. Axani - June 17, 2020

The KamLAND frontend analog electronics (FEA) take the AC coupled signal from a single photomultiplier tube (PMT), amplify and condition the signal such that it can be digitized by the **Zynq UltraScale+ RFSoC RF-ADC**. The following describes a reference design that is capable of providing the correct amplification for a low gain (**LGain**) and high gain (**HGain**) channel, over the desired bandwidth (500MHz). This design introduces a example implementation of the digital baseline recovery (**DBRL**) — a correction applied to the waveform via an RF-DAC to compensate for droop/overshoot introduced by the AC coupling.

This document will first give an overview and the requirements of the FEA, then go through the FEA stages one at a time — presenting simulations and design requirements. After that, the document will show the full circuit simulation results; illustrating the expected noise, frequency response, and an example transient waveform. Following this, a description of the differential to single-ended DAC circuit is presented.

The end of the document contains an example 4-layer PCB containing 3 FEA channels. It is currently being manufactured as an expansion board to the ZCU111, RFSOC test board. We plan to use this for an in-situ test at KamLAND during Fall 2020.

The simulation is performed using Texas Instruments **TINA TI**.  
The circuit design and layout were performed using **KiCAD**.

A GitHub repository contains the design files, located here:

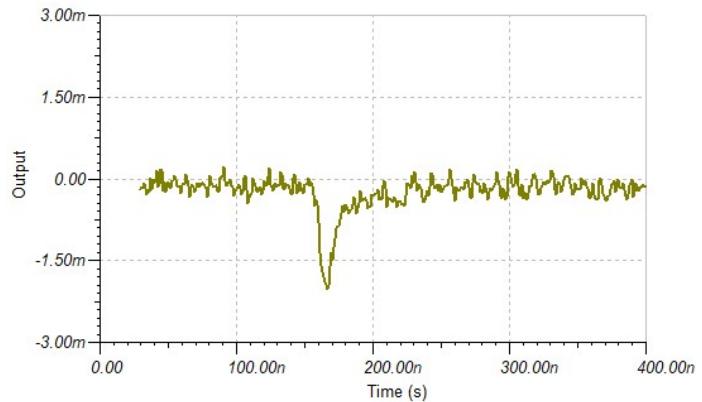
<https://github.com/spenceraxani/KamLAND-FEA>



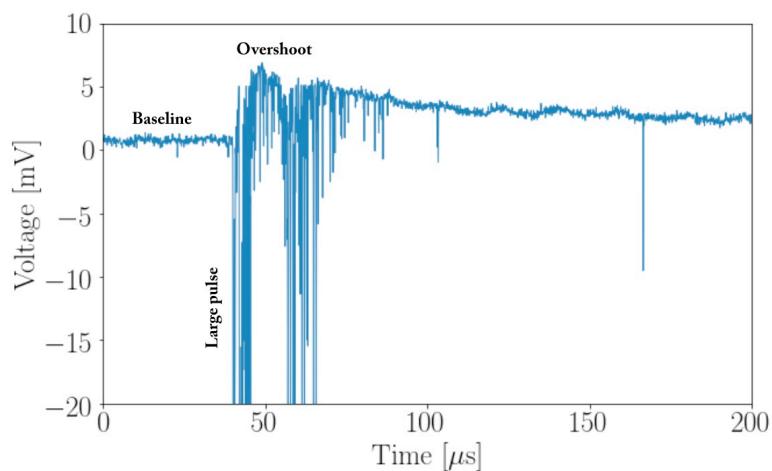
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Technology

## Requirements

The photomultipliers (PMT) are AC coupled to the front end electronics via a large capacitor. The uni-directional AC coupled signals (negative) are assumed to produce signals ranging from 100mV to -8V. **Large signals** are rare — order Hz — and tend to be order microseconds in length. These originate from cosmic ray muons passing through the KamLAND detector. **Small signals**, originating from single photoelectrons, are expected to be between 0.1 and 6mV. These are much more frequent — order 20kHz. The primary frequency component of the small signals are  $\sim$ 10-100MHz, and are only  $\sim$ 20s of nanoseconds in length . An example small signal (single photoelectron) is shown on the right.



The large signals produce two issues. First, since they contain a large amount of charge, the droop/overshoot introduced by the AC coupling can be substantial and cause issues with the data acquisition system. The overshoot time constant is several 100 microseconds (adjustable design), and we **must** be able to extract small pulses that “ride” on the overshoot. We aim to accomplish this with a *Digital Baseline Recovery System*, which compensates for the overshoot using a digital to analog converter (RF-DAC). An example of overshoot from the KamLAND detector is shown below.



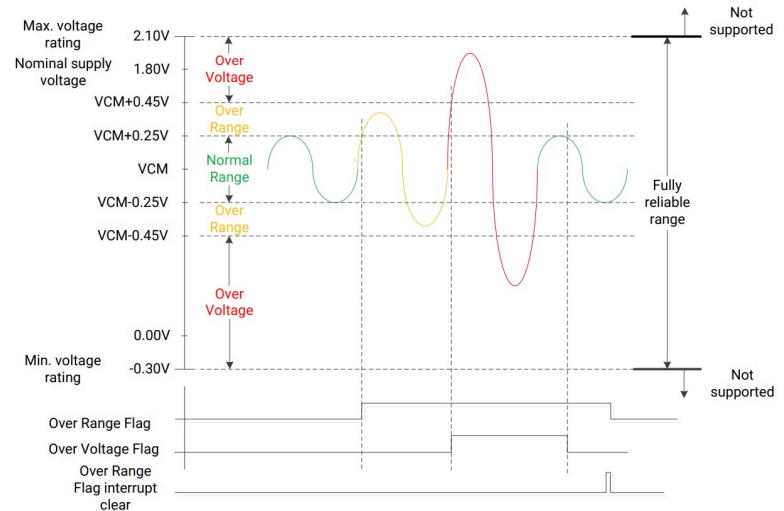
The second issue produced by large signals is due to saturation of the electronics. Once saturated, we can no longer calculate the required baseline correction. Therefore, there must be ample room in the output voltage range to accommodate this. The last part of this document describes the current DAC electronics.

We aim to have two digitizers. The high-gain digitization (**HGain**) is part of the RFSOC and digitizes the small signals at 1GSPS (RF-ADC, 12-bit). This means that we desire the front-end analog (FEA) electronics to have a bandwidth below 500MHz (First Nyquist zone). This channel should have a gain of approximately 6dB (voltage gain of 2). However, the gain from the PMTs has been observed to decrease overtime, therefore, the gain on the FEA should be able to accommodate a change of another 6dB with minimal impact on the performance.

The RF-ADC on the RFSOC operates at a common mode

voltage of 1.2V, with a range of  $\pm 0.25\text{V}$  (right). It has an effective resolution of 12-bits, corresponding to a discrete step size of 0.13mV. The RMS noise on the HGain channel should not be more than this. Also note, that this channel must be protected against the large signals.

**Figure 10: Threshold, Over Range, and Over Voltage Levels**



The low-gain (**LGain**) channel will likely be digitized by a 250MSPS digitizer. My guess is that it will also be single ended input, differential output. We require that it is able to accept input pulses with a peak voltage  $>8\text{V}$ . The following describes the reference design which instead uses a separate channel from the RF-ADC, which means the signal has to be attenuated by -24dB. However, the design allows for a rather large change in the gain by simply changing the values of the voltage divider prior to amplifier.

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## Requirements Summary:

### HGain FEA:

- 500MHz bandwidth. Digitization is expected to be 1GSPS.
- Capable of Av = 6dB to 20dB. This gives this channel an effective range from ~0-100PE, assuming the average PE peak voltage is ~2.5mV, with a resolution of 0.1mV. Gain loss in the PMT aging can be compensated for with higher larger Av.
  - 0.13mV RMS noise (max).
  - Single-ended input (50Ohm coax), differential output, operating between 1.2V +/-0.25V.
  - Digital baseline recovery via RF-DAC.
  - Voltage protection for op amps and RF-ADC against large signals.

### LGain FEA:

The LGAIN channel needs to be able to digitize input pulses from the PMT ranging from 100mV to -8V.

- 125MHz bandwidth. Digitization at 250MSPS\*\*.
- Capable of -24dB to -4dB attenuation.
- Single-ended input, differential output (likely). operating between 1.2V +/-0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection against large signals.

### DAC (digital baseline correction):

- 10-100MHz-capable correction
- positive voltage correction, 0-50mV dynamic range after attenuator.
- >8-bit resolution

\*\* Note: The current design uses the RF-ADC to measure this channel. Eventually, we would like a dedicated fast ADC at 250MSPS for this channel.

# TinaTI Simulation and circuit description

## Inverting buffer (1st stage)

The inverting buffer (perhaps providing some small amplification) is the first stage of the FEA. We impedance match the 50Ω (Av = -6dB), AC coupled, PMT connection near the inverting terminal of a high speed op amp (currently chosen to be the LMH6703 or LMH6702). The termination resistor needs to be correctly assigned to minimize reflections. It can be calculated through  $RS = RT \parallel RG$ .

The inverting configuration is more stable than the non-inverting configurations at unity gain. This configuration also allows us to connect the high input impedance, non-inverting terminal to the RF-DAC for the digital baseline restoration (DBLR).

The SOT-23 package (lower H2 and H3 distortion) of the LMH6703 operates at +/- 5.5V rails with ultra-low distortion (-100/-96 dBc) current feedback amplifier. With also low noise (1.83 nV/√Hz), and a high slew-rate (3100 V/μs). The output range of the amplifier is 1.2V within the rails (output between -4.3V and 4.3V). Ideally, we would supply +/-6V, if possible. Link: <https://www.ti.com/lit/ds/symlink/lmh6702.pdf?ts=1591103993527>

We protect the input of the inverting buffer with clamping diodes. These limit the input range to -5.1V to 400mV (assuming a voltage drop of 400mV). We keep this amp at unity gain since it must be able linearly buffer input signals from 100mV to -8.0V.

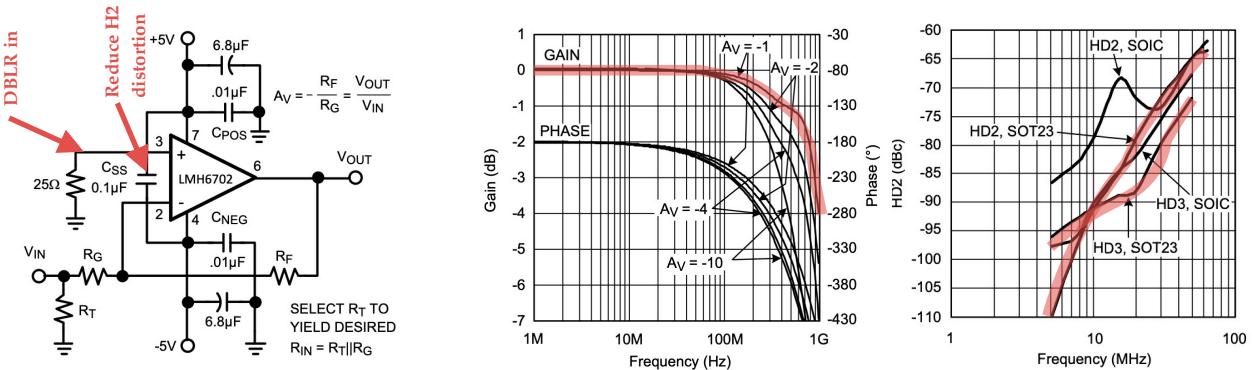


Figure 25. Recommended Inverting Gain Circuit

### Disadvantages of Inverting buffer design:

1. We introduce a DBLR level shifting signal to the non-inverting terminal via the RF-DAC. The noise from the RF-DAC is amplified by  $1+R_2/R_1$ , whereas the signal is only amplified by  $R_2/R_1$ . We need to perform the DBLR at the first stage since the correction needs to be

applied to both the HGain and LGain channels, using a single DAC. The voltage divider ( $25.5 / (5000+25.5) = 0.005$ ), will lower the noise from the DBLR.

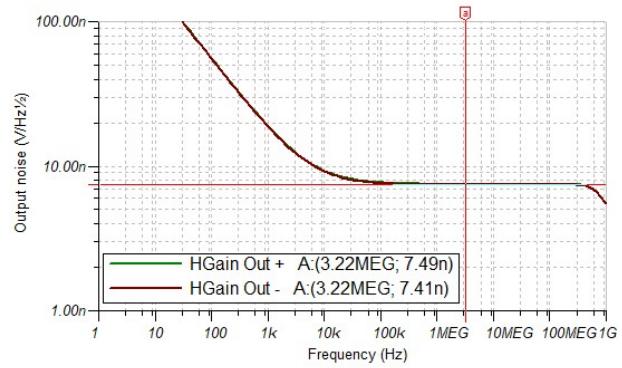
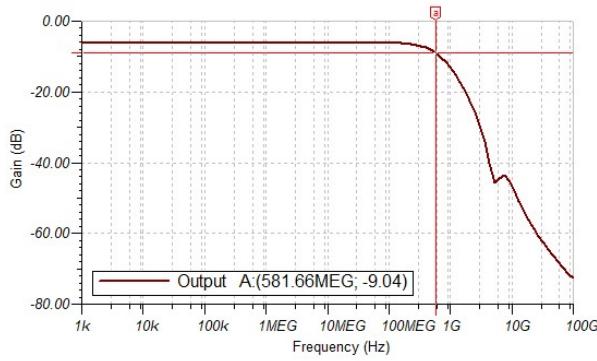
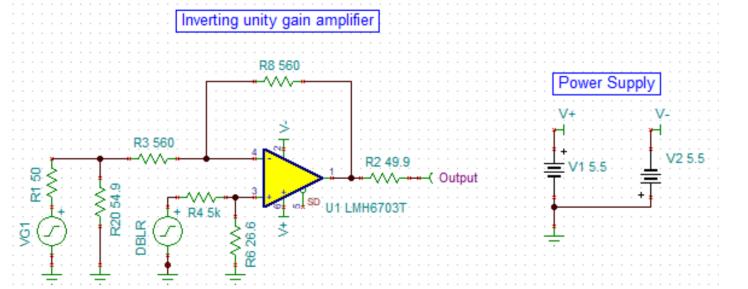
### TINA TI simulation of inverting buffer:

The gain is defined by the ratio of R8 / R3. R20 is used to terminate the 50Ohm input, thus providing a -6dB loss, we require termination precision greater than of 0.1%. The op amp is powered with +/-5.5V, producing an output range from +/-4.3V, or an input from +/-8.6V (for unity gain).

The output resistor R2 isolates the output of the amplifier. It might not be needed. The DBLR connection is used to inject waveforms, that is, this is the RF-DAC connection used to provide the digital baseline restoration (DBLR). The voltage divider formed by R4 and R6, reduce the full range of the DAC from 2.5V to 50mV (at 14-bit). The DBLR is on the first stage since we want it to correct the waveform prior to dividing the signal into the LGain and HGain channels. The downside of this is, though, that the correction will be delayed by the subsequent stages, digitization, and RF-DAC output.

R20 should be equal to the parallel resistance, R3 and R8, for the LMH6703 (SOT-23 package) is optimized to be 560Ohms. The terminating resistor R20, should be equal to  $1/(1/50-1/R3)$  for the 50Ohm input. The data sheet recommends R6 = 250Ohms.

RMS noise ~  $11\text{nV}/\sqrt{\text{Hz}}$  at a bandwidth of 100MHz is 0.11mV. Noise of the RF-DAC, however is amplified by  $1+R8/R3$  after passing through the voltage divider. Care must be taken to ensure that the noise from the DAC is sufficiently small.



The frequency response is shown in the simulation. The -3db from the flat region is marked. Here is found to be at 581MHz. Using R3 = R8 smaller than 560Ohms will increase the -3dB cutoff, however may introduce some peaking. 560Ohms is the recommended value from TI, see image on the right from the data sheet for the LMH6703.

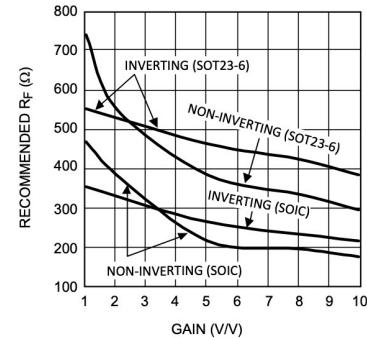


Figure 27. Recommended  $R_F$  vs. Gain

# HGain Non-Inverting amplifier

The non-inverting amplifier is the 2nd and 3rd stage for the HGain channel. This amplifier is used to provide the necessary gain for this channel. RG can be used to change the gain of the amplifier. We use the same op amp as the buffer (LMH6702 or LMH6703). Using two Non-Inverting amplifiers allows us to easily provide gains up to 20dB without impacting the frequency response (cutoff ~500MHz, or the first Nyquist zone for the 1GSPS RF-ADC).

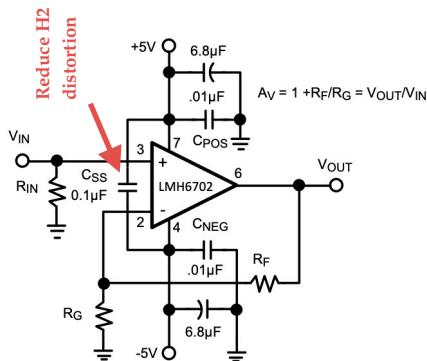
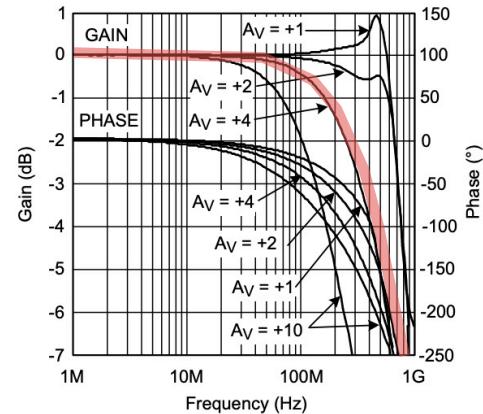


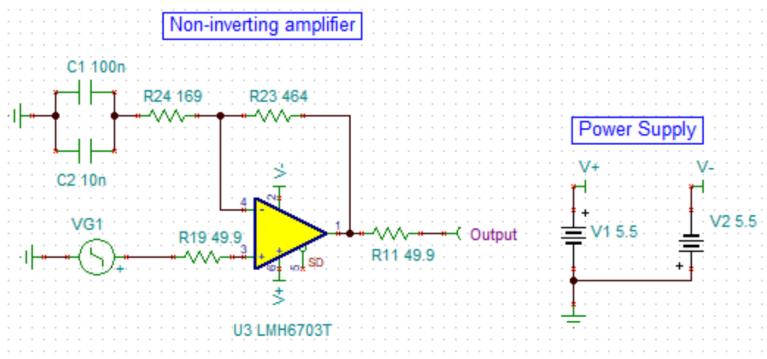
Figure 24. Recommended Non-Inverting Gain Circuit



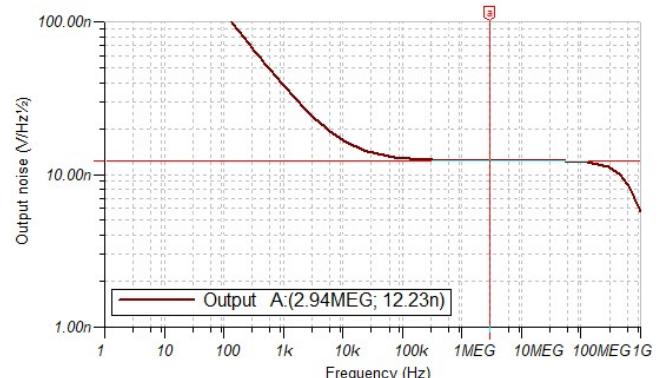
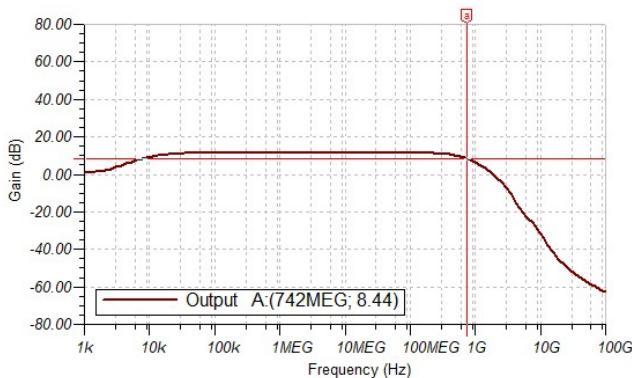
The inverting terminal is connected to the ground via two capacitors. The capacitors reduce the amplification of low frequencies to unity. You can see this in the simulated frequency response below.

## TINA TI simulation (see images below):

Non-inverting configuration. Gain =  $1+R_{23}/R_{24}$ . R19 might not be needed. It is used to isolate the non-inverting input to the op amp from capacitive loading, should be placed as close as possible to the input, same side of PCB, small SMT component. Same goes for R11. If the signal traces are short enough <5mm, these can be neglected. Another option is to remove the power and ground plane below this trace. C1 and C2 limit the low frequency gain (<10KHz) to unity.



The determined 3dB frequency rolloff happens as 742MHz.



# HGain Differential Amplifier

We now take the output of the 3rd-stage non-inverting amplifier and differentiate the signal. This is accomplished using the 1.5GHz GBP TI LMH6552 (or the LMH6550). It also allows for amplification up to  $A_v = 4$  (however we'll keep this at unity gain), and has a similar slew rate to the LMH6702 (3800-V/ $\mu$ s at unity gain. Current feedback amplifier). This differential op amp also has an integrated output common mode control to connect to the common mode of the RF-ADC ( $V_{cm} = 1.2V$ ).

The feedback resistors should be 270-390Ohms with 0.1% value uncertainty. Similarly,  $R_G$  must also have sub-0.1% precision. Bypass  $V_{cm}$  with a 0.1uF capacitor. The design needs to be symmetric.

The final version should have the WSON LMH6552 package rather than the 8-SOIC package since it has better thermal properties. The test board that I am designing uses the 8-SOIC since it has to be manufactured by hand.

We also need this amplifier to level shift the uni-directional signal such that we maximize the range of the RF-ADC. This is accomplished by level shifting the signal by biasing the non-inverting terminal using a precision voltage source. However, if the gain changes in the future, the level shifting voltage will also need to be changed. A resistor connected to  $V_{OS}$  controls the level shifting. I'll mention this again below, once we see the circuit.

We protect the input of the differential amplifier using clamping diodes. This limits the input range to -400mV to 400mV. The optimal range is +/-250mV, however, the RF-ADC can safely handle up to +/-1V. The diodes are not included in the simulation due to in-availability of SPICE models.

The series resistors on the output isolate the capacitive loading from the RF-ADC (unknown value). They may need to be modified from 10-1k.

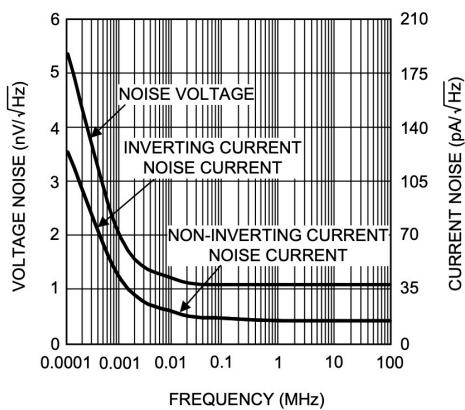


Figure 33. Input Noise vs Frequency

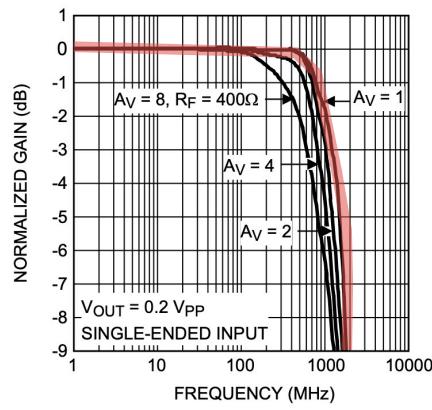


Figure 2. Frequency Response vs Gain

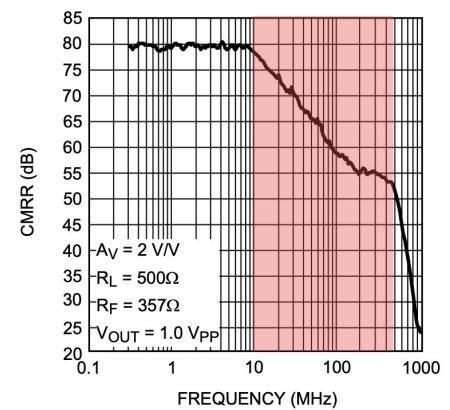


Figure 29. CMRR

## TINA TI simulation:

$V_{CM}$  (common mode voltage) of the differential amplifier connects to the common mode of the RF-ADC. As shown in the image to the below.  $V_{CM}$  is feed by a voltage follower at 1.2V. The LMH6552 op amp recommends using a 0.1 $\mu$ F cap on  $V_{CM}$ .

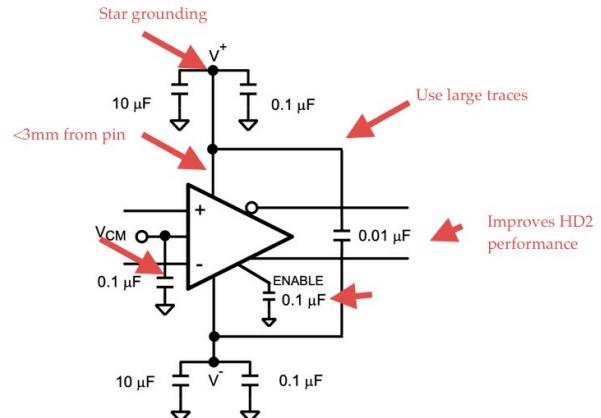
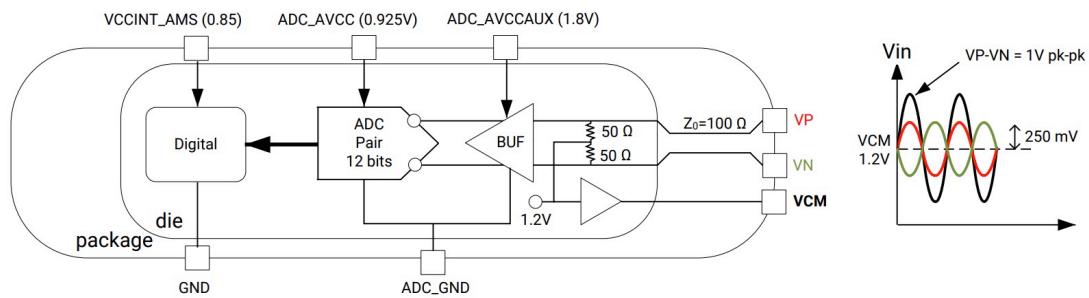
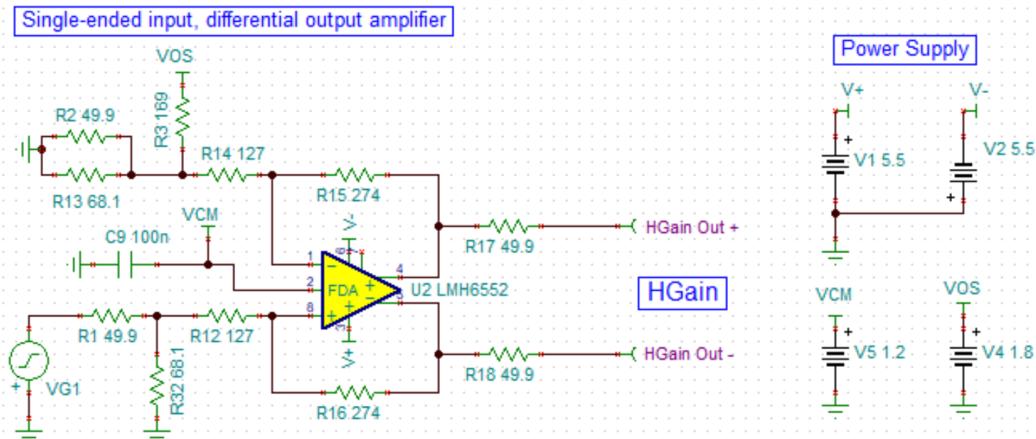


Figure 53. Split Supply Bypassing Capacitors

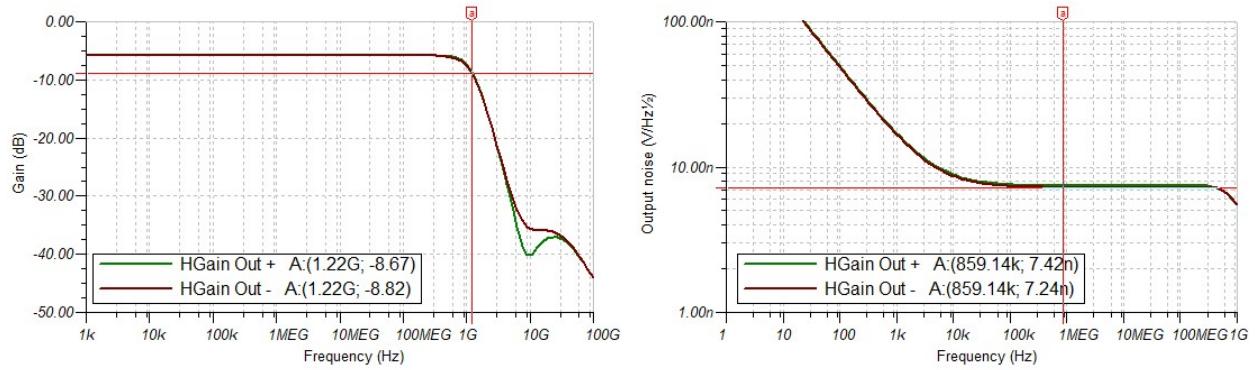
Figure 8: RF-ADC Analog Input



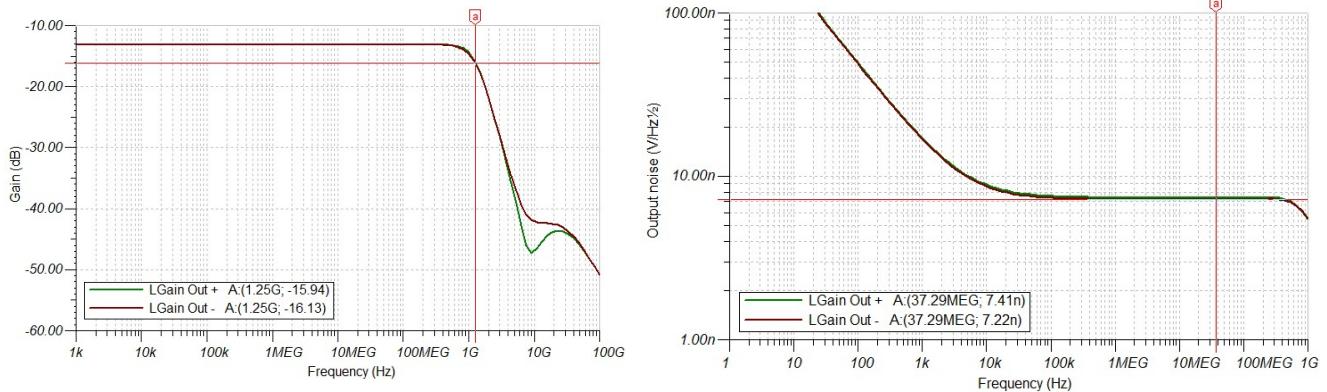
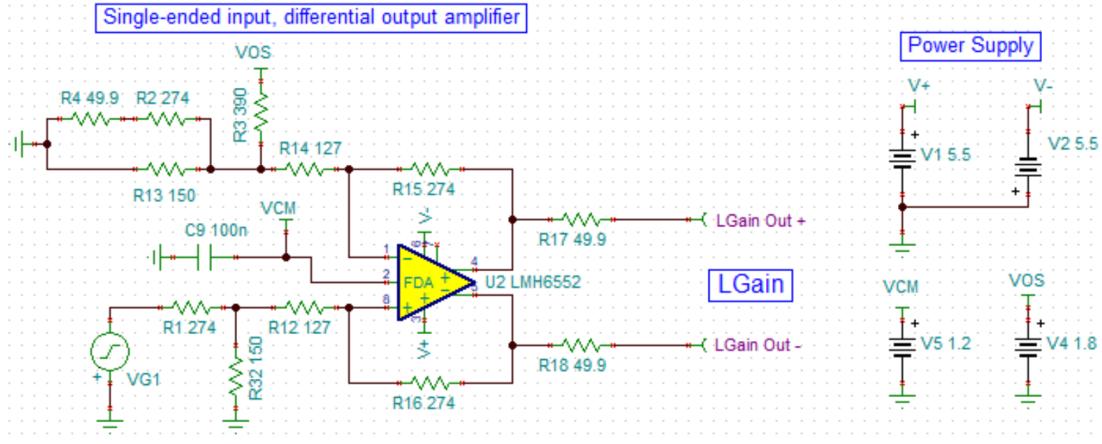
The connection in the simulation below,  $V_{OS}$ , supplies the level shifting used to maximizes the useable range of the RF-ADC. R17 and R18 are used to isolate the op amp from capacitive loading from the RF-ADC input. This op amp can provide amplification, however the current configuration uses it at unity gain. R32 is the termination resistor.



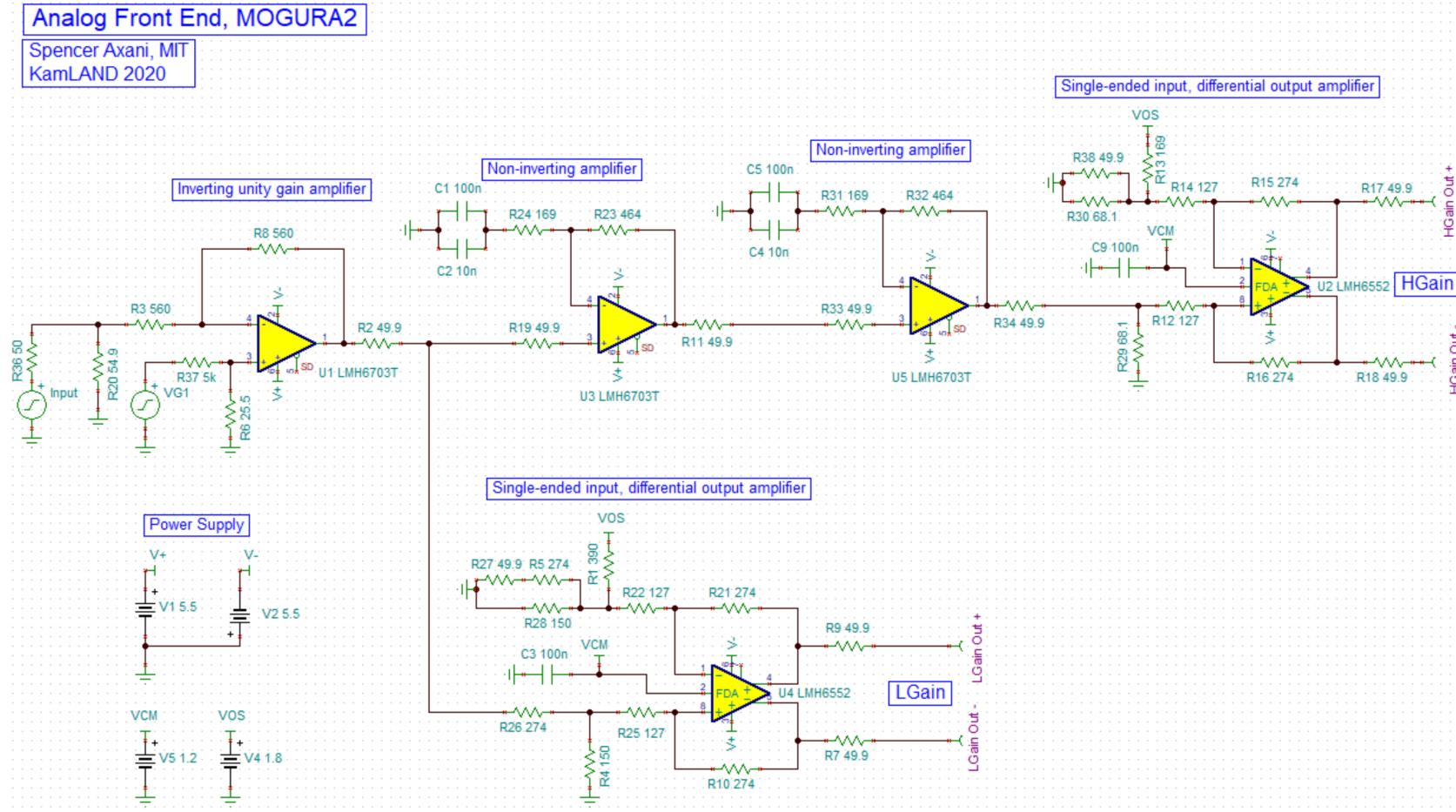
The -3dB cutoff frequency is 1.22GHz. And the noise density is lower than 7.4nV/sqrt(Hz) in our bandwidth of interest.



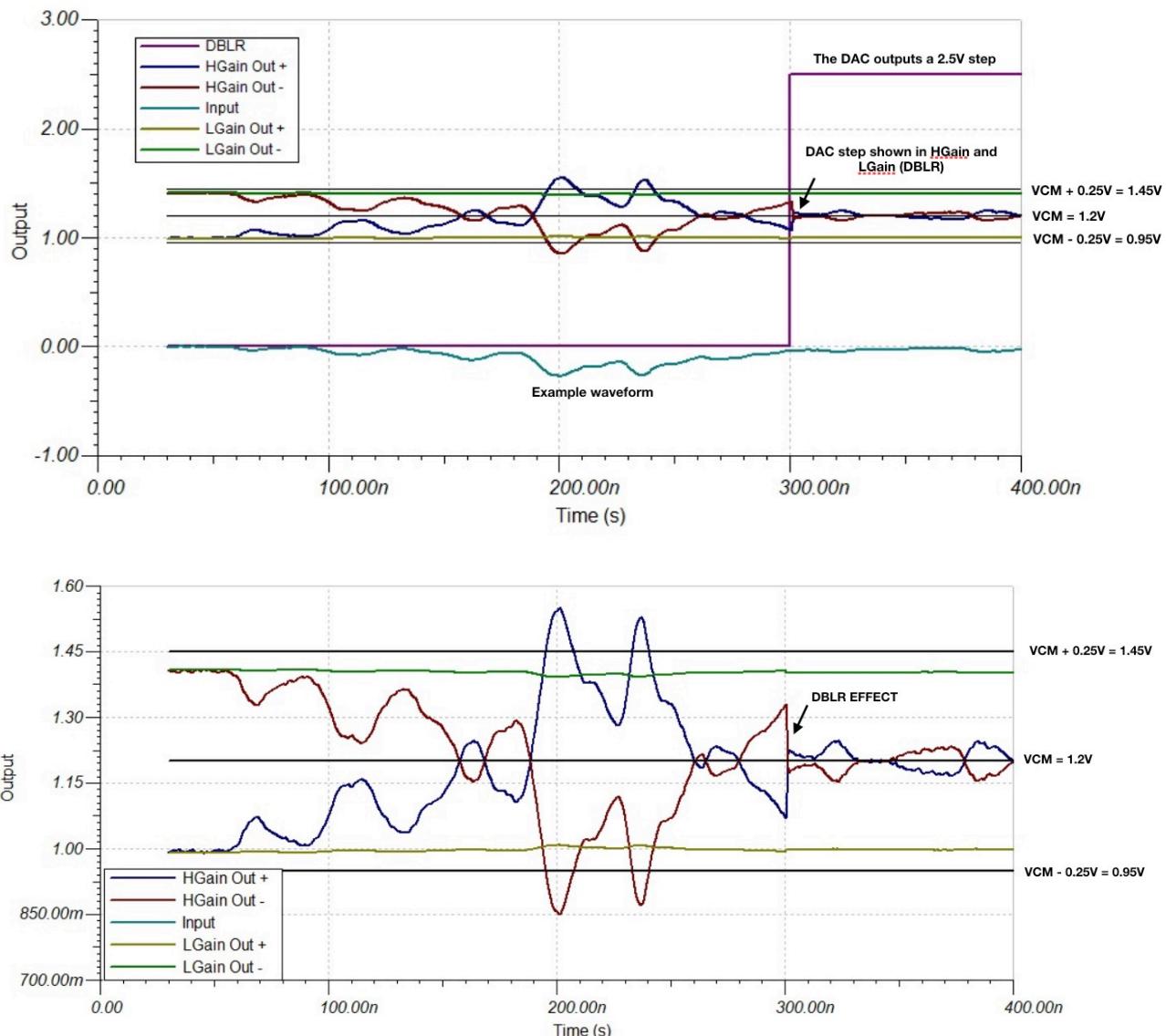
The LGain differential channel uses a very similar setup to the HGain differential amp, although for an attenuator before the amp. Below, I show the circuit, and then in the next section, you can see all the circuit stages together.



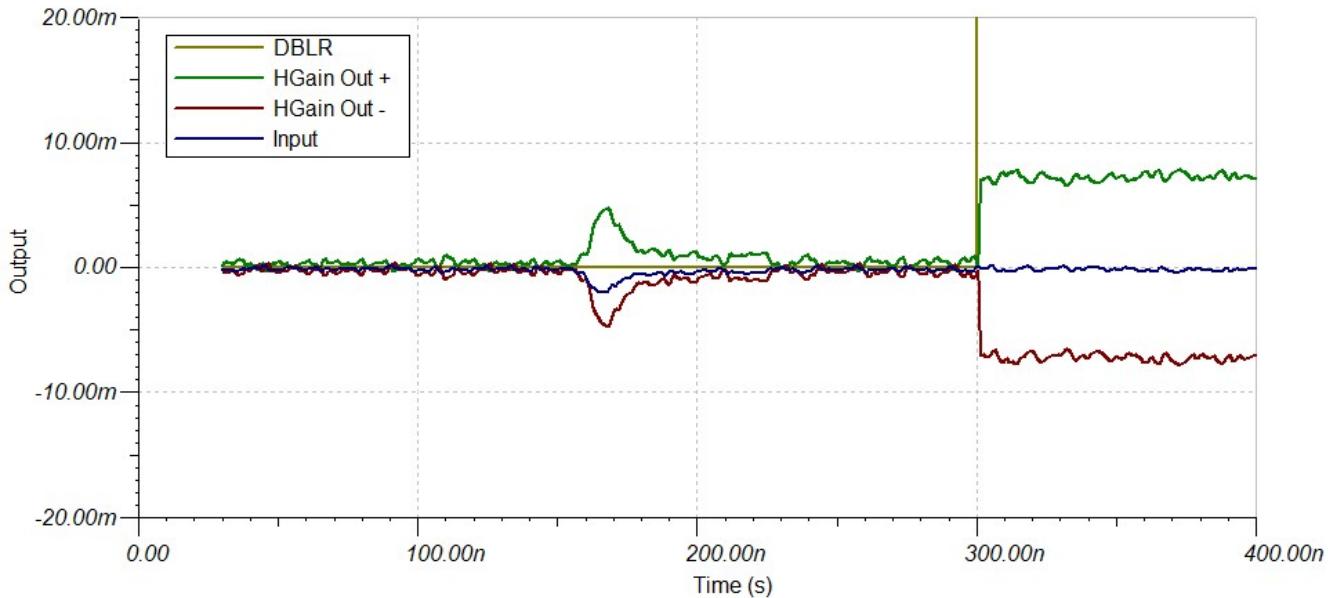
## Full simulation



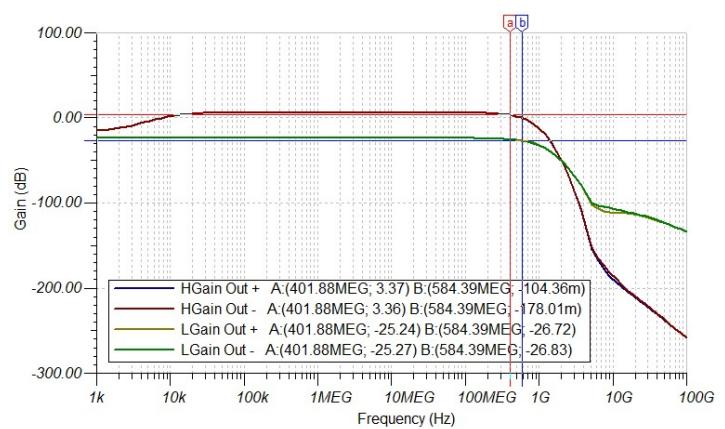
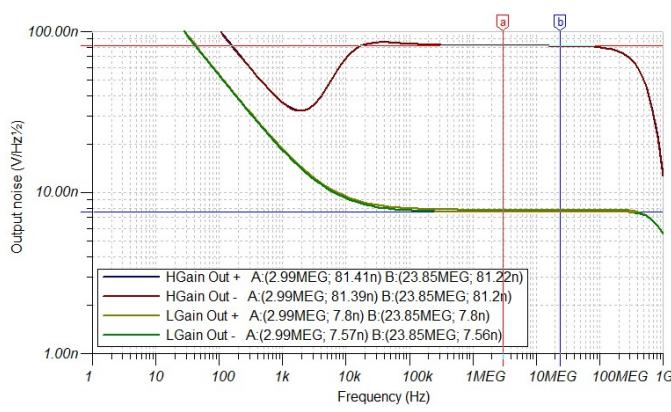
Transient simulation using an example input waveform (from KamLAND) with a range from 0 to -250mV is shown below in light blue. The common mode voltage from the RF-ADC (1.2V) along with the +/-0.25V allowed range is shown as black lines. The DBLR input (RF-DAC) is shown in purple as a step pulse from 0 to 2.5V at 300ns. The step pulse is passed through the voltage divider on the inverting op amp stage, reducing it to the maximum anticipated overshoot level (~50mV). The HGain channel outputs are shown in dark blue and red, and the LGain channel outputs (barely visible, due to the large signal attenuation) are shown in green and yellow.



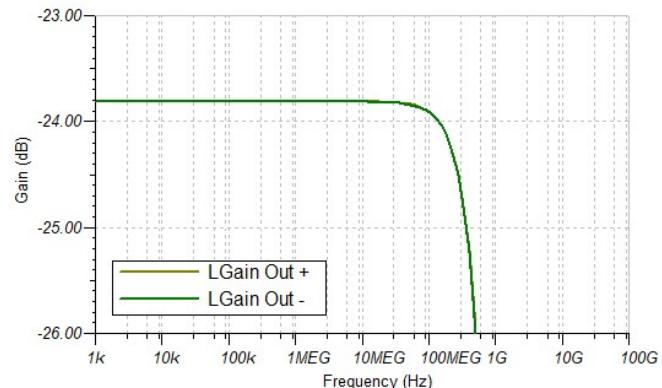
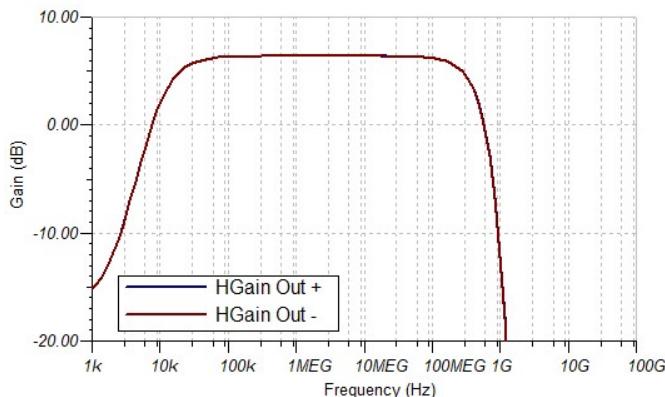
Below is shows the performance using a single photoelectron pulse on the HGain channel. The SPE has a peak amplitude of -3mV (dark blue). The outputs (red and green) from the HGain differential are AC coupled in this example, to show them on the same scale. Yellow, is a 100mV input pulse step function from the DBLR. It manifests itself as a 7.5mV step in the HGain output.



The following two figures show the gain and noise density for the differential outputs on HGAIN and LGAIN.



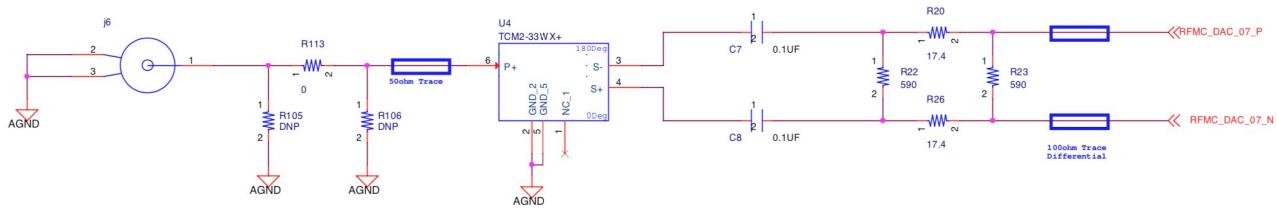
The following figures show the linearity of the HGAIN (left) and LGAIN (right) channels. The HGain curve shows the low frequency attenuation from the two capacitors on the negative input to the two amplification circuits.



# DAC requirements

The RF-DAC will be used to provide the digital baseline recovery. The RF-DAC appears to operate between 0 and 2.5V, with 14-bits of resolution. While the RF-DAC can operate at 6GSPS, we actually only need it for adding ~MHz frequency corrections (see overshoot waveform in the second figure of this document). The differential output from the DAC is first passed through a differential to single-ended op amp attenuator (unless there are better ways to perform the differential to single-ended conversion). The Xilinx method is to use a transformer, specifically, for their DAC conversion they use the TCM2-33WX+ transformer, which appears as though the frequency response is from 10MHz to 3GHz, making it unsuitable for the MHz signals that are of interest. The Xilinx converter schematic is shown below.

## 0-1GHz Channels Minicircuit Balun [LF]



We expect the overshoot to introduce order 10mV of distortion to the baseline. Therefore, the DAC output is attenuated from 0-2.5V to 0-50mV, through a voltage divider.

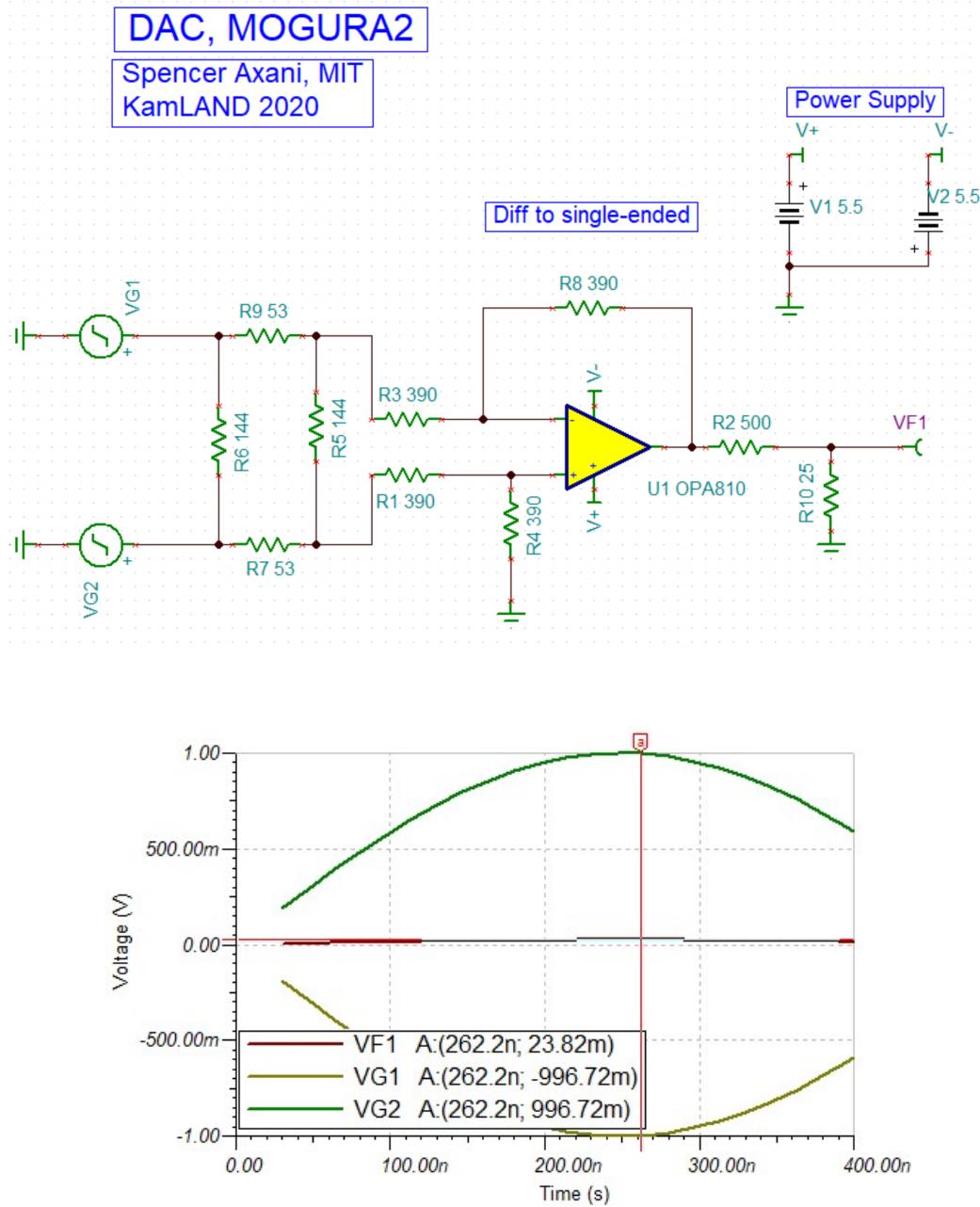
An untested requirement is that the RF-DAC correction is applied very shortly after the waveform digitization. There will be approximately 10ns of added delay simply from the analog electronics as well. The delay from digitization to correction application (either made through the FPGA or CPU) is unknown but will be tested shortly once the labs are open.

### TINA TI Simulation:

The simulation below shows the input of a 1MHz sine wave, and the output at VF1. The corresponding voltage drop is  $\sim 50x$ . It is desirable to have an op amp with a low total response time, as well as 10-100MHz gain band-width product. The Pi-attenuator at the input from VG1 and VG2 attenuates the signal prior to the op amp, and the voltage divider at the output of the op amp further attenuates the signal. The total attenuation for this circuit should be capable of -34dB.

If you look back at the section **HGain Full simulation**, the output of the circuit below connects to the non-inverting terminal of the first stage amplifier (labelled there as DBLR, in a

red box). That is the correction from the DAC is inserted into the first stage such that it modifies both the LGain and HGain channels.



We are also manufacturing a RF-DAC expansion board for the ZCU111, this, along with the RF-ADC counterpart are subsequently described.

## Reference design, RF-ADC expansion board

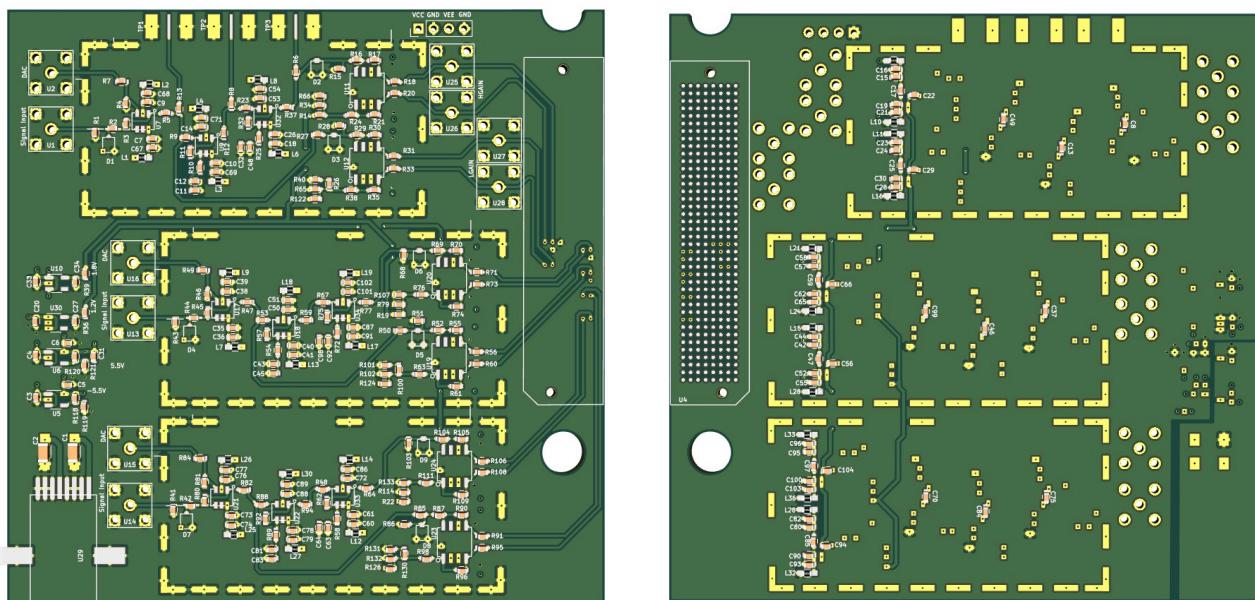
The following shows the current 3-channel FEA ZCU111 expansion board (4-layer, 10cm x 10cm). For information relating to each component (placement recommendations, purpose...), please zoom in and look for blue lettering near the component of interest. The circuit, designed in KiCAD, can be found in the GitHub repository.

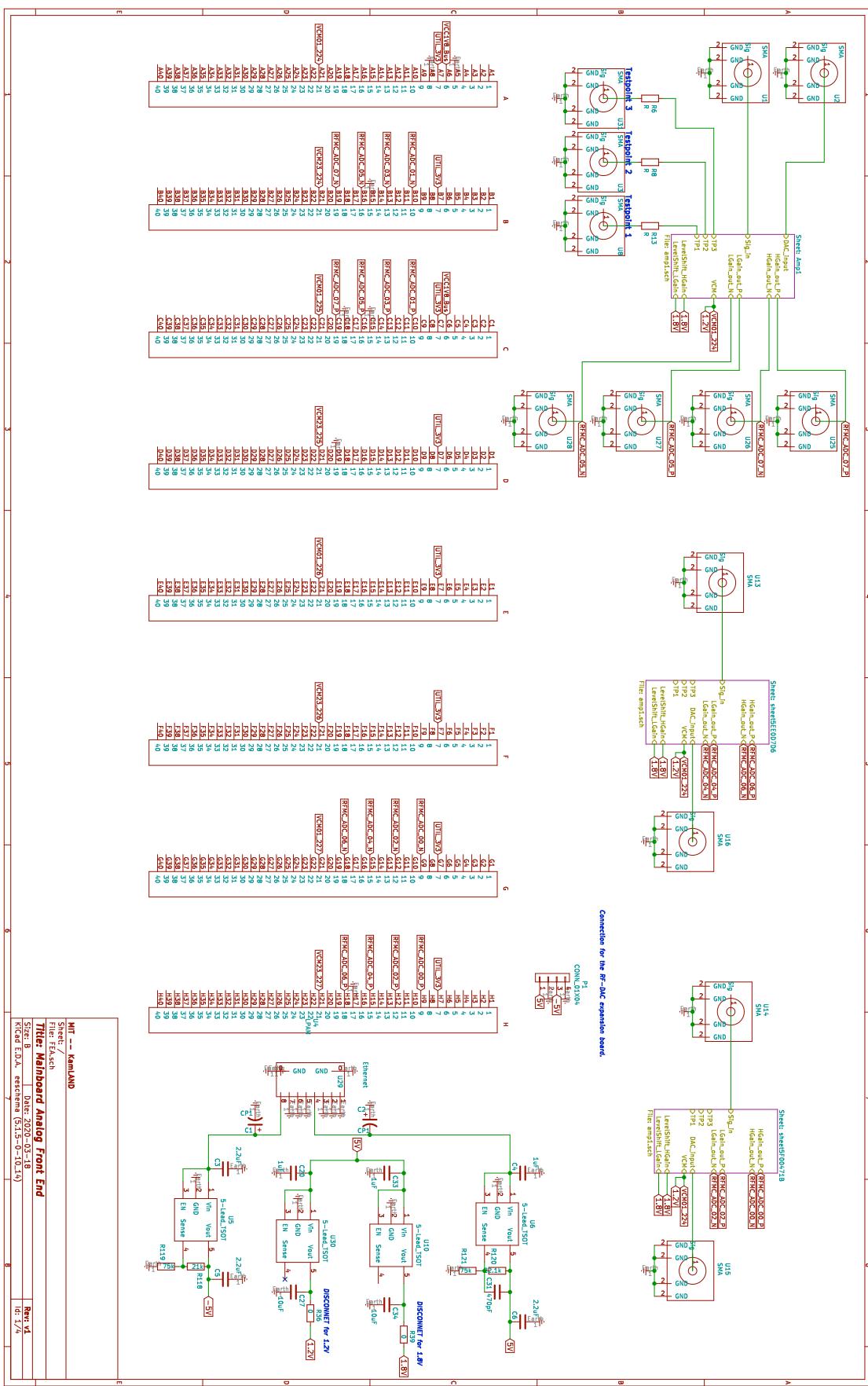
The ZCU111 board does output a 1.8V utility line, which we will use for level shifting the differential signal. We also use the 1.2V common mode connection from the ZC111.

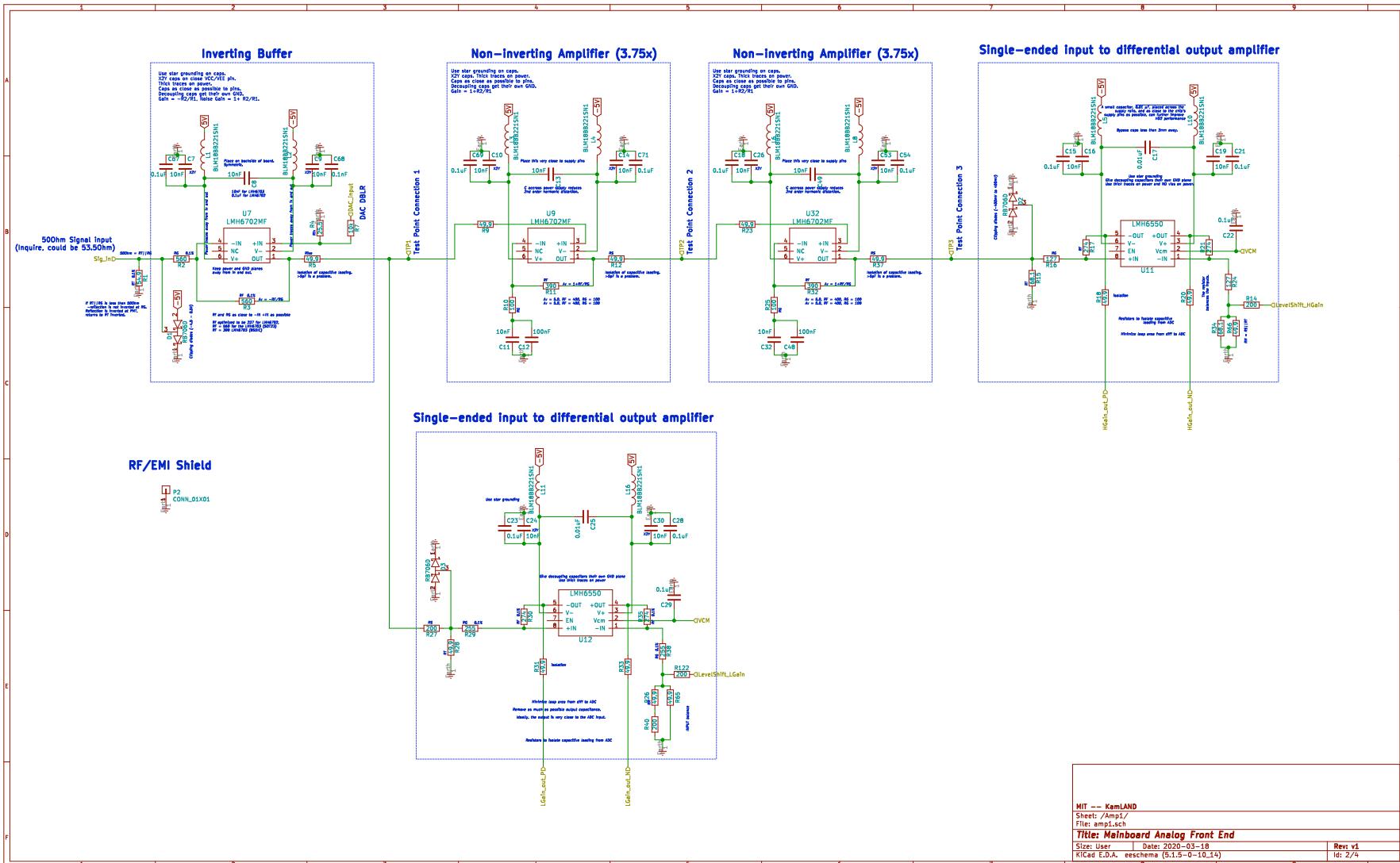
Since these boards are to be tested with the ZCU111, there is a built-in voltage regulator for the 1.8V and 1.2V lines. When plugged into the ZCU111, these two should be disconnected.

The boards are powered externally with a +/-10V power supply. The voltages are then lowered to +/-5.5V via two voltage regulators which supply power to the op amps. The power connector is actually an ethernet connection, which might appear strange, but should work sufficiently well, since the power draw from these boards are probably ~1W. I chose an RJ45 connection since the cables are abundant and if we loose the cable, building another one while in the lab should be simple enough — simply splice an RJ45 cable.

The first channel has test outputs at each FEA stage. The other two channels do not.







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File: ampi.sch

Title: Mainboard Analog Front End

Size: User Date: 2020-03-18

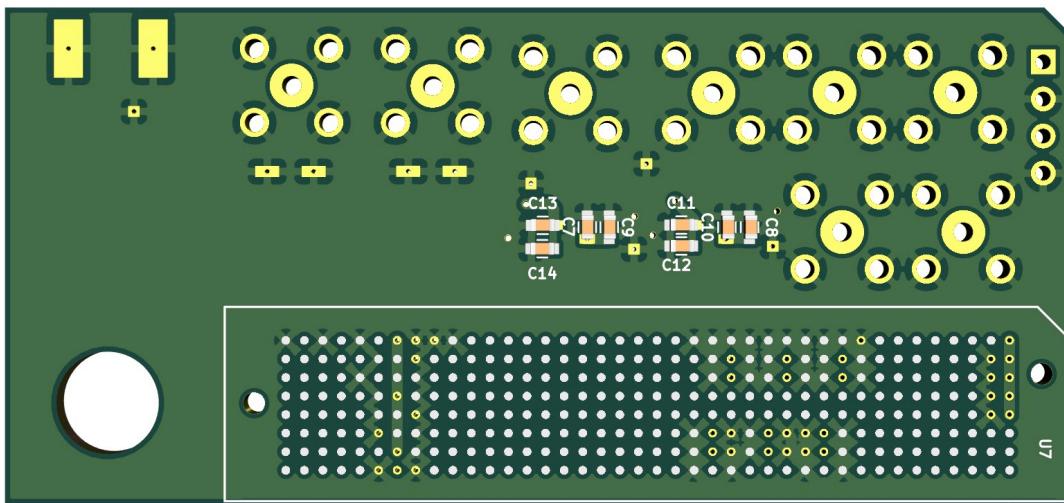
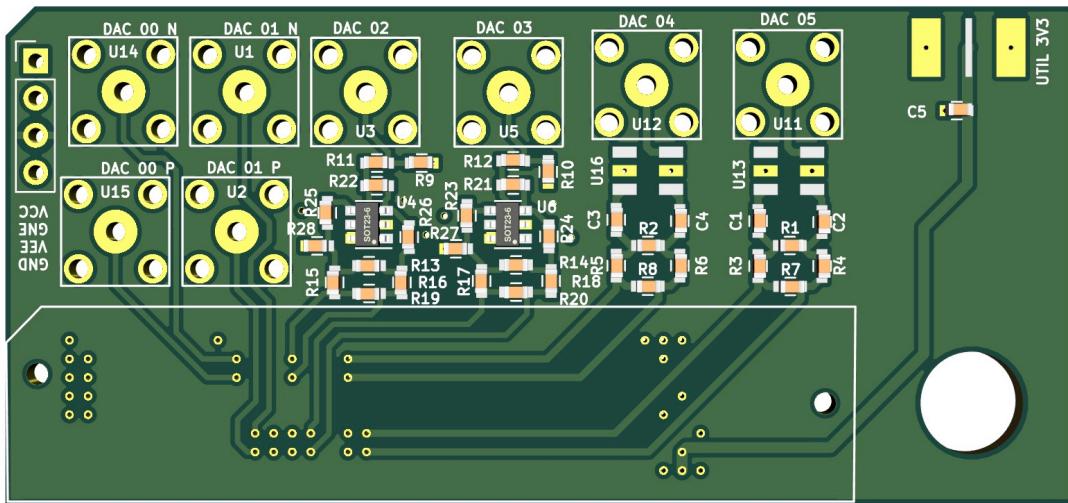
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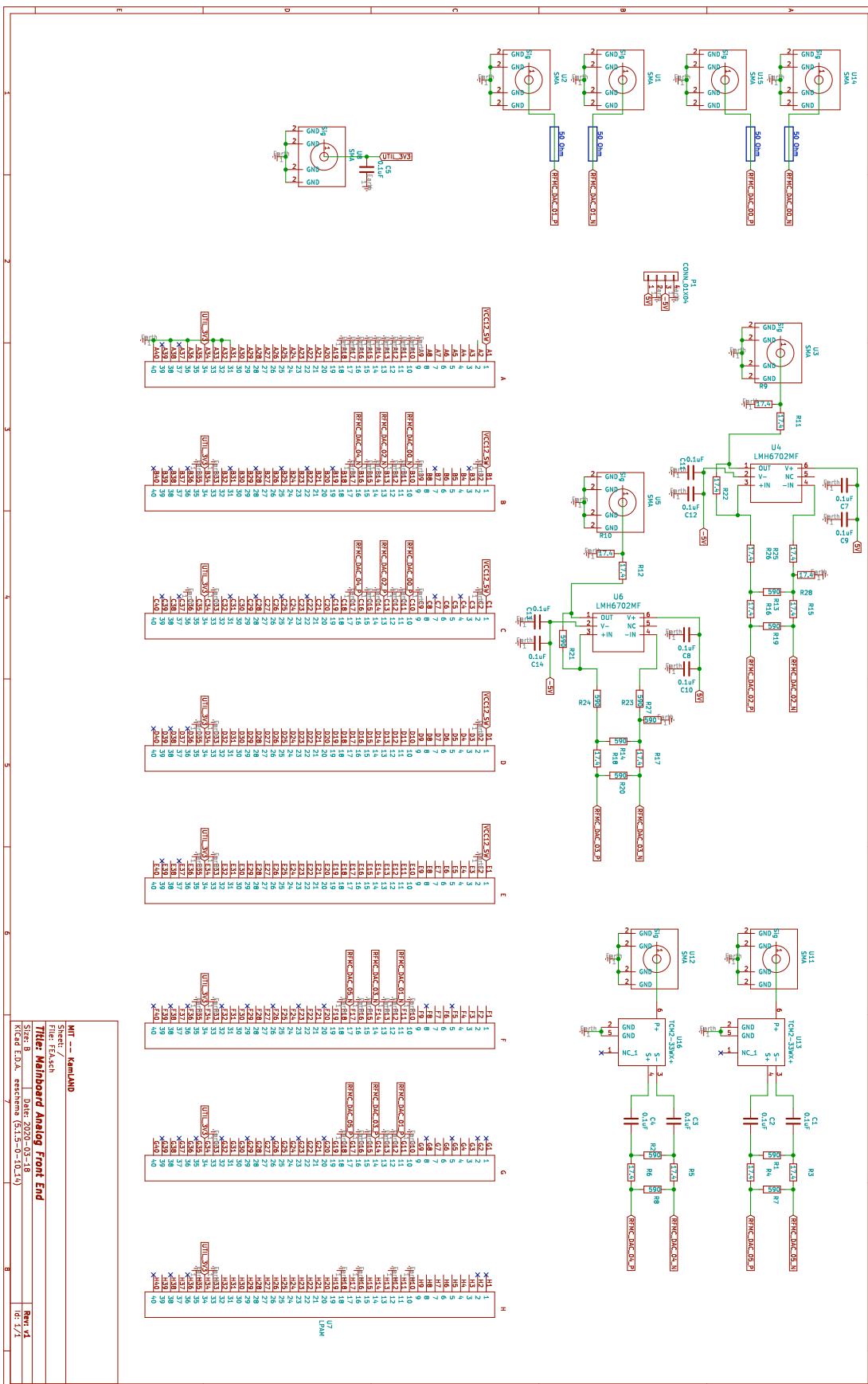
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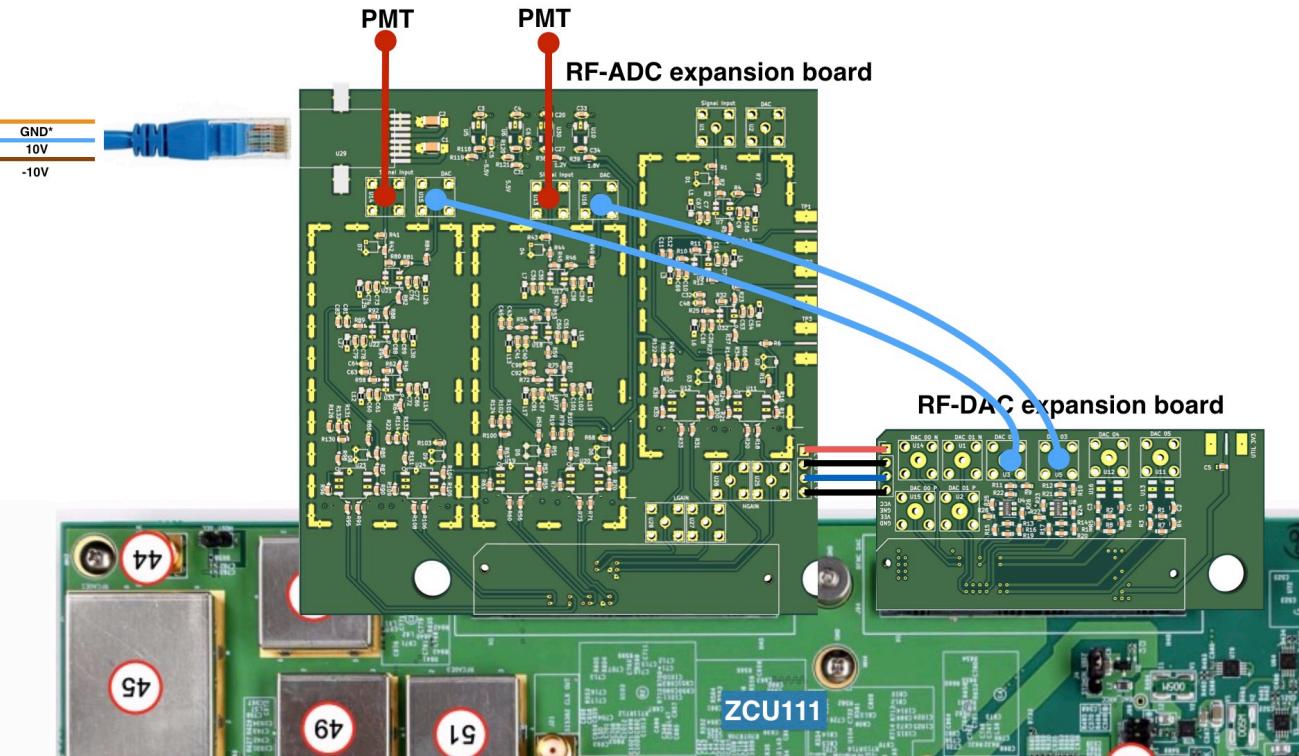
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## Reference design, RF-DAC expansion board

The following shows the current 2-channel FEA ZCU111 RF-DAC expansion board (4-layer, 10cm x 3.4cm). DAC 00 and 01 connects to the raw RF-DAC output from the ZCU111. DAC 02 and 03 combine the positive (P) and negative (N) RF-DAC output using the op amps U4 and U6. Finally, DAC 04 and 05 use the transformer recommended by Xilinx to combine the P and N RF-DAC outputs. The transformer, TCM2-33WX+, operates between 10-3000MHz, therefore it isn't suitable for the DBLR, which requires much lower frequencies (down to ~100kHz). This board requires +/-5V to power the op amps. This supply comes from a wired connection to the RF-ADC board.







## References:

Xilinx: [https://www.xilinx.com/support/documentation/ip\\_documentation/usp\\_rf\\_data\\_converter/v2\\_0/pg269-rf-data-converter.pdf](https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_0/pg269-rf-data-converter.pdf)

ZCU111 schematic can be found in the datasheets folder.

XM500 (another expansion board for the ZCU111) can be found in the datasheets folder.