KamLAND analog expansion board v3

MoGURA2 design document

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The KamLAND frontend analog electronics (FEA) takes the AC coupled signal from a single photomultiplier tube (PMT), amplifies and condition the signal such that it can be digitized by a **Zynq UltraScale+ RFSoC RF-ADC**. The following describes a reference design that is capable of providing the correct amplification for a Low Gain (**LGain**) and High Gain (**HGain**) channel, over the desired bandwidth (100MHz, 250MHz, respectively). This design introduces an example implementation of the digital baseline recovery (**DBRL**) — a correction applied to the waveform via an RF-DAC to compensate for droop/overshoot introduced by the AC coupling.

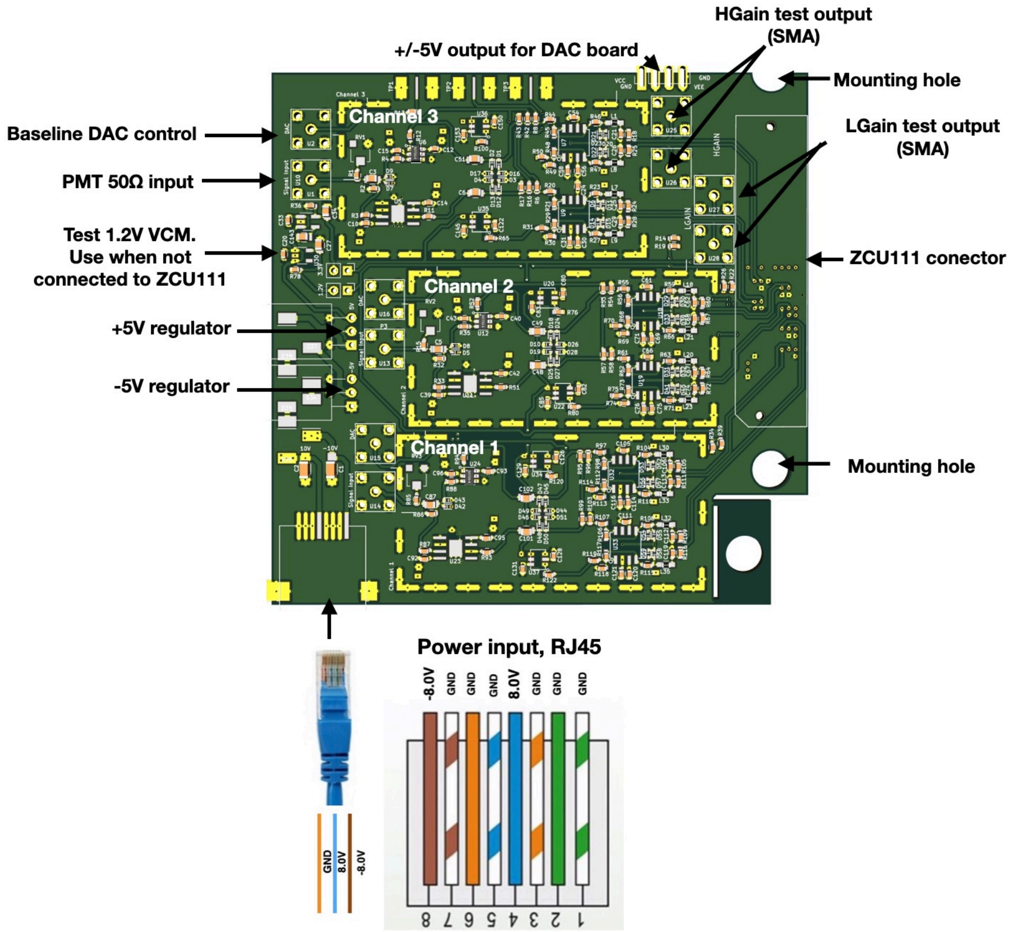
This document is to document the design of the expansion board used to connect to the RF-ADC of the ZCU111, shown on the next page.

We'll start with a requirements section, then describe the full circuit, finally provide the simulation and description of each channel.

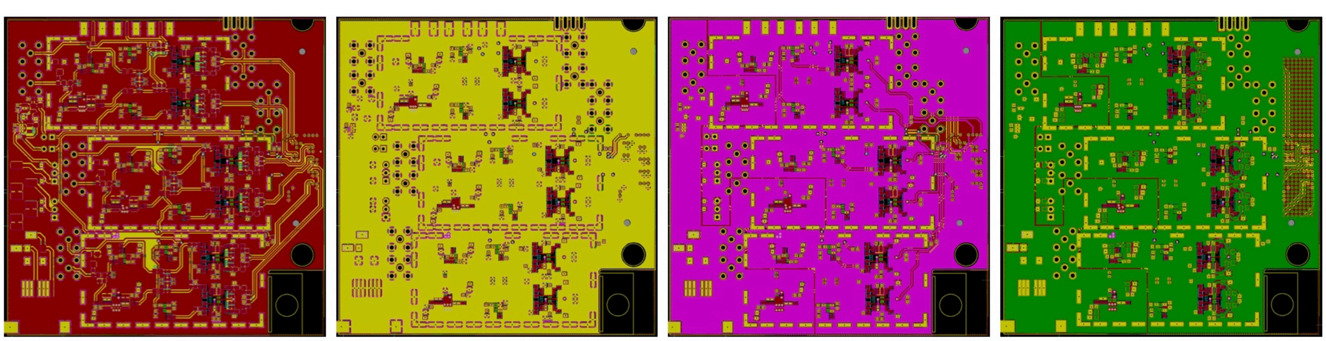
The simulation is performed using Texas Instruments **TINA TI**.
The circuit design and layout were performed using **KiCAD**.

A GitHub repository contains the design files, located here:
https://github.com/spenceraxani/KamLAND-FEA

Massachusetts Institute of Technology

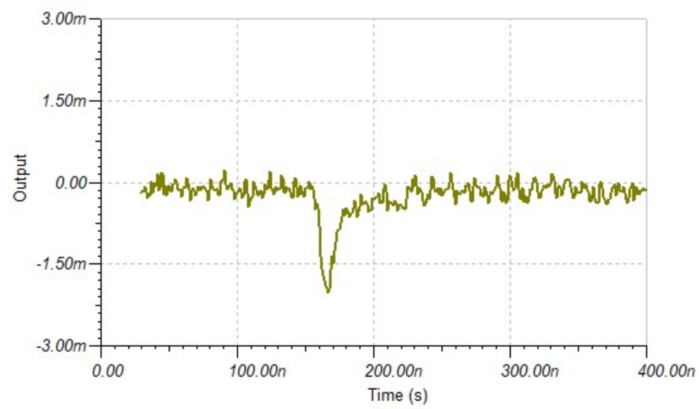


This board is powered with +/-8V.
Both FDA use the LMH6552. The LGain head amp is the THS3091.
The board was shipped with the 1.2V regulator disconnected. That means that when you plug it into the ZCU111, the VCM from each channel will supply the 1.2V.

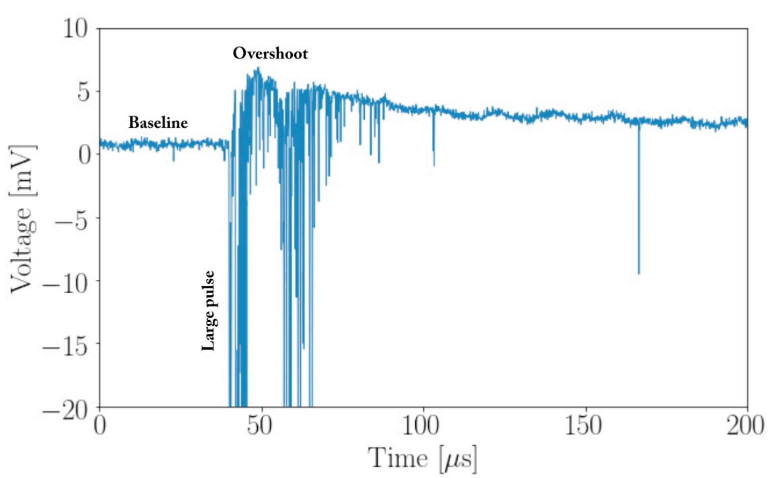


Requirements

The photomultipliers (PMT) are AC coupled to the front end electronics via a large capacitor. The uni-directional AC coupled signals (negative) are assumed to produce signals ranging from 1mV to -8V. **Large signals** (~Volt-scale) are rare — order Hz — and tend to be order microseconds in length. These originate from cosmic ray muons passing through the KamLAND detector. **Small signals**, originating from single photon detection, are expected to be between 0.1 and 6mV. These are much more frequent — order 20kHz per PMT. The primary frequency bandwidth of the small signals are ~100MHz. An example small signal (single photoelectron) is shown on the right.



The large signals produce two issues. First, since they contain a large amount of charge, the droop/overshoot introduced by the AC coupling can be substantial and cause issues with the data acquisition system. The overshoot time constant is several 100 microseconds (adjustable design), and we **must** be able to extract small pulses that "ride" on the overshoot. We aim to accomplish this with a *Digital Baseline Recovery System*, which compensates for the overshoot using a digital to analog converter (RF-DAC). An example of overshoot from the

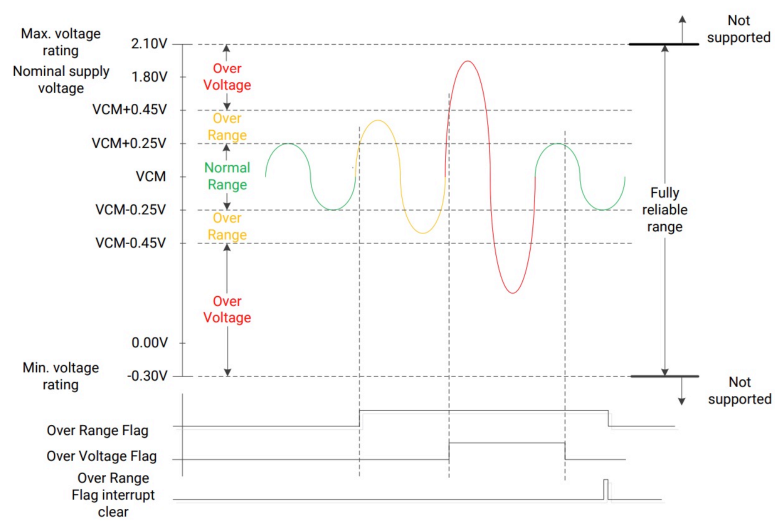


KamLAND detector is shown below.

The second issue produced by large signals is due to saturation of the electronics. Once saturated, we can no longer calculate the required baseline correction. Therefore, there must be ample room in the output voltage range to accommodate this. The last part of this document describes the current DAC electronics.

We aim to have two digitizers per PMT. The high-gain digitization (**HGain**) is part of the RFSOC and digitizes the small signals at 1GSPS (RF-ADC, 12-bit). This means that we desire the front-end analog (FEA) electronics to have a bandwidth below 500MHz (First Nyquist zone). Additional gain is applied to improve the signal to noise ratio. This channel should have a gain of approximately 10dB (voltage gain of x3). However, the gain from the PMTs has been observed to decrease overtime, therefore, the gain on the FEA should be able to accommodate a change of another ~12dB with minimal impact on the performance. The RF-ADC on the RFSOC operates at a common mode voltage of 1.2V, with a range of +/-0.25V relative to Vcm (right). It is a 12-bits, ADC, which corresponds to a discrete step size of 0.13mV, least significant bit. The RMS noise on the HGain channel should not be more than this. Also note, that this channel must be protected against the large signals.

Figure 10: **Threshold, Over Range, and Over Voltage Levels**



The low-gain (**LGain**) channel will likely be digitized by a 250MSPS, 14-bit, digitizer. My guess is that it will also be single ended input, differential output. We require that it is able to accept input pulses with a peak voltage -8V. The following describes the reference design which instead uses a separate channel from the RF-ADC, which means the signal has to be attenuated by -24dB. However, the design allows for the a rather large change in the gain by simply changing the values of the voltage divider prior to amplifier.

Requirements Summary:

HGain FEA:

- 250MHz bandwidth. Digitization is expected to be 2GSPS, downsampled to 1GSPS.
- Capable of Av = 10dB to 22dB. This gives this channel an effective range from ~0-60PE, assuming the average PE peak voltage is ~2.5mV, with a resolution of 0.13mV. Gain loss in the PMT aging can be compensated for with higher larger Av, or an optional additional amplifier.
- 0.13mV RMS noise (max), relative to the input.
- Single-ended input (50Ohm coax), differential output, operating between 1.2V (VCM) +/-0.25V.
- Digital baseline recovery via RF-DAC.
- Voltage protection for op amps and RF-ADC against large signals.

LGain FEA:

The LGAIN channel needs to be able to digitize input pulses from the PMT ranging from +100mV to -8V.

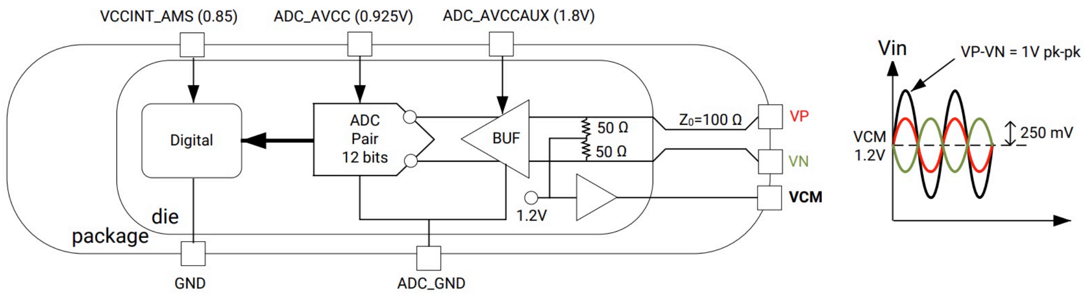
- 100MHz bandwidth. Digitization at 250MSPS**.
- Capable of -24dB to -12dB attenuation.
- Single-ended input, differential output. Operating between 1.2V +/-0.25V, this will depend on the VCM of the chosen ADC.
- Digital baseline recovery via RF-DAC.
- Voltage protection against large signals.

DAC (digital baseline correction):

- 100MHz-capable correction
- positive voltage correction, 0-50mV dynamic range after attenuator.
- >8-bit resolution

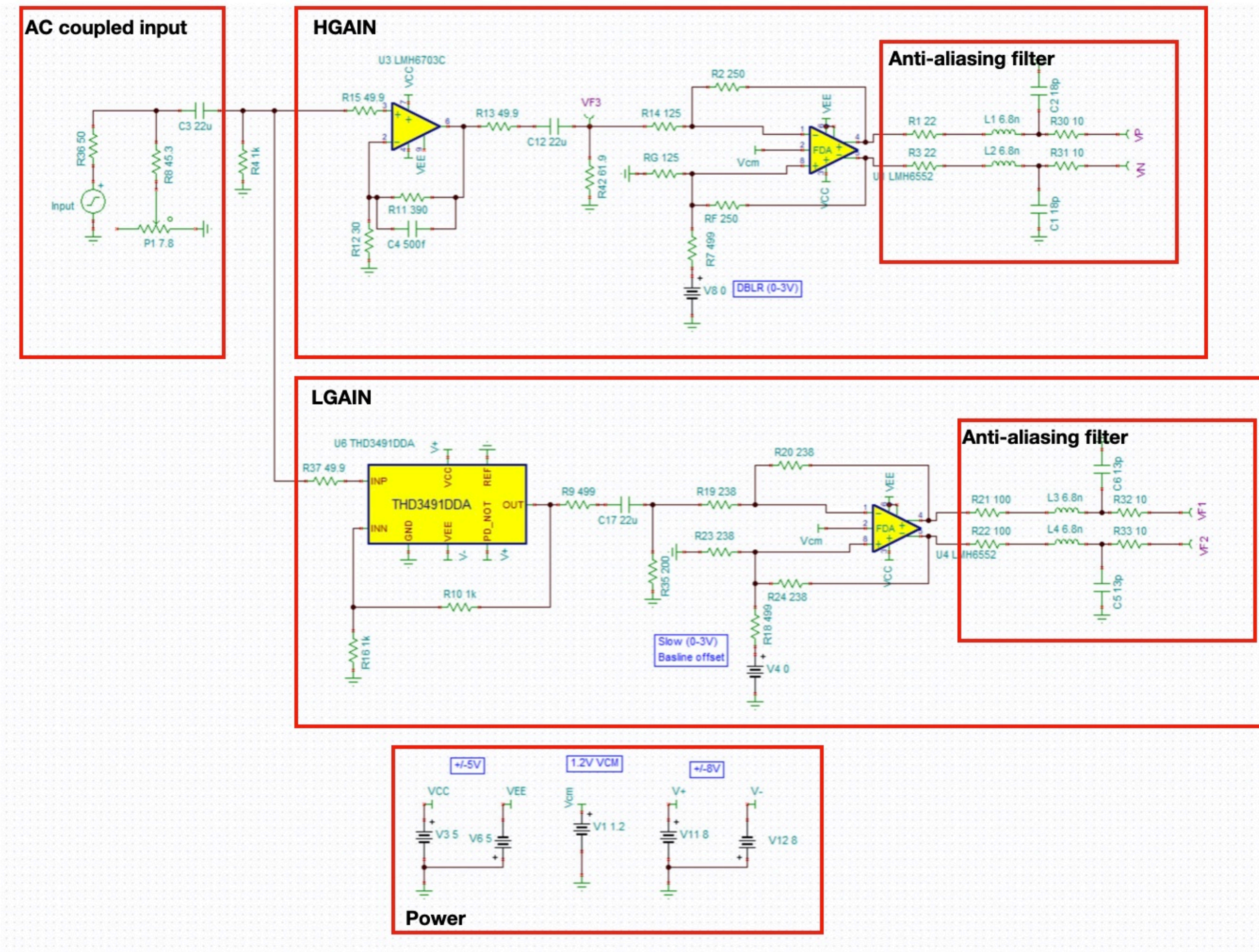
** Note: The current design uses the RF-ADC to measure this channel. Eventually, we would like a dedicated fast ADC at 250MSPS for this channel.

Figure 8: **RF-ADC Analog Input**



Some general notes:

- We need to minimize the signal reflection. Impedance matching is necessary, and we will likely actually back terminate the input, at the PMT output, and at the front end input.
- Minimize noise such that no appreciable noise above 500MHz exits the analog circuit. This is done through selection of op amps and an anti-aliasing filter. Below 500MHz, we can potentially provide some digital filtering.
- Since the signals are uni-directional (negative-going), we bias the waveform (or level shift) such that we can maximize the dynamic range of the ADC.



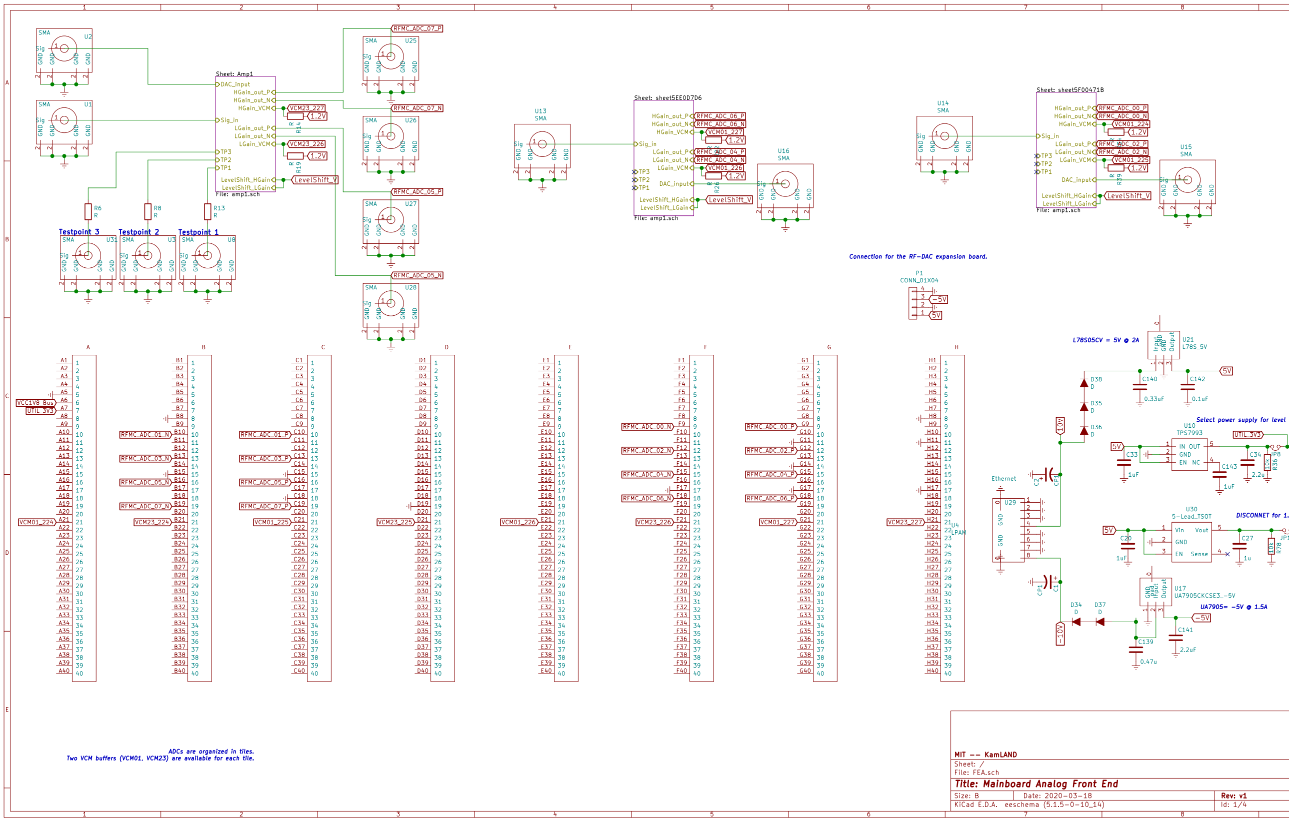
Full circuit description

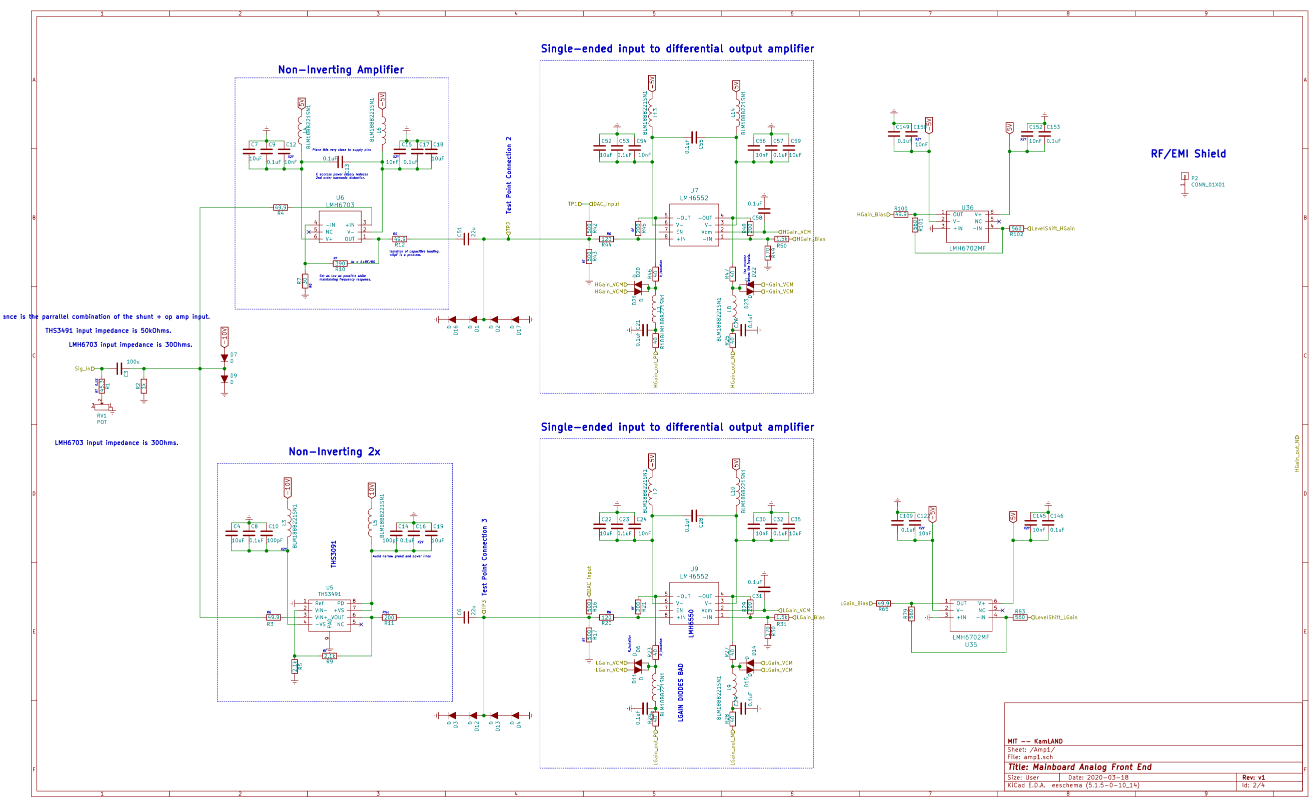
The input is AC coupled, and terminated to 50Ohms. Originally, I had a buffer amplifier prior to the split to HGAIN and LGAIN, however this was introducing additional noise. We use the non-inverting configuration on the input to each amplification channel in order to reduce noise as well as to provide a high-impedance input. The output if referenced to the common mode voltage of the ADC, in this case, 1.2V.

The HGain channel is first amplified, then AC coupled into a fully differential amplifier. We can provide a voltage on the non-inverting input to bias the waveform (maximizing the dynamic range), and to provide the low-latency digital baseline correction. The output of the differential amplifier is then passed through an anti-aliasing filter to cut-off higher frequencies, reducing the high frequency noise entering the 1st Nyquist zone of the digitizer

The LGain channel is first ~buffered (actually, x2), then attenuated through a voltage divider. It then get's differentiated and passed through an AA filter. We can provide a voltage on the non-inverting input to bias the waveform (maximizing the dynamic range). The output if referenced to the common mode voltage of the ADC, in this case, 1.2V.

A vectorized full circuit for the printed expansion board is shown below.


Connection for the RF-DAC expansion board.
Select power supply for level shifter
ADCs are organized in tiles.
Two VCM buffers (VCM01, VCM23) are available for each tile.
MIT -- KamLAND
Sheet: /
File: FEA.sch
Title: Mainboard Analog Front End
Size: B
Date: 2020-03-18
Rev: v1
Id: 1/4


Non-Inverting Amplifier
Single-ended input to differential output amplifier
RF/EMI Shield
THS3491 input impedance is 50kOhms.
LMH6703 input impedance is 300hms.
Non-Inverting 2x
Test Point Connection 2
Test Point Connection 3
MIT -- KamLAND
Sheet: /Amp1/
File: amp1.sch
Title: Mainboard Analog Front End
Size: User
Date: 2020-03-18
Rev: v1
Id: 2/4

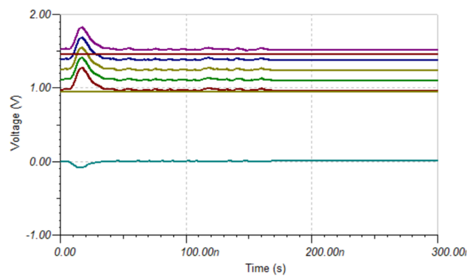
HGain description

A non-inverting amplifier is the 1st stage of the gain of the amplifier. We use the SOT-23-6 package LMH6703 current-feedback amplifier. Given the +/-5V supply, the input common mode voltage range is +/-3.8V. Given that the expected largest signal from the PMT is -8V (rare), and we impedance match the FEA input, we should not expect to exceed the input specifications to this amplifier. The LMH6703 datasheet is located here:
https://www.ti.com/lit/ds/symlink/lmh6703.pdf?ts=1618929300743&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FLMH6703

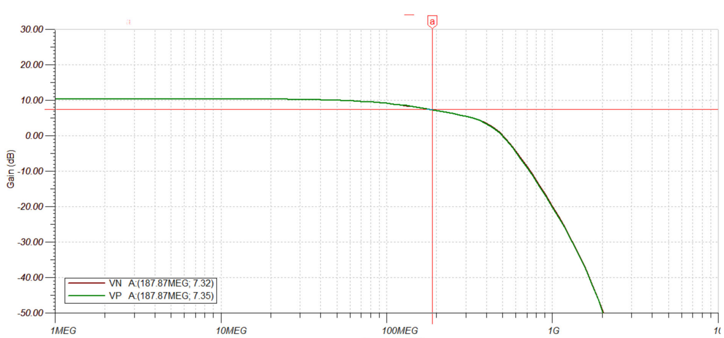
The gain on the 1st amplifier is set by the ratio between the feedback and gain resistors. The feedback resistor should be kept around 390Ω to optimize the frequency response. A feedback capacitor is added to slightly reduce the cutoff frequency. We add an input and output capacitor to isolate the amplifier. The output is AC coupled to the input of the differential amplifier to remove the offset DC voltage from the 1st stage amplifier. The next version of this expansion board will include an option footprint for an identical second stage amplifier, incase we need the additional 12dB gain.

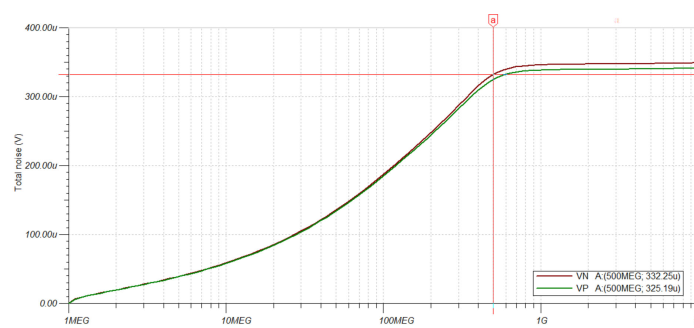
The FDA is selected to be the LMH6552 op amp. This differential amplifier is rather similar to the LMH6550, although it has slightly larger frequency response and lower input referred noise. The datasheet is located here:
https://www.ti.com/lit/ds/symlink/lmh6552.pdf?ts=1618933781951&ref_url=https%253A%252F%252Fwww.google.com%252F

We use the fact that the common mode voltage is non-zero on the fully differential amplifier (FDA) to provide a first order level shifting bias. This is the purpose of the resistor to ground (R42) on the inverting input of the FDA. Further biasing and baseline corrections can be applied through the voltage injected at V8, which, in our case will be the RF-DAC. The response of one of the FDA outputs, after applying five different voltages from 0-3V from the DAC is shown on the right. Some additional gain is also provided from the FDA.



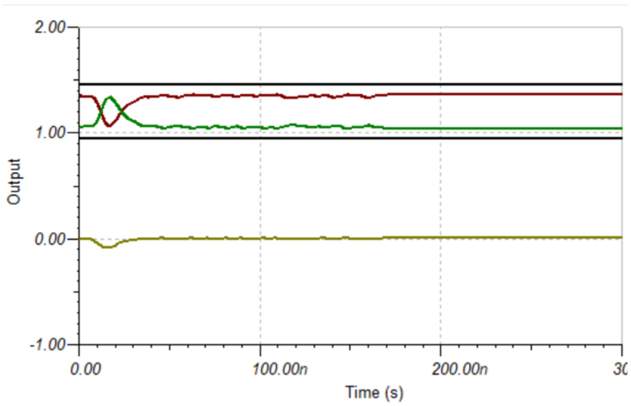
The frequency response of the HGain output is shown below on the left. We get a cutoff frequency at 187.87 MHz, with a flat-band gain of 10.34dB. The cutoff frequency response can be increased or decreased using the AA filter.

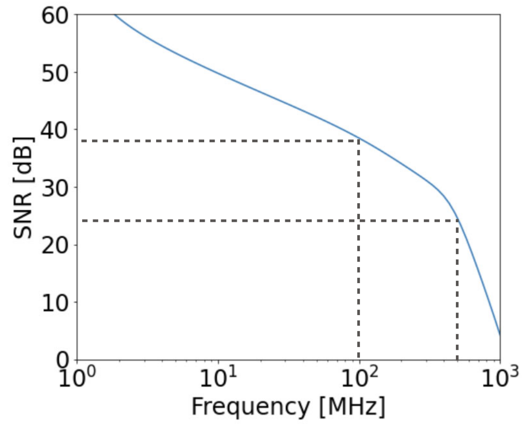




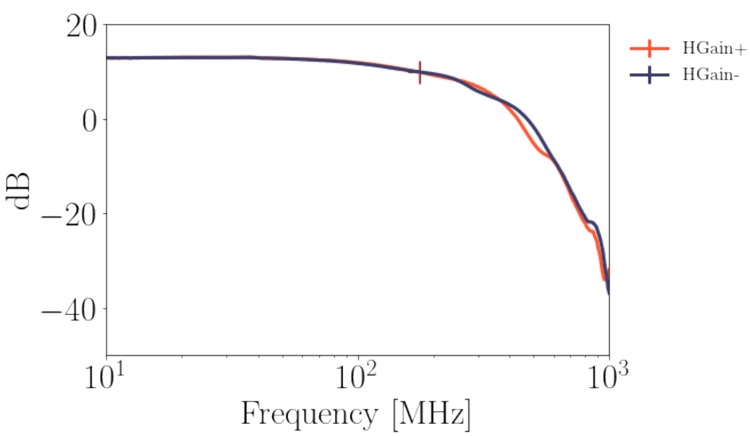
The total noise (RMS) at the output of HGAIN is shown on the upper right. At a bandwidth of 500MHz we find a total noise of .33mV, however given that the gain on this channel is x3.1, this is equivalent to ~0.1mV of noise relative to the input and comparable to the ADC quantization noise. Since our signal bandwidth is ~100MHz, we can further use digital filtering to reduce the noise to 0.19mV on the output, although it may not be needed.

The transient response of HGAIN, shown below for a 100mV input pulse is shown below on the left. The signal to noise, defined for a signal input of 5.5mV, is shown below on the right. For a 100MHz @ 5.5mV input signal, and the total RMS noise shown in the above image, the signal to noise given the analog simulation above, yields a SNR of ~39dB. At 500MHz, it drops down to ~25dB.





The TINA TI simulation results shown above agree quite well with the measured performance using a spectrum analyzer. I do see an additional +3dB at the flatland in the data compared to simulation, which has yet to be resolved.



The actual values of the AA filter on the output of the FDA are subject to change and optimization. For the values shown there, we achieve

LGain description

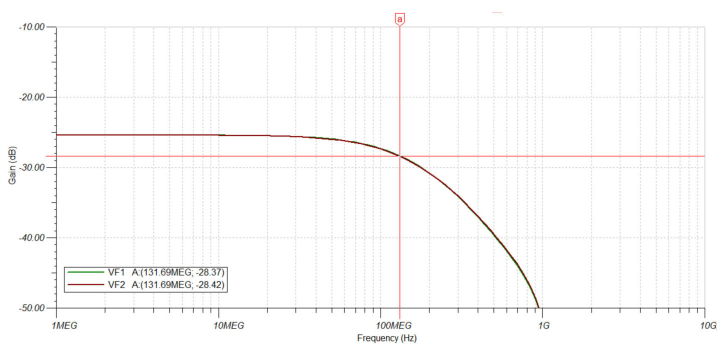
A non-inverting amplifier is the 1st stage of the LGain channel. This channel uses the THS3091 amplifier on the input. This amplifier has a larger input common mode voltage range to accept larger pulses. Given the +/-8V supply voltage, the input common mode is +/-6.5V. The datasheet can be found here.
https://www.ti.com/lit/ds/symlink/ths3091.pdf?ts=1618938652058&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTHS3091

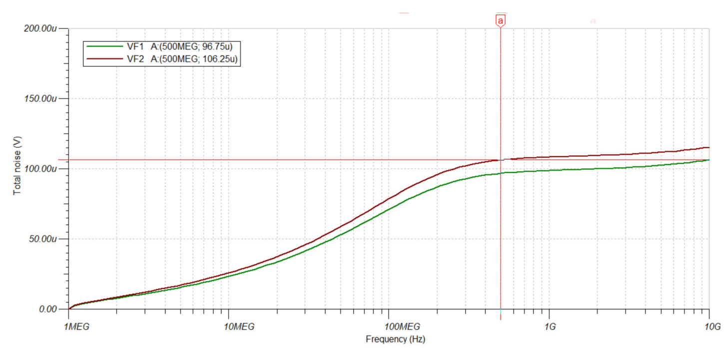
Similarly to the HGain channel, the FDA is selected to be the LMH6552 op amp. The datasheet is located here:
https://www.ti.com/lit/ds/symlink/lmh6552.pdf?ts=1618933781951&ref_url=https%253A%252F%252Fwww.google.com%252F

We use the fact that the common mode voltage is non-zero on the fully differential amplifier (FDA) to provide a first order level shifting bias. This is the purpose of the resistor to ground on the inverting input of the FDA. Further biasing and baseline corrections can be applied through the voltage injected at the non-inverting terminal, which, in our case will be the a separate DAC.

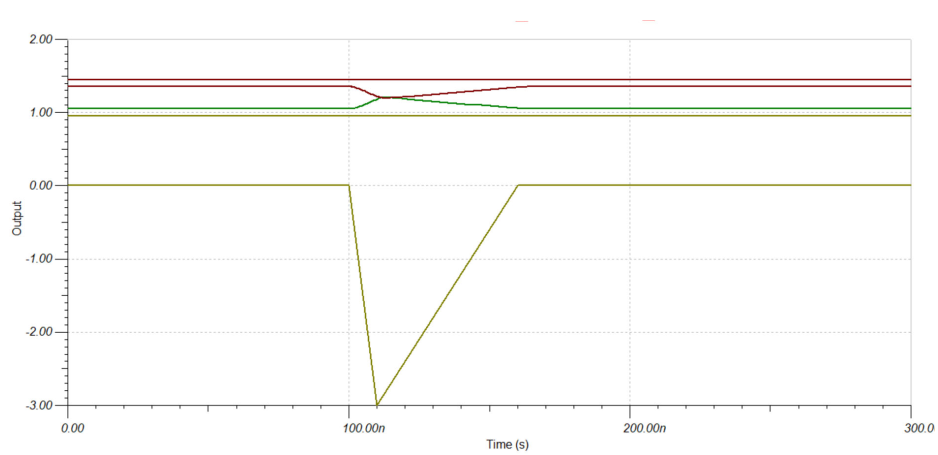
The frequency response of the LGain output is shown below on the left. We get a cutoff frequency at 131 MHz, with a flat-band gain of -25.37dB. The cutoff frequency response can be increased or decreased using the AA filter.

The total noise, RMS, is shown on the bottom right, although with this channel, it's not particularly important.



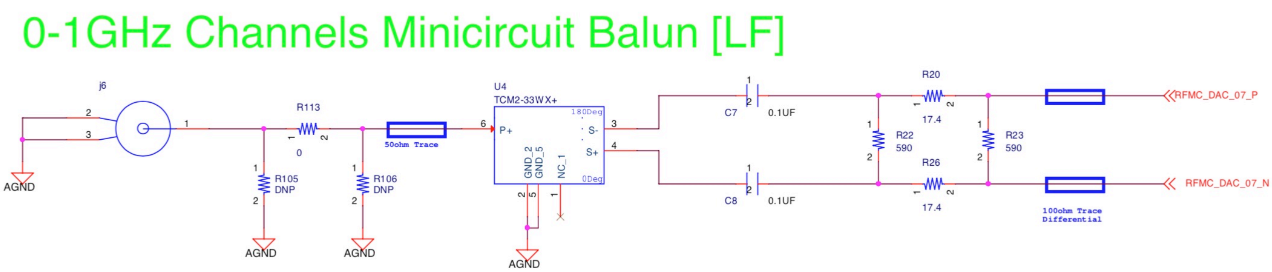


The transient response for a -3V signal is shown below.



DAC requirements

The RF-DAC will be used to provide the digital baseline recovery. The RF-DAC appears to operate between 0 and 2.5V, with 14-bits of resolution. While the RF-DAC can operate at 6GSPS, we actually only need it for adding ~MHz frequency corrections (see overshoot waveform in the second figure of this document). The differential output from the DAC is first passed through a differential to single-ended op amp attenuator (unless there are better ways to perform the differential to single-ended conversion). The Xilinx method is to use a transformer, specifically, for their DAC conversion they use the TCM2-33WX+ transformer, which appears as though the frequency response is from 10MHz to 3GHz, making it unsuitable for the MHz signals that are of interest. The Xilinx converter schematic is shown below.



References:
Xilinx: https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_0/pg269-rf-data-converter.pdf

ZCU111 schematic can be found in the datasheets folder.

XM500 (another expansion board for the ZCU111) can be found in the datasheets folder.