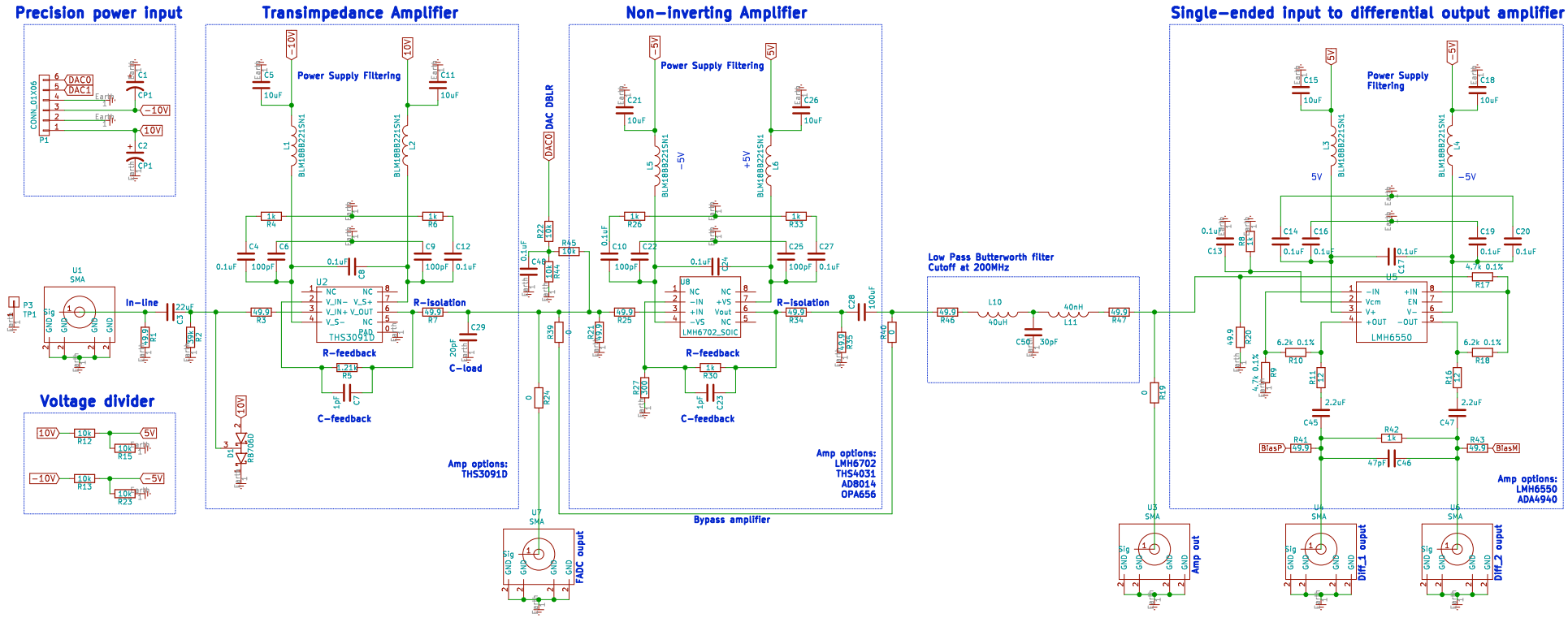

NOTES

In-line
50Ohm signal trace. Thick trace.
No vias on signal.
All signal on top layer.

C-load
RC filter. 50 and 20pF. Fc = 160MHz

R-isolation
R isolation very close to V_out.
Minimizes capacitive loading.
Use 0603, non-handsoldering pads.
Same resistance as track impedance

R-feedback
Close to input and ouput pins as possible.
Large values add JN noise.
Small values make instabilities.
Check values in datasheet.

Power Supply Filtering
Wide traces on power lines.
100pF decoupling cap as close as possible to VS- and VS+
100pF on IC side

C-feedback
Helps with stray capacitance.
*Likely remove for final design, or sub 1pF values.

MIT -- KamLAND	
Sheet: /	
File: FEA.sch	
Title: Mainboard Analog Front End	
Size: B	Date: 2020-03-18
KiCad E.D.A. eeschema (5.1.5-0-10_14)	Id: 1/1

Rev: v1

http://www.ti.com/lit/ml/slyp173/slyp173.pdf

Low pass filter: https://rf-tools.com/lc-filter/

EMF Sheild
SMA preferred over BNC
Keep components small, 0603 all smt
MULTIPLE Vias Everywhere
Short fat traces to reduce I
Round traces. No 90s.
GND and V pour removed near IC IO
Symetric power supply filtering