
Hacking a Telescope: Motor Control for PAT Development

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Group 66 Intern Presentation

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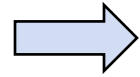
About Me

- **Hometown: Newton, MA**
- **Education: University of Vermont**
 - Electrical Engineering
 - Rising senior
- **Other**
 - Lacrosse
 - Skiing





Outline



- **Motivation**
- **Motor & Encoder**
- **Elmo**
- **FPGA**
- **Future Work**



Motivation

- **Sensors required to test PAT capabilities using stars are available in advance of certain actuators (e.g., gimbal)**
- **Need to test/calibrate sensors**
 - **Need control over COTS actuators to allow for sensor testing**
- **Goal: converge on the target quickly and smoothly**
- **Need high-rate position and time updates from gimbal axes and actuating mirrors (current rate: 1Hz, desired rate: 100Hz)**
- **Faster position/time updates = faster misalignment model updates = faster error correction**





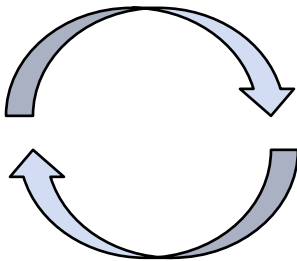
Motivation: Optical Path Misalignment Model

Gimbal Axis	Entrance Mirror
G1 (Elevation)	M5
G2 (Azimuth)	M7

Mirror	Description
M1:4	Telescope
M5	El Periscope
M6	Coudé Relay
M7	Az Periscope
M8	Out-of-plane Fold
M9	FSM
M10	LBM
M11	PBS

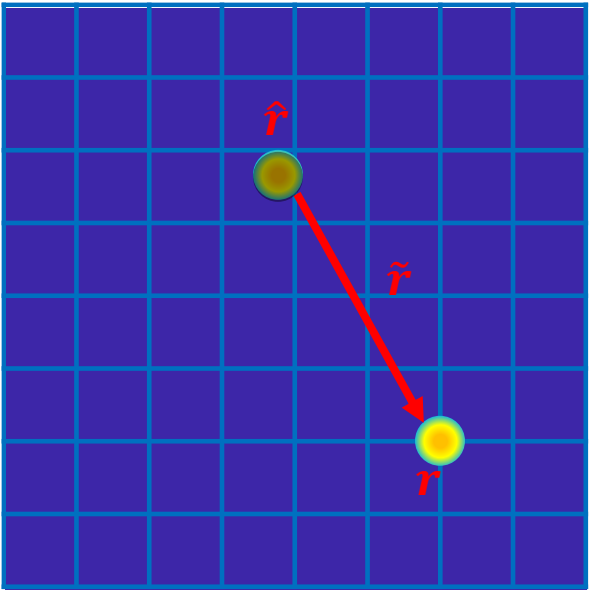
Mirror Actuation
Gimbal Actuation

Expected target spot location: \hat{r}



Misalignment Updates:

$$\hat{\epsilon}^+ = \hat{\epsilon}^- + \frac{\partial \tilde{r}}{\partial \epsilon} \tilde{r}$$



FPA Measurements

Optical model can be updated on measurements of FSM and gimbal positions



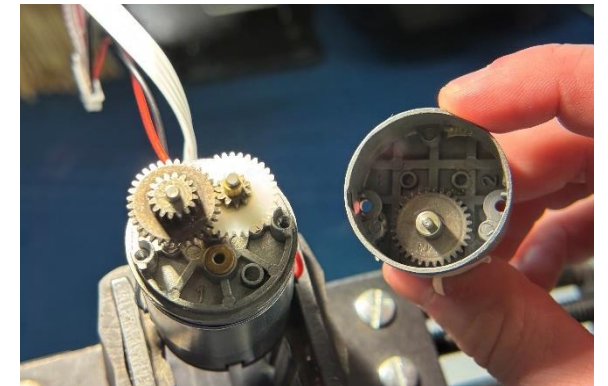
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Motor & Encoder

- **Celestron NexStar Telescope**
- **Azimuth and elevation controlled by brushed DC motors**
- **54:1 Gear ratio**
- **6-pin connector feeds into motor driver board**
 - **Motor +**
 - **Motor –**
 - **+5V**
 - **GND**
 - **B (quadrature signal)**
 - **A (quadrature signal)**

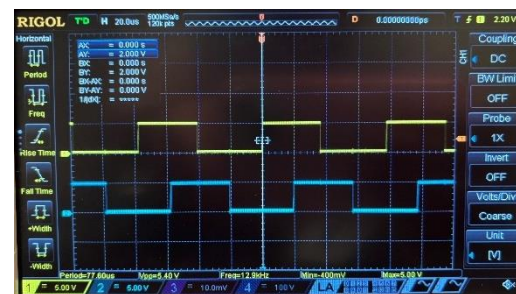
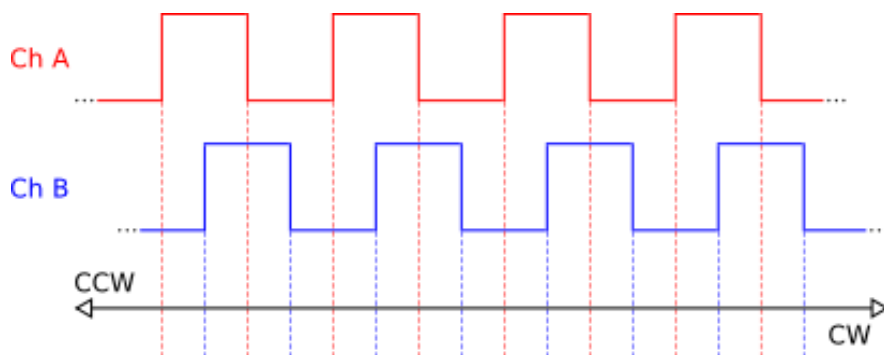
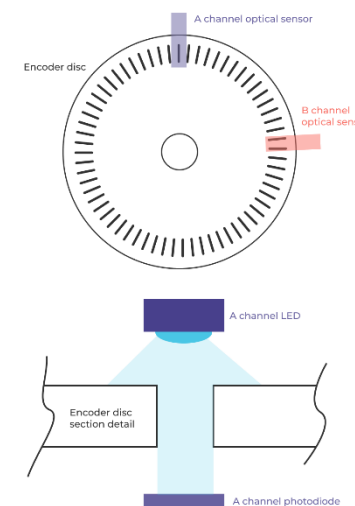




Motor & Encoder

- US Digital E4T optical encoder
- Outputs single-ended A & B quadrature signals
- $400 \text{ CPR}_{\text{internal}} \rightarrow 1,600 \text{ PPR}_{\text{internal}}$
- Use gear ratio to find $\text{PPR}_{\text{external}}$

$$\rightarrow \frac{1 \text{ External Revolution}}{54 \text{ Internal Revolutions}} = \frac{1,600 \text{ PPR}_{\text{internal}}}{1 \text{ Internal Revolution}}$$
$$\rightarrow 54 \times 1,600 = 86,400 \text{ PPR}_{\text{external}}$$



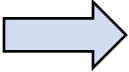
A (yellow) leads B (blue)



B (blue) leads A (yellow)



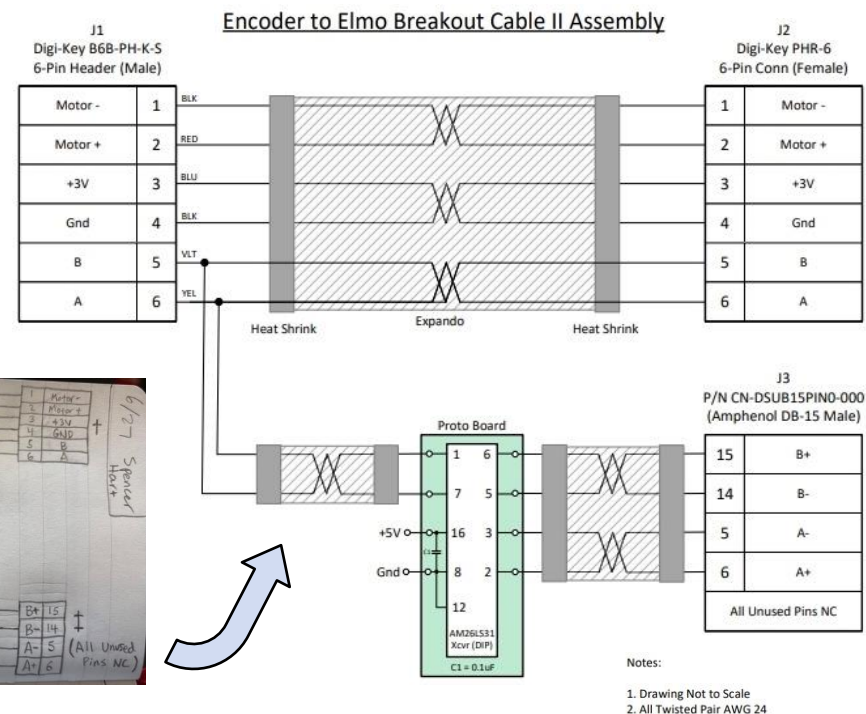
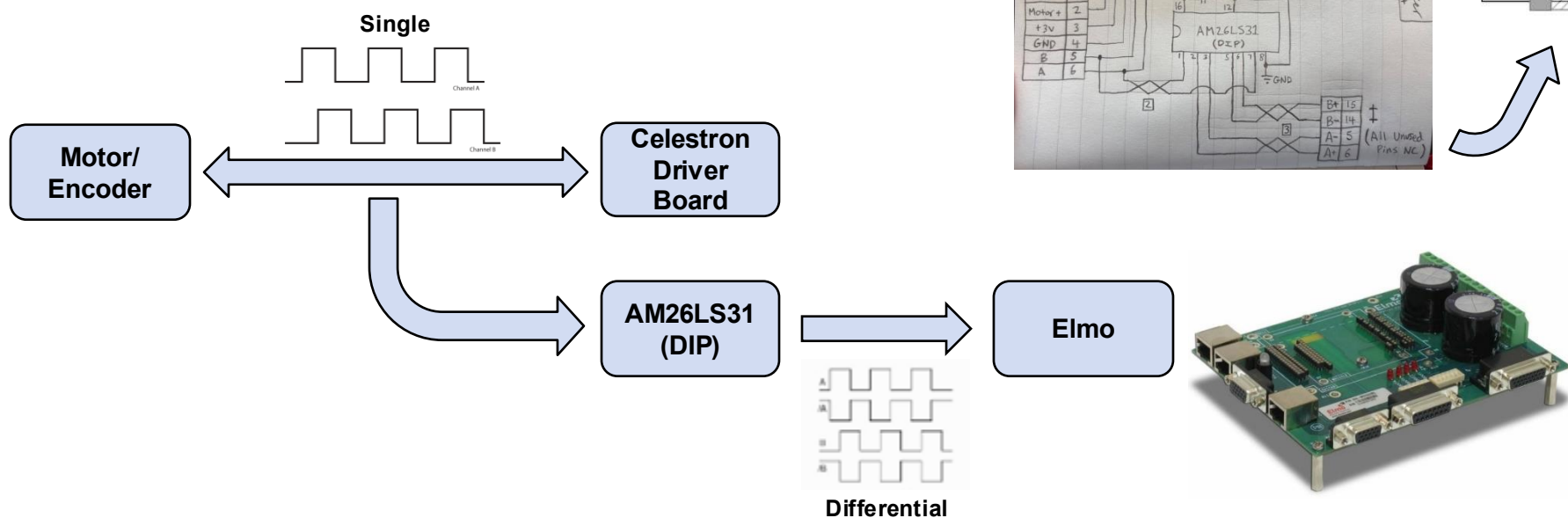
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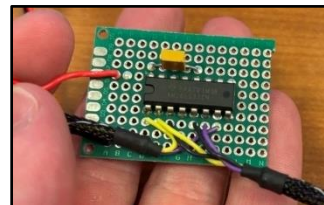
Elmo

- Elmo Motion Control Evaluation Board
- Uses RS232 or CAN to communicate
- Use case 1: “sniff” encoder for position value
- Expects differential quadrature signals
- Single-differential converter required



TITLE
Encoder to Elmo Breakout Cable II

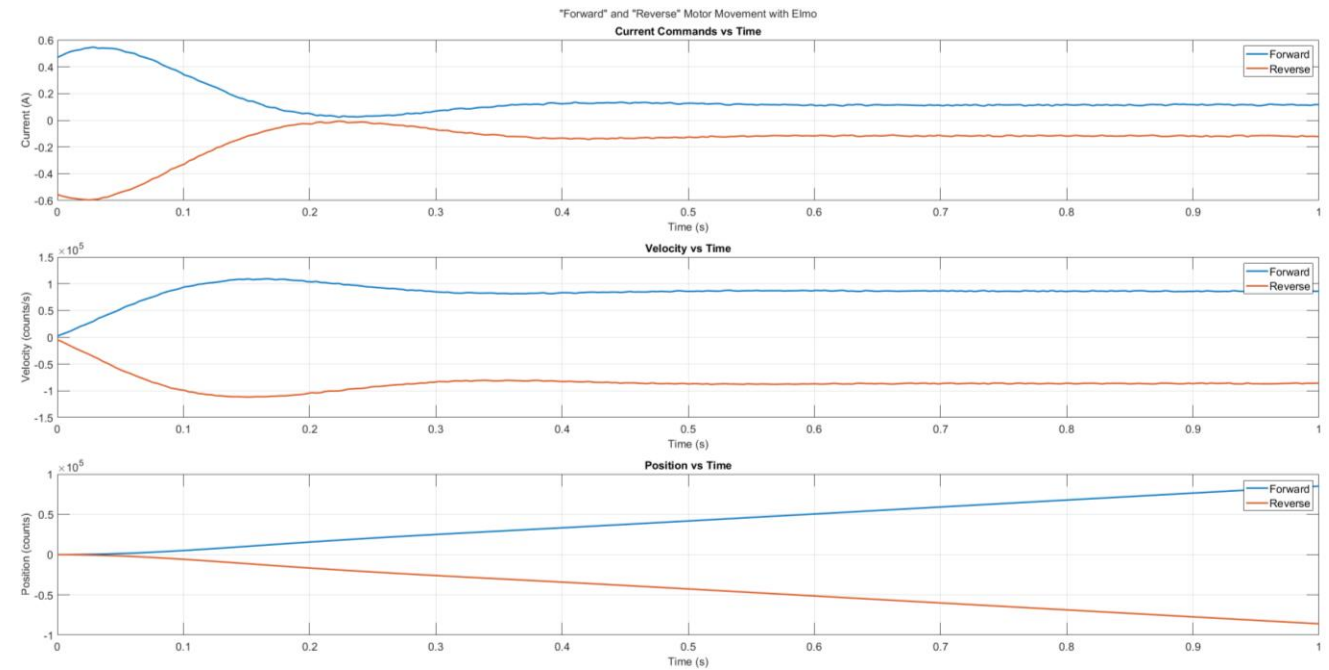
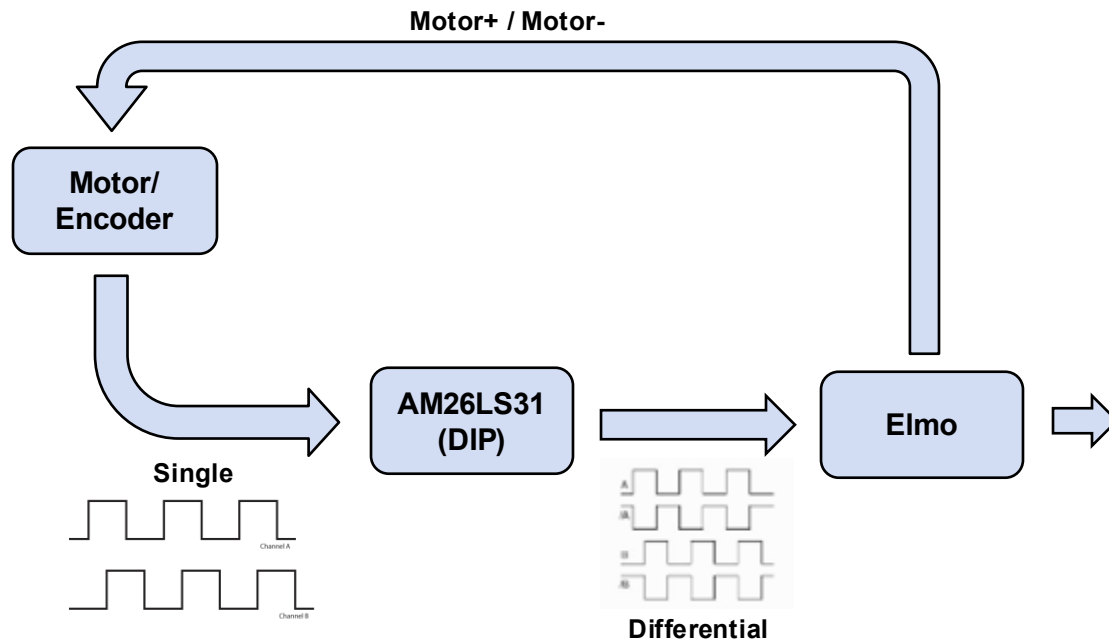
Designer: S. Hart
Revision: 2
Drawn: T. Miller
Date: 07-01-25
Project: Line
Sheet 1 of 1





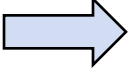
Elmo

- Use case 2: drive motor and “sniff”
- Eliminates use of Celestron driver board
- Currently: start, stop, forward, reverse capabilities with velocity control





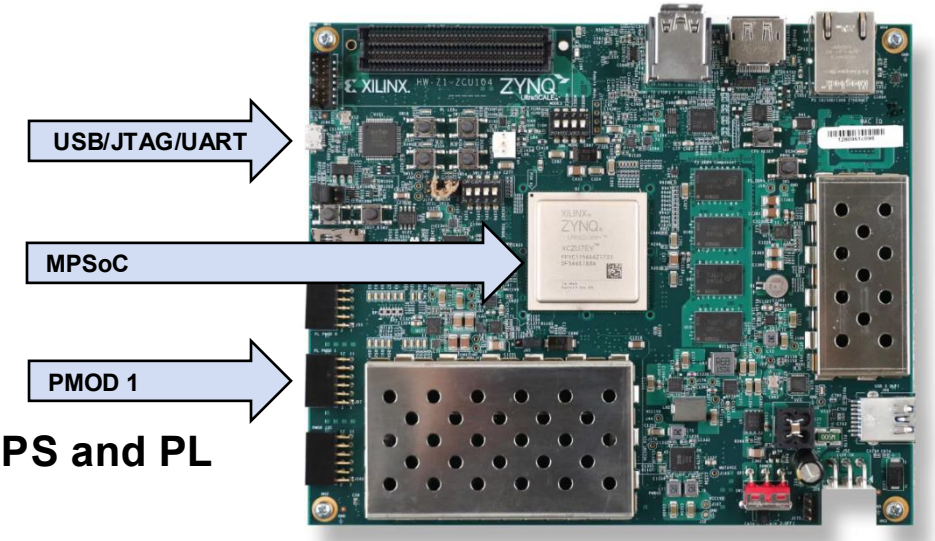
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-  • **FPGA**
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FPGA

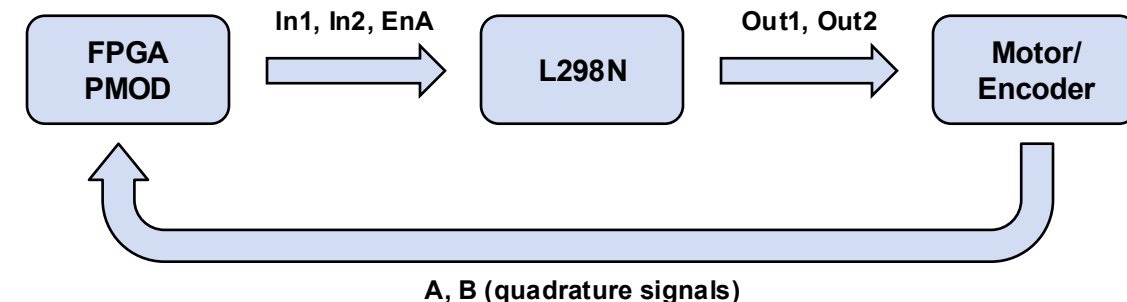
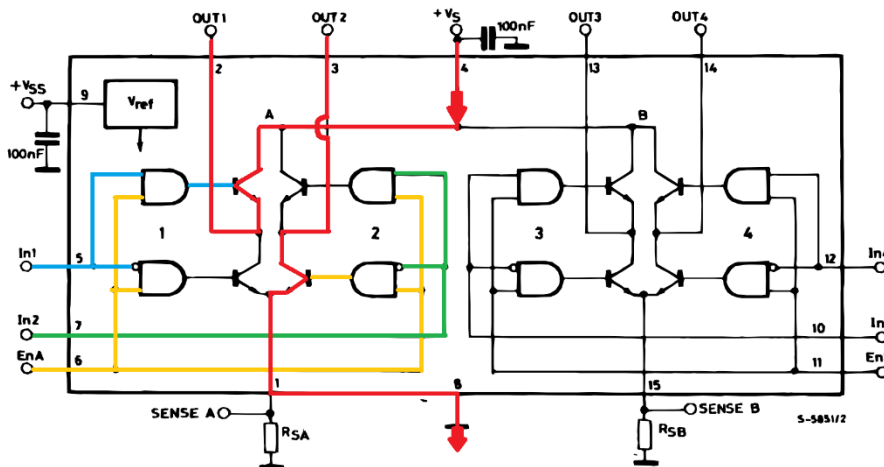
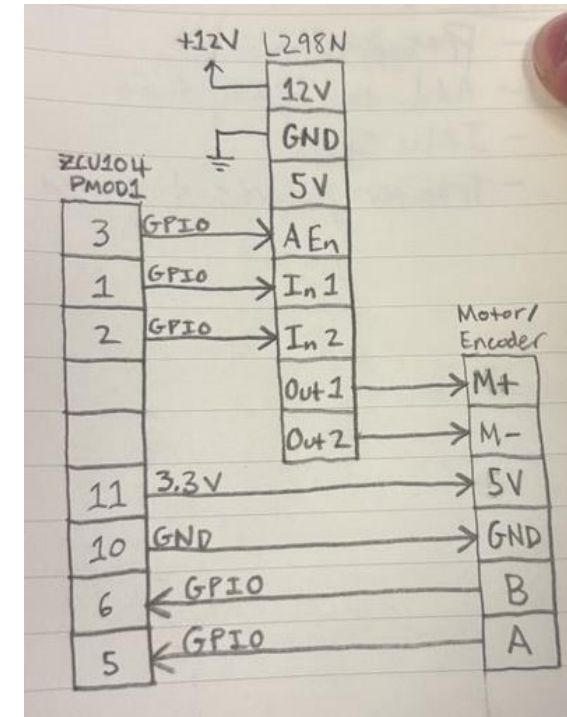
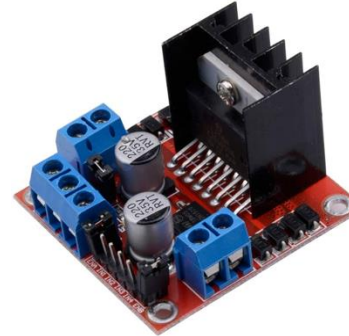
- **Xilinx Zynq UltraScale+ MPSoC ZCU104**
- **MPSoC = Multi-Processor System on Chip**
 - **Single integrated circuit with both PS and PL**
 - PS = Processing System → APU, RPU, GPU
 - PL = Programmable Logic → FPGA fabric
 - AXI = Advanced eXtensible Interface → Connections between PS and PL
- **FPGA = Field Programmable Gate Array**
 - High clock rates and parallel processing
 - Low latency and high throughput
 - Rapid, dynamic prototyping, unlike an ASIC
 - Simulation
 - Interfacing with other hardware components
 - Real-time visualization and control of both internal and external components
 - No overhead of an OS → handled by PS in the case of Zynq





FPGA

- FPGA motor control
- L298N H-bridge (motor driver)
 - EnA → motor on/off or PWM
 - In1, In2 → control motor spin direction
 - Out1, Out2 → drive motor (motor+ / motor-)
- PMOD
 - GPIOs → output direction and PWM, take in quadrature





FPGA

- Vivado Design Suite
 - HDL design, simulation, synthesis, and implementation
- Testbench design / simulation

```
-- Clock period
constant clk_period : time := 10 ns;

-- Procedure (or function to be "called") to generate quadrature pulses
procedure quadrature_step(
    signal A : out std_logic; -- "out" because it will be generated as an output to simulation
    signal B : out std_logic; -- "out" because it will be generated as an output to simulation
    forward : in boolean      -- Boolean to dictate direction of simulated motor
) is
begin
    if forward then -- if forward is TRUE
        -- Sequence: 00 -> 01 -> 11 -> 10 -> 00
        A <= '0'; B <= '0'; wait for 4 * clk_period; -- 40 ns wait period between signal changes
        A <= '0'; B <= '1'; wait for 4 * clk_period;
        A <= '1'; B <= '1'; wait for 4 * clk_period;
        A <= '1'; B <= '0'; wait for 4 * clk_period;
    else -- if forward is FALSE
        -- Reverse: 00 -> 10 -> 11 -> 01 -> 00
        A <= '0'; B <= '0'; wait for 4 * clk_period;
        A <= '1'; B <= '0'; wait for 4 * clk_period;
        A <= '1'; B <= '1'; wait for 4 * clk_period;
        A <= '0'; B <= '1'; wait for 4 * clk_period;
    end if;
end procedure;

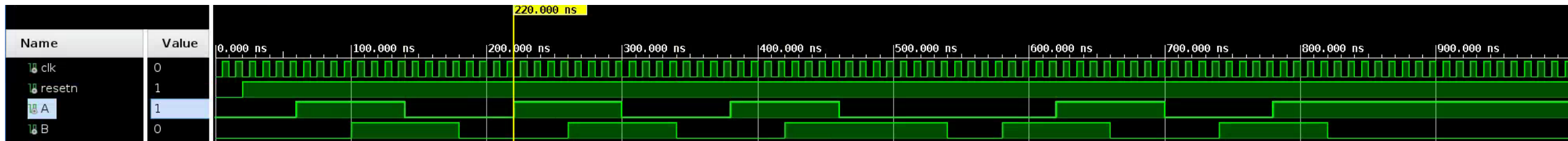
-- Stimulus process
stim_proc : process -- Do stuff!
begin
    -- Reset
    wait for 20 ns;
    resetn <= '1';

    -- Forward rotation: 3 steps
    for i in 1 to 3 loop
        quadrature_step(A, B, false); -- Call procedure "quadrature_step", set forward to false
    end loop;

    -- Wait and print
    wait for 40 ns;

    -- Reverse rotation: 2 steps
    for i in 1 to 2 loop
        quadrature_step(A, B, true); -- Call procedure "quadrature_step", set forward to false
    end loop;

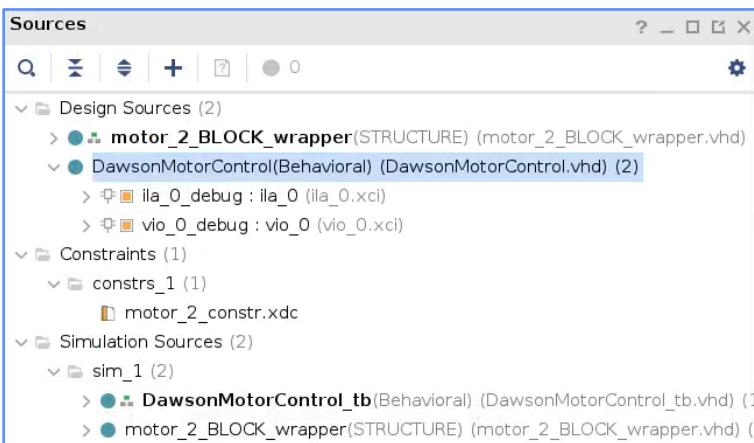
    -- Wait and finish
    wait for 100 ns;
    assert false report "Simulation completed" severity note;
    wait; -- forever
end process;
```





FPGA

- Block design
- Top level HDL design
- ILA / VIO IP blocks



```
-- Quadrature Decoder process
process(clk)
    -- "process" is the main description area of the behavior of the "thing"
    -- Processes run in parallel!
    -- "process(clk)" indicates the process uses synchronous logic
begin
    -- begin process
    if rising_edge(clk) then
        -- Logic sequence evaluated upon rising clock edges
        if resetn = '0' then
            -- If asynch. reset LOW --> reset values to 0
            position_vec <= (others => '0');
            A_prev <= '0';
            B_prev <= '0';
        else
            -- else, register A & B values and increment position_vec according to the logic sequence below
            A_reg <= A;
            B_reg <= B;

            if (A_reg /= A_prev) or (B_reg /= B_prev) then
                -- (Best illustrated with drawings...)
                if (A_prev = '0' and B_prev = '0') then
                    if (A_reg = '1') then
                        position_vec <= position_vec + 1;
                    elsif (B_reg = '1') then
                        position_vec <= position_vec - 1;
                    end if;
                elsif (A_prev = '1' and B_prev = '0') then
                    if (B_reg = '1') then
                        position_vec <= position_vec + 1;
                    elsif (A_reg = '0') then
                        position_vec <= position_vec - 1;
                    end if;
                elsif (A_prev = '1' and B_prev = '1') then
                    if (A_reg = '0') then
                        position_vec <= position_vec + 1;
                    elsif (B_reg = '0') then
                        position_vec <= position_vec - 1;
                    end if;
                elsif (A_prev = '0' and B_prev = '1') then
                    if (A_reg = '1') then
                        position_vec <= position_vec - 1;
                    elsif (B_reg = '0') then
                        position_vec <= position_vec + 1;
                    end if;
                end if;
            end if;
            A_prev <= A_reg;
            B_prev <= B_reg;
        end if;
    end if;
end process;

-- Update_prev values

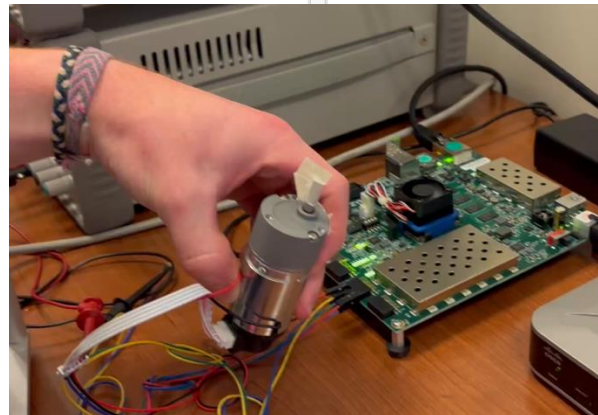
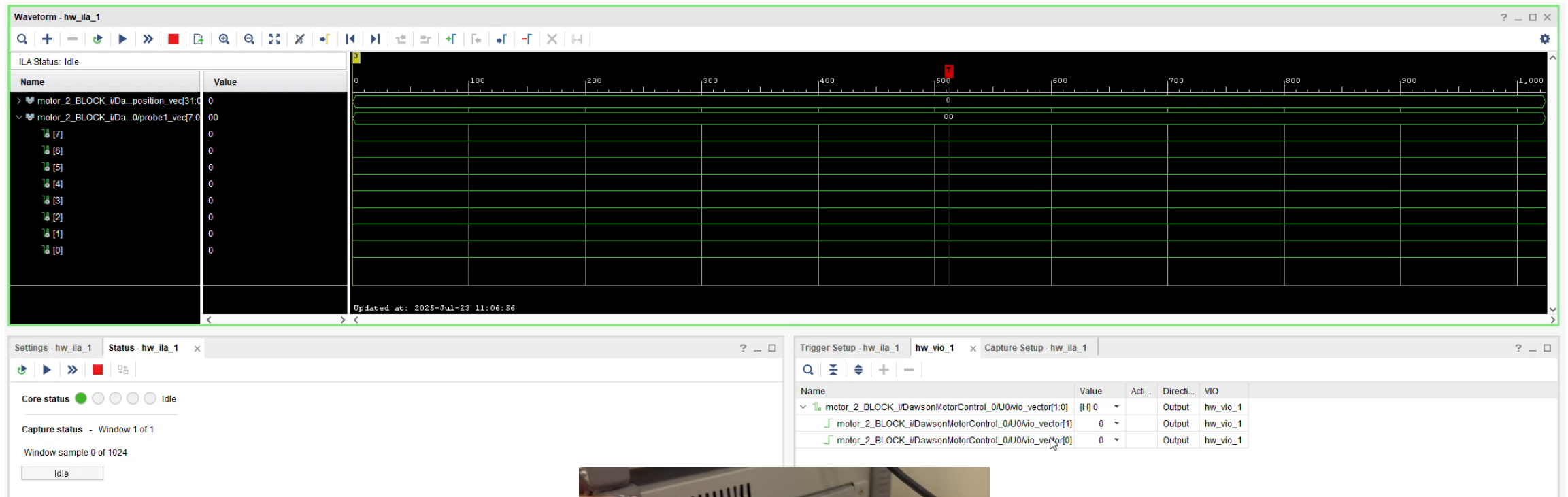
-- Direction Control process
process(clk)
begin
    -- begin process
    if rising_edge(clk) then
        if resetn = '0' then
            In1 <= '1';
            In2 <= '0';
        else
            if (dir(0) = '0') then
                In1 <= '1';
                In2 <= '0';
            else
                In1 <= '0';
                In2 <= '1';
            end if;
        end if;
    end if;
end process;
```

A leads B

B leads A



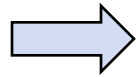
FPGA





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- **Future Work**



Future Work

- **Elmo path or Zynq path both viable for motion control**
- **Elmo path**
 - **Pre-existing software, known hardware**
 - **Convenient motion control and graphing capabilities**
 - **Sometimes difficult to navigate, limited examples online**
- **Zynq path**
 - **Can do what the Elmo does**
 - **Can also read FPA frames → “One-Stop Shop Controller”**
 - **Reduce hardware footprint on testbed**
 - **Would implement PWM and PID control for smoother velocity and tracking control**
 - **Would implement seamless interface between PS and PL using AXI bus**
- **Dual motor control to replicate true gimbal with azimuth and elevation axes**



Thank You!

- Alicia Volpicelli
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- Robert D'Ambra
- Robert Murphy
- Tasha LaSpisa
- Timothy Yarnall
- Tobias Chang
- Tom Miller
- Group 66
- Group 72