Assignment No.6

Code/Sub: 2113114/Computer Organization & Architecture   **Year/Sem: SE-III**

Date of Announcement: **Date of Submission:**

Corse Outcome 2113114.6: Analyze the impact of pipeline hazards and discriminate between structural, data, and control hazards.

Q. No	Question	Bloom Level
1	A computer architecture student runs a program on a 5-stage pipeline CPU (IF, ID, EX, MEM, WB). One section of code causes unexpected behavior: 1. LOAD R1, 0(R2) 2. ADD R3, R1, R4 3. SUB R5, R1, R6 They notice that the ADD and SUB instructions use a value in R1 before it's written back by the LOAD. The CPU does not stall automatically. Analyze the type of hazard occurring in this scenario. Break down why it happens in a pipeline. Suggest at least two techniques to mitigate this type of hazard.	Analyze
2	In a pipelined RISC processor, the following loop causes irregular instruction flow: assembly LOOP: BEQ R1, R2, EXIT	Analyze

	ADD R3, R3, R4
	
	SUB R1, R1, #1
	
	J LOOP
	
	EXIT: NOP
	
	The student observes that the pipeline executes wrong instructions when the BEQ branch is taken. They ask you to explain what's going wrong.
	
	Analyze the type of pipeline hazard present. Appraise the reason behind its occurance, and discuss at least two techniques used in modern processors to mitigate this hazard.	

3	A processor uses a unified memory for both instructions and data. While executing a program with back-to-back LOAD and JUMP instructions, performance drops. A deeper look reveals both instructions try to access memory at the same clock cycle. Analyze what kind of pipeline hazard this is. Appraise about shared hardware that contributes to the issue and choose architectural solutions to resolve or mitigate this hazard.	Analyze