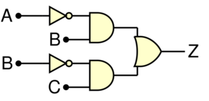
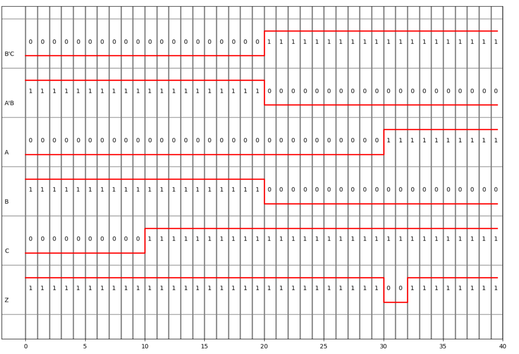
EET3300 Module 7 - Timing

1. Draw a timing diagram for $Z(A, B, C) = (A' B + B' C)$.

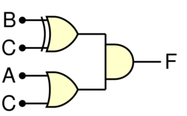
- Inverters have a propagation delay of 2 ns
- AND and OR gates have a propagation delay of 5 ns. The input signals are shown in figure 9.5.

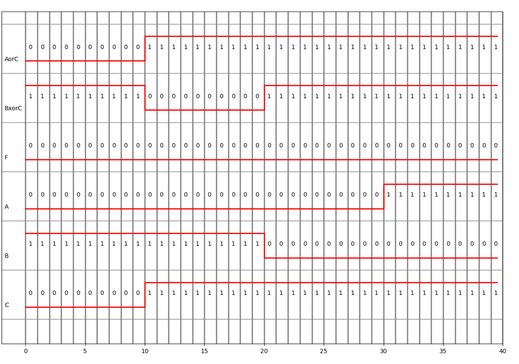




2. Draw a timing diagram for $F(A, B, C) = (B \oplus C)(A + C)$.

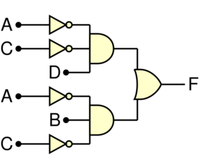
- AND gates have a delay of 2 ns
- OR gateshave a delay of 3 ns
- XOR gates have a delay of 5 ns. The input signals are shown in figure 9.5.

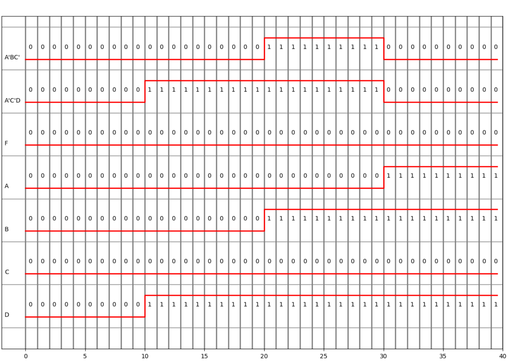




4. Draw a timing diagram for $F(A, B, C, D) = A^{'}C^{'}D + A^{'}BC^{'}$

All logic gates have a propagation delay of 5 ns. The input signals are shown in figure 9.6.





5. Look up the datasheet for the 74LS139A 2 to 4 decoder.

- Although we haven't discussed decoders yet, you will be able to interpret the logic diagram which only uses inverters and NAND gates. Assuming that every logic gate has a delay of 10 ns, draw the output for 1Y 1 giving the input signals shown in figure 9.7

Hazards

1. Find a hazard-free SOP expression for $F(A, B, C) = \Sigma m(2, 3, 5, 7)$.

3. Find a NAND-only hazard-free expression for $F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 6, 11) + \Sigma d(8, 12, 13)$