Experiment 2

Multi-Function Gate

Digital Systems

EEE3342C-20FALL 0011

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Equipment:

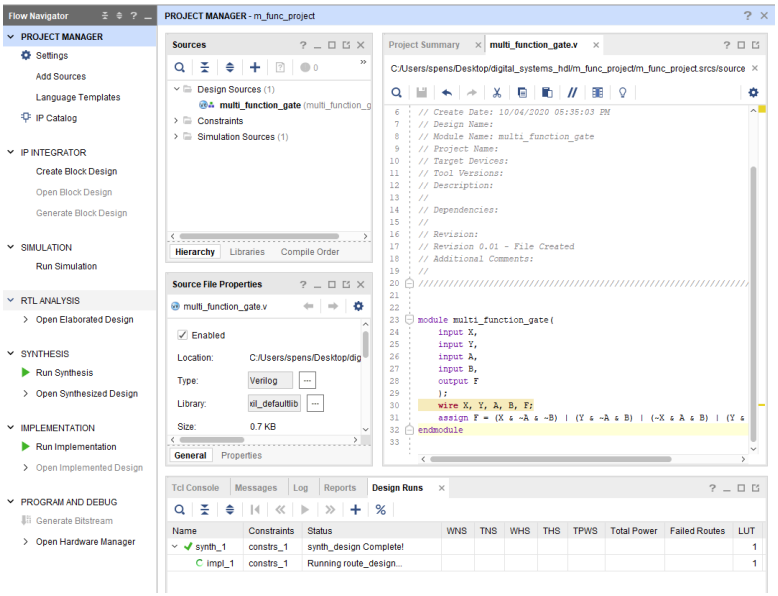
The Xilinx's FPGA VIVADO HLx Editions design tools are available in the laboratory. These tools can also be downloaded from Xilinx's web site at www.xilinx.com. The WebPack version of this tool that we use for the laboratory experiments are located under the support download section at the related website (https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloa dNav/vivado-design-tools/2017-4.html). Please take note that the file download size exceeds 1 GB and also during the installation process updates may have to be installed. It can take you up to a few hours to download and install the software on your computer. The user does not need to have the BASYS development board interface to the computer to design and simulate an FPGA.

Objective:

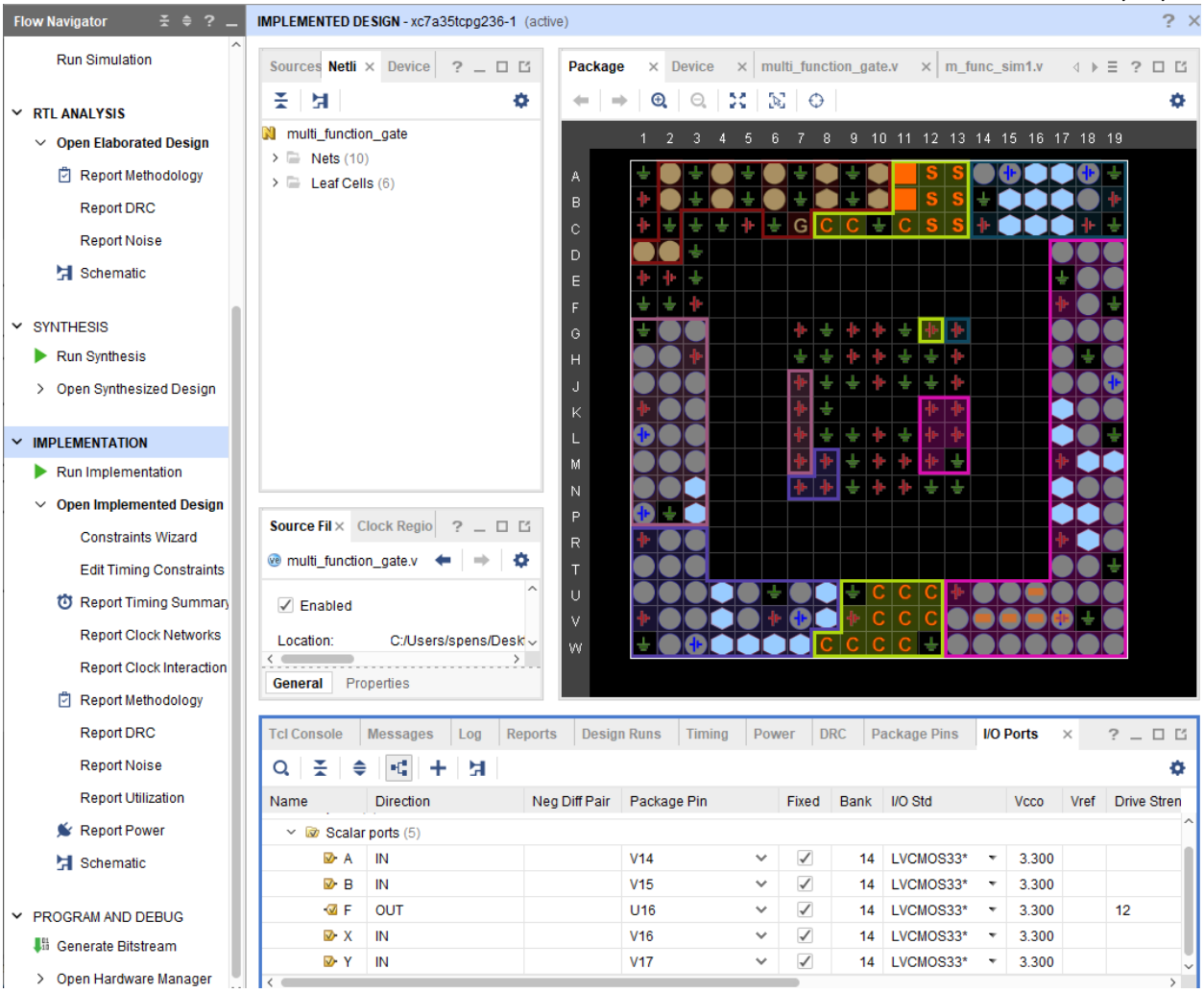
The objective is to design and implement a multi-function gate with the Xilinxs FPGA Vivado tools and to display the results of the experiment. The Vivado tools will be used to design, simulate, and create (virtually) a multi-function gate.

Design Steps:

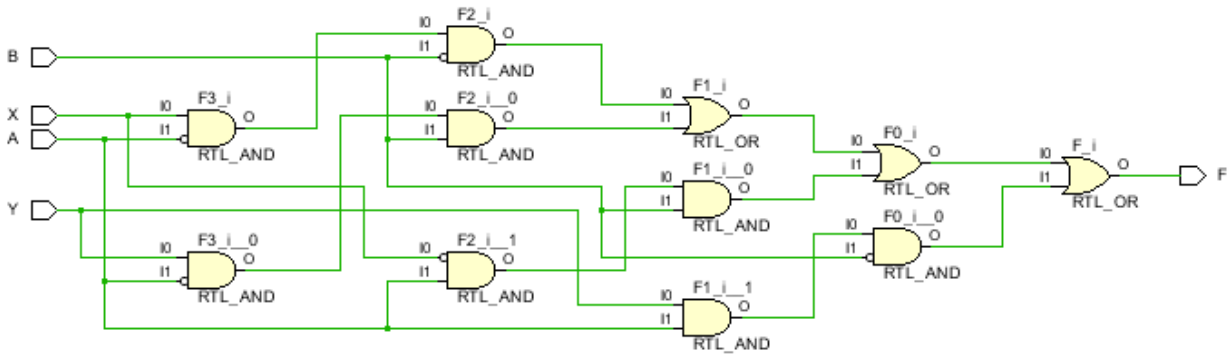
I created the project (m_func_proj) and added all inputs and the single output. I then programmed the logic of the multi-functional gate.



I then ran synthesis and implementation, to implement I/O Planning and Schematics. I then connected all the inputs and outputs to the I/O Planning.



Then I generated the schematic of the multi-functional gate.

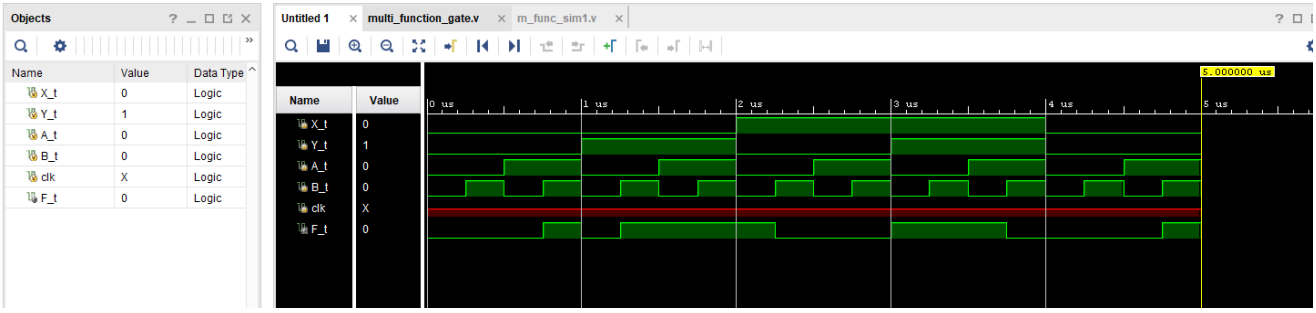


I then programmed the logic for the simulation.

C:/Users/spens/Desktop/digital_systems_hdl/m_func_project/

```
17      // Revision 0.01 - File Created
18      // Additional Comments:
19      //
20      //////////////////////////////////////
21
22
23      module m_func_sim1(
24
25          );
26          reg X_t;
27          reg Y_t;
28          reg A_t;
29          reg B_t;
30          reg clk;
31          wire F_t;
32
33          multi_function_gate UUT(
34              .X(X_t),
35              .Y(Y_t),
36              .A(A_t),
37              .B(B_t),
38              .F(F_t)
39              );
40          initial begin
41              X_t = 1'b0;
42              Y_t = 1'b0;
43              A_t = 1'b0;
44              B_t = 1'b0;
45              //clk = 1'b0;
46          end
47          //always #5 clk = ~clk
48          always #2000 X_t = ~X_t;
49          always #1000 Y_t = ~Y_t;
50          always #500 A_t = ~A_t;
51          always #250 B_t = ~B_t;
52      endmodule
```

I then ran a behavioral simulation of the logic design.



Pre-Lab:

1. Read this experiment carefully to become familiar with the experiment.

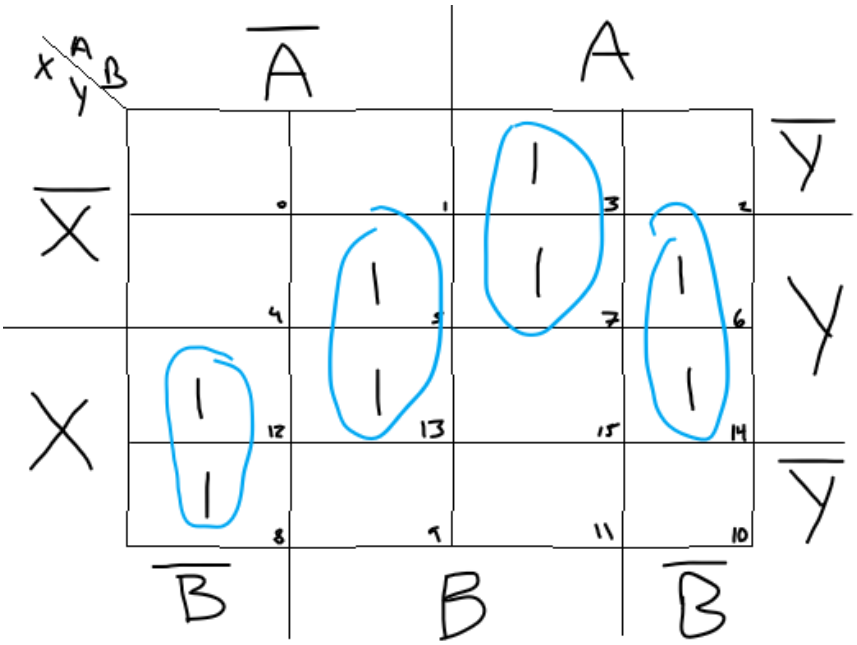
2. Represent the output F as a function of X, Y, A and B on a truth table.

X	Y	A	B	OUT
0	0	0	0	0

0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

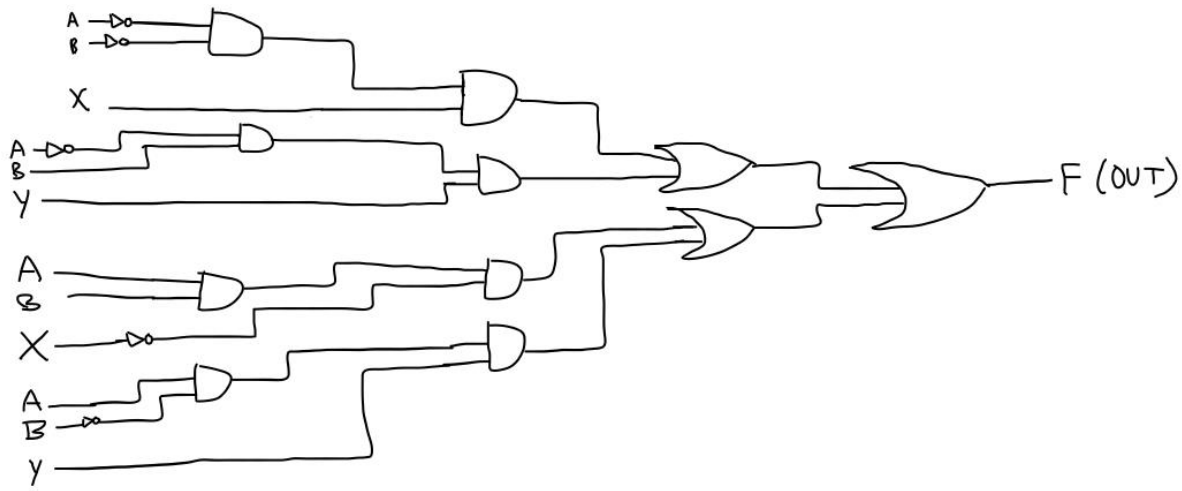
F = ∑m(3,5,6,7,8,12,13,14)

3. Write the minimum logic expression, as a sum-of-products for the function F.



F = XA'B' + A'BY + ABX' +YB'A

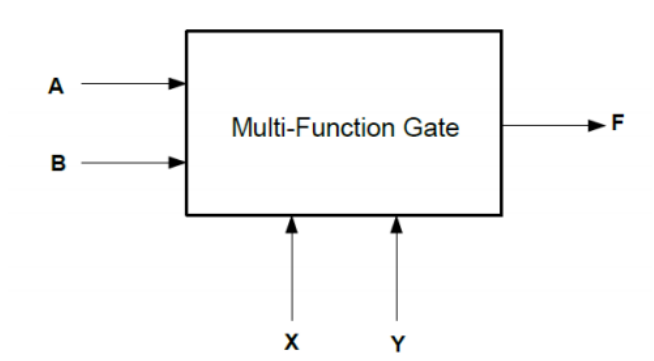
4. Draw logic diagrams for the above expressions using AND's, OR's, and Inverters.



Multi-Function Gate Schematic

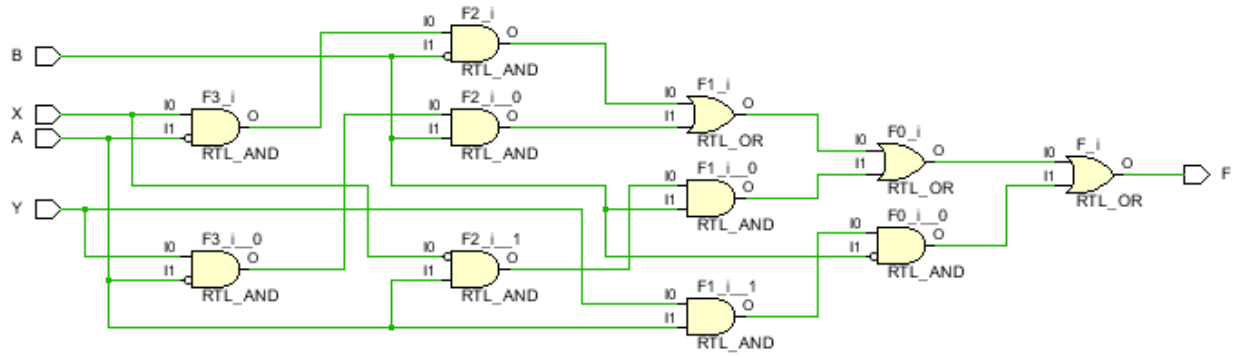
Logic Diagram:

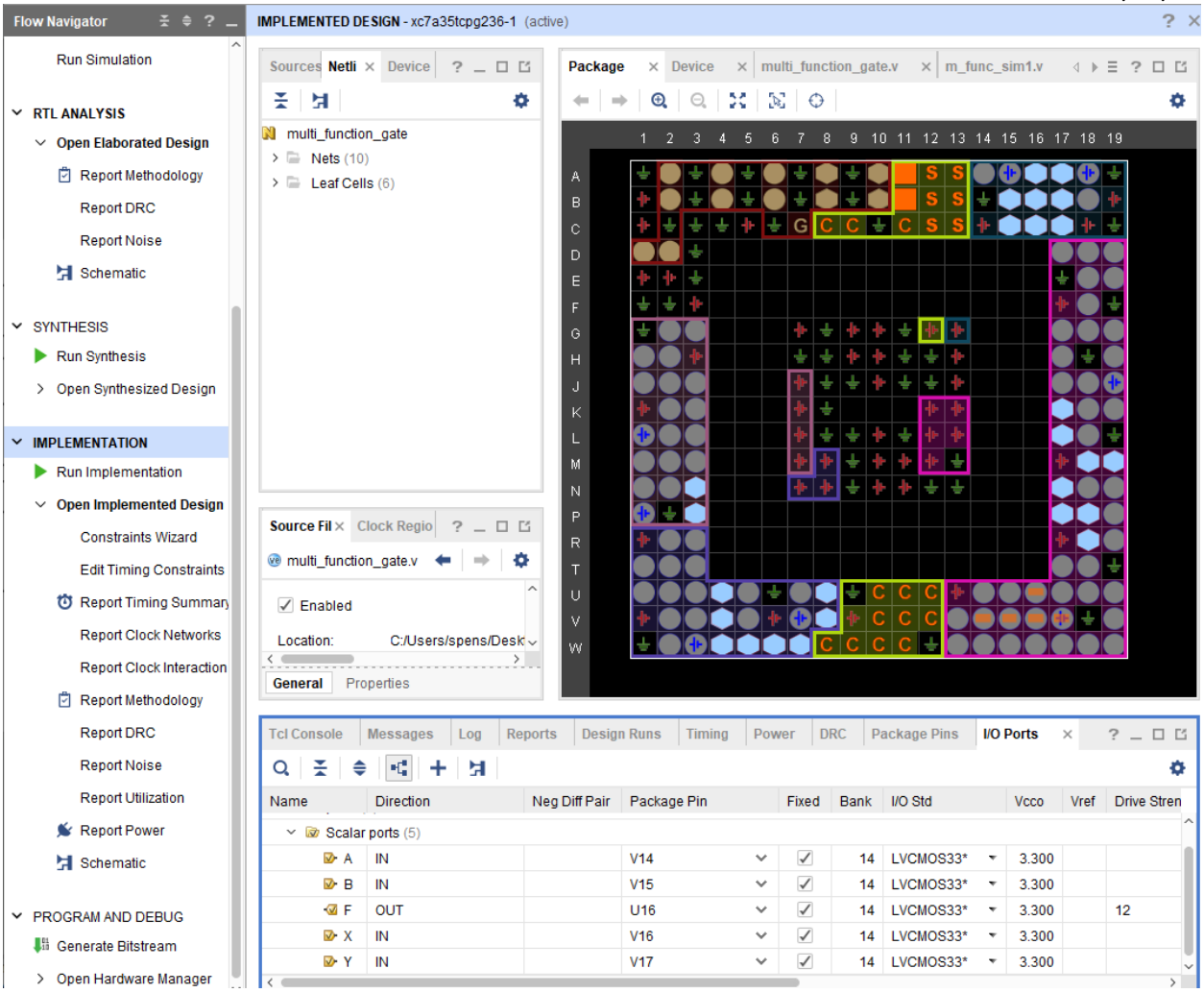
The resulting schematic diagram for the MULTI-FUNCTIONAL gate.



Design Specification Plan:

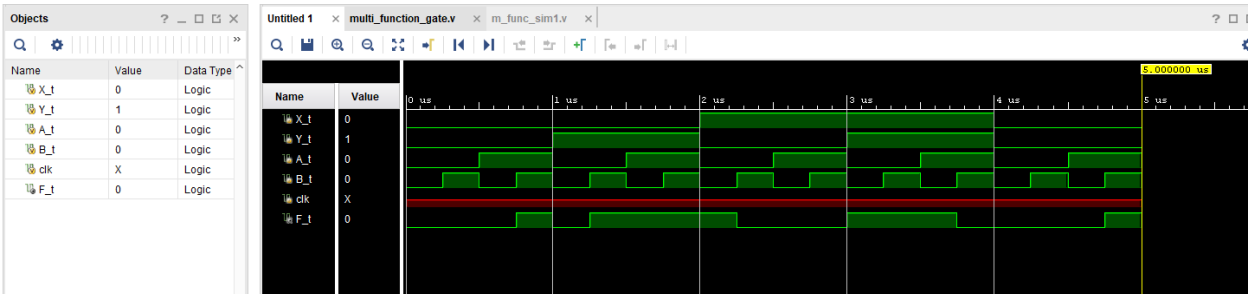
This is the design specification for an MULTI-FUNCTIONAL gate. It has four inputs (X, Y, A, and B) and one output (F).





Results Statement:

Here is the simulation results for the MULTI-FUNCATIONAL gate.

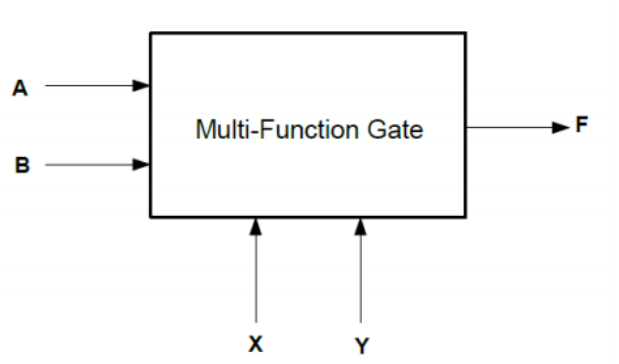


SW6	SW7	SW0	SW1	LED7
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Multi-Function Gate Verilog

Logic Diagram

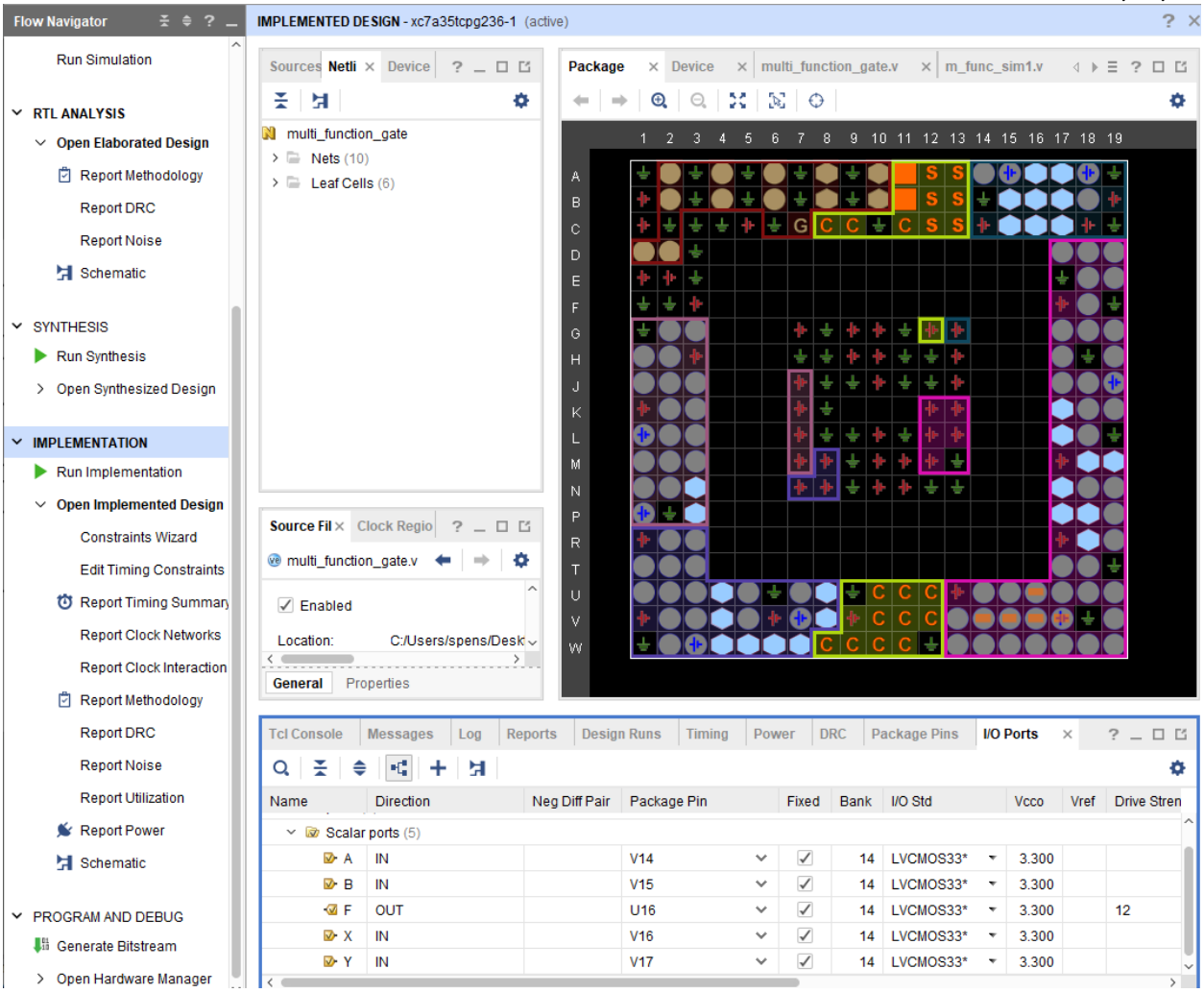
The results from the simulation testing for the simulation for a MULTI-FUNCTIONAL gate.



Design Specification Plan

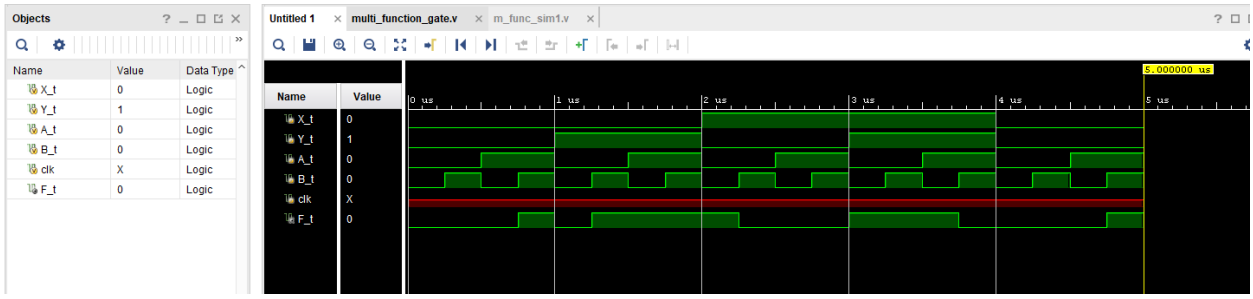
This is the design specification for an MULTI-FUNCTIONAL gate. It has four inputs (X, Y, A, and B) and one output (F).

```
// Create Date: 10/04/2020 05:35:03 PM
// Design Name:
// Module Name: multi_function_gate
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module multi_function_gate(
    input X,
    input Y,
    input A,
    input B,
    output F
    );
    wire X, Y, A, B, F;
    assign F = (X & ~A & ~B) | (Y & ~A & B) | (~X & A & B) | (Y &
endmodule

```



Results Statement

Explanation of pictures and tables.

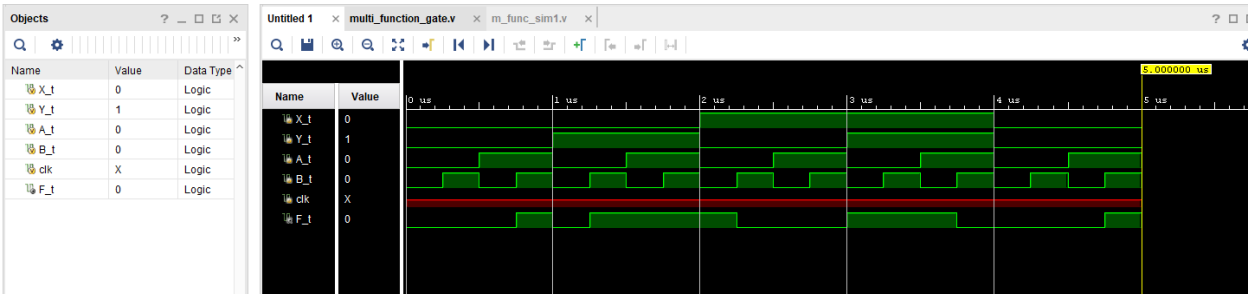


SW6	SW7	SW0	SW1	LED7
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Test Plan

The initial design was tested through a simulation based off of the test bench, which was programmed for every possible input, which would give every output.

(Multi-functional gate)



Conclusion

My results were what I expected, and all the test and simulation results were correct and agreed with the logic that was programmed. By running the gate through a simulation and then analyzing it was interesting, and lead to further understanding of the logic gates functionality and how it functions.

1. Can this Multi-Function Gate be operated as an Inverter? If yes, explain how.

It can be used as a NOT gate if both inputs are joined together and the X and Y input are high (set as When this is done, X and Y function as a NAND gate, and when that happens, the NAND gate operates like an inverter.

2. Will the change in the number of inputs or outputs affect the number of operation select lines? Explain.

The number of outputs does not have an effect on the number of operation select lines. This is because each output is connected to a certain operation. So, by changing the amount of operations will increase the amount of outputs, but increasing the amount of outputs does not effect on the amount of operation select lines in the circuit.

3. Will the change in the number of functions alter the number of operation select lines? Explain.

Yes, if the number of functions is increased, the number of operation select lines are also increased, since there will be more functions to select, so there will need to be more operation select lines. The square root of the number of functions is how many select lines you will need.

4. Have you met all the requirements of this lab (Design Specification Plan)?

Yes.

5. How should your design be tested (Test Plan)?

My design was tested by running the circuit design through a detailed simulation that tested each input value, in all the combinations, and after checking each one, the results match the truth table. That would verify that the logic design if correct.

Answers To In-Class Activities:

1. C (RTL Analysis > Schematics)

2. D (F = !X!YAB+!XY!AB+!XYA!B+!XYAB+X!Y!A!B+XY!A!B+XY!AB+XYA!B)