Furkan Eris

Sunnyvale, CA
✉ furkan7@gmail.com
https://www.linkedin.com/in/furkan-eris/

Education

2016 – 2022 **Boston University, USA**, *Doctorate of Philosophy, ECE, GPA: 3.92/4.0.*
2016 – 2020 **Boston University, USA**, *Masters of Science, ECE, GPA: 3.92/4.0.*
2012 – 2016 **Bogazici University, Turkey**, *Bachelors of Science, EEE, GPA: 3.5/4.0.*
2012 – 2016 **Bogazici University, Turkey**, *Bachelors of Science, Physics, GPA: 3.5/4.0.*
2015 – 2016 **University of Texas at Austin, USA**, *Exchange Term, ECE, GPA: 3.52/4.0.*

Skills & Abilities

Programming: Python, System Verilog, Verilog, C/C++, ASSEMBLEY (X86, RISC-V)
Tools: Cadence Virtuoso, Cadence Hspice, Synopsys DC, Synopsys ICC, DSENT, HotSpot, LaTeX, LabView, VCS, Gitlab CI
Libraries: PThreads/OpenMP, CUDA, Scikit-Learn, Pandas

Professional Activities

June 2022 – Current **MTS Silicon Design Engineer**, *AMD (Advanced Micro Devices) Research*, Sunnyvale, CA, USA.
- Working on next-next generation of large-scale system designs for HPC and ML applications.
- Focusing on ML-based system optimization and networking on large systems.

June 2021 – Dec 2021 **Cores Performance Part-Time**, *AMD (Advanced Micro Devices)*, Boxborough, MA, USA.
- Confidential project at AMD for resource assessment and prediction.

Aug 2019 – May 2020 **Cores Performance Intern**, *AMD (Advanced Micro Devices)*, Boxborough, MA, USA.
- Designed adaptor for many-core processors.
- Built and tested adaptor in run-time systems with major overhauls to the algorithm leading to 4 patents.

May 2018 – Dec 2018 **Cores Performance Intern**, *AMD (Advanced Micro Devices)*, Boxborough, MA, USA.
- Responsible for exploring novel ideas to improve upon existing core architecture and increase IPC.
- Showed good increase in IPC which led to a patent submission and a paper submission in process.

Summer 2015 **Defense Intern**, *Aselsan*, Ankara Turkey.
- Developed kalman-filter-based tracking system for missiles.

Summer 2014 **Wind Energy Intern**, *Siemens*, Istanbul Turkey.
- Researched and implemented ad-hoc prediction mechanisms using data-backed insights into wind turbine sites and yield from those cites.

PhD Research Projects

Aug 2020 – June 2022 **Secure Standard Cell Design**.
- Used optical techniques to image chip layouts, based on certain design patterns, secured the IP of chips using nanoantennas.
- Pushed custom standard cells through all PNR steps all the way from the standard cell library construction to sending a tapeout in GF-22nm.
- Currently investigating methods of machine learning to automatically insert optical signatures into existing standard cells.

Aug 2018 – June 2022 **Hardware Adaptation Using Machine Learning (Collab. Between AMD and BU)**.
- Currently investigating novel methods to improve the performance of next generation processors.
- Built a non-invasive low-overhead adapter to perform run-time adaptation of the prefetcher settings in order to increase the processor performance.
- Extensively evaluated using industry benchmarks from SPEC2006, SPEC2017, SPECjbb, Cloud, Server, Client, and more.

Aug 2017 – May 2020 **Cross-Layer Network Design for 2.5D Systems**.

- Optimized cross-layer network on three separate layers: the physical layer with microbump overheads and physical routing, the circuit layer with 2.5D circuit models done in HSPICE and circuit optimization, and the logical layer made out of multiple electrical networks.
- Extensively optimized 2.5D link design using wire width, repeaters per micron, microbump capacitance, wire lengths, voltage frequency settings, wire dimensions such as pitch, different link designs such as active and passive interposer links, and different technology nodes.
- Evaluated work using industry application benchmarks such as PARSEC, SPLASH-2, and UHPC.

Patents

2021 Invariant Statistics-Based Configuration Of Processor Components, *AMD*, US Patent Pending 17/217,101.

2020 Hardware Configuration Selection Using Machine Learning Model, *AMD*, US Patent Pending 17/133,581.

2020 Multi-Class Multi-Label Classification Using Clustered Singular Decision Trees For Hardware Adaptation, *AMD*, US Patent Granted US11,455,252.

Publications

ISCA'23 C. Demirkiran, **F. Eris**, G. Wang, J. Elmhurst, N. Moore, N. Harris, A. Basumallik, V. Reddi, A. Joshi, D. Bunandar, An Electro-Photonic System for Accelerating Deep Neural Networks, **Tentative**

TACO'23 **F. Eris***, K. Eris, M. Louis, J. Abellan, A. Joshi, ML-Based Prefetcher Adapter,

ICML'22 K. Eris, **F. Eris**, and B. Kulis, A Distributional Perspective on Self-Supervision for Few-Shot Learning, **Tentative**

ICML'22 **F. Eris**, K. Eris, H. Gold, L. Shamieh, N. Shukla, M. Mahdavi, A. Joshi, and V. Narayanan, Secure Your Standard Cells, RL-based CAD Flow to Automatically Insert Nanoantennas, **Tentative**

DAC'21 S. Canakci*, L. Delshadtehrani, **F. Eris**, M. Taylor, M. Egele, A. Joshi, DirectFuzz: Automated Test Generation for RTL Designs using Directed Graybox Fuzzing

MLArchSys'21 **F. Eris***, M. Louis, S. Canakci, J. Abellan, A. Joshi, Custom Tailored Suite of Random Forests for Prefetcher Adaptation

TCAD 2020 **F. Eris**, A. Joshi, A. Kahng, Y. Ma*, S. Mojumder and T. Zhang, Cross-Layer Co-Optimization of Network Design and Chiplet Placement in 2.5D Systems

ICCAD'18 A. Coskun, **F. Eris***, A. Joshi, A. Kahng, Y. Ma and V. Srinivas, A Cross-Layer Methodology for Design and Optimization of Networks in 2.5D Systems

DATE'18 **F. Eris**, A. Joshi, A. Kahng, Y. Ma*, S. Mojumder and T. Zhang, Leveraging Thermally-Aware Chiplet Organization in 2.5D Systems to Reclaim Dark Silicon

BARC'18 A. Coskun, **F. Eris**, A. Joshi, A. Kahng , Y. Ma*, S. Mojumder and T. Zhang, Reclaiming Dark Silicon Using Thermally-Aware Chiplet Organization in 2.5D Integrated Systems

Academic Activity/ Teaching Experience

2018 – 2021 Expert Reviewer *OJCS 2020, OJCS 2021, DAC 2018, DAC 2019, DAC 2020, ICCAD 2020*.

2017 – 2018 Graduate Teaching Fellow for course *Introduction to Logic Design*, *Boston University*.

Awards

2017 – 2018 Best GTF (Graduate Teaching Fellow) of the year , *Boston University, USA*

2016 – 2017 ACM Turing Award Student Scholarship, *ACM, USA*

2016 – 2017 A. Richard Newton Young Student Fellow, *DAC, USA*

2016 – 2017 Boston University Deans Fellowship, *Boston University, USA*

2015 – 2016 First Place in the 6th annual national LED Circuit Design Conference, *Turkey*

2014 – 2016 Tubitak Science Scholarship, *TUBITAK (Scientific and Technological Research Council of Turkey)*

2013 – 2016 Siemens Academic Achievement Scholarship, *Siemens, Turkey*

2012 – 2016 Turkish Government Top 100 Student Scholarship, *Republic of Turkey, Turkey*

2012 – 2016 Bogazici University High Honors Deans List, *Bogazici University, Turkey*