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18CS33

Third Semester B.E. Makeup Examination, January 2020

DIGITAL ELECTRONICS

Time: 3 Hours

Max. Marks: 100

Instructions: 1. Answer any one question from each Unit.

			L	CO	PO	M
		UNIT - I				
1	a.	Solve the following Boolean Expression to get the reduced form and draw the logic circuit using NAND gates only. $Y = B + AB' + ACD + AC'$	(3)	(1)	(1)	(06)
	b.	Apply K-Map reduction technique to obtain the reduced POS expression for the given Boolean function. $F(A,B,C,D) = \prod M(0,1,5,9,13,14,15) \cdot d(3,4,7,10,11)$	(3)	(1)	(2)	(06)
	c.	Solve the given Boolean function by using Quine Mc Clusky method and find the essential prime implicants. $F(A,B,C,D) = \sum m(1,3,5,10,11,12,13,14,15)$	(3)	(1)	(2)	(08)
		OR				
2	a	Realize the given Boolean expression using NAND gates and find the minterms for the same. $F = AC + AB'C + ACD$	(2)	(1)	(1)	(06)
	b	Make use of K-Map reduction technique to obtain the reduced SOP expression for the given Boolean function. $F(A,B,C,D) = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$	(3)	(1)	(2)	(06)
	c	Identify all the prime and essential prime implicants of the following Boolean function using Quine Mc Clusky method. $F(A,B,C,D) = \sum m(2,3,6,7,8,9,13,15)$	(3)	(1)	(2)	(08)
		UNIT – II				
3	a.	Define a Multiplexer. Implement the given Boolean function using 8:1 multiplexer. Consider D as MEV. $F(A,B,C,D) = \Sigma m(0,1,3,4,5,7,9,11,13,15)$.	(3)	(2)	(1)	(06)
	b.	Design and illustrate a 1-bit magnitude comparator with a neat diagram and truth table.	(3)	(2)	(2)	(06)
	c.	Define Decoder. Design and explain a BCD-to-Decimal decoder.	(3)	(2)	(2)	(08)
		OR				
4	a	Design a 4-bit odd parity generator. Write any one application of the same.	(2)	(2)	(1)	(06)
	b	Compare Decoder and Demultiplexer., make use of suitable Decoder and multi-input OR gate to implement the following functions. $F1(A,B,C) = \sum m(1,3,7)$ $F2(A,B,C) = \sum m(2,3,5)$ $F3 = \sum m(0,1,5,7)$	(2)	(2)	(2)	(06)
	c	How a PAL is different from PLA? Realize the following functions using PAL. $Y1 = A'B'C' + A'BC + A'BC + ABC'$ $Y2 = ABC$	(1)	(2)	(2)	(08)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

UNIT – III

5 a. Explain propogation delay time. If propogation delay is 20 nano seconds what is the maximum clock frequency. Draw the circuit for PT forming circuit.
(3) (3) (1) (06)

b. Realize SR flip flop using NOR gates.
(3) (3) (2) (06)

c. Derive the characteristics equations for SR , JK flip flops with state transition diagram and write the excitation tables.
(3) (3) (2) (08)

OR

6 a. Explain working of (i) gated JK flip flop (ii) gated D flip flop.
(2) (3) (1) (06)

b. Explain working of JK master slave flip flop.
(2) (3) (1) (06)

c. Derive the characteristics equations for T , JK flip flops with state transition diagram and write the excitation tables
(3) (3) (2) (08)

UNIT - IV

7 a. List out the applications of a shift register and with a neat logic diagram explain the working of serial adder.
(2) (3) (1) (06)

b. How to convert JK flp flop into T flip flop and explain the steps.
(1) (3) (1) (06)

c. Design a MOD-6 synchronous upcounter using JK flip flops and explain its operation with a neat logic diagram and truth table.
(3) (3) (2) (08)

OR

8 a. Develop the logic diagram of a 4 bit Serial In Parallel Out shift register and explain its working.
(3) (3) (2) (06)

b. Explain with a neat diagram and Truth Table 3-bit Ripple down counter using JK flip flops.
(2) (3) (1) (06)

c. Design a MOD-8 synchronous upcounter using JK flip flops and explain its operation with a neat logic diagram and truth table.
(3) (3) (1) (08)

UNIT -V

9 a. Explain the working of 2-bit Simultaneous A/D converter.
(2) (3) (1) (06)

b. Develop verilog program for following circuits in Data flow model.
1. 4:1 Multiplexer 2. 1-bit Full Adder
(3) (4) (2) (06)

c. Explain 4-bit R-2R ladder Digital to Analog converter and find the output for the input 1001 and 1100 when V = +5 volts.
(2) (3) (1) (08)

OR

10 a. Explain the working of 4-bit Successive Approximation type A/D converter.
(2) (3) (1) (06)

b. Develop verilog program for following circuits in Data flow model.
1. 2:4 Decoder 2. 8:1 Multiplexer
(3) (4) (2) (06)

c. Explain 4-bit R-2R ladder DAC and find the output when DAC input is 11010 and voltage v = +5v.Also what is the voltage resolution?
(2) (3) (1) (08)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

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18CS/IS33

Third Semester B.E. Semester End Examination, Dec./Jan. 2019-20

DIGITAL ELECTRONICS

Time: 3 Hours

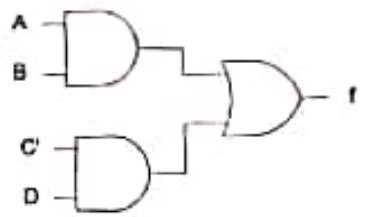
Max. Marks: 100

Instructions: 1. Answer one full question from each unit.

UNIT - I

			L	CO	PO	M
1	a.	Solve the given Boolean function using Boolean algebra and realize using NAND gates. $Y = A'BC + ABC + ABC' + AB$	(3)	(1)	(1)	(06)
	b.	Make use of K-Map reduction technique to obtain the simplified SOP expression for the given Boolean function and realize using logic gates. $F(A,B,C,D) = \Sigma m(2,3,4,5,6,7,10,11,12)$	(3)	(1)	(2)	(06)
	c.	Apply Quine McClusky reduction technique to simplify the given Boolean expression and draw the logic circuit for the same. $F(A,B,C,D) = \Sigma m(0,1,2,3,4,5,12,13,14) + d(6,15)$	(3)	(1)	(2)	(08)

OR

2	a.	List the minterms for the given logic circuit.  	(3)	(1)	(1)	(06)
	b.	Make use of K-Map reduction technique to obtain the simplified POS expression for the given Boolean function and realize by using NOR gates.. $F(A,B,C,D) = \Pi M(0,1,4,5,8,12,13)$	(3)	(1)	(2)	(06)
	c.	Apply Quine McClusky reduction technique to simplify the given Boolean expression and find essential prime implicants. $F(A,B,C,D) = \Sigma m(1,3,5,7,12,13,14,15)$	(3)	(1)	(2)	(08)

UNIT – II

			L	CO	PO	M
3	a.	Implement the given Boolean function using 8:1 multiplexer. Consider A as MEV. $F(A,B,C,D) = \Sigma m(0,1,3,4,5,7,9,11,13,15)$.	(3)	(2)	(2)	(06)
	b.	Define decoder. Implement following functions using suitable decoder $f_1(A,B,C) = \Sigma m(0,1,6)$ $f_2(A,B,C) = \Sigma m(2,4,6)$	(3)	(2)	(1)	(06)
	c.	Design 2-bit magnitude comparator with the help of neat logic diagram. Implement the same using basic gates.	(3)	(2)	(2)	(08)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

OR

4 a. Design an Odd parity generator circuit for 3- bit binary data.

(3) (2) (2) (06)

b. Define Multiplexer. Explain the working of 4:1 multiplexer. Implement the given Boolean function using 4:1 multiplexer using A as MEV.
F(A,B,C) = Σm (0,2,4,7)

(3) (2) (2) (06)

c. Differentiate between PAL and PLA. Implement the following Boolean functions using PLA.
f_1 (A,B,C) = Σ m(0,1,7)
f_2 (A,B,C) = Σ m(4,5,7)

(3) (2) (2) (08)

UNIT - III

L CO PO M

5 a. Illustrate the working of a positive edge triggered SR flip flop and draw a neat sketch of its output waveforms.

(2) (3) (1) (06)

b. Determine the characteristic equations of SR, T and D flip flops.

(5) (3) (2) (06)

c. With a neat circuit diagram explain the working of a master-slave JK flip flop and write the advantages.

(2) (3) (1) (06)

OR

6 a. Compare a latch and a flip flop? Construct SR latch using NAND/NOR gates.

(2) (3) (1) (06)

b. Explain the characteristics of an ideal clock and find the clock frequency for a system when the cycle time is 5ns.

(2) (3) (1) (06)

c. Derive the characteristics equations for SR, JK flip flops with state transition diagram and write the excitation tables.

(2) (3) (1) (08)

UNIT - IV

L CO PO M

7 a. Show how SR flip flop is converted to JK flip flop.

(3) (3) (2) (06)

b. Explain with neat waveform 4 bit Johnson counter.

(2) (3) (2) (06)

c. Design MOD-6 synchronous counter using JK flip flop.Draw the logic diagram for the same.

(4) (3) (2) (08)

OR

8 a. Show how JK flip flop is converted into T flip flop.

(3) (3) (2) (06)

b. Explain with neat waveform 4 bit ring counter.

(2) (3) (2) (06)

c. Analyze the given sequential circuit and draw state diagram for same.

(4) (3) (2) (08)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

			L	CO	PO	M
		UNIT -V				
9	a.	Explain the working of 2 bit parallel comparator(simultaneous conversion) A/D Converter with neat circuit diagram.	(2)	(3)	(2)	(06)
	b.	Write HDL program for 4:1 multiplexer and full adder.	(3)	(4)	(2)	(06)
	c.	With neat sketch explain the working of 4 bit R-2R binary ladder DAC. Define resolution of D/A converter. What is resolution for 8 bit DAC if V = +5V.	(2)	(3)	(1)	(08)
		OR				
10	a.	Explain the working of 4 bit successive approximation ADC with neat circuit diagram.	(2)	(3)	(1)	(06)
	b.	Explain the working of R-2R ladder DAC. Find the output voltages for the inputs 11000 and 10010 if Logic 0= 0V and 1 =+10V.	(2)	(3)	(1)	(08)
	c.	Write HDL program for (i) Y = ABC' + AB'C +AB (ii) 2:4 decode	(3)	(4)	(2)	(06)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)