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Digital Electronics OBA-2

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USN : 2GI19CS175 Course : 18CS33

1.) SR flip flop :

The truth table for SR flip flop

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	? (forbidden)

Drawing a K-Map using above truth table

Q_n	$\bar{S}\bar{R}_{00}$	$\bar{S}R_{01}$	SR_{11}	$S\bar{R}_{10}$
$\bar{Q}_n$ 0	0	0	X	1
Q_n 1	1	0	X	1

From here,

$Q_{n+1} = (SR + S\bar{R}')(Q_n + \bar{Q}'_n) + Q_n(S'\bar{R}' + S\bar{R}')$

∴ Characteristic Eqn : $Q_{n+1} = S + Q_n\bar{R}'$

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1.) * JK Flip Flop

Truth table for JK flip flop.

J	K	Q_{n+1}
0	0	Q_n (last state)
0	1	0
1	0	1
1	1	$\bar{Q}_n$ (toggle)

Drawing K-map using above truth table

Q_n \ JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

From here;

$Q_{n+1} = Q_n'(JK + JK') + Q_n(J'K' + JK')$

∴ Characteristic Eqn : $\boxed{Q_{n+1} = JQ_n' + K'Q_n}$

* T flip-flop:

Truth table for T flip flop.

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n \ T	0	1
0	0	1
1	1	0

Drawing K-Map using above table

∴ Characteristic Eqn: $\boxed{Q_{n+1} = TQ_n' + T'Q_n}$

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1.) * D flip flop :

Truth table for D flip flop

D	Q_{n+1}
0	0
1	1

Characteristic eqn $Q_{n+1} = D$

2.) *Excitation Table of SR flip flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

*Excitation Table of T flip flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

*Excitation Table of JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

* Excitation table of D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

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3.) JK flip flop can be converted into T-flip flop by making $T = J = K$.

Step 1:
Construct the characteristic table of T flip-flop & excitation table of J-K flop-flop.

T	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	1	x	0
1	0	1	1	x
1	1	0	x	1

Step 2:
Using K map, find the boolean expression for J & K in terms of T.

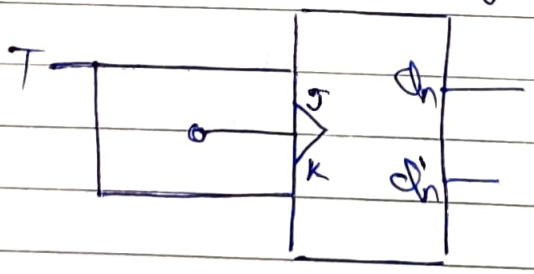
T \ Q_n	0	1
0		x
1	1	x

$J = T$

T \ Q_n	0	1
0	x	
1	x	1

$K = T$

Step 3:
Construct the circuit diagram for the conversion of J-K flip-flop into T flip flop



Logic Diagram

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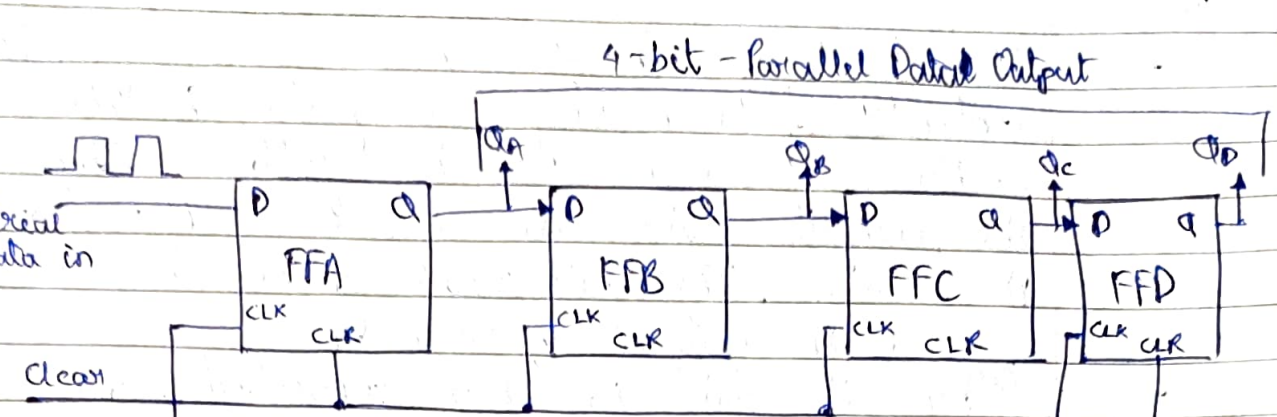
4.)



4 bit serial-in to parallel (SIPO) Shift Register:

→ The operation is as follows. Lets assume that all flip-flops (FFA to FFD) have just been RESET (CLEAR input) & that all the outputs Q_A to Q_D are at logic level "0" i.e no parallel data output.

→ If a logic "1" is connected to DATA input pin of FFA then on 1st clock pulse the output of FFA & then on first clock pulse the output of FFA & the resulting Q_A will be set HIGH to logic "1" with all the other outputs still remaining Low at logic "0". Assume now that the DATA input pin of FFA has returned LOW again to logic "0" giving us one data pulse or 0-1-0.

→ The second clock pulse will change the output FFA to logic "0" & the output FFB & Q_B HIGH to logic "1" as its input D has logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_B.

→ When the third clock pulse arrives the logic "1" value moves to the output of FFC (Q_C) & so on until the arrival of fifth clock clock pulse which set all the output Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level

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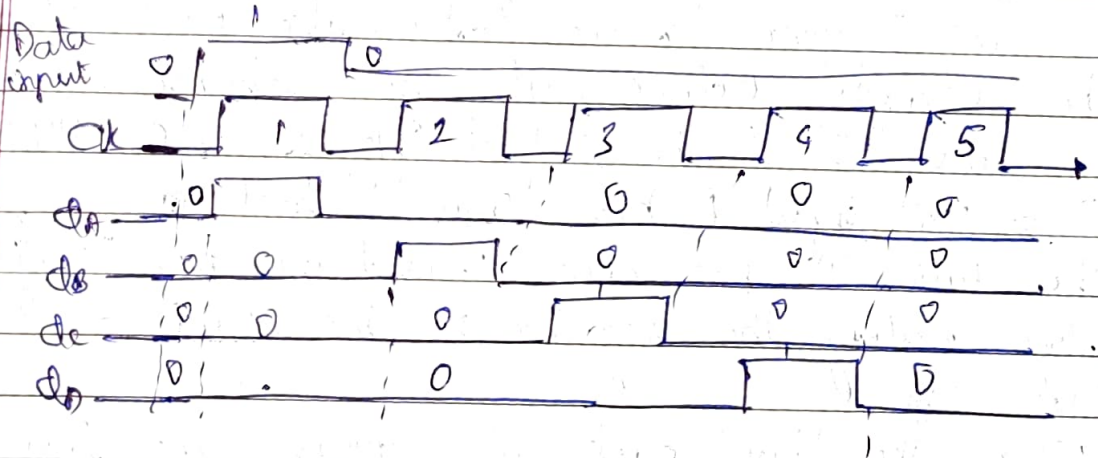
4.)

→ The effect of each clock pulse is to shift the data contents of each stage one pulse to the right, & this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the output of Q_A to Q_D

→ Then the data has been converted from a serial data input signal to a parallel data output. The truth table & following waveforms show the propagation of the logic "1" through the register from left to right as follows:

Basic data movement through A shift register:

Clock pulse No	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0



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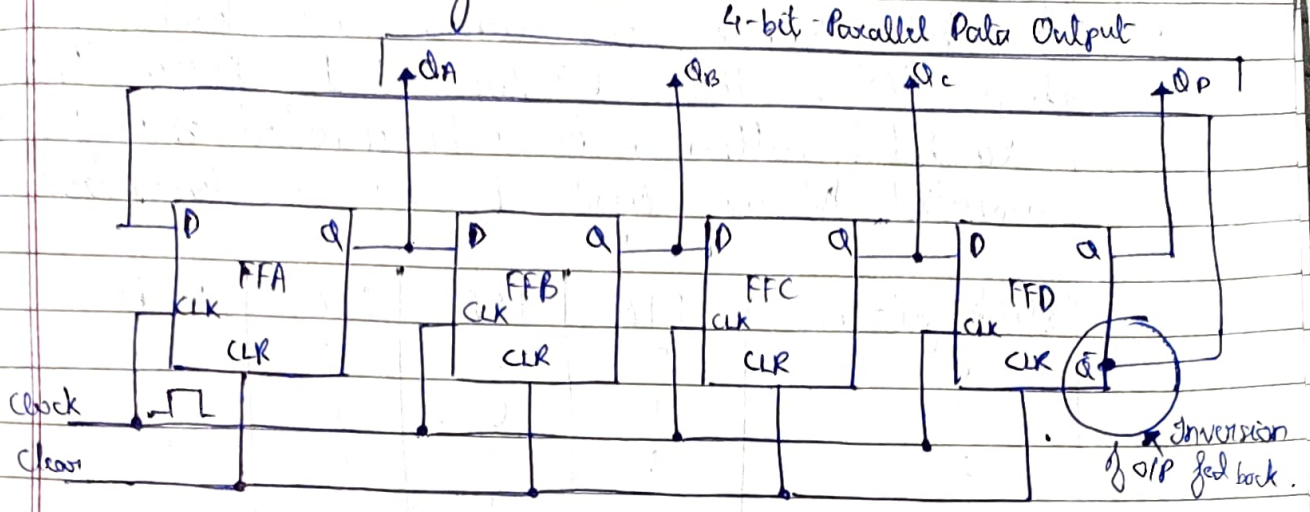
4-) 4-bit Johnson Ring Counter.



→ The Johnson Ring counter or Twisted ring counter is another shift register with feedback exactly the same as the standard Ring Counter, except that the inverted output $\bar{Q}$ of the last flip flop is now connected back to the input D of the first flip flop.

→ The main advantage of this type of ring counter is that it only needs half the number of flip flops compared to standard ring counter then its modulo number is halved. "So a n-stage" Johnson counter will circulate a single data bit giving sequence of 2n different states and can therefore be considered as a "mod-2n counter".

→ 4 bit Johnson ring counter: This inversion of Q before it is fed back to input D causes the counter to "count" in a different way. Instead of counting through a fixed set of patterns like normal ring counter such as for a 4 bit counter, "0001" (1), "0010" (2), "0100" (4), "1000" (8) & repeat, the Johnson counter counts up & then down as the initial logic "1" passes through it to the right replacing the preceding logic.

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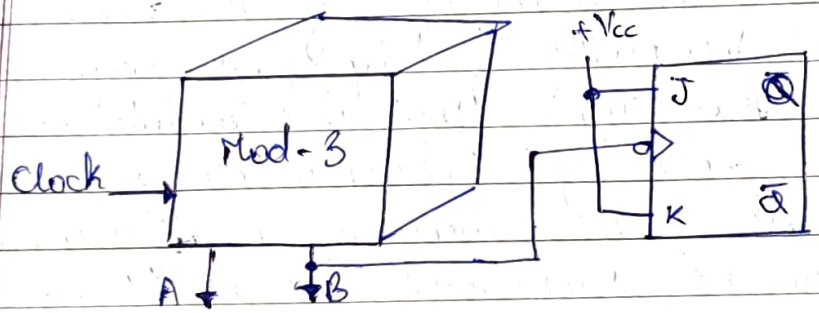
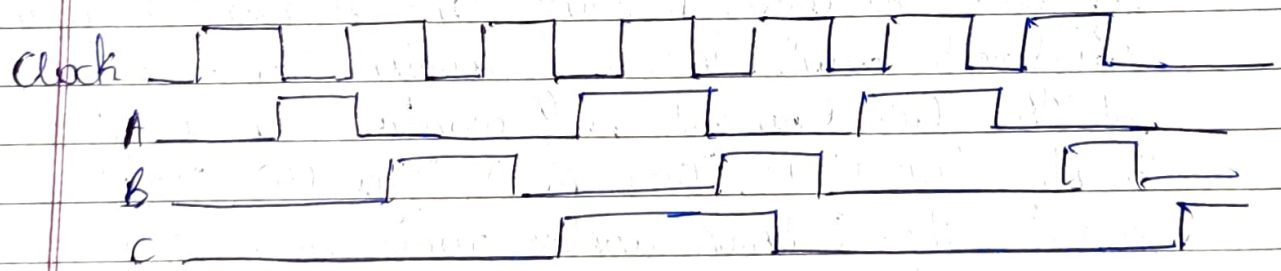
→ A 4-bit Johnson ring counter passes blocks of four logic "0" & then 4 logic "1" thereby producing an 8 bit pattern. As the inverted op $\bar{Q}$ is connected to the input D, this is demonstrated below.

Clock pulse no	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

5)



(a) 3 x 2 Mod-6 counter



(b) Waveforms

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5) If we consider a basic flip-flop to be a mod-2 counter, we see that a mod-4 counter (2 flip-flops in series) is simply 2 mod 2-counters in series. Similarly, a mod-8 counter is simply a 2×2×2 connection & so on. Thus a great number of higher-modulus counters can be formed by using the product of any number of lower-modulus counters. For instance, suppose that we connect a flip-flop at the B output of the mod-3 counters, the result is a (3×2=6) mod-6 counter as shown in figure. The output of the single flip-flop is labeled C. Notice that it is a symmetrical waveform & it also has a frequency of one-sixth that of the input clock. Also, this can no longer be considered a synchronous counter since flip-flop C is triggered by flip-flop B, that is, the flip flop do not all changes states in synchronism with the clock.