A

Project Report

on

"Implementation of a boolean function using **8:1 MULTIPLEXER"**

Submitted by

by

Sumeet P Bafna (USN: 2GI19CS157)
Venkatesh Dhongadi (USN: 2GI19CS175)
Vivek Jadhav (USN: 2GI19CS185)
Vivek Valagadde (USN: 2GI19CS186)

Department of Digital Electronics

KLS Gogte Institute of Technology,

Udyambag, Belgaum - 590008, Karnataka, India

THEORY:

- Multiplexer is a combinational circuit that is one of the most widely used in digital design.
- The multiplexer is a data selector which gates one out of several inputs to a single o/p. It has n data inputs & one o/p line & m select lines where $2^m = n$ shown in fig a.
- Depending upon the digital code applied at the select inputs one out of n data input is selected & transmitted to a single o/p channel.
- Normally strobe (G) input is incorporated which is generally active low which enables the multiplexer when it is LOW. Strobe i/p helps in cascading.
- IC 74151A is an 8: 1 multiplexer which provides two complementary outputs Y & Y. The o/p Y is same as the selected i/p & Y is its complement. The n: 1 multiplexer can be used to realize a m variable function. ($2^m = n$, m is no. of select inputs)

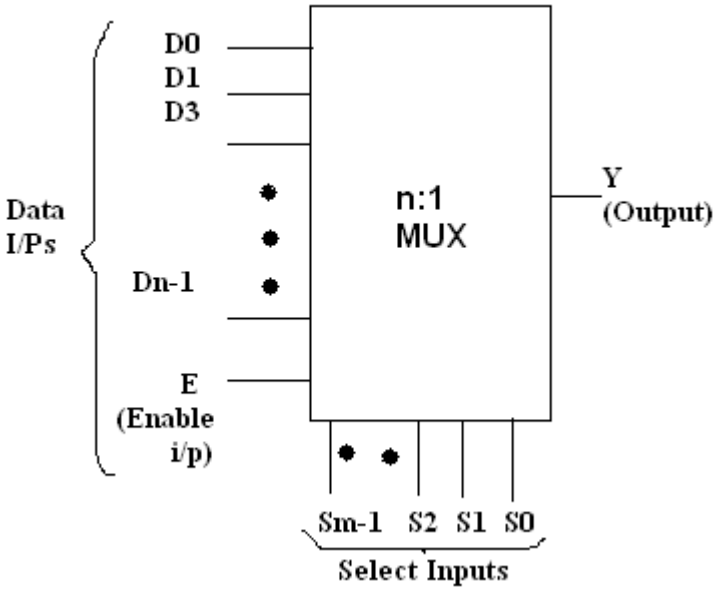


Fig. a Block diagram of n:1 MUX

Necessity of multiplexers:

- In most of the electronic systems, the digital data is available on more than one line. It is necessary to route this data over a single line.
- Under such circumstances we require a circuit which selects one of the many inputs at a time.
- This circuit is nothing else but a multiplexer, which has many inputs, one output & some select inputs.
- Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections.

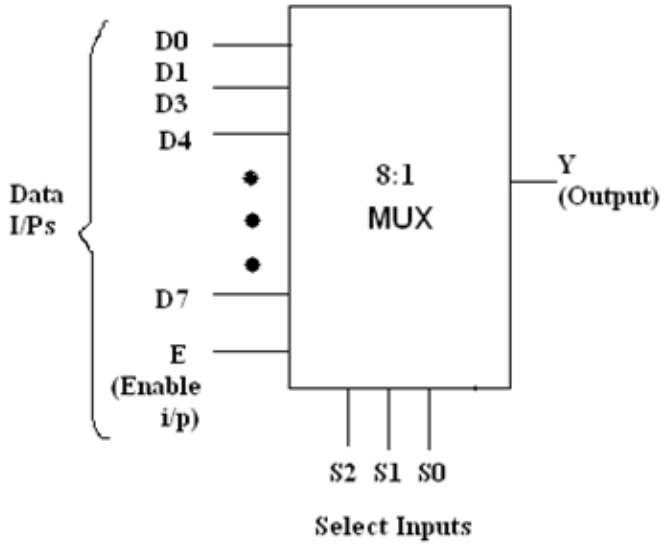
Types of MUX:

1. 2:1 MUX 2. 4:1 MUX 3) 8:1 MUX

4. 16:1 MUX 5. 32:1 MUX

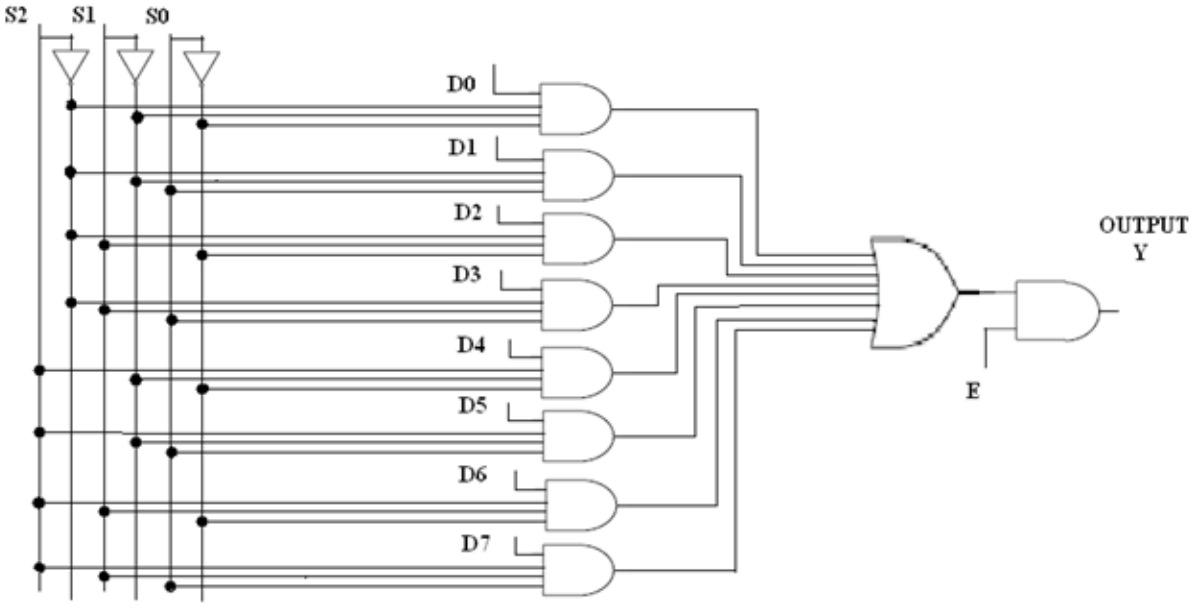
8:1 Multiplexer:

It has eight data inputs D0 to D7, three select inputs S0 to S2, an enable input and one output.



Enable	Select Inputs			Output
E	S2	S1	S0	Y
0	×	×	×	0
1	0	0	0	D0
1	0	0	1	D1
1	0	1	0	D2
1	0	1	1	D3
1	0	0	0	D4
1	0	0	1	D5
1	0	1	0	D6
1	0	1	1	D7

Fig. Block diagram of n: 1 MUX Fig. ***Truth Table of 8:1 MUX***



$$Y = E.[\overline{S2}\ \overline{S1}\ \overline{S0}\ D0 + \overline{S2}\ \overline{S1}\ S0\ D1 + \overline{S2}\ S1\ \overline{S0}\ D2 + \overline{S2}\ S1\ S0\ D3 + S2\ \overline{S1}\ \overline{S0}\ D4 + S2\ \overline{S1}\ S0\ D5 + S2\ S1\ \overline{S0}\ D6 + S2\ S1\ S0\ D7]$$

Problem Statement:

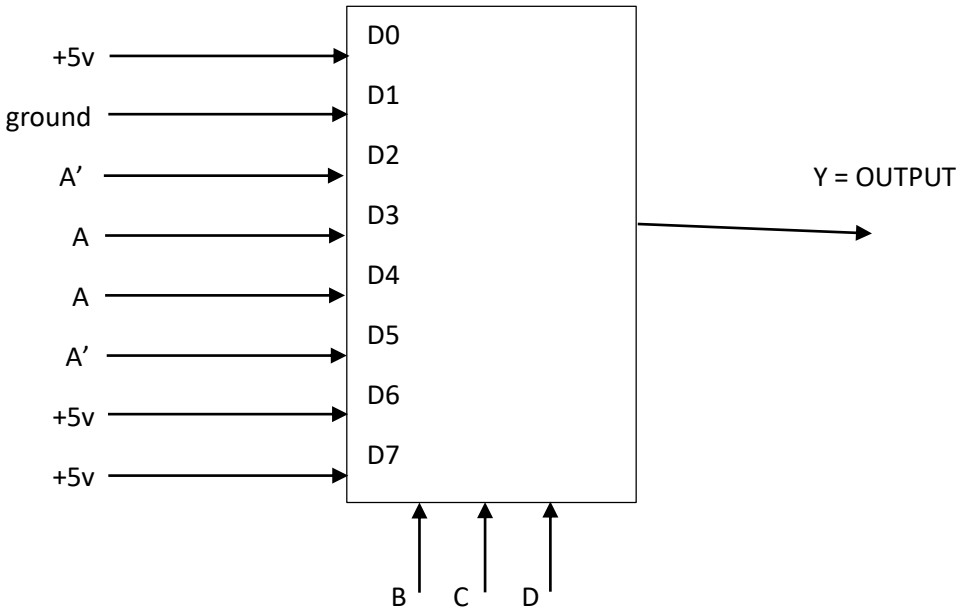
Implementation of 4-variable Boolean Function using 8:1 Multiplexer by using IC 74LS151(8:1 Mux). F (A, B, C, D) =Σm(0,2,5,6,7,8,11,12,14,15)

Solution:

Taking *A* as MEV

	D0	D1	D2	D3	D4	D5	D6	D7
A=0	0	1	2	3	4	5	6	7
A=1	8	9	10	11	12	13	14	15
	1	0	$\bar{A}$	A	A	$\bar{A}$	1	1

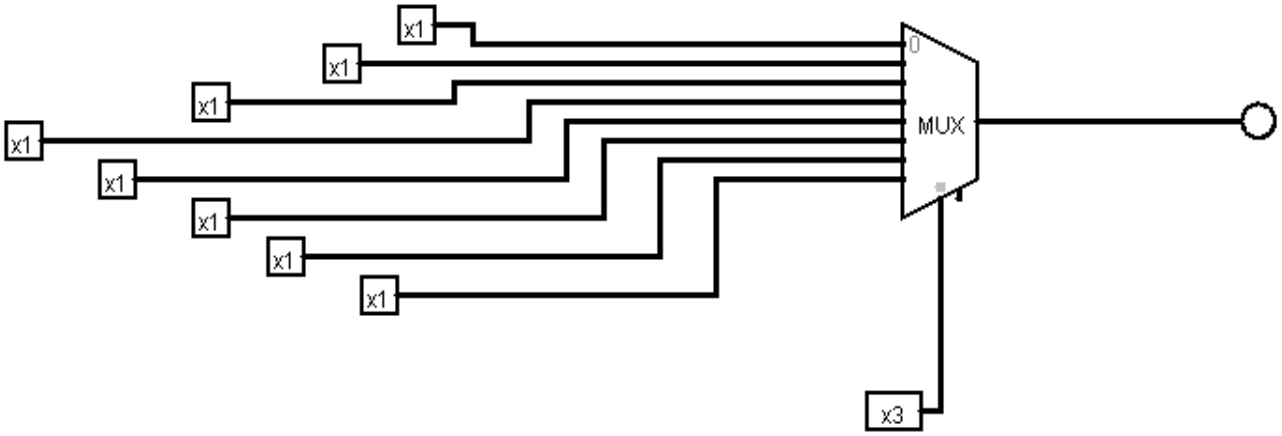
Diagram of multiplexer:



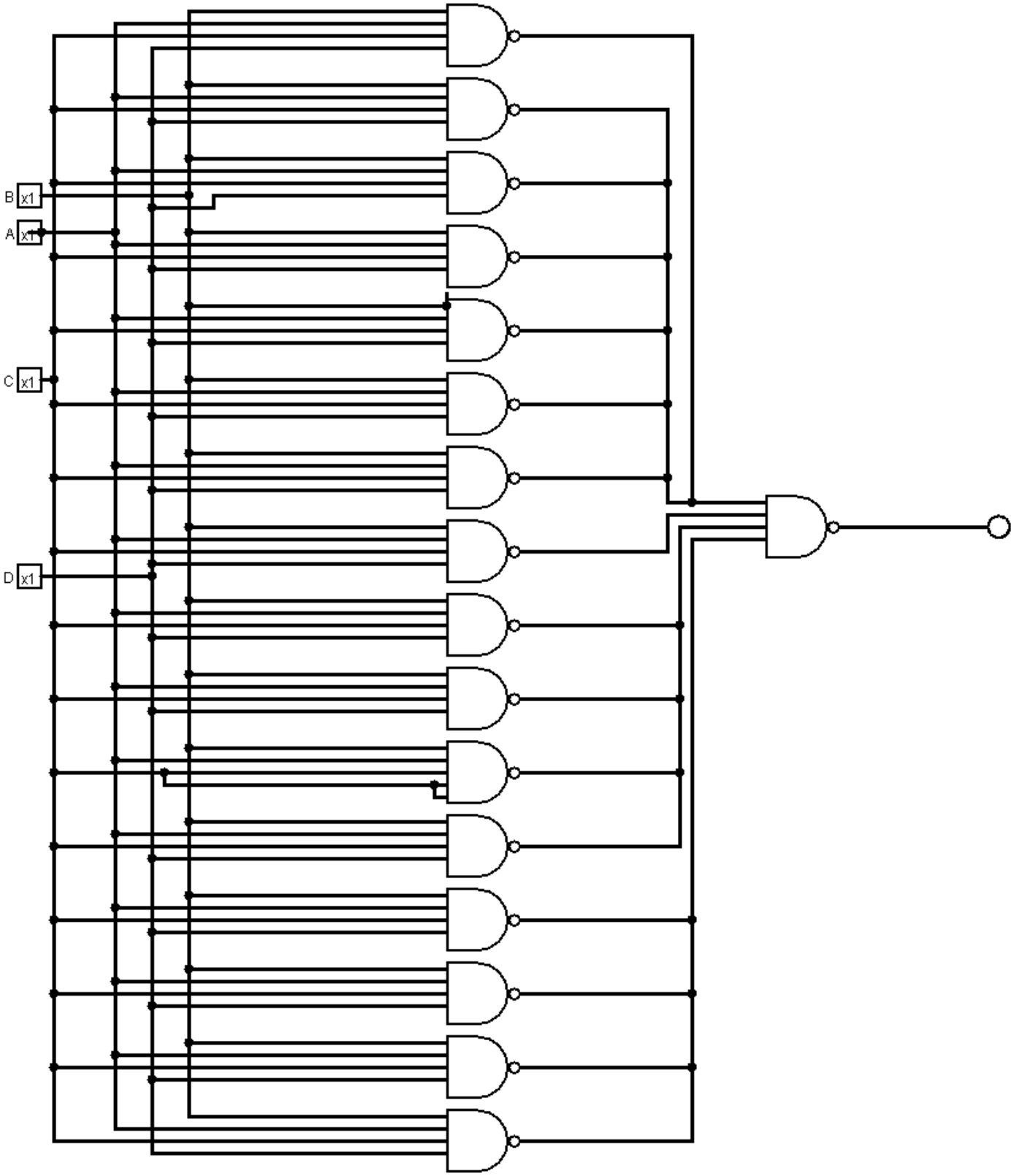
Truth table for the given sum:

A	B	C	D	Output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

REALIZATION:



LOGIC DIAGRAM:



Conclusion:

SOP expression can be successfully implemented by 8 : 1 multiplexer as show above by taking any one of the variable as map entered variable (MEV) .Multiplexer can also be demonstrated successfully by designing a logic circuit as show above and also the output can be verified for different input combinations

References:

- Donald P Leach, Albert Paul Malvino and Goutam Saha: Digital Principles and Applications, 7th Edition and onwards, Tata McGraw Hill, 2011.
- https://www.google.co.in/