8-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR
WITH AUTO-DIRECTION SENSING AND ±15-kV ESD PROTECTION

Check for Samples: TXB0108

## FEATURES

- **1.2 V to 3.6 V on A Port and 1.65 to 5.5 V on B Port (V_{CCA} ≤ V_{CCB})**
- **V_{CC} Isolation Feature − If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State**
- **OE Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 4-µA Max I_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **A Port**
    - **2000-V Human-Body Model (A114-B)**
    - **1000-V Charged-Device Model (C101)**
  - **B Port**
    - **±15-kV Human-Body Model (A114-B)**
    - **±8-kV Human-Body Model (A114-B) (YZP Package Only)**
    - **1000-V Charged-Device Model (C101)**

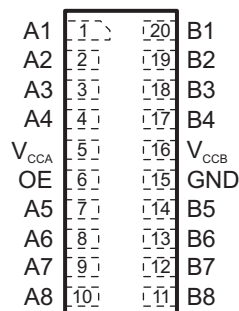## APPLICATIONS

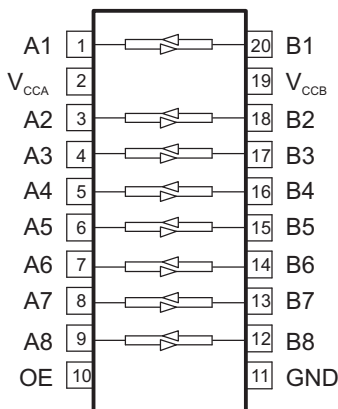- **Handset, Smartphone, Tablet, Desktop PC**

GXY OR ZXY PACKAGE
(BOTTOM VIEW)
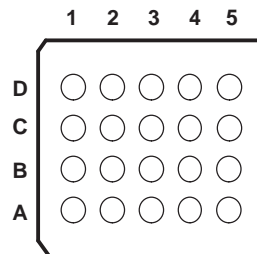
TERMINAL ASSIGNMENTS
(20-Ball GXY/ZXY Package)

	1	2	3	4	5
D	V_{CCB}	B2	B4	B6	B8
C	B1	B3	B5	B7	GND
B	A1	A3	A5	A7	OE
A	V_{CCA}	A2	A4	A6	A8

DQS PACKAGE
(TOP VIEW)

A1	1	20	B1
A2	2	19	B2
A3	3	18	B3
A4	4	17	B4
V_{CCA}	5	16	V_{CCB}
OE	6	15	GND
A5	7	14	B5
A6	8	13	B6
A7	9	12	B7
A8	10	11	B8

PW PACKAGE
(TOP VIEW)

A1	1	20	B1
V_{CCA}	2	19	V_{CCB}
A2	3	18	B2
A3	4	17	B3
A4	5	16	B4
A5	6	15	B5
A6	7	14	B6
A7	8	13	B7
A8	9	12	B8
OE	10	11	GND

RGY PACKAGE
(TOP VIEW)

A1   B1

V_{CCA}	2	19	V_{CCB}
A2	3	18	B2
A3	4	17	B3
A4	5	16	B4
A5	6	15	B5
A6	7	14	B6
A7	8	13	B7
A8	9	12	B8

10   11

OE   GND
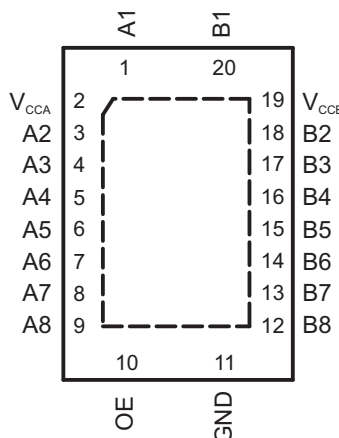
YZP PACKAGE
(BALL SIDE VIEW)
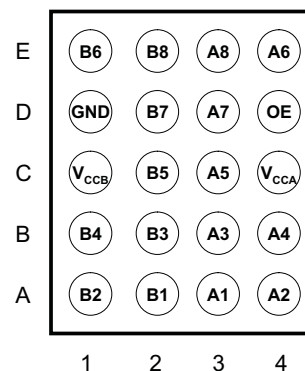
Note: For the RGY package, the exposed center thermal pad must be connected to ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0101 is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Table 1. ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	TXB0108RGYR	YE08
	SON – DQS	Reel of 2000	TXB0108DQSR	5MR
	TSSOP – PW	Reel of 2000	TXB0108PWR	YE08
	VFBGA – GXY	Reel of 2500	TXB0108GXYR	YE08
	VFBGA – ZXY (Pb-free)	Reel of 2500	TXB0108ZXYR	YE08
	DSBGA - YZP	Reel of 2500	TXB0108YZPR	5M

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN DESCRIPTION

PIN NUMBER			NAME	FUNCTION
PW, RGY	DQS	YZP		
1	1	A3	A1	Input/output 1. Referenced to V_{CCA}.
2	5	C4	V_{CCA}	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}.
3	2	A4	A2	Input/output 2. Referenced to V_{CCA}.
4	3	B3	A3	Input/output 3. Referenced to V_{CCA}.
5	4	B4	A4	Input/output 4. Referenced to V_{CCA}.
6	7	C3	A5	Input/output 5. Referenced to V_{CCA}.
7	8	E4	A6	Input/output 6. Referenced to V_{CCA}.
8	9	D3	A7	Input/output 7. Referenced to V_{CCA}.
9	10	E3	A8	Input/output 8. Referenced to V_{CCA}.
10	6	D4	OE	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
11	15	D1	GND	Ground
12	11	E2	B8	Input/output 8. Referenced to V_{CCB}.
13	12	D2	B7	Input/output 7. Referenced to V_{CCB}.
14	13	E1	B6	Input/output 6. Referenced to V_{CCB}.
15	14	C2	B5	Input/output 5. Referenced to V_{CCB}.
16	17	B1	B4	Input/output 4. Referenced to V_{CCB}.
17	18	B2	B3	Input/output 3. Referenced to V_{CCB}.
18	19	A1	B2	Input/output 2. Referenced to V_{CCB}.
19	16	C1	V_{CCB}	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.
20	20	A2	B1	Input/output 1. Referenced to V_{CCB}.
	—		Thermal Pad	For the RGY package, the exposed center thermal pad must be connected to ground.

Product Folder Link(s): *TXB0108*

TYPICAL OPERATING CIRCUIT
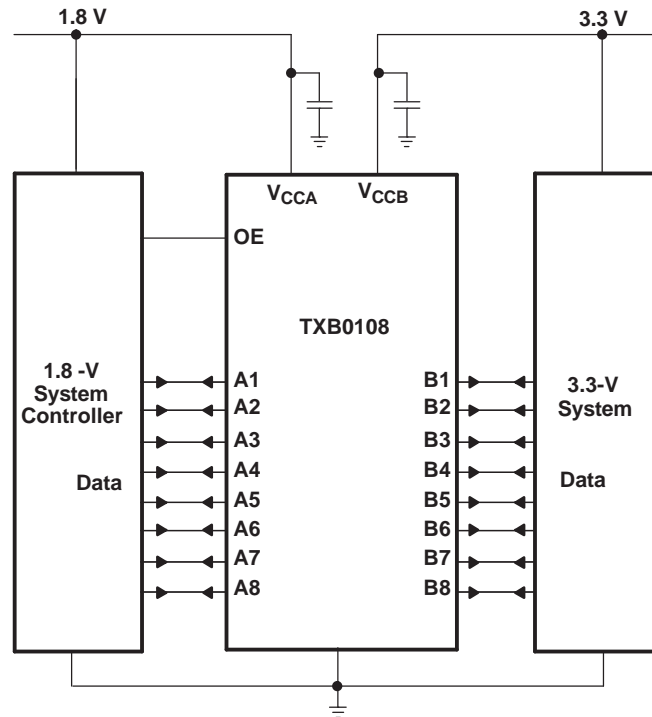
Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]	A inputs	–0.5	V_{CCA} + 0.5	V
		B inputs	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance	DQS package		TBD	°C/W
		GXY/ZXY package[4]		78	
		PW package[4]		83	
		RGY package[5]		37	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

TXB0108

Recommended Operating Conditions[1] [2]

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} x 0.65 [3]	V_{CCI}	V
		OE			V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} x 0.35 [3]	V
		OE	1.2 V to 3.6 V		0	V_{CCA} x 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

Product Folder Link(s): *TXB0108*

Electrical Characteristics[1] [2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C MIN	TYP	MAX	−40°C to 85°C MIN	MAX	UNIT
V_{OHA}		I_{OH} = −20 µA	1.2 V			1.1				V
			1.4 V to 3.6 V					V_{CCA} − 0.4		
V_{OLA}		I_{OL} = 20 µA	1.2 V			0.9				V
			1.4 V to 3.6 V						0.4	
V_{OHB}		I_{OH} = −20 µA		1.65 V to 5.5 V				V_{CCB} − 0.4		V
V_{OLB}		I_{OL} = 20 µA		1.65 V to 5.5 V					0.4	V
I_I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
I_{off}	A port		0 V	0 V to 5.5 V			±1		±2	µA
	B port		0 V to 3.6 V	0 V			±1		±2	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1		±2	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06				µA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					2	
			0 V	5.5 V					−2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4				µA
			1.4 V to 3.6 V						5	
			3.6 V	0 V					−2	
			0 V	5.5 V					2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5				µA
			1.4 V to 3.6 V						10	
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05				µA
			1.4 V to 3.6 V						5	
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3				µA
			1.4 V to 3.6 V						5	
C_I	OE		1.2 V to 3.6 V	1.65 V to 5.5 V	5				5.5	pF
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V	5				6.5	pF
	B port				8				10	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

Timing Requirements

T_A = 25°C, V_{CCA} = 1.2 V

			V_{CCB} = 1.8 V TYP	V_{CCB} = 2.5 V TYP	V_{CCB} = 3.3 V TYP	V_{CCB} = 5 V TYP	UNIT
	Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V MIN	MAX	V_{CCB} = 2.5 V ± 0.2 V MIN	MAX	V_{CCB} = 3.3 V ± 0.3 V MIN	MAX	V_{CCB} = 5 V ± 0.5 V MIN	MAX	UNIT
	Data rate			50		50		50		50	Mbps
t_w	Pulse duration	Data inputs	20		20		20		20		ns

Product Folder Link(s): TXB0108

TXB0108

Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t_w	Pulse duration	Data inputs	19		17		17		17		ns

Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t_w	Pulse duration	Data inputs	14		10		10		ns

Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

Switching Characteristics

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V TYP	V_{CCB} = 2.5 V TYP	V_{CCB} = 3.3 V TYP	V_{CCB} = 5 V TYP	UNIT
t_{pd}	A	B	9.5	7.9	7.6	8.5	ns
	B	A	9.2	8.8	8.4	8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis}	OE	A	20	17	17	18	ns
		B	20	16	15	15	
t_{rA}, t_{fA}	A-port rise and fall times		4.1	4.4	4.1	3.9	ns
t_{rB}, t_{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
$t_{SK(O)}$	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max data rate			20	20	20	20	Mbps

Product Folder Link(s): *TXB0108*

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	ns
		B	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.2	8.4	0.8	7.6	0.5	7.1	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	ns
		B	6.1	33.9	5.2	23.7	5	19.9	5	17.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

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TXB0108

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.4	1	5.3	0.9	4.7	ns
	B	A	1	7	0.6	5.6	0.3	4.4	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis}	OE	A	5	16.9	4.9	15	4.5	13.8	ns
		B	4.8	21.8	4.5	17.9	4.4	15.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	4.9	0.8	4	ns
	B	A	0.5	5.4	0.2	4	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis}	OE	A	4.5	13.9	4.1	12.4	ns
		B	4.1	17.3	4	14.4	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

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Product Folder Link(s): *TXB0108*

Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V_{CCB}							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns, OE = V_{CCA} (outputs enabled)	9	8	7	7	7	7	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		35	26	27	27	27	27	28	
	B-port input, A-port output		26	19	18	18	18	20	21	
C_{pdA}	A-port input, B-port output	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	

Submit Documentation Feedback 9

Product Folder Link(s): *TXB0108*

TXB0108

PRINCIPLES OF OPERATION

Applications

The TXB0108 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

Architecture

The TXB0108 architecture (see Figure 1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0108 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at V_{CCO} = 1.2 V to 1.8 V, 50Ω at V_{CCO} = 1.8 V to 3.3 V and 40Ω at V_{CCO} = 3.3 V to 5 V.
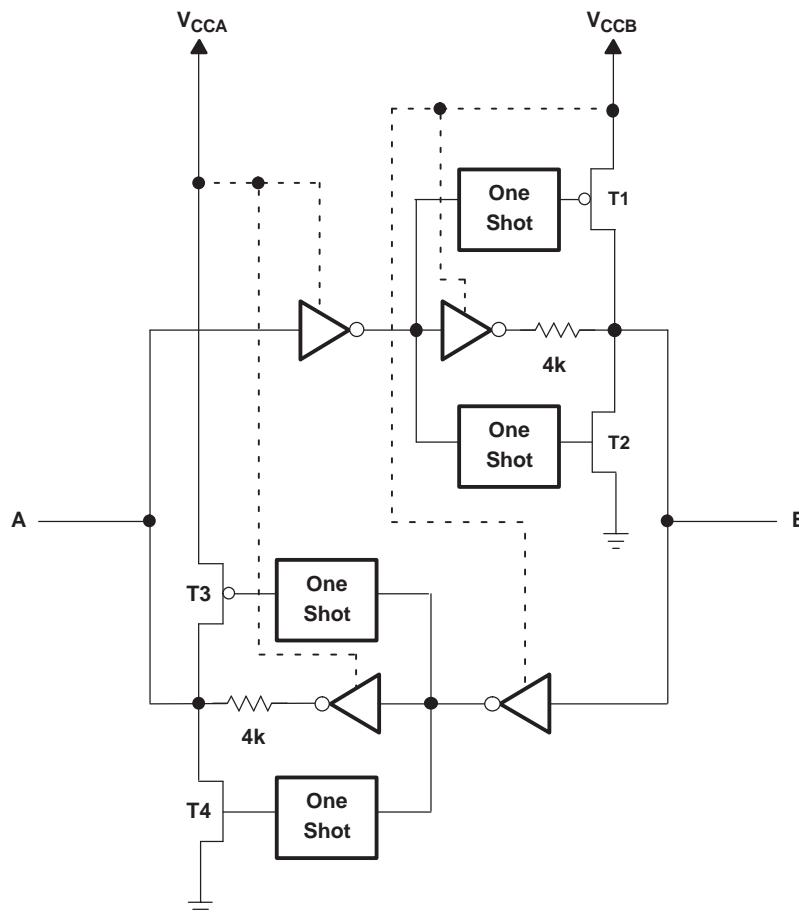
Figure 1. Architecture of TXB0108 I/O Cell

Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0108 are shown in Figure 2. For proper operation, the device driving the data I/Os of the TXB0108 must have drive strength of at least ±2 mA.

Product Folder Link(s): *TXB0108*
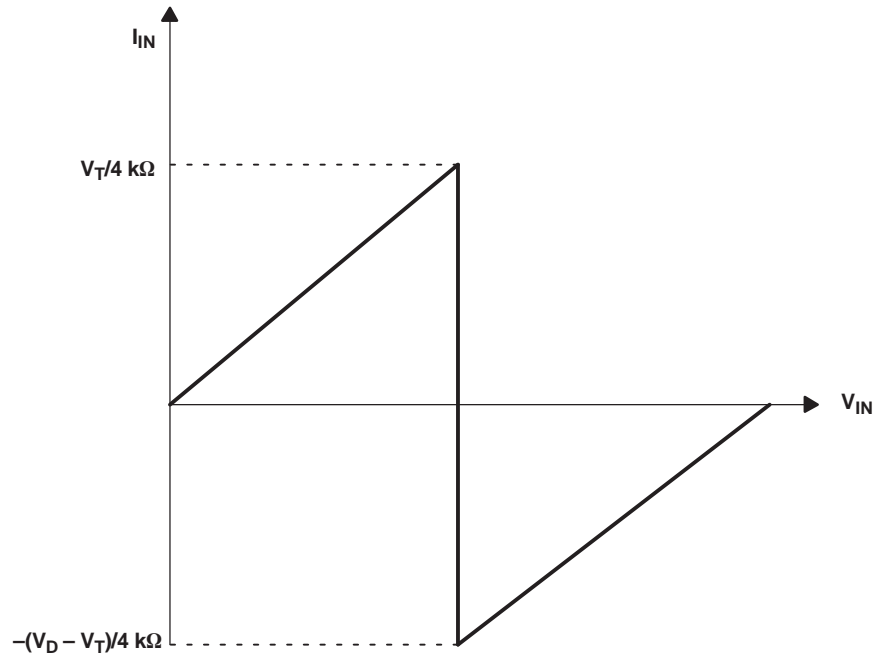
A. V_T is the input threshold voltage of the TXB0108 (typically $V_{CCI}/2$).

B. V_D is the supply voltage of the external driver.

Figure 2. Typical I_{IN} vs V_{IN} Curve

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0108 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0$ V).

Enable and Disable

The TXB0108 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistors on I/O Lines

The TXB0108 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0108 have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0108.

For the same reason, the TXB0108 should not be used in applications such as I^{2}C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

PARAMETER MEASUREMENT INFORMATION
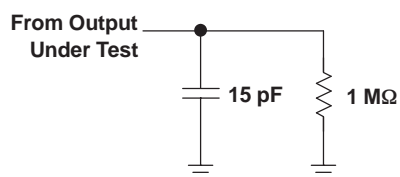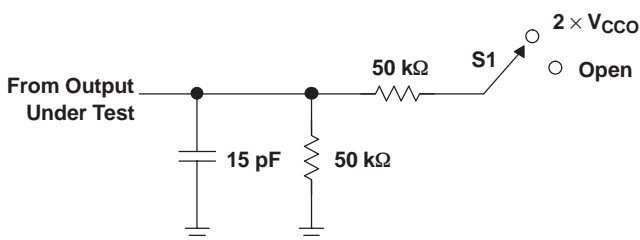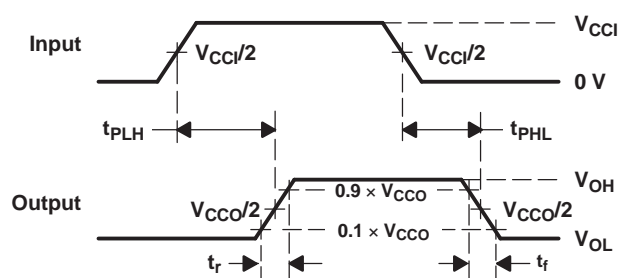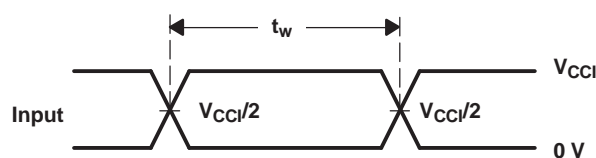
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuits and Voltage Waveforms

Product Folder Link(s): *TXB0108*

REVISION HISTORY

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
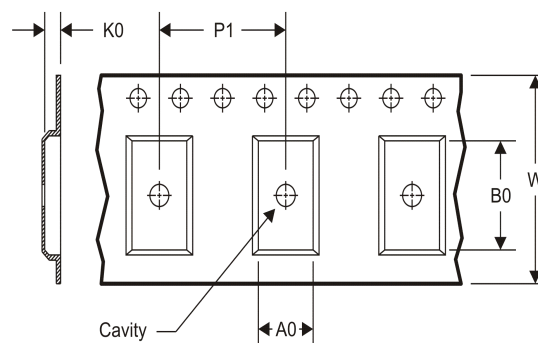
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0108PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TXB0108RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TXB0108RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TXB0108YZPR	DSBGA	YZP	20	3000	180.0	8.4	1.99	2.49	0.56	4.0	8.0	Q1
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.8	3.3	1.0	4.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0108PWR	TSSOP	PW	20	2000	346.0	346.0	33.0
TXB0108RGYR	VQFN	RGY	20	3000	346.0	346.0	29.0
TXB0108RGYR	VQFN	RGY	20	3000	355.0	350.0	50.0
TXB0108YZPR	DSBGA	YZP	20	3000	210.0	185.0	35.0
TXB0108ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	340.5	338.1	20.6

ZXY (S−PBGA−N20)　　　　　　　　PLASTIC BALL GRID ARRAY
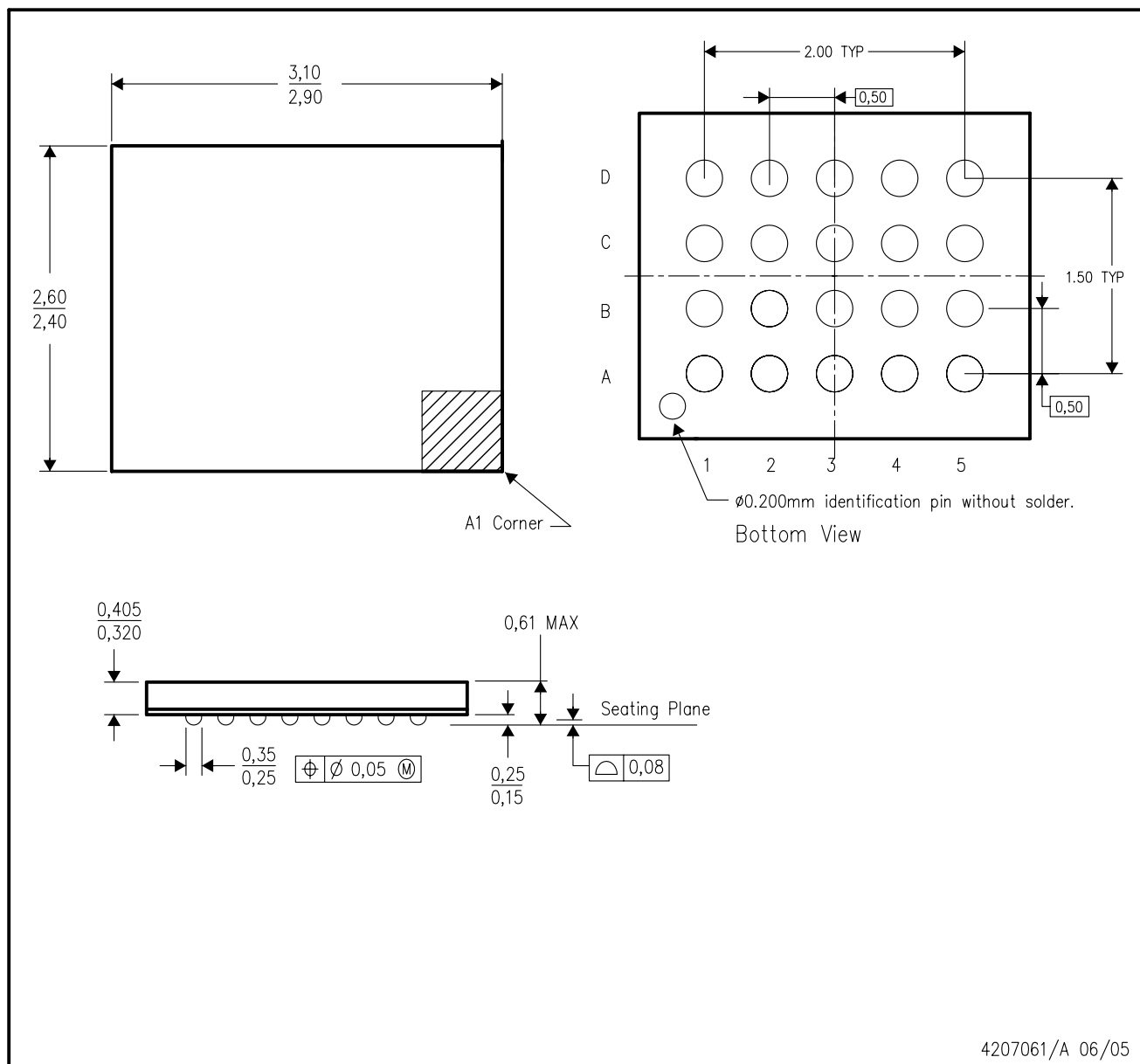
3,10
2,90

2,60
2,40

A1 Corner

2.00 TYP

0,50

D

C

1.50 TYP

B

A

0,50

1　2　3　4　5

⌀0.200mm identification pin without solder.

Bottom View

0,405
0,320

0,61 MAX

Seating Plane

0,35
0,25

⌖ ⌀ 0,05 Ⓜ

0,25
0,15

⌒ 0,08

4207061/A 06/05

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　This package is a lead−free solder ball design.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65
0,30
0,19
⊕ 0,10 Ⓜ

20   11

Ⓓ 4,50
   4,30   6,60
                 6,20

0,15 NOM

Gage Plane

0°−8°

0,25

1   10

6,60
6,40

Ⓒ

0,75
0,50
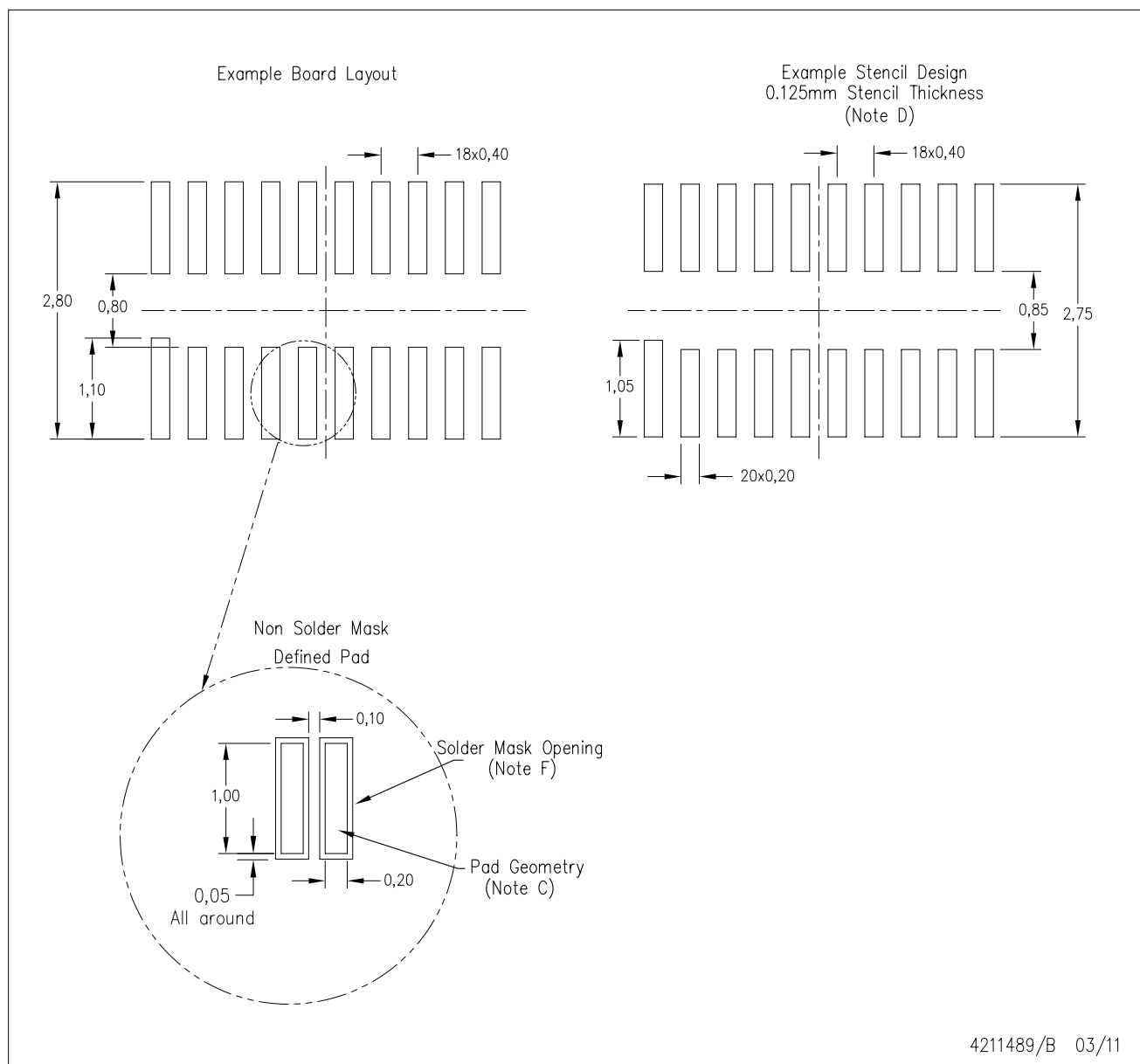
1,20 MAX

0,15
0,05

Seating Plane

⬠ 0,10
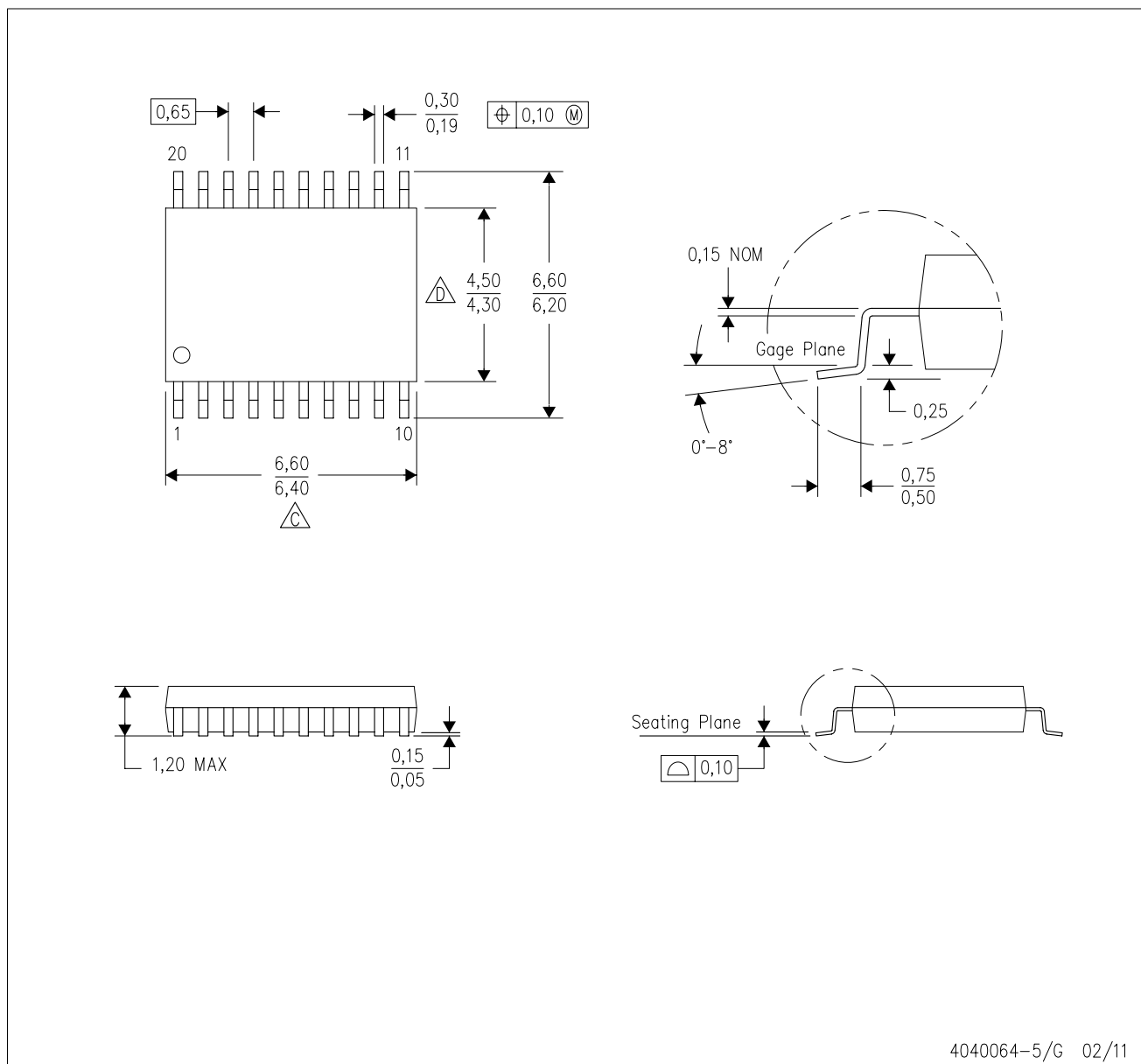
4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153
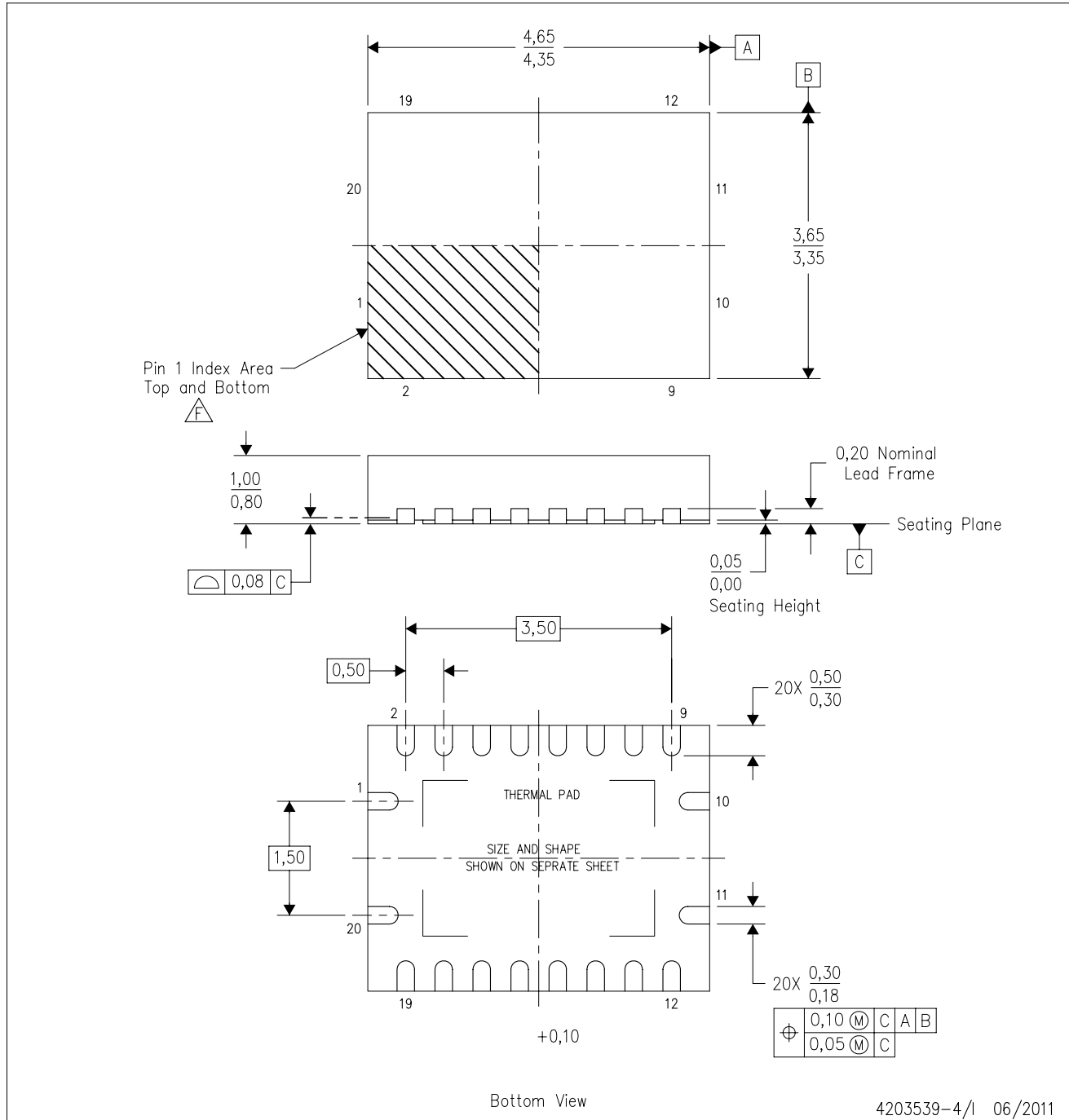
TEXAS INSTRUMENTS
www.ti.com

RGY (R-PVQFN-N20)   PLASTIC QUAD FLATPACK NO-LEAD

4203539-4/I   06/2011

Bottom View

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M-1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No-Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
              The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO-241 variation BA.

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RGY (R−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,05±0,10

3,05±0,10
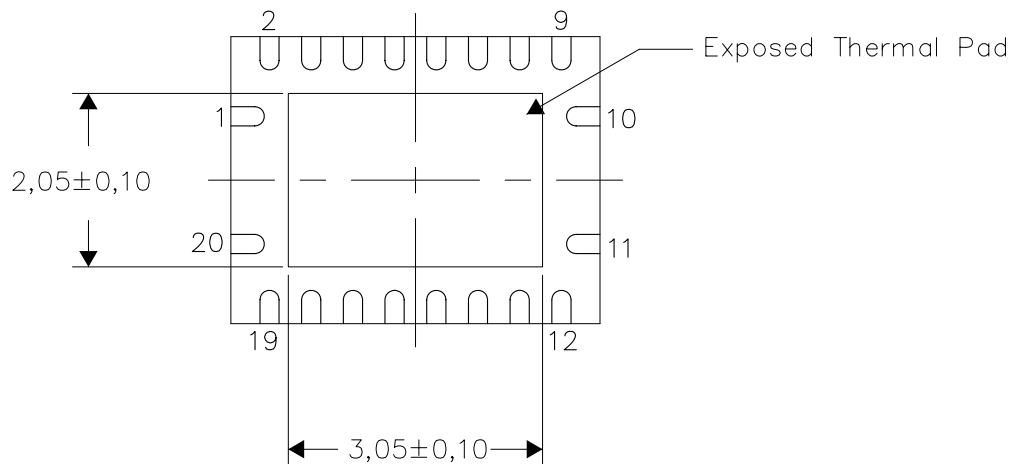
Bottom View

Exposed Thermal Pad Dimensions

4206353−4/O 11/11

NOTE: All linear dimensions are in millimeters

RGY (R—PVQFN—N20)   PLASTIC QUAD FLATPACK NO—LEAD
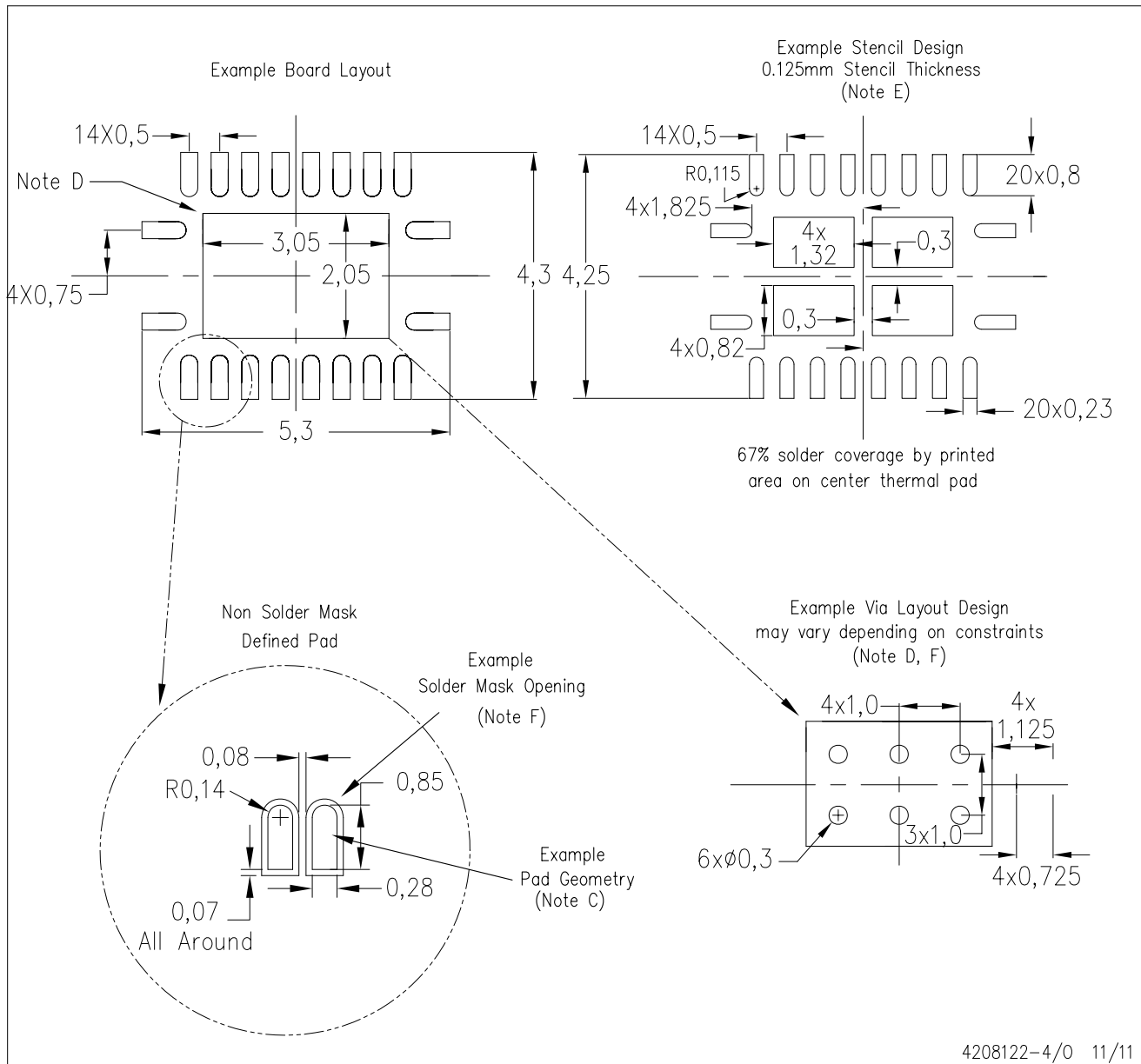
Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

14X0,5

Note D

3,05

2,05

4,3 4,25

4X0,75

5,3

14X0,5

R0,115

4x1,825

4x
1,32

0,3

20x0,8

0,3

4x0,82

20x0,23

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

Example
Pad Geometry
(Note C)

All Around

Example Via Layout Design
may vary depending on constraints
(Note D, F)

4x1,0

4x
1,125

6xØ0,3

3x1,0

4x0,725

4208122—4/0 11/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC—7351 is recommended for alternate designs.
         D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack
             QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
             for specific thermal information, via requirements, and recommended board layout.
             These documents are available at www.ti.com <http://www.ti.com>.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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DQS (R−PUSON−N20)   PLASTIC SMALL OUTLINE NO−LEAD

$\frac{4,05}{3,95}$ [A]

[B]

20   11

$\frac{2,05}{1,95}$

Pin 1 Index Area
Top and Bottom

1   10

$\frac{0,55}{0,45}$

0,10 Nominal
Lead Frame

// | 0,05 | C

Seating Plane

$\frac{0,05}{0,00}$
Seating Height

⌒ | 0,05 | C

C

3,60

0,40

$\frac{0,70}{0,60}$

19X $\frac{0,60}{0,50}$

1   10

Pin 1 Identifier
0,10 X 45°

20   11

20X $\frac{0,25}{0,15}$

⊕ | 0,07 Ⓜ | C | A | B
  | 0,05 Ⓜ | C

Bottom View
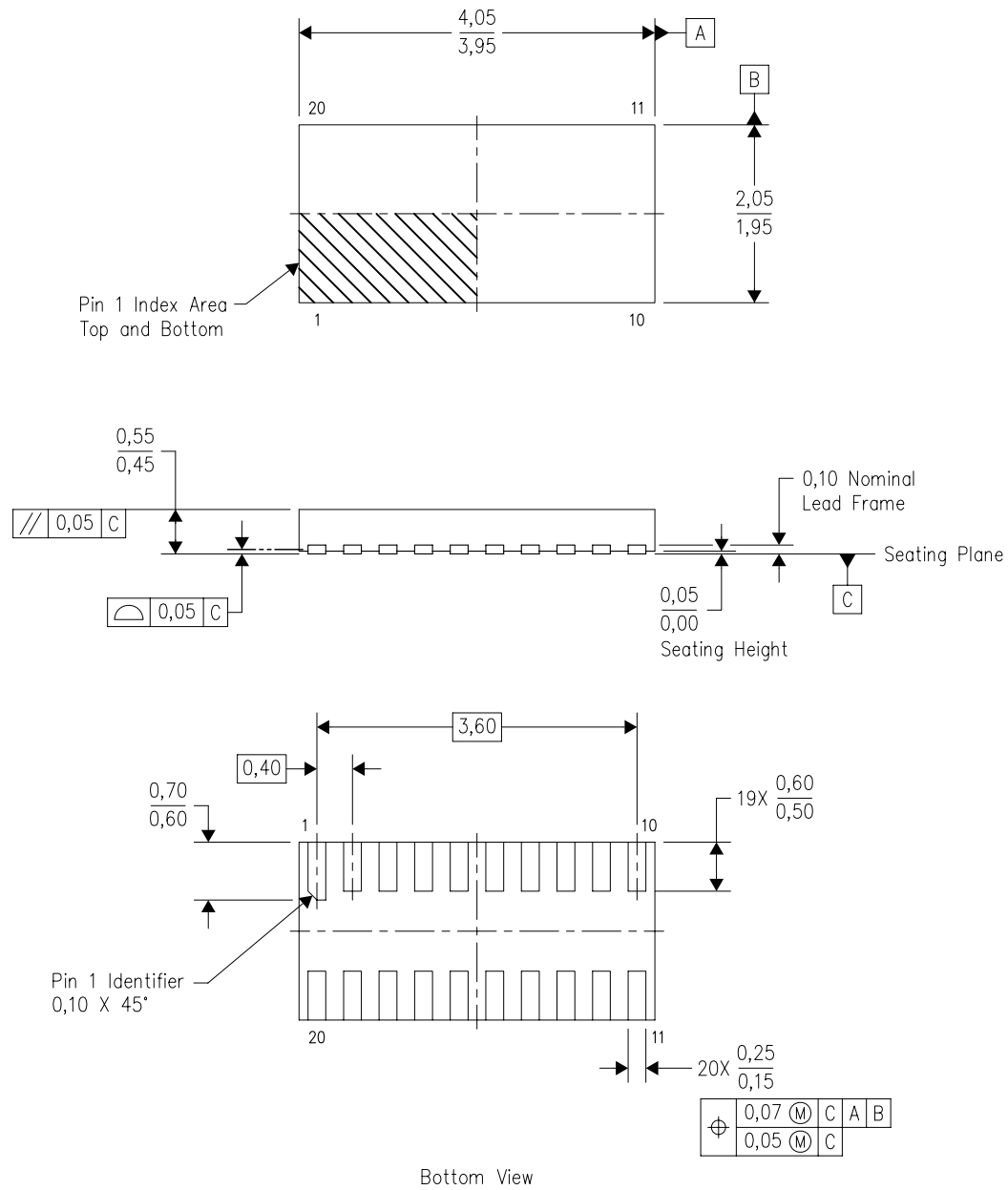
4210558/B 03/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   SON (Small Outline No−Lead) package configuration.

DQS (R–PUSON–N20)   PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

Example Stencil Design
0.125mm Stencil Thickness
(Note D)

18x0,40

18x0,40

2,80   0,80

1,10

0,85   2,75

1,05

20x0,20

Non Solder Mask
Defined Pad

0,10

Solder Mask Opening
(Note F)

1,00

Pad Geometry
(Note C)

0,05
All around

0,20

4211489/B   03/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         E.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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