PCIe215

PROGRAMMABLE DIGITAL INPUT/OUTPUT AND COUNTER/TIMER BOARD

This Instruction Manual is supplied with the PCIe215 board to provide the user with sufficient information to properly utilise the product as purchased. The information contained has been reviewed and is believed to be accurate and reliable; however **Amplicon Liveline Limited** accepts no responsibility for any problems caused by errors or omissions. Specifications and instructions are subject to change without notice.

PCIe215 Instruction Manual Part Nº 85 113 264 Issue B

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1 INTRODUCTION

1.1 The Amplicon 200 Series

The **Amplicon 200 Series** of Personal Computer based data acquisition products provide high performance, affordable hardware with user sympathetic software. The 200 Series is designed for users requiring fast or complex data I/O to the host PC and comprises a range of boards and software to handle most analog and digital signal types.

When a large scale system is required, multiple boards can be added from the 200 Series without conflict. For analog input systems, the capacity of the PC mounted hardware can be extended by external expansion panels to provide a convenient to use system with low cost per channel and maintained high performance.

1.2 Features of the PCIe215

The PCIe215 board is designed to meet stringent performance requirements and ease of use.

- 48 bit flexible, programmable digital I/O.
- Six 16-bit, 10MHz counter/timers with on board 10MHz crystal oscillator timing source, each with six programmable counter modes.
- Crystal clock/divider with 5 rates, independently software selectable for each counter/timer clock input.
- Interrupt controlled operations, with the facility for interrupts to be generated from on board timers or one of four external signals.
- PCIe Bus version 2.1 Plug and play interface.
- Device driver software compatible with Windows.
- VB.NET, C#.NET, Delphi, LabVIEW, Agilent/HP VEE and Visual Basic.
- Backwards compatible with PCI215

The PCIe215 is a plug-in, multi-function digital I/O board. The board can be used on any PC that supports the PCI bus version 2.1. The card is supplied with Windows 2000 onwards compatible device drivers.

1.3 General Description

The PCIe215 is a PCIe plug-in board which provides 48 bits of parallel digital input/output and six 16 bit counter/timers. The board can be used on any PC that supports the PCIe bus version 2.1. The card is supplied with Windows compatible device drivers and LabVIEW drivers.

1.3.1 Backwards Compatibility

The PCIe215 supports all relevant features of the earlier PCI bus product, the PCI215.

1.3.2 The Software

The PCIe215 is supplied with the Amplicon DVD-ROM. This contains all the software for the card, and is documented in the Amplicon AMPDIO software manual. This manual can be accessed when the software is installed from the DVD.

1.4 What the Package Contains

⚠ CAUTION

Some of the components on the board are susceptible to electrostatic discharge, and proper handling precautions should be observed. As a minimum, an earthed wrist strap must be worn when handling the PCIe215 outside its protective bag. Full static handling procedures are defined in British Standards Publication BSEN100015/BSEN100015-1:1992.

When removed from the bag, inspect the board for any obvious signs of damage and notify Amplicon if such damage is apparent. Do not plug a damaged board into the host computer. Keep the protective bag for possible future use in transporting the board.

The package as delivered from **Amplicon Liveline Ltd**. contains:-

1. The plug-in card as ordered, in a protective bag. The PCIe215 is identified by the type number printed on the board.

   PCIe215 PCIe Bus Digital input/output and counter timer card Part Nº 96 113 263

2. Distribution software and manual on DVD Part Nº 85 040 046

Any additional accessories (mating connectors, software etc.) may be packed separately.

1.5 The Amplicon Warranty Covering the PCIe215

This product is covered by the warranty as detailed in the Terms and Conditions stated on the web site at www.amplicon.com.

1.6 Contacting Amplicon Liveline Limited for Support or Service

The PCIe215 boards are designed and manufactured by Amplicon Liveline Ltd and maintenance is available throughout the supported life of the product.

1.6.1 Technical Support

Should this product appear defective, please check the information in this manual and the Ampdio32manual appropriate to the program in use to ensure that the product is being correctly applied.

If a problem persists, please request Technical Support in one of the following ways:

Telephone:	UK	01273 944 835
Fax:	UK	01273 570 215
Email:		support@amplicon.com
Web:		www.amplicon.com

It will assist the support engineer if you have the following information available when you call:

Date of purchase
Your account number or postcode
The Operating System you are running under
The specification of your computer
The nature of your problem and the results of any tests you have conducted
The version number of your Amplicon DVD-ROM.

1.6.2 Repairs

If the PCIe215 requires repair then please return the goods enclosing a repair order detailing the nature of the fault. If the PCIe215 is still under warranty, there will be no repair charge unless any damage is a consequence of improper use.

For traceability when processing returned goods, a Returned Materials Authorisation (RMA procedure is in operation. Before returning the goods, please request an individual RMA number by contacting Amplicon Technical Support by telephone or fax on the above numbers. Give the reason for the return and, if the goods are still under warranty, the original invoice number and date. Repair turnaround time is normally five working days but the Service Engineers will always try to co-operate if there is a particular problem of time pressure.

Please mark the RMA number on the outside of the packaging to ensure that the package is accepted by the Goods Inwards Department.

Address repairs to:

The Service Department
AMPLICON LIVELINE LIMITED
Centenary Industrial Estate
Brighton, East Sussex
BN2 4AW
England

2 GETTING STARTED

2.1 General Information

The PCIe215 cards are Plug and Play compatible and come complete with all the software required to install and operate the card in any PCIe compliant host PC running under Windows and allow full card functionality.

2.2 Host Computer Requirements

When installing one or more PCIe215 series boards, ensure that the host computer has sufficient capacity. Take into account other boards or adapters that may be installed in the computer when assessing physical space, address space in the I/O map, interrupt levels and the power requirements.

This board is suitable for use in any PC compatible computer that can provide a single PCIe Bus x1 lane slot, with sufficient space for a half-length card.

The computer must run under one of the following operating systems: Windows 2000 onwards.

2.3 Installing the Board

ENSURE THAT THE POWER TO THE COMPUTER IS SWITCHED OFF BEFORE INSTALLING OR REMOVING ANY EXPANSION BOARD. OBSERVE HANDLING PRECAUTIONS NOTED IN SECTION 1.4.

REPAIR OF DAMAGE CAUSED BY MIS-HANDLING IS NOT COVERED UNDER THE AMPLICON WARRANTY.

DO NOT MAKE ANY MODIFICATIONS TO A BOARD THAT IS ON EVALUATION

Please refer to the manufacturer's hardware manual supplied with the PC for instructions on how to remove the cover and install devices into a PCIe slot. The PCIe215 may be installed in any available position in the machine provided that there is no restriction specified for that location by the computer manufacturer.

The PCIe215 board is a Plug and Play device. The installation software supplied will handle the configuration of the card.

When the board is physically installed in the PC, and the PC is rebooted, The Windows operating system will detect new hardware and prompt for installation of the device drivers.

2.4 Software Installation

You will be guided through installation of the card automatically when you run the AMPDIO.EXE set-up program from the Amplicon DVD-ROM.

2.5 Application Software

Example application software, including source code for the applications and the DLL are installed by the AMPDIO.EXE set-up program. When the set-up program is run and software is extracted to

a suitable directory (e.g. C:\AMPLICON\AMPDIO), the examples and DLL source code can be found in subdirectories off this directory.

2.6 Digital I/O

This digital I/O board features an FPGA configured to provide the functions of two uncommitted 82C55 Programmable Peripheral Interface (PPI) chips which can be configured by user software to operate in a variety of modes.

The digital I/O facility of the PCIe215 provides 48 lines in two clusters of three 8 bit ports, labelled:
DIO Port XA0 - XA7, DIO Port XB0 - XB7 and DIO Port XC0 - XC7;
DIO Port YA0 - YA7, DIO Port YB0 - YB7 and DIO Port YC0 - YC7.

Each cluster is further divided into two groups of 12 bits each, group A comprising the 8 bits of port A and the high order 4 bits of port C, and Group B comprising the 8 bits of port B and the low order 4 bits of port C. When port C is split in this mode, note that when a half byte of data is being read from or written to port C, those four bits occupy the appropriate high or low end of a full byte, the other four bits not being used.

Full details of programming the 82C55 PPI at register level, in its various modes, are shown in the device specification in Appendix **App82C55.pdf** in the \MANUAL subdirectory on the Amplicon DVD-ROM. The three basic operating modes are summarized below.

Mode 0 (Basic I/O)

This mode is the power-up default with all ports set as input (i.e. high impedance).

In mode 0, the PPI provides simple I/O operations. No control signals are required and the ports defined as input reflect the current state of digital signals on the lines (no latching). The lines of output defined ports are set to zero on the mode change, and when a port is loaded, the outputs are latched to that value.

All 24 bits can be used for input or output arranged as any combination of two 8 bit ports and two 4 bit ports.

Mode 1 (Strobed I/O)

Mode 1 provides I/O operations on Group A and/or Group B each with a simple handshake protocol. In either group, the 4-bit port is used for status and control of the associated 8-bit port. An IRQ facility in this mode is available on the PCIe215.

Each 8-bit port can be used uni-directionally for either input or output operations, both being latched.

Mode 2 (Strobed Bi-directional I/O)

This mode of operation can be applied to group A only, and provides one 8 bit bi-directional data port and one 5 bit control and status port with IRQ facility. Both input and output operations are latched. Port B can be used in mode 0 or 1 while port A is in mode 2.

Mixed Mode

The ports of the PPI can be programmed to operate in a mixed combination of modes that in some cases leave bits of port C unused for control or status purposes. These unused bits can be programmed for use as inputs or outputs.

2.7 Counter Timers Setup & Control

The PCIe215 has two 82C54 counter timers (CTCs) which occupy clusters Z1 & Z2. Each 82C54 provides three 16-bit counter/timers which can be independently programmed to operate in any one of the six modes with BCD or Binary count functions as follows:

Mode 0 Interrupt on Terminal Count

Mode 1 Hardware Re-triggerable One-shot

Mode 2 Rate Generator

Mode 3 Square Wave

Mode 4 Software Triggered Mode

Mode 5 Hardware Triggered Strobe (Re-triggerable)

All timing operations are under the control of a crystal clock source. This source is used internally and divided down for input to the 16 bit programmable counter/timers. The clock input to the counter/timer can also be selected as an external clock source.

The counter/timer output, or by alternative selection, external triggers, provides the trigger pulses used in the modes as described above. The various interconnections are set up by the 'Counter Connections Register' under initial program control.

7	6	5	4 3	2 1 0
0	0	Z1/2 0= Z1 1= Z2	Counter Timer 00 – Counter 0 01 – Counter 1 10 – Counter 2 11 – Reserved	Clock Source 000 – CLKn 001 – 10MHz 010 – 1MHz 011 – 100kHz 100 – 10kHz 101 – 1kHz 110 – OUT n-1 111 – Ext Clock

FIGURE 2.1 GROUP Z CLOCK CONFIGURATION REGISTERS

7	6	5	4 3	2 1 0
0	0	Z1/2 0= Z1 1= Z2	Counter Timer 00 – Counter 0 01 – Counter 1 10 – Counter 2 11 – Reserved	Gate Source 000 – VCC, enabled 001 – GND, disabled 010 – GATn 011 - /OUT n-2 100 – Reserved 101 – Reserved 110 - /GATn 111 – OUT n-2

FIGURE 2.2 GROUP Z GATE CONFIGURATION REGISTERS

Full details of programming the 82C54 Counter timers at register level are shown in Appendix APP82C54.pdf in the \MANUAL subdirectory on the Amplicon DVD-ROM.

2.8 Enhanced Features

2.8.1 Enabling Enhanced features

The digital IO pins are connected to the 82C55 for compatibility with the PCI215 by default. To enable the fully configurable outputs it is necessary to enable “enhanced features” and to configure the output pins.

The “enhanced features enable” is an 8-bit register at BA + 100_{16}. Write 01_{16} to the register to enable enhanced features to allow the counter timer outputs pins to be configured.

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	Enable

FIGURE 2.3 ENHANCED FEATURES ENABLE REGISTER

2.8.2 Configuring Digital IO pins

The digital IO pins on the PL1 connector pins are connected to the 82C55 PPI by default for compatibility with the PCI215. However each pin can be individually configured to behave as default or be overridden to act as an output

7	6	5	4	3	2	1	0
invert	X	X	X	0000 Default 0001 Off 0010 High 0011 Reserved 0100 Reserved 0101 Z1 Counter Timer Out 0 0110 Z1 Counter Timer Out 1 0111 Z1 Counter Timer Out 2 1000 Z2 Counter Timer Out 0 1001 Z2 Counter Timer Out 1 1010 Z2 Counter Timer Out 2			

FIGURE 2.4 OUTPUT CONFIGURATION REGISTER

2.9 The PCIe Interface

The PCIe215 is a PCIe bus slave card. Communication between the host PC and the PCIe215 digital I/O board is via the PCIe bus. This bus provides data, address, interrupt and control lines together with the power supply for the PCIe215.

The PCIe215 is allocated two Base addresses in the available memory address space. PCI BAR 0 (LCR) is the PCIe215 Local Bus configuration register access space. We use this to access a low-level interrupt enable register only. PCI BAR 1 (BA) is the main register space.

The board base address and PC IRQ are set up by the PCI enumerator software during installation. Interrupt sources are classified by the position in an interrupt source register and each source is maskable by a bit in an interrupt mask register.

The PCIe215 uses only the +3.3 V supply from the host PC.

PCI MEMORY ADDRESS (Base + Offset)	FUNCTION	8/32 bit	IN/ OUT
BA + 00_{16}	Data to/from port A of PPI X	8	In/out
BA + 08_{16}	Data to/from port B of PPI X	8	In/out
BA + 10_{16}	Data to/from port C of PPI X	8	In/out
BA + 18_{16}	Control word for PPI X	8	Out
BA + 20_{16}	Data to/from port A of PPI Y	8	In/out
BA + 28_{16}	Data to/from port B of PPI Y	8	In/out
BA + 30_{16}	Data to/from port C of PPI Y	8	In/out
BA + 38_{16}	Control word for PPI Y	8	Out
BA + 80_{16}	Ctr Z1 – 0	8	In/out
BA + 88_{16}	Ctr Z1 – 1	8	In/out
BA + 90_{16}	Ctr Z1 – 2	8	In/out
BA + 98_{16}	Ctr Z1 – Control	8	In/out
BA + $A0_{16}$	Ctr Z2 – 0	8	In/out
BA + $A8_{16}$	Ctr Z2 – 1	8	In/out
BA + $B0_{16}$	Ctr Z2 – 2	8	In/out
BA + $B8_{16}$	Ctr Z2 – Control	8	In/out
BA + $D0_{16}$	Clock connection Z1/Z2	8	Out
BA + $E8_{16}$	Gate connection Z1/Z2	8	Out
BA + $F0_{16}$	IER Interrupt enable/status	8	In/out
BA + 100_{16}	Enhanced feature enable	8	In/out
BA + 120_{16}	Version	8	In
LCR + 50_{16}	Low-level interrupt enable register	32	In/out
BA + 900_{16}	Pin 4 Output configuration (X1 A0)	32	In/out
BA + 908_{16}	Pin 5 Output configuration (X1 A1)	32	In/out
BA + 910_{16}	Pin 6 Output configuration (X1 A2)	32	In/out
BA + 918_{16}	Pin 7 Output configuration (X1 A3)	32	In/out
BA + 920_{16}	Pin 8 Output configuration (X1 A4)	32	In/out
BA + 928_{16}	Pin 9 Output configuration (X1 A5)	32	In/out
BA + 930_{16}	Pin 10 Output configuration (X1 A6)	32	In/out
BA + 938_{16}	Pin 11 Output configuration (X1 A7)	32	In/out
BA + 940_{16}	Pin 12 Output configuration (X1 B0)	32	In/out
BA + 948_{16}	Pin 13 Output configuration (X1 B1)	32	In/out
BA + 950_{16}	Pin 14 Output configuration (X1 B2)	32	In/out
BA + 958_{16}	Pin 15 Output configuration (X1 B3)	32	In/out
BA + 960_{16}	Pin 16 Output configuration (X1 B4)	32	In/out
BA + 968_{16}	Pin 17 Output configuration (X1 B5)	32	In/out
BA + 970_{16}	Pin 18 Output configuration (X1 B6)	32	In/out
BA + 978_{16}	Pin 19 Output configuration (X1 B7)	32	In/out
BA + 980_{16}	Pin 20 Output configuration (X1 C0)	32	In/out
BA + 988_{16}	Pin 21 Output configuration (X1 C1)	32	In/out
BA + 990_{16}	Pin 22 Output configuration (X1 C2)	32	In/out
BA + 998_{16}	Pin 23 Output configuration (X1 C3)	32	In/out
BA + $9A0_{16}$	Pin 24 Output configuration (X1 C4)	32	In/out
BA + $9A8_{16}$	Pin 25 Output configuration (X1 C5)	32	In/out
BA + $9B0_{16}$	Pin 26 Output configuration (X1 C6)	32	In/out
BA + $9B8_{16}$	Pin 27 Output configuration (X1 C7)	32	In/out
BA + $D00_{16}$	Pin 4 Output configuration (Y1 A0)	32	In/out

BA + $D08_{16}$	Pin 5 Output configuration (Y1 A1)	32	In/out
BA + $D10_{16}$	Pin 6 Output configuration (Y1 A2)	32	In/out
BA + $D18_{16}$	Pin 7 Output configuration (Y1 A3)	32	In/out
BA + $D20_{16}$	Pin 8 Output configuration (Y1 A4)	32	In/out
BA + $D28_{16}$	Pin 9 Output configuration (Y1 A5)	32	In/out
BA + $D30_{16}$	Pin 10 Output configuration (Y1 A6)	32	In/out
BA + $D38_{16}$	Pin 11 Output configuration (Y1 A7)	32	In/out
BA + $D40_{16}$	Pin 12 Output configuration (Y1 B0)	32	In/out
BA + $D48_{16}$	Pin 13 Output configuration (Y1 B1)	32	In/out
BA + $D50_{16}$	Pin 14 Output configuration (Y1 B2)	32	In/out
BA + $D58_{16}$	Pin 15 Output configuration (Y1 B3)	32	In/out
BA + $D60_{16}$	Pin 16 Output configuration (Y1 B4)	32	In/out
BA + $D68_{16}$	Pin 17 Output configuration (Y1 B5)	32	In/out
BA + $D70_{16}$	Pin 18 Output configuration (Y1 B6)	32	In/out
BA + $D78_{16}$	Pin 19 Output configuration (Y1 B7)	32	In/out
BA + $D80_{16}$	Pin 20 Output configuration (Y1 C0)	32	In/out
BA + $D88_{16}$	Pin 21 Output configuration (Y1 C1)	32	In/out
BA + $D90_{16}$	Pin 22 Output configuration (Y1 C2)	32	In/out
BA + $D98_{16}$	Pin 23 Output configuration (Y1 C3)	32	In/out
BA + $DA0_{16}$	Pin 24 Output configuration (Y1 C4)	32	In/out
BA + $DA8_{16}$	Pin 25 Output configuration (Y1 C5)	32	In/out
BA + $DB0_{16}$	Pin 26 Output configuration (Y1 C6)	32	In/out
BA + $DB8_{16}$	Pin 27 Output configuration (Y1 C7)	32	In/out

FIGURE 2.5 PCIE215 REGISTER ASSIGNMENTS

2.9.1 IER Interrupts Enable / Status Register

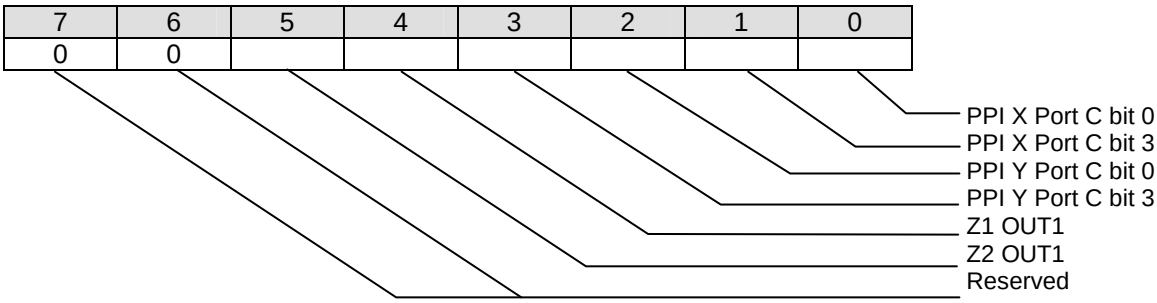


FIGURE 2.6 INTERRUPT ENABLE / STATUS REGISTER

Setting a bit to 1 in the interrupt enable register enables the associated interrupt source. Setting a bit to 0 disables the associated interrupt source. When enabled, a rising edge on an interrupt source signal causes an interrupt (if interrupts are enabled in the low-level interrupt enable register). The interrupt service routine can check the interrupt status register to determine which interrupt source(s) have triggered. To clear the interrupt, all the interrupt sources which have triggered need to be temporarily disabled by setting the appropriate bits of the interrupt enable register to 0. The bits can be set back to 1 to re-enable the interrupt sources.

2.9.2 Low-level Interrupt Enable Register

This is a 32-bit read and write register at offset 50_{16} in the local configuration register area (PCI BAR 0). Write 80_{16} to the register to enable PCIe interrupts.

31 – 8	7	6 - 0
Reserved (0)	Enable	Reserved (0)

FIGURE 2.7 LOW-LEVEL INTERRUPT ENABLE REGISTER

3 ELECTRICAL CONNECTIONS

This chapter describes the signal and control connections that the user must make between the PCIe215 and any external devices. These I/O connections are made through the D-type connector protruding from the PC adapter slot corresponding to the chosen board position. The metal shell connected to the local PC chassis ground. All signals are referred to the relevant signal ground.

3.1 78 way D-type Connector (SK1 - User I/O)

Connections from the PCIe215 to the user devices are made via a 78 way D-type connector.

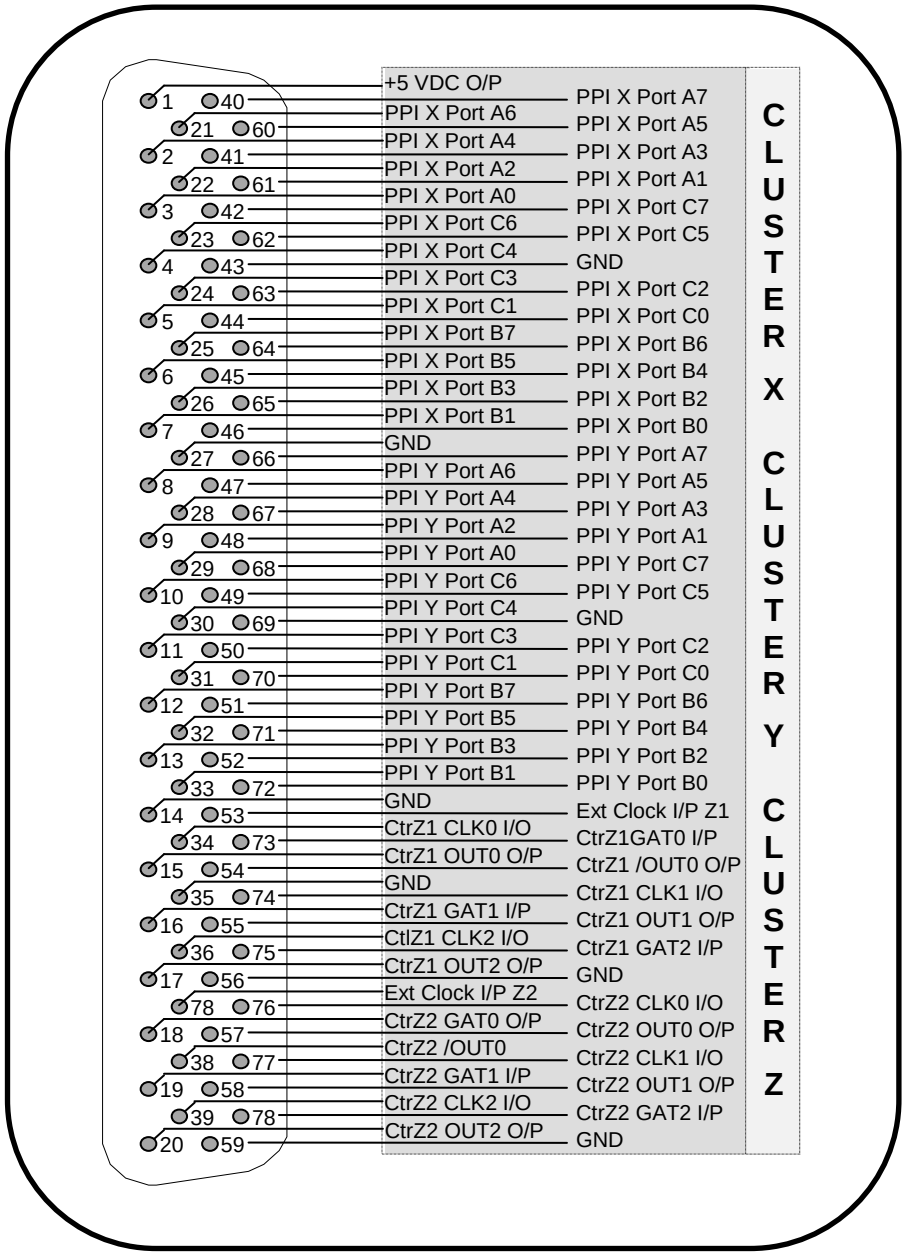


FIGURE 3.1 I/O CONNECTOR

A mating 78 way male connector is available from Amplicon as a separate item.

3.2 Voltage Outputs Available on SK1

In addition to the 48 digital I/O lines and counter timer signals, the PC +5 VDC voltage rail is brought out on SK1, the I/O connector. No more than 1.0 A should be drawn from the +5 V rail. Refer to the computer technical reference manual for total current availability from the source power supplies.

3.3 Use of Shielded Cables

In order to maintain compliance with the EMC directive, 89/336/EEC, it is mandatory that the final system integrator uses good quality screened cables for external connections. It is up to the final system integrator to ensure that compliance with the Directive is maintained. Amplicon Liveline offers a series of good quality screened cables for this purpose. Please contact our sales staff.

3.4 On board Pull Up Resistors & Jumper Settings

The digital I/O lines on ports A, B and C are TTL compatible. The input lines all feature additional circuitry which make them able to accept higher input voltages without damage.

Each IO pin has a dedicated pull up resistor that can be connected to +5v or +12v via jumper link J2.

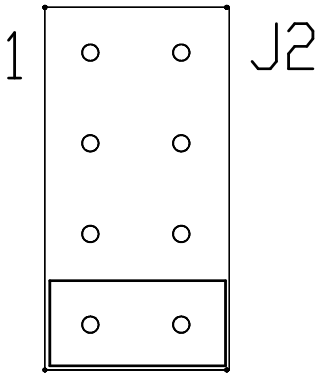


FIGURE 3.2 PULL UP RESISTOR JUMPER

In the diagram above the jumper is shown linking pins 7 to 8. This is the default 'park' position which leaves the pull up resistors unconnected.

J2 Jumper Position	Function
1 to 2	All IO lines pulled up to PC +5 volt supply via on board resistor networks
3 to 4	All IO lines pulled up to PC +12 volt supply via on board resistor networks
5 to 6	Pull up resistors floating
7 to 8	Pull up resistors floating (FACTORY DEFAULT)

FIGURE 3.3 PULL UP RESTSTOR JUMPER FUNCTION

3.5 Digital I/O Examples

The following examples illustrate common ways in which the IO pins may usefully connected. In all cases the application software defines the direction of the IO pin only. No other software settings need to be made to enable the different IO configurations.

3.5.1 PCIe DIO IO Pin as a TTL Compatible Input / Output

This is the simplest mode of operation. The IO Pin acts as a standard TTL compatible input or output as configured by application software. Refer to the specifications for the maximum current the IO pin can source and sink.

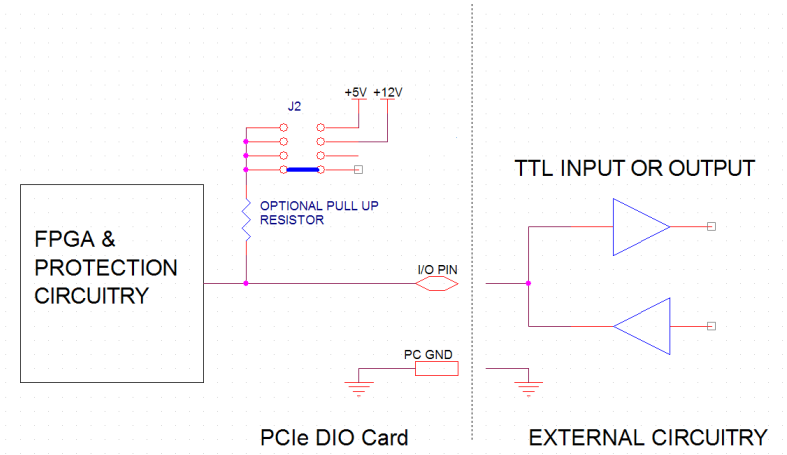


FIGURE 3.4 IO PIN AS A TTL COMPATIBLE INPUT / OUTPUT

3.5.2 PCIe DIO IO Pin as a Volt Free Contact Input

In this example the IO pin is configured as a volt free contact (VFC) input. In this example the external input control is represented by a switch and could equally well be a relay or semiconductor device. With the switch open the input will be pulled high (logic '1') to +5v by the pull up resistor on the PCIeDIO. When the switch is closed the IO pin will be pulled low (logic '0').

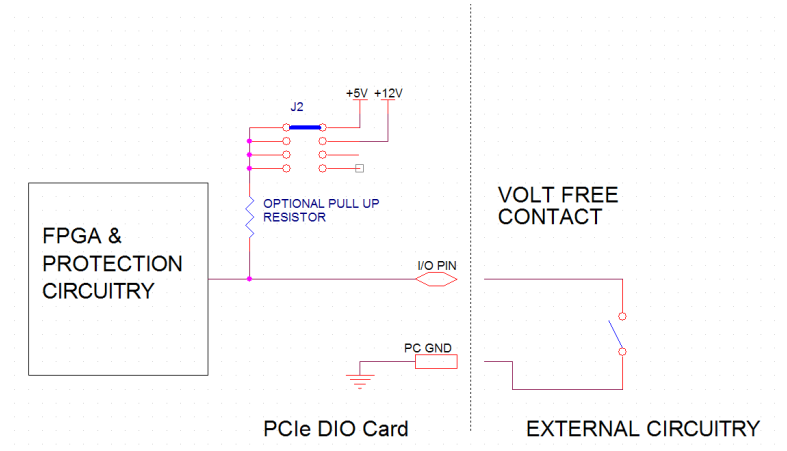


FIGURE 3.5 PCIE DIO IO PIN AS A VOLT FREE CONTACT INPUT

3.5.3 PCIe DIO IO Pin as a High Voltage Tolerant Input

When configured by application software as an input the IO pin can withstand voltages well in excess of +5v. This is extremely useful for interfacing to industrial +12v and +24v signals. On power up all IO pins default to Inputs. Refer to the specifications for the maximum voltage the IO pin can withstand without damage.

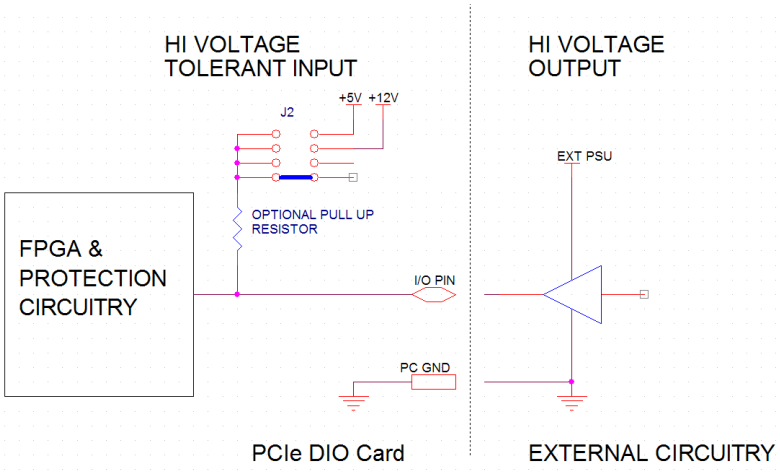


FIGURE 3.6 IO PIN AS A HIGH VOLTAGE TOLERANT INPUT

3.5.4 PCIe DIO IO Pin as a Current Sinking Output

In this example the IO pin is configured as a current sinking output. The load is shown connected to an external power supply in this example but the load current can be supplied from the PC +5v or +12v if required. Refer to the specifications for the maximum current the IO pin can sink and the maximum voltage the IO pin can withstand without damage.

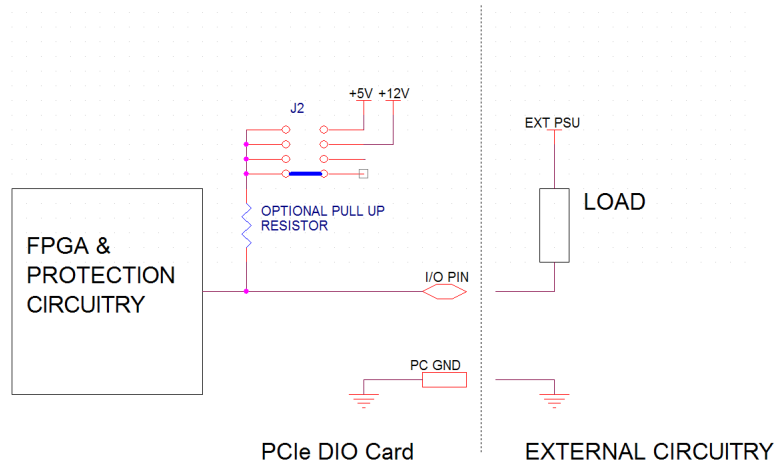


FIGURE 3.7 IO PIN AS A CURRENT SINKING OUTPUT

3.5.5 PCIe DIO IO Pin as a +12v Hi Impedance Output

When configured by application software as an output the IO pin can be configured to drive a +5 or +12v output via the on board pull up resistor. Refer to the specifications for the maximum current the IO pin can source and sink.

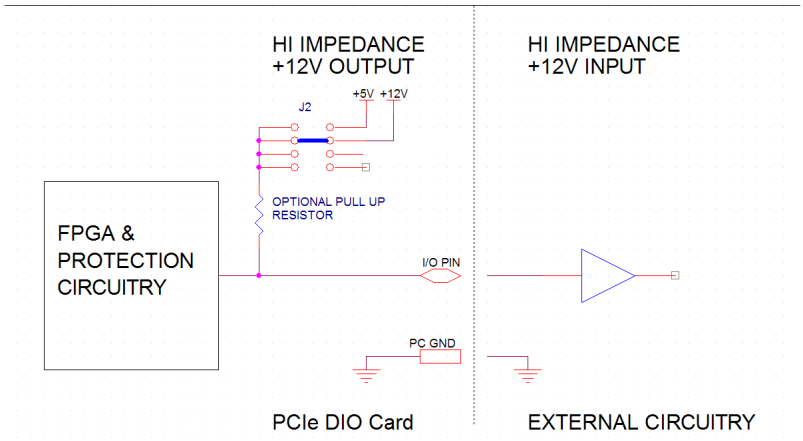


FIGURE 3.8 IO PIN AS A +12V HI IMPEDANCE OUTPUT

3.5.6 PCIe DIO IO Pin as an Output Referenced to an External PSU

When configured by application software as an output the IO pin can be configured to drive an output referenced to an external power supply via an external pull up resistor. The value of the resistor used is calculated to ensure sufficient drive to the load and at the same time limit the current the IO pin is required to sink when driving a logic Low output. Refer to the specifications for the maximum current the IO pin can sink.

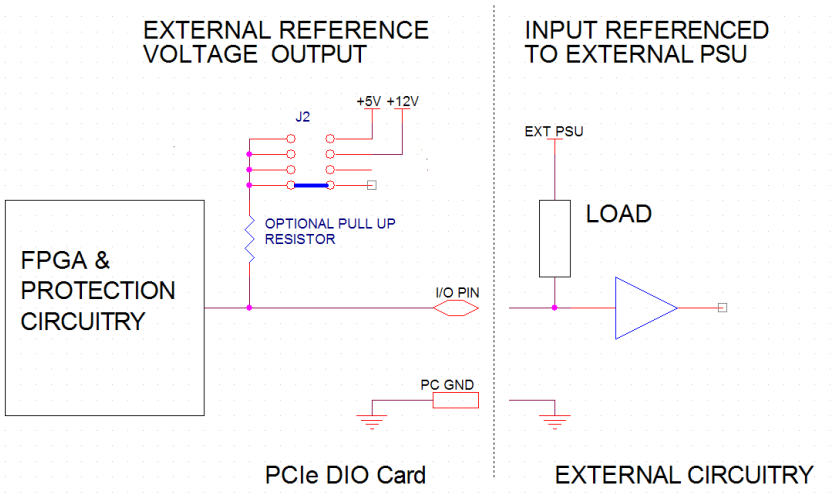


FIGURE 3.9 IO PIN AS AN OUTPUT WITH EXTERNAL PULL-UP RESISTOR

4 PROGRAMMING THE PCIE215

The PCIe215 is supplied with Windows drivers. Programming for use under other operating systems is beyond the scope of this manual. A Dynamic Link Library (DLL) is supplied to provide an Application Programming Interface (API) for user programs.

4.1 Copyright

Software supplied with the PCIe215 is **Amplicon** copyright. Permission is granted for the purchaser of the PCIe215 to incorporate any part of the **Amplicon** copyright software into related application programs, and to use, resell or otherwise distribute such application programs for operation with PCIe215 hardware purchased from **Amplicon Liveline Limited.**

4.2 Guide to User Programming

When developing an application specific program, it is advised that the supplied driver and dynamic link library functions be used for Windows applications. Please refer to the ADIO software manual, **ampdio.pdf**, for details of programming using the functions in the DLL.

For programming at register level, reference should to be made to section 2 describing the assignments of each I/O register in the PCIe215. Reference should also be made to the 82C55 Appendix **App82C55.pdf** in the \MANUAL subdirectory on the Amplicon DVD-ROM for details of programming the 82C55 at register level. Support is not available for this method of programming.

4.3 Interfacing with Commercial Software Packages

The supplied software examples are not intended to be stand alone applications programs, other than for demonstration and test purposes. To meet most user requirements, either a dedicated program must be written using the functions and examples provided or the PCIe215 can be interfaced to a commercial applications package.

Other Applications Packages

Further interface packages to commercial software will be made available as requirements expand. Check the 'README' files on the distribution DVD, and/or the **Amplicon website** or Sales Department for the latest information.

APPENDICES

A TECHNICAL SPECIFICATIONS

A.1. Electrical Specification

Counter / Timer

Features	PCIe215 has two 82C54 or equivalent counter/timers CTCs (arranged as Z1 & Z2). Each CTC provides: Three independent 16 bit counters Six programmable counter modes, binary or BCD
Internal Clock Source	10 MHz, derived from crystal controlled oscillator or software selectable Initial tolerance ±50 ppm Frequency drift over temp. range ±50 ppm
Clock Divider	Clock pre-scalers provide alternative clock frequencies of 10MHz, 1MHz, 100 kHz, 10 kHz, 1 kHz or external clock source.
Ext Clock/Gate Input	The three counter clock inputs, and two counter gate inputs can be driven by external signals. This signal is referred to digital ground and must be within the range:
External Clock	10 MHz (max) Square Wave
Counter Outputs	The non-inverted, buffered outputs counters two OUT2 is available on the user I/O connector.
Digital I/O Ports	48 I/O lines arrange as two clusters of three 8 bit ports (A, B and C). Each cluster programmable as two groups of 12 bits (group A, group B) and used in three modes of operation. Each Control block (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues proper commands to its associated ports. Control Group A - Port A and Port C upper (C7 - C4) Control Group B - Port B and Port C lower (C3 - C0) Mode 0: Basic I/O (Group A, group B) Mode 1: Strobed I/O (Group A, group B) Mode 2: Bidirectional bus (Group A only)
Digital Inputs	'Low' input voltage -0.3V to +0.8V) TTL 'High' input voltage +2.2V to +50V) compatible
Digital Outputs	'Low' output voltage, +0.4V max at 2.5mA 'High' output voltage, +2.4V min at -2.5mA +50V max, with external PSU

User I/O Connector	78 way female D-sub. 48 digital I/O lines, counter/timer signals, power and ground.
Address Range	The board's address range is assigned by the plug and play mechanism.
IRQ Range	A single PC Interrupt is required by the card and is assigned an IRQ by the plug and play mechanism.
Power	Powered by +3.3 Volts from the host PC bus. PCIe215 draws 200mA or up to 300mA when all 48 digital output lines are fully loaded. The following PC bus voltages are available at the user I/O connector: 5 VDC at 1A. Subject to current being available from PC power supply.

A.2. Software Specification

The distribution software is supplied on a DVD-ROM.

Windows Driver Software provides Application level access to all the advanced features of the card from these operating systems.

A.3. Environmental Conditions

Environment

The PCIe215 is designed to operate in a PC. Particular attention is paid at the design stage to minimise emission of noise and susceptibility to external radiated noise.

Specific conditions

I/O Positions Required	One PCIe bus version 2.1 I/O adapter slot with room for half-length card.
Board Dimensions	Length 80 mm Height 95 mm
Temperature Range	Operating 0° C to +60° C Storage -20 to +70° C
Humidity Range	5% to 95% non-condensing
Power Requirements	3.3 Vdc from host computer power supply. 130 mA PCIe215 typical operating Excluding power supplied to external system via user connector.
Dissipation	Each PCIe215 will dissipate typically 1.0 Watts of heat excluding any isolation modules fitted
Handling	Normal static handling precautions apply. Damage could result if not observed

Order Codes

96 113 263	PCIe215 Digital input/output and counter timer card

Optional Accessories

Amplicon Order Code	Description
9096 6333	EX233 termination and distribution panel (& manual)
9096 6363	EX213 24 channel output panel with relays and Isolated logic panel
9096 6373	EX230 24 channel input panel with isolated, common & contact closure inputs
9194 5953	78 pin connector kit
9099 3384	78 way interconnect cable (2m) for EX233
9096 6349	78 way interconnect cable (1m) for EX233
9101 4890	37 way cable (1m) EX233 to EX213/230

B PRINTED CIRCUIT ASSEMBLY DRAWINGS

B.1. ASSEMBLY DETAIL

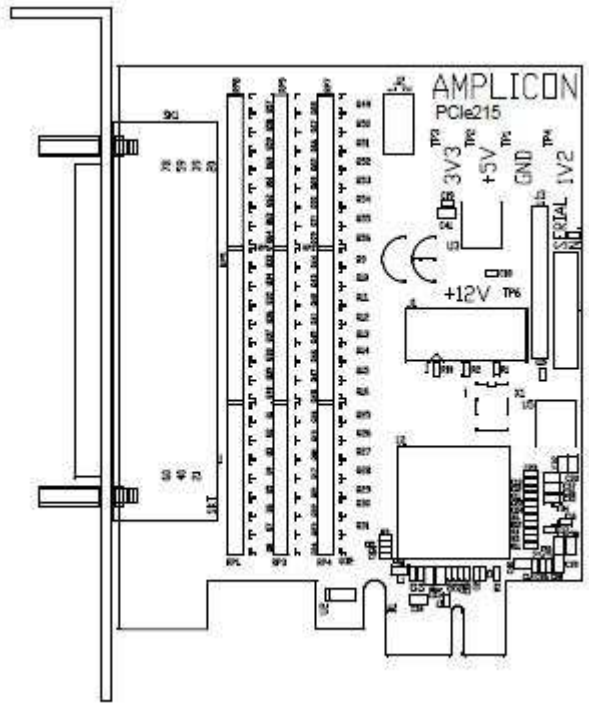
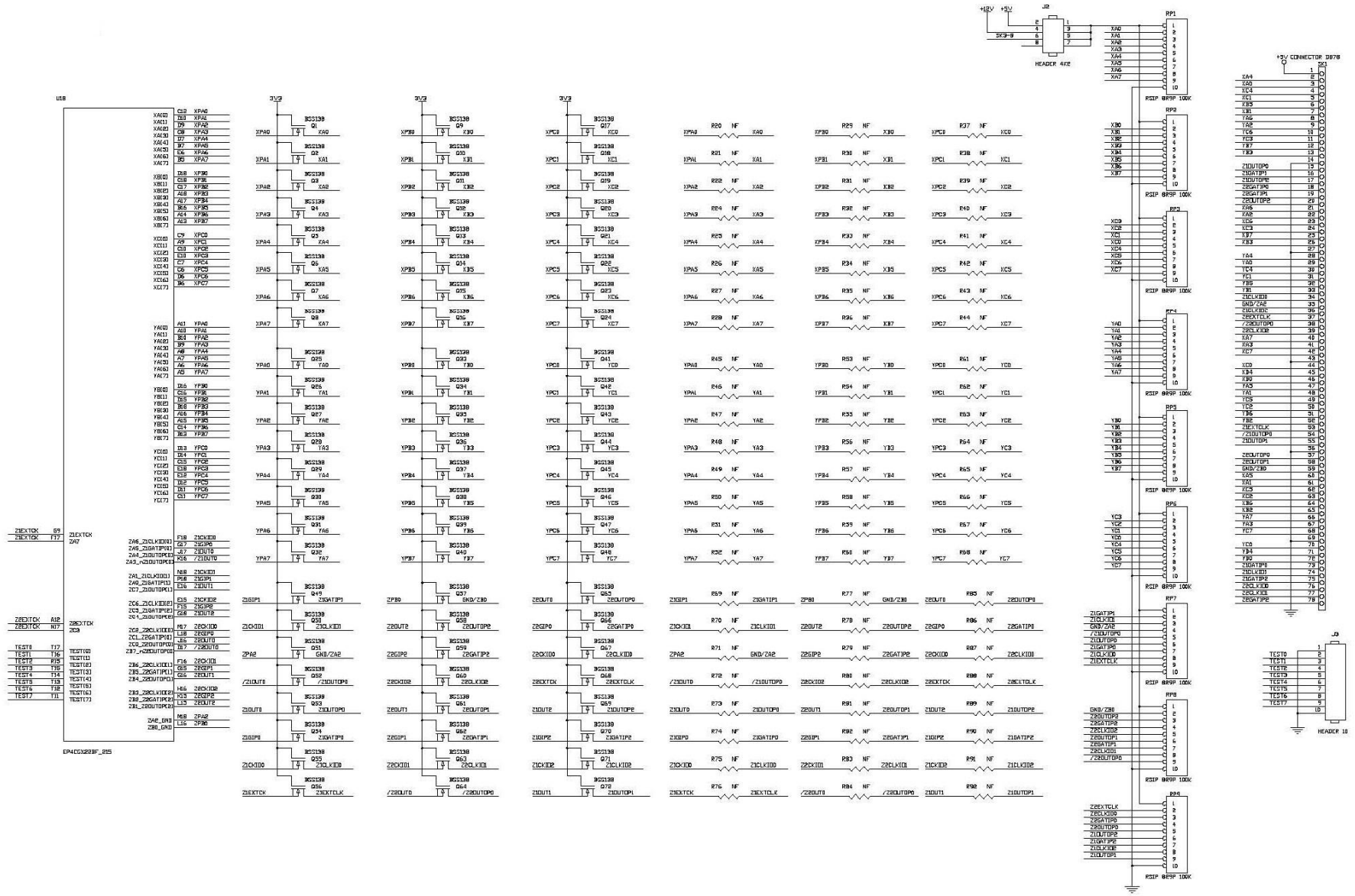
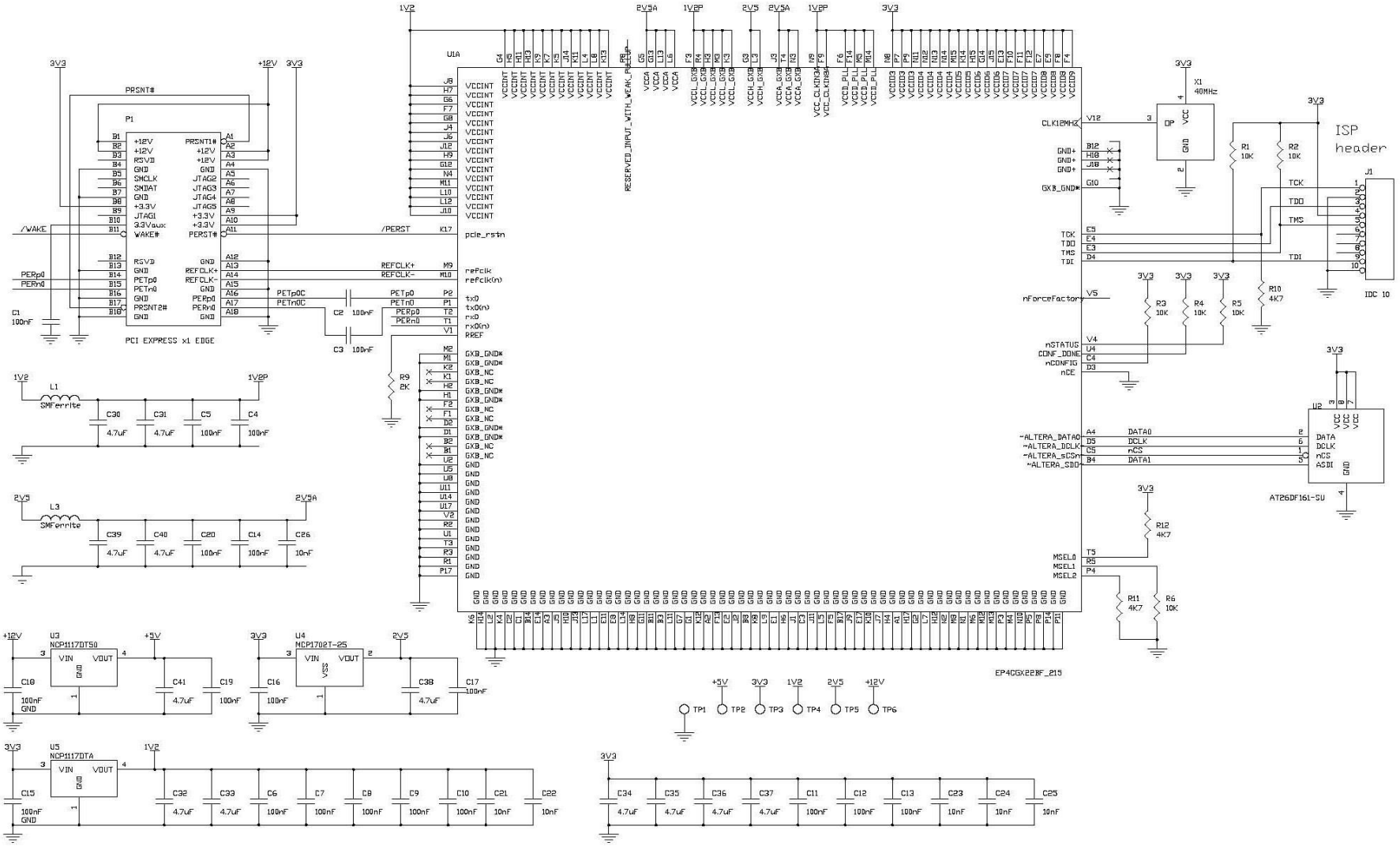


FIGURE 4.1 PCIE215 PRINTED CIRCUIT ASSEMBLY




PCI EXPRESS x1 EDGE
EP4CGX22BF_215
AT26DF161-SU
IDC 10
ISP header