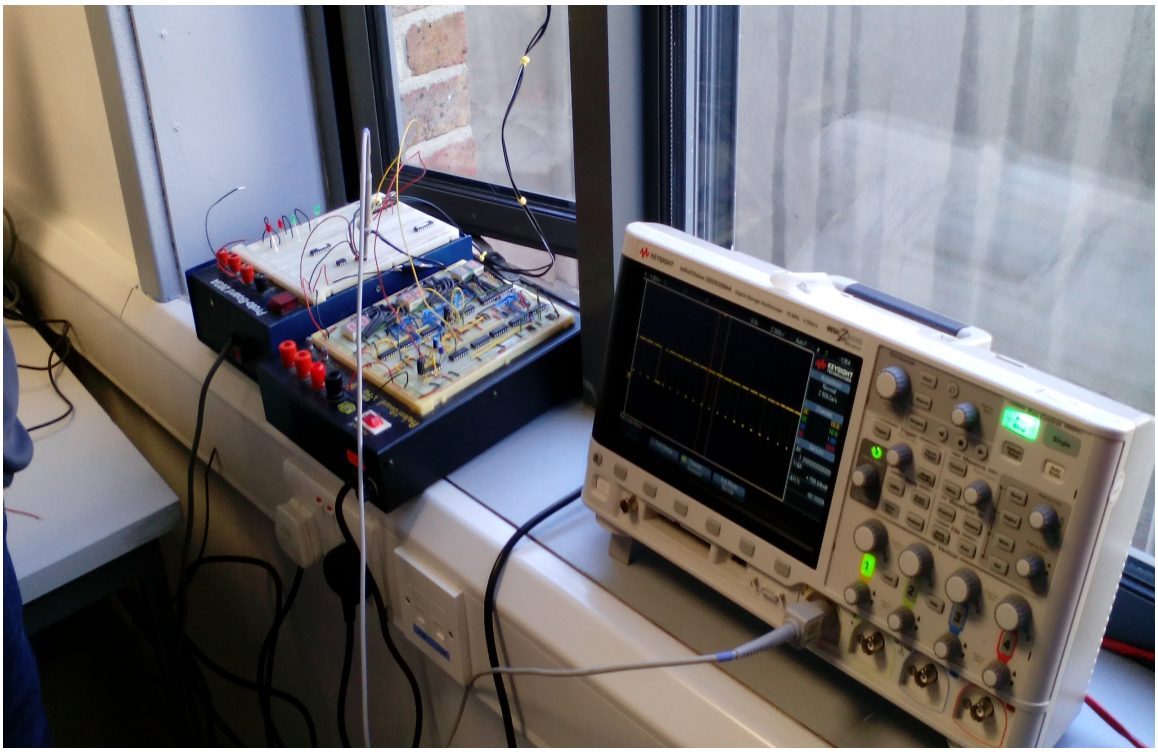
3C6b – Digital Electronics Design Project

Rugby Radio



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Abstract

The project proposed was a circuit that could decode the rugby clock signal and display the information received in form of hh/mm/ss. The circuit was designed and simulated using Multisim software and found to behave like expected. Next it was implemented in silicon and its individual modules were tested with the help of an Arduino microcontroller; the design passed all the tests to which it was submitted and at the very end was connected to a signal receiver and proved to be able to display real time information as decoded from the rugby radio signal so meeting the requirements.

Introduction

This report describes in detail the process of design, testing and implementation of the above-mentioned circuit.

This lab exercise was designed with the purpose to develop the practical knowledge of digital logic gates, displays, and the use of microprocessors such as Arduino. It was also meant to help students gain further experience in the design, simulation, implementation and testing of digital circuits. Also it was supposed to help develop the team–working capacities of the students and by the means of the requirement of the submission of a lab report it offered students an opportunity to practice their technical writing communication skills.

The exercise was chosen in such a way as to ensure the use of basic building blocks of digital circuits. It required the use of a variety of chips such as counters, monostable multivibrators, flip flops and shift registers as well as AND, OR and NOT gates. It also required the use of 7 segments LED displays and the corresponding latch/decoder/driver chip. A combination of 6 of these LED displays was to be used to represent the numbers for hour, minutes and seconds respectively. The team of students had to come up with the overall design and any logic needed for the circuit to perform as required.

The design was chosen in order to simplify the overall circuit, minimize the number of components needed and maximise the use of the functionalities of the individual chips.

The workflow was to be divided in the following main steps:

- Design with the aid of Multisim software package
- Test in the virtual environment
- Implementation in silicon
- Unit testing with the aid of Arduino microcontroller
- Overall testing with the aid of the oscilloscope
- Final testing with the rugby radio signal receiver
- Demonstration

Circuit Description

Before describing the whole circuit some word have to be said about the functionality of the chips used to implement the design. Next there will be a short description of the chips involved and their functionality.

The CD4029 chip is a presetable up/down counter chip, which counts by adding one value to the counter at every rising edge of the clock signal. It is worth mentioning some its useful functionalities as follows:

- Preset/enable – active high uses the 4 Jam inputs to reset to counter to the specified value
- Up/Down – makes the chip count upwards when high and downwards otherwise.
- Carry-out - active low is set when the counter reaches the maximum value while counting upwards or zero when counting downwards.
- Binary/Decade makes the chip count in binary when high and decade otherwise

Below, on figure 1, is a schematic representation of the CD4029 chip and its pin configuration.

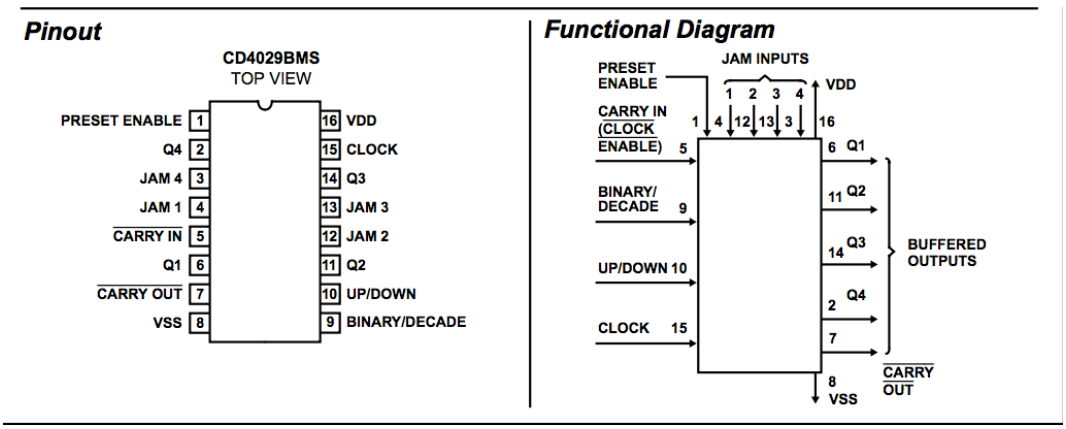


Figure 1 CD4029 Schematics

The CD4538 chip is a retriggerable/resettable monostable multivibrator. It can be set to trigger at either rising or falling edge in response of 2 inputs A and B. The width of the output pulse is give by the combination of the Cx and Rx constants.

It works by switching from the stable state to the unstable state under the influence of an external trigger such as a rising edge or a falling edge. The time it stays on the unstable state depends on the resistor/capacitor pair. There is a logarithmic relationship between the value of the product RC and the time length that the monostable vibrator is kept in the unstable state.

The figure 2 below presents the schematics of the chip and a list of with the name of the pins and their function.

Pin Description

Pin No.	Pin Name	I/O	Function
1	T1A	—	Passive component connection pin 1(CHA)
2	T2A	—	Passive component connection pin 2(CHA)
3	$\overline{C}$DA	I	Reset input (CHA)
4	AA	I	Input A(CHA)
5	BA	I	Input B(CHA)
6	QA	O	Output Q(CHA)
7	$\overline{Q}$A	O	Output $\overline{Q}$(CHA)
8	VSS	—	Power supply (-)
9	$\overline{Q}$B	O	Output $\overline{Q}$(CHB)
10	QB	O	Output Q(CHB)
11	BB	I	Input B(CHB)
12	AB	I	Input A(CHB)
13	$\overline{C}$DB	I	Reset input (CHB)
14	T2B	—	Passive component connection pin 1(CHB)
15	T1B	—	Passive component connection pin 2(CHB)
16	VDD	—	Power supply (+)

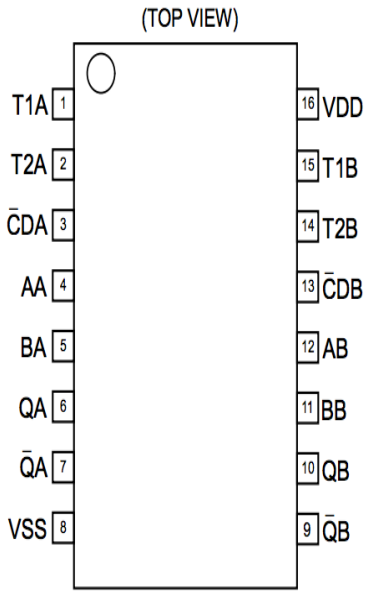


Figure 2 CD 4538 Schematics

The CD4015 chip is a dual 4-stage shift register with serial input and parallel output. It can be used to store up to 4 bits of data/unit, from a serial input and output it as parallel 4 bits outputs to a display for example or to be used as inputs for another circuit that needs parallel input of data. Each stage is composed by a D-type flip-flop. All stages can be reset to logic 0 asynchronously of the clock by a high signal on the reset pin of the unit. Each unit has independent pins as follows:

- DATA for the serial data input
- CLOCK for the clock signal
- RESET for the reset signal which is active high
- Q1, Q2, Q3, Q4 parallel outputs

It stores 1 bit of data at every rising edge of the clock signal. The data from the first stage is shifted over into the second stage and so until it reaches the final stage to be pushed “out” on the next clock bit. So every bit of data is kept for 4 clock bits. If the output 4 of the first unit is connected to the data input of the second unit the chip behaves as an 8-bit storage unit. Two or more chips can be connected this way in order to achieve the desired capacity.

Figure 3 below shows the pin configuration and the functional diagram of CD 4015 chip.

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	CLOCK A CLOCK B	Clock Input
6, 14	RESET A RESET B	Reset Input
7, 15	DATA A DATA B	Data Inputs
5, 4, 3, 10	QnA	Outputs A-Stage
13, 12, 11, 2	QnB	Outpus B-Stage
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

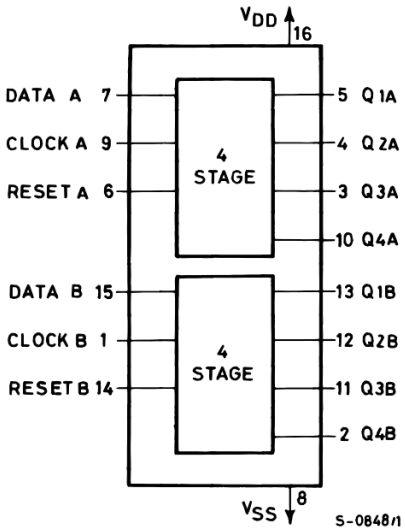


Figure 3 CD4015 Schematics

The CD4013 chip is a dual D-type flip-flop, which contains two data type flip-flops that can be used as data registers or counter and toggle applications by connecting the NOTQ output to the data input. Each unit has independent data, set, reset and clock inputs and Q and NOTQ outputs. Both set and reset are asynchronous and active high. The chip works by transferring the value of the data input to the output Q at every rising edge of the clock signal.

Figure 4 below shows the pin configuration and the functional diagram of CD 4013 chip.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Q1	O	Channel 1 output
2	$\overline{Q1}$	O	Inverted channel 1 output
3	CLOCK1	I	Channel 1 clock input
4	RESET1	I	Channel 1 reset
5	D1	I	Channel 1 data input
6	SET1	I	Channel 1 set
7	V_{SS}	—	Ground
8	SET2	I	Channel 2 set
9	D2	I	Channel 2 data input
10	RESET2	I	Channel 2 reset
11	CLOCK2	I	Channel 2 clock input
12	$\overline{Q2}$	O	Inverted channel 2 output
13	Q2	O	Channel 2 output
14	V_{DD}	—	Power supply

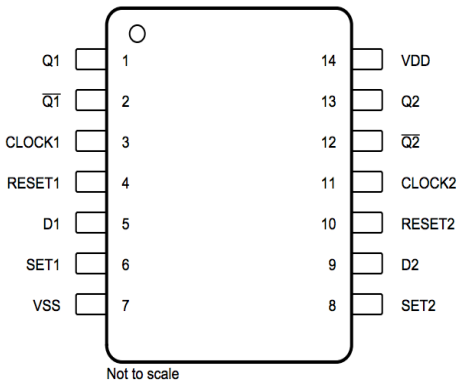


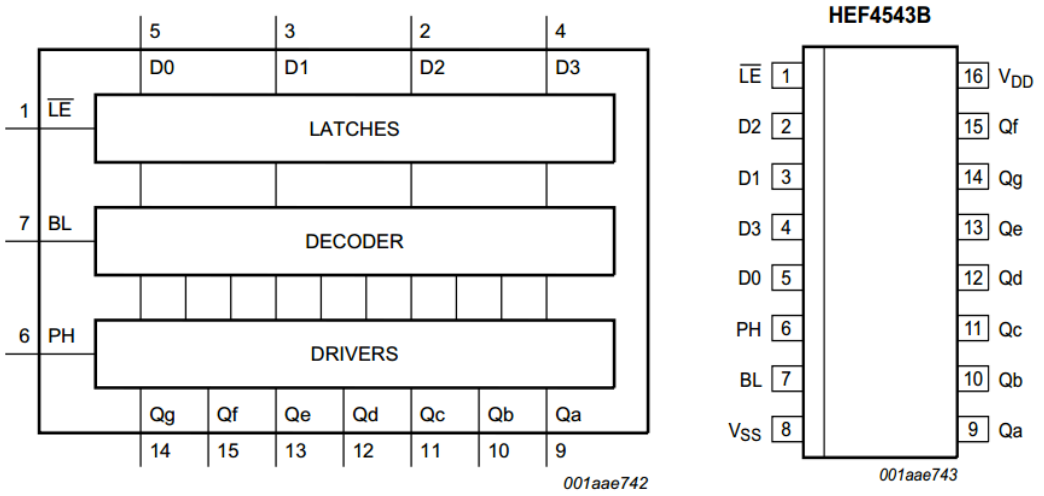
Figure 4 CD 4013 Schematics

The CD 4543 chip is a BCD to & segments display latch/decoder/driver. It takes in 4 inputs D0 to D3 and stores them when latch enable input (LE) is low. It also provides the possibility of blanking the display when the blanking input (BL) is high. The function table phase can be inverted by providing a high signal to the phase input (PH). The chip has seven buffered segments outputs Qa to Qg.

The chip is used to provide storage for a BCD value coming from a parallel output of a shift register for example, which is then decoded onto a seven-output format

that suits the 7 segments LED displays. The chip is also used to drive the LED display.

Figure 5 below is providing the pin configuration, pin description and functional diagram of the CD4543 chip.

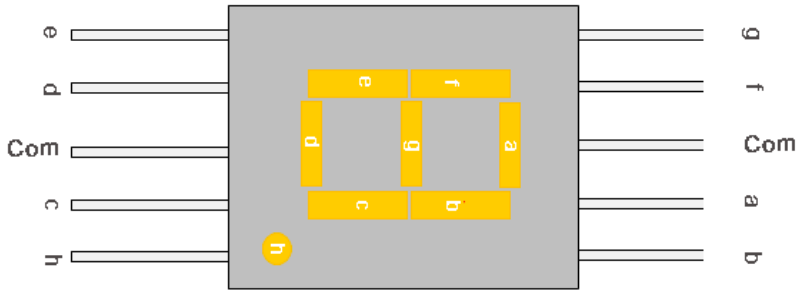


Symbol	Pin	Description
$\overline{LE}$	1	latch enable input (active LOW)
D0 to D3	5, 3, 2, 4	address (data) input
PH	6	phase input (active HIGH)
BL	7	blanking input (active HIGH)
V_{SS}	8	ground supply voltage
Qa to Qg	9, 10, 11, 12, 13, 15, 14	segment output
V_{DD}	16	supply voltage

Figure 5 CD 4543 Schematics

The last chip used was the 7 segments LED display. It connects to the output of the CD 4543 and displays the values provided to it in digits from 0-9 or characters. It needs to be grounded but since both Ground pins are shorted only one of them is connected to ground. It is good practice not to relay on the 4543 chip alone to drop the current in order to protect the LED segments but to make use of individual resistors for every input.

Figure 6 shows the pin configuration of the 7 segments LED display.



The Rugby Signal, named after the first location it was transmitted from in Rugby UK, contains the UK national standards for date, time and frequency and is currently being transmitted from Anthorn, Cumbria UK. [1]. The signal encodes:

- year
- month
- day of month
- day of week
- hour
- minute
- British Summer Time (in effect or imminent)
- DUT1 (a parameter giving UT1-UTC; see the information sheet link below for more explanation)

For the purpose of this exercise only the hour, minutes and seconds part of the signal had to be decoded and displayed.

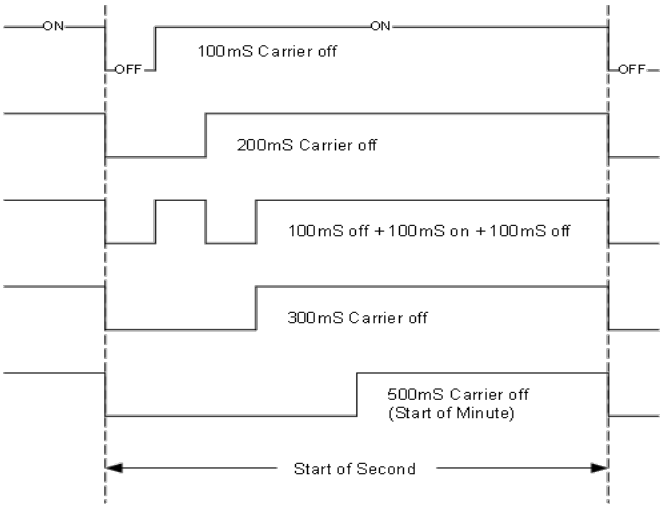


Figure 7 Rugby Signal

The MSF time code format is summarised in figure 7 above. The modulation used is simple on-off modulation with the signal considered to be active low. Every new second is marked by a low of 100ms on the signal while the next 100ms is dedicated to carrying information on bit A followed by another 100ms period which encodes information on bit B. The start of a new minute is marked by the excusive sequence 01111110 in bit A. A period of 500ms of carrier signal being turned off during the second 59 is also used to mark a new minute. During this time the station encodes the information for the next minutes signal and resumes transmission.

The diagram below in figure 8 is a graphical representation of how bits A and B are used to encode the information. The seconds containing information referring to the time are as follows:

- Seconds from 39-44 encode hour information
- Seconds from 45-51 encode minutes information

MSF time code
Shaded bits are fixed

Bit	A	B	Meaning	Bit	A	B	Meaning	Bit	A	B	Meaning
00	1	1	Minute mark	20	10	0	Year (00–99)	40	10	0	Hour (00–23)
01	0	+0.1	DUT1 (0.1–0.8) Unary encoding, bit set if DUT1 ≥ Weight	21	8	0		41	8	0	
02	0	+0.2		22	4	0		42	4	0	
03	0	+0.3		23	2	0		43	2	0	
04	0	+0.4		24	1	0		44	1	0	
05	0	+0.5		25	10	0	Month (01–12)	45	40	0	Minute (00–59)
06	0	+0.6		26	8	0		46	20	0	
07	0	+0.7		27	4	0		47	10	0	
08	0	+0.8		28	2	0		48	8	0	
09	0	−0.1	DUT1 (−0.1−−0.8) Unary encoding, bit set if DUT1 ≤ Weight	29	1	0		49	4	0	
10	0	−0.2		30	20	0	Day of month (01–31)	50	2	0	
11	0	−0.3		31	10	0		51	1	0	
12	0	−0.4		32	8	0		52	0	0	Minute marker 01111110
13	0	−0.5		33	4	0		53	1	STW	Summer time warning.
14	0	−0.6		34	2	0		54	1	P1	Year (17A–24A) — Odd parity over
15	0	−0.7		35	1	0		55	1	P2	Day (25A–35A)
16	0	−0.8		36	4	0	Day of week Sunday=0 Saturday=6	56	1	P3	DOW (36A–38A)
17	80	0	Year (00–99)	37	2	0		57	1	P4	Time (39A–51A)
18	40	0		38	1	0		58	1	ST	Summer time in effect.
19	20	0		39	20	0	Hour (00–23)	59	0	0	Unused, always 0.

Figure 8 MSF time code

The following approach was taken in order to design the overall circuit:

- The signal was connected as input to one unit of the monostable (***CD4538***) chip, which was set up to detect the falling edge. The RC couple was chosen as to provide a pulse of length 450ms. This was achieved by using a combination of a 22uf in parallel with 4.7uf capacitors and a 27Kohms resistor. In the circuit schematic this monostable is called Min Monostable since is used to detect the new minute. The output of the Minutes Monostable is used as follows:
    - It is used in connection with the rugby signal itself by the flip-flop (***CD4013***) chip to detect when the signal is off between the 300ms and 500ms period of the signal. When that occurs means that a new minute is coming.
    - It is also used as the reset signal by the units of seconds counter (***CD4029***) chip as clock signal.
    - The rising edge of the output is used to trigger the Seconds Monostable (***CD4538***) chip, which is set to detect a rising edge and is dedicated to detecting the new second. The pulse width of this monostable was set to 150ms as to ensure that its falling edge corresponds to the middle of bit A part of the signal. The RC combination used was a 33uf capacitor and a 5Kohms resistor. The Seconds Monostable output is inverted and used as clock signal by

all shift register (***CD4015***) chips which in this configuration and having the rugby signal as input store and shifts a bit of information every second.

- The output of the flip-flop chip is used to trigger the Latch Signal Monostable whose output is in turn used as latch signal for the latch/decoder/driver (***CD 4543***) chips for units and tens of hours and minutes instructing them when to read the shift register (***CD4015***) chips and store the value of the next hour and minutes. The output signal of the Latch Signal Monostable is also used as preset-enable signal by the tens and units of seconds counter chips. The pulse width of this monostable was set to 150ms and the RC combination used was a 33uf capacitor and a 5Kohms resistor.
- The carry-out signal from the units of seconds counter (***CD4029***) chip is used as clock signal of the tens of seconds counter (***CD4029***) chip. The outputs of the units and tens of second counters serve as input to units and tens of second latch/decoder/driver (***CD 4543***) chips respectively.
- Each latch/decoder/driver (***CD 4543***) chip drives a 7 segments display chip. The output of the driver is connected to the inputs of the display using 330ohms resistors in order to lower the current and protect the LED segments.

The Diagram below in figure 9 represents the logic flow and connections of the circuit designed for the purpose of this exercise.

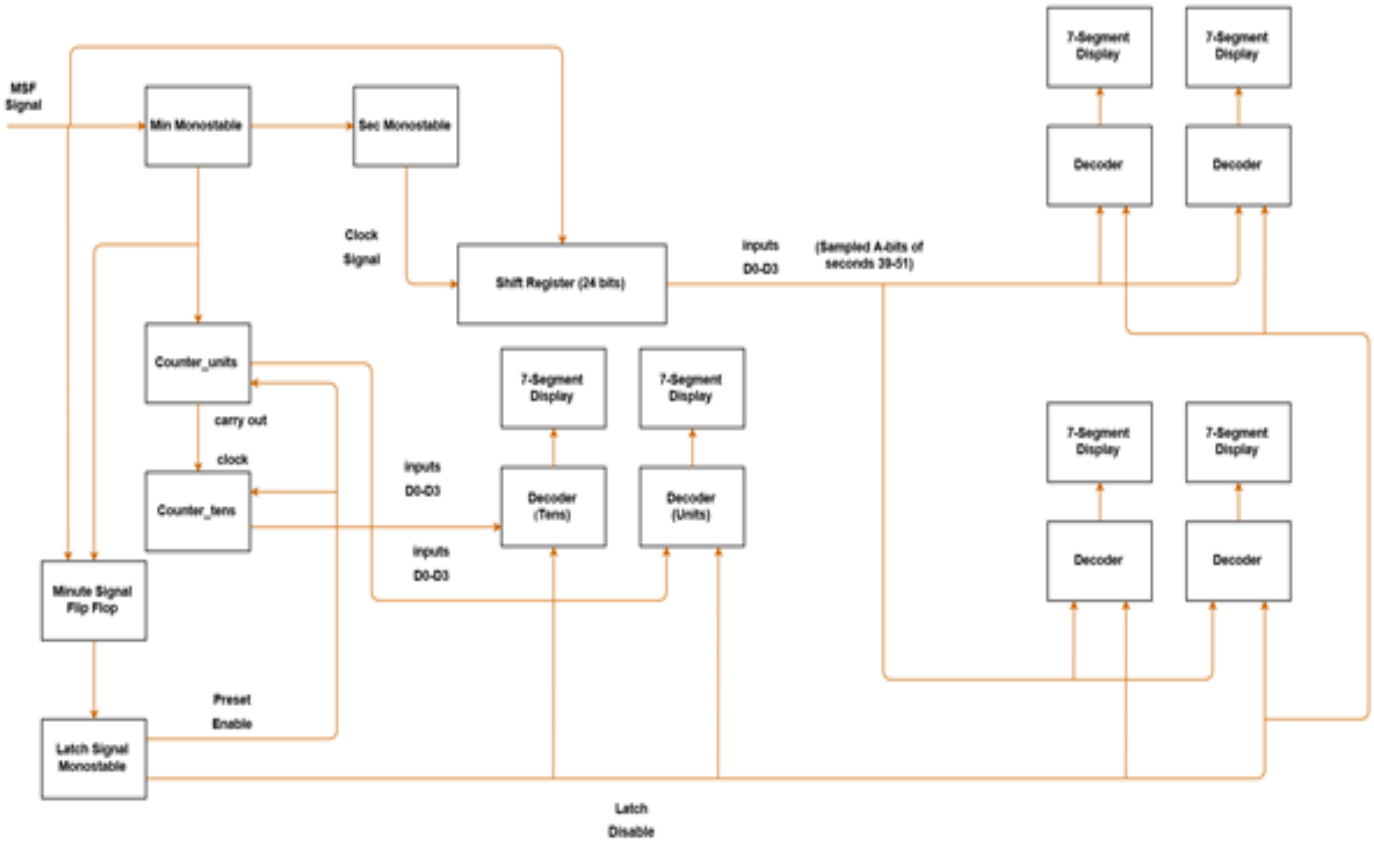


Figure 9 showing a block diagram representation of the circuit

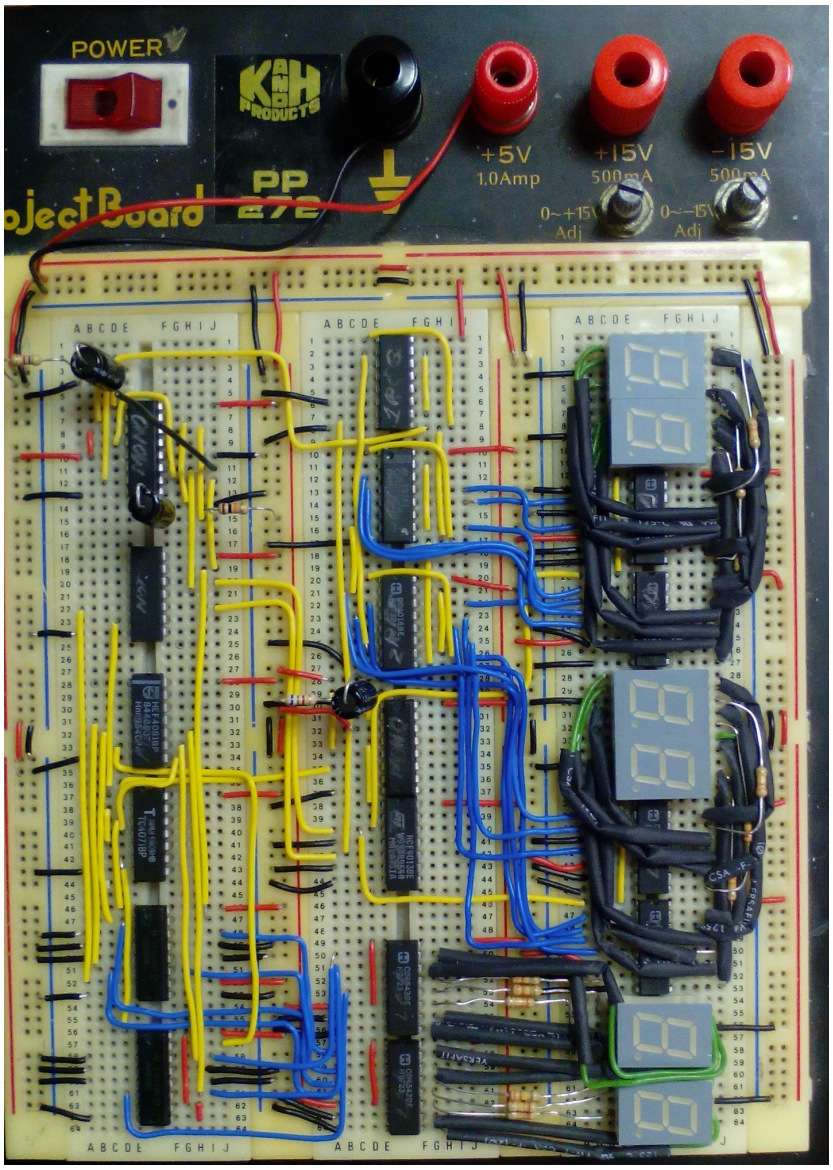


Figure 6 Final implementation of the circuit

Testing

Once the logic and block diagram were ready the overall circuit was divided into logic blocks and the simulation environment Multisim was used to implement a virtual version of each one of them. Each block was then tested to see if it behaved as expected. The logic blocks were:

- Minutes and seconds monostables. They were tested for the correct output in response to the simulated Rugby input. Also the RC combination for each of them was cheeked to assure the correct pulse width.

- Units and tens of second counters. They were tested to ensure that they would reset properly and only count from 0 to 9 and from 0 to 5 respectively.
- Shift registers. They were tested to see if they were shifting and storing information correctly and that the configuration was executed properly.
- Latch/decoder/driver + 7 segment display. The pin connections were checked and the inputs to the decoder chip were hard codded as to check if the 7 segments display was showing the correct number.

When all the logic blocks were tested and confirmed that were working properly the same simulation environment, Multisim, was used to build a version of the overall circuit and test it.

The second phase of testing was done once the circuit was implemented in silicone on the breadboard. The microcontroller Arduino was used to feed inputs to different parts of the circuit an also to check if the outputs were as expected. Tests were conducted using the same logic blocks as depicted above.

Last before connecting the circuit to the rugby signal simulator continuity tests were conducted with the multimeter. The pulse with of each of the 3 monostables was checked with the oscilloscope to ensure the correct values.

Once all these tests were conducted the circuit was connected to the signal generator and finally to the rugby signal receiver itself.

The chips were placed on a breadboard and the wiring was done according to the Multisim schematic. The wire were colour coded as follows:

- Red - 5V
- Black – ground
- Blue – connection between the counters/shift registers to latch/decode/drive chips
- Green – connection from the latch /decode/drive chip to 7 segments display.
- Yellow – connection between the monostables and the rest of the components

The chips were placed in such a way as to minimize the use of the breadboard and also such that the wiring would not get messy. This was considered to be good practice, as it would facilitate visual inspection needed for further testing and troubleshooting.

Results

The tests performed on the Multisim environment showed that each logic block tested performed as desired. The test to the overall version of the circuit was unsuccessful due to a software error, which the group could not sort out.

Last the signal generator was connected and it was discovered that the pin configuration of the latch/decoder/driver chips was wrong due to human error.

After the correction has been made the circuit behaved flawlessly passing all tests to which it was subjected, decoding both the signal provided by the signal generator and the signal from the Rugby signal receiver.

Certain instability of the circuit was detected and after many checks of the connections and logic employed it was concluded that the breadboard was faulty and introduced a false reset signal due to which the counters were restarted.

Discussion/Conclusions

The design proved to be effective in decoding the signal and displaying the correct hour minute and displaying a synchronised count of the seconds. Due to a faulty breadboard it presented some instability. The team made a steady progress during the whole period without major time related pressure. Each of the team members contributed equally to the project.

A more careful consideration should be given to supplementary checks in order to avoid human errors like the one that occurred. Also a lesson learned was to perform a set of checks on the breadboard in order to ensure that a breadboard in good working order would be selected.

The exercise as a whole proved to be very engaging and it achieved its main objectives as a learning tool.

References

Fig 1 www.intersil.com/content/dam/Intersil/documents/cd40/cd4029bms.pdf

Fig 2 http://www.bdtic.com/datasheet/rohm/bu4538b-e.pdf

Fig 3 https://www.bucek.name/pdf/4015.pdf

Fig 4 http://www.ti.com/lit/ds/symlink/cd4013b.pdf

Fig 5 http://assets.nexperia.com/documents/data-sheet/HEF4543B.pdf

Fig 6 https://circuitdigest.com/article/7-segment-display\

Figure 7 http://www.lydiard.plus.com/msf.htm

Figure 8 https://en.wikipedia.org/wiki/Time_from_NPL

1 - http://www.npl.co.uk/science-technology/time-frequency/products-and-services/time/msf-radio-time-signal