计算机系统结构课程　第2次作业

黄昊　　*20204205*

- Consider the unpipelined processor. Assume that it has a *1ns* clock cycle and that it uses *4 cycles* for branches and stores and *5 cycles* for other operations. Assume that the relative frequencies of branch and store operations are *15% and 10%*, respectively.
- Consider a pipelined processor. Assume the slowest stage takes *1ns* and clock skew and register setup add *0.2 ns* to the clock period.
- **How much speedup in the instruction execution rate will we gain from an ideal pipeline?**

Solution:

execution time for **pipelined processor**: $1ns + 0.2ns = 1.2ns$
execution time for **unpipelined processor**: $(15\% + 10\%) \times 4 + (1 - 25\%) \times 5 = 4.75ns$
speedup: $4.75ns/1.2ns = 3.96$