计算机系统结构课程　第4次作业

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Given: A cache can hold 64 KByte data. Data are transferred between main memory and the cache in blocks of 4 bytes each. The main memory consists of 16 Mbytes, with each byte directly accessible by a 24-bit address.

A　How many cache blocks in the cache?

$$the\ number\ of\ cache\ block\ in\ the\ cache = \frac{64KB}{4B} = 16K = 2^{14}$$

B　How many blocks in the memory?

$$the\ number\ of\ cache\ block\ in\ the\ cache = \frac{16MB}{4B} = 4M = 2^{22}$$

C　For the direct-mapping cache, how many bits for tag and cache line in a memory address, respectively?

$$bits\ for\ tag = 24 - 14 - 2 = 8bits$$
$$bits\ for\ cache\ line = 4 \times 8 + 8 + 1 = 41bits$$

D　For the associative cache, how many bits for tag in a memory address?

$$bits\ for\ tag = 24 - 2 = 22$$

E　For the 4-way set associative cache, how many bits for tag and set[1] in a memory address, respectively?

$$bits\ for\ tag = 24 - 12 - 2 = 10$$
$$bits\ for\ set = 4 \times 8 \times 4 = 128bits$$
$$numbers\ for\ set = \frac{64KB}{4 \times 4B} = 4K = 2^{12}$$

F　How many tag comparisons are needed in each memory access for direct-mapping, associative and four-way set associate cache, respectively?

$$the\ number\ of\ comparisons\ in\ direct\ mapping : 1$$
$$the\ number\ of\ comparisons\ in\ associative : 2^{14}$$
$$the\ number\ of\ comparisons\ in\ four\ way\ set\ associate : 4$$

[1]Due to the ambiguous of the question, the bits for set and the number of set was both answered.