SC60 NFC

Reference Design

Smart LTE Module Series

Rev. SC60_NFC_Reference_Design_Rev.A

Date: 2018-04-20

Status: Released

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About the Document

History

Revision	Date	Author	Description
A	2018-04-20	Sea BAI	Initial

Contents

1 Reference Design

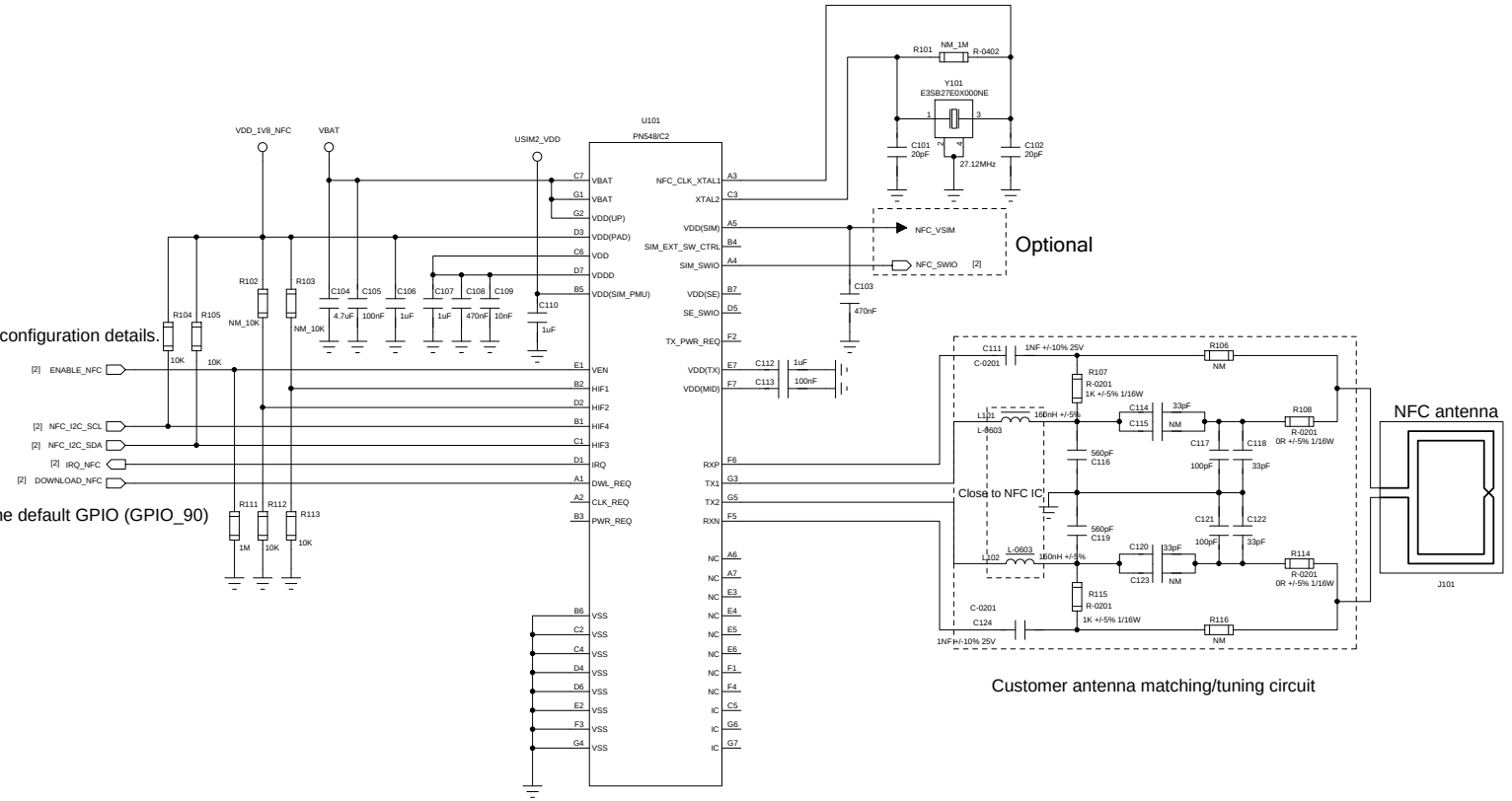
1.1. Introduction

This document provides the reference design for the connection between Quectel SC60 module and Near Field Communication (NFC) transceiver IC.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

NFC Peripheral Circuit



Please refer to the table below for I2C address configuration details.

IRQ_NFC needs wakeup interrupt. The default GPIO (GPIO_90) connected to it supports the function.

HIF2	HIF1	I2C address (R/W=0,write)	I2C address (R/W=1,read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

WRITE ADDRESS 0x50 READ ADDRESS 0x51

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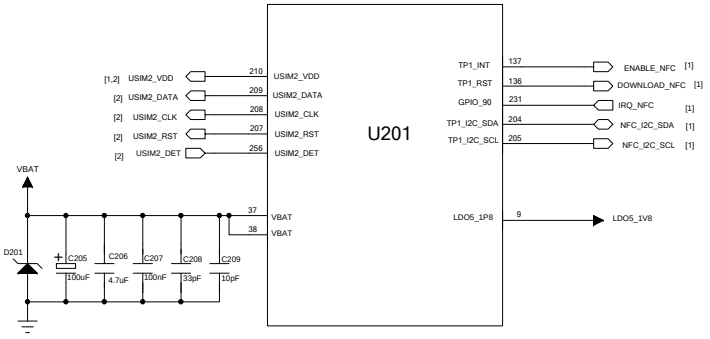
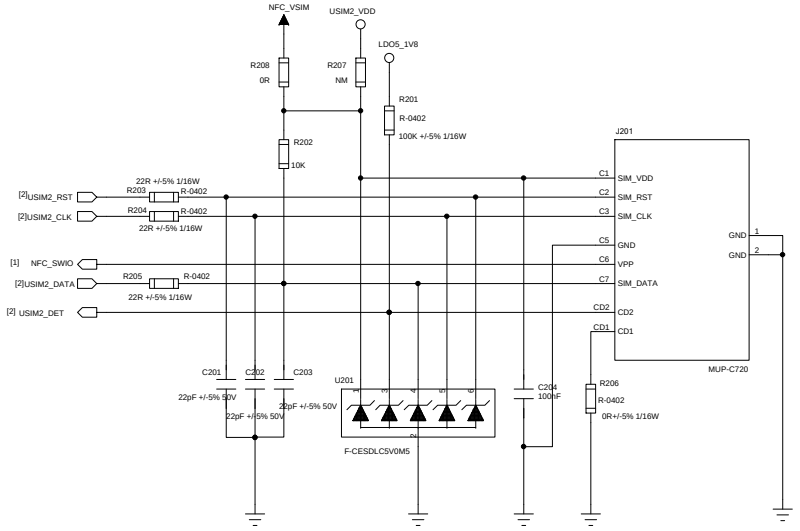
SC60 Module

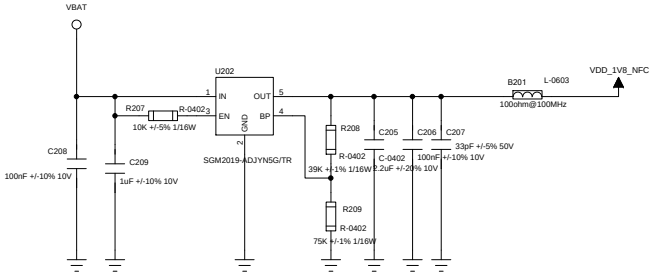


Note:
For more details about SC60 reference design, please refer to *Quectel_SC60_R1.0&R2.0_Reference_Design* or *Quectel_SC60_R1.1&R2.0_Reference_Design*.

Main (U)SIM



LDO Circuit for NFC



Notes:
1. VBAT can be connected to battery.
2. Vout=[(R208+R209)/R209]*1.207=1.83V

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