splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) asked a question.
12h ago (/s/question/0D5KZ00000uFXGr0AO/vivado-incorrectly-merges-srlc16e-blocks-and-rewires-d-input-to-the-wrong-signal)

Vivado incorrectly merges SRLC16E blocks and rewires D input to the wrong signal

Given the attached design, Vivado 2024.2 produces incorrect logic during implementation. The original RTL instantiates two separate SRLC16E blocks, each with its own D input:

```
SRLC16E #(.INIT(16'h6655)) _060_ (
  .A0(_017_), .A1(_017_), .A2(_013_), .A3(_013_),
  .CE(1'b1), .CLK(_019_), .D(_013_), .Q(_061_), .Q15(_062_)
);
SRLC16E #(.INIT(16'h07A0)) _065_ (
  .A0(_003_), .A1(_062_), .A2(_003_), .A3(_007_),
  .CE(1'b1), .CLK(_019_), .D(_029_), .Q(_066_), .Q15(_067_)
);
```

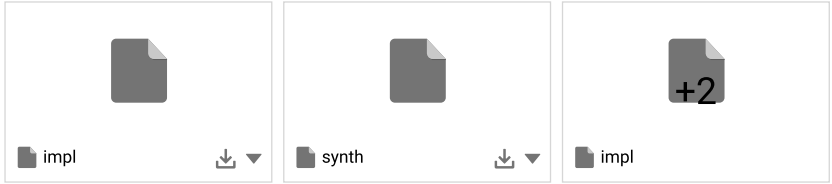
In the post-implementation output (write_verilog -mode funcsim), both SRLs are incorrectly merged into one SRLC32E block:

```
SRLC32E #(.INIT(32'h07A06655)) _060__065_ (
  .A({1'b1,_007_,_003_,NLW__060__065__A_UNCONNECTED[1],_003_}),
  .CE(1'b1), .CLK(_019_), .D(_013_), .Q(_066_), .Q31(_067_)
);
```

Critically, the D pin now only connects _013_ (originally only for the first SRL), and _029_ (connected to input _999_) is dropped. This results in incorrect data being shifted into the SRL and wrong values on _067_ (Which is connected to an output).

This violates functional equivalence.
The bug is triggered with the following files:

Vivado version: 2024.2
Device: xc7a35ticsg324-1L



IMPLEMENTATION (/S/TOPIC/0TO2E000000YKXVWAO/)

7 answers 74 views

You and drjohnsmith (/s/profile/0052E00000N2no4QAB) like this.

Top Rated Answers

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
3 hours ago

Hi @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) , I have filed a Change Request with the factory to look into this issue.
The optimization of SRL is happening during power_opt_design phase (before place_design phase) which is causing this issue.

For workaround, you can skip this power_opt_design step which you are running after opt_design phase.

Selected as Best Like Remove as Best

All Answers

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
Edited 6h ago

Sorry can't open folders on the phone
But .
Is this the entirety of the code ?
Functional equivalence is not down at the lut / register level , so it's possible the function of the overall is equivalent even if this particular sel is not. .

Like Reply Select as Best

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
3 hours ago

Hi @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) , I have filed a Change Request with the factory to look into this issue.
The optimization of SRL is happening during power_opt_design phase (before place_design phase) which is causing this issue.

For workaround, you can skip this power_opt_design step which you are running after opt_design phase.

Selected as Best Like Reply Remove as Best

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
an hour ago

Can I double check please @hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
This is described by @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) as a change in function, implied it's between code and post p and route
I.e. the code generated by the tools that goes into the dogs does NOT perform the same at the functional level as the code that was put into the synthesiser .
Your reply seems to say it's "just" a power consumption effect,
The former , a functional difference is MAJOR worry , whilst a power consumption of one SRL is a very minor worry.
Can you clarify please .

Like Reply Select as Best

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
an hour ago

Hi @drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member) ,
This concerned logic optimization has happened during power_opt_design phase which changed the netlist even before the placer started.

Like Reply Select as Best

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
an hour ago

So your saying the power_opt_dsesign can change the function of a design ,unit just optimise it , but change what a design does ?
Functional equivalent . you design a system that you put in say 2 and 3 and got answer 5 , and after the tool run makes the fpga, you put in 2 and 3 and get out 5.
Your saying that power_opt_design has changed a design so it's not functionaly equivalent, i.e after synthesis etc I could put in 2 and 3 and get out 6 !
That's a major bug .
This needs to be clarified please . .

Like Reply Select as Best

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
an hour ago

Hi @drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member) at least for this design, power_opt_design changed the netlist, which does not seem functionally equivalent.
You can check the same at your end using bug.v present here.
Though only power_opt_design at post opt stage causes the issue here.
There is post place power_opt_design phase as well which is not causing any issue.

So i can only provide further info on what went wrong at post-opt power_opt_design stage, post factory debug.

Like Reply Select as Best 1 like

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
44 minutes ago

Thank you
So your saying that the tools are changing the code written such that the generated fpga might not behave as your code says .
I.e. as per my example above , it's going to be possible because of the big that the output is wrong .
This is a very major bug .
I'll give you an hour to check , but if this is such a big the major companies I consult for are going to have to stop using xilinx parts !

Please be very aware of what your saying ..

Like Reply Select as Best

Write an answer...

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