splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) asked a question.
18h ago (/s/question/0D5KZ00000uqhzD0AQ/vivado-incorrectly-optimizes-away-an-alwayshigh-signal-during-optdesign)

Vivado incorrectly optimizes away an always-high signal during opt_design

When implementing the following design `bug.v` this part of the design:

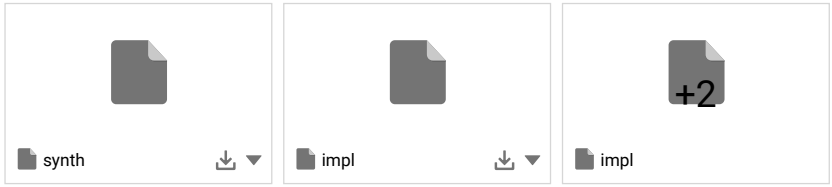
```
1  LUT1 #(.INIT(2'h3)) _103_ (.I0(_03_), .O(_04_));
2  LUT1 #(.INIT(2'h1)) _143_ (.I0(_04_), .O(_05_));
```

Should always ensure that _04_ is always 1'b1 and _05_ is always 1'b0. However after running opt_design both _04_ and _05_ are replaced with 1'b0 on the CFGLUT5 primitive.

This results in the wrong value on the I0 pin of CFGLUT5 giving the wrong values on the O5 and O6 pins.

This violates functional equivalence.
The bug is triggered with the following files:

Vivado version: 2024.2
Device: xc7a35ticsg324-1L



IMPLEMENTATION (/S/TOPIC/0TO2E000000YKXVWAO/)

9 answers 131 views

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Top Rated Answers

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
8 hours ago

Hi @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) I found functional equivalence difference in between post link and post opt netlist and hence filed a change request with the factory to look into it.

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All Answers

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
18 hours ago

You say functional equivilance

But you are loo,ing deep inside the fpga,
The tool are alowed to, if not encouraged to, optimise the design base, provided the function of the entirety is the same,
The tools are very clever ,
When you run the test bench of the complete codename are the resukts the same ?
you can not look at code before and after synthesis and expect every gate to be identical,

Like Reply Select as Best

splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London))
6 hours ago

Hi @drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member),

You're absolutely right that tools can optimize internals freely as long as functional equivalence is preserved. The issue here is that the optimization in opt_design changes behaviour, not just structure.
In this case, _04_ was supposed to be a constant 1'b1 , but was optimized to 1'b0, which then propagates incorrect values into a CFGLUT5. This isn't a minor gate change, it causes observable incorrect outputs.
We confirmed this by running post-synthesis vs. post-implementation simulations: the results differ. So this isn't just looking "too deep", it's a real functional mismatch.

Best,
splogdes

Like Reply Select as Best 1 like

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
6 hours ago

That's real scary!
Sorry I'm on phone , so can't look at your text files to easily
Is this a standalone bit of code, that one can test bench , and show the function after synthesis is different ?
My worry is I've been down this route before of "finding a bug" deep inside some function , in the post synthesis output compared to the pre p and r .
But the tools had been much cleverer than me and done some other changes in the code , that made the outputs all correct.
This is such a big thing if it's true , I've a few companies on tender hooked here .

Like Reply Select as Best

agertb (/s/profile/0054U00000Fh97iQAB) (AMD)
9 hours ago

Hi @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London))

If you want to prevent the tool from optimizing a specific cell or signal in the design, you can apply the DONT_TOUCH (https://docs.amd.com/r/en-US/ug901-vivado-synthesis/DONT_TOUCH) attribute by setting it in the RTL code.

To verify, check the elaborated or synthesized design to see if the LUT is present. If the LUT exists and has a DONT_TOUCH attribute applied, the implementation process will preserve it without modification.

Thanks,
Agert

Like Reply Select as Best

drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
9 hours ago

@agertb (/s/profile/0054U00000Fh97iQAB) (AMD)
I think your missing the point @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) is making , and that has us all very worried .

@splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) has made a few posts , with bits they say the tools are changing such that there code is no longer functioning the same as before synthesis.
Which is a BIG worry

Are you saying @agertb (/s/profile/0054U00000Fh97iQAB) (AMD) that to ensure the tools don't change the function of our code , we need to put don't touch on every part ?
Surely that would stop the tools optimising the code , which we all assume and want .

Either this is a real bug , and the tools are proven to have changed the function of the foga, or the tools can be trusted and the examples @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) shows are sub circuits that in the full function of the foga make no difference .

Which is it ?

Like Reply Select as Best

EdMoore (/s/profile/0054U00000EGWRMQA5) (Member)
Edited 7h ago

Does an init value of 2'h1 on an LUT1 really give you a constant output of 0 ?
2'h1 would give you an inverter.
2'h0 would give you a constant 0.

Like Reply Select as Best 1 like

splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London))
6 hours ago

Hi @EdMoore (/s/profile/0054U00000EGWRMQA5) (Member) ,

To clarify: the LUT init for _103_ is 2'h3, which always outputs 1'b1 regardless of input, it's a constant driver. This output connects to a second LUT (_143_) with 2'h1, which implements an inverter. So _04_ is always 1'b1, and _05_ is always 1'b0. Both _04_ and _05_ are then connected to the .I0 and .I1 ports respectively, of the CFGLUT5. After opt_design both these inputs are replaced by 1'b0, meaning input .I0 has been optimized incorrectly. This violates functional correctness. The logic driven by the CFGLUT5 changes as a result.

Best,
splogdes

Like Reply Select as Best

hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
8 hours ago

Hi @splogdes (/s/profile/005KZ000000duhKYAQ) (Imperial College London (London)) I found functional equivalence difference in between post link and post opt netlist and hence filed a change request with the factory to look into it.

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drjohnsmith (/s/profile/0052E00000N2no4QAB) (Member)
7 hours ago

@hemangd (/s/profile/0052E00000N2nMvQAJ) (AMD)
How can it not be a major error in the tools if we can not trust them not to change functionality?

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