Doc version: HME-P1(P060)DSE01, Feb. 2020
For more information about Pegasus Family, please go to www.hercules-micro.com

1. Overview

The HME-Pegasus P1P060 family is a low-power, high-performance and high-density FPGA device which supports the most advanced programmable logic, IO expansion, high bandwidth memory operation and high speed data communication. Built on a mature 40 nm process technology the Pegasus family offers a new, more efficient, 6-input lookup table (LUT) logic with dual-register and rich selection of built-in system-level blocks. These include 18 Kb (2 x 9 Kb) block RAMs, second generation DSP56V1 slices, DDR memory controllers and PHY, enhanced PLL, and clock management blocks, power optimized high-speed serial transceiver blocks, PCI Express® compatible Endpoint blocks, advanced system-level power management modes, 1MSPS XADC, auto-detect configuration options, and enhanced IP security with AES protection. Pegasus P1P060 family offers the best solution for high-volume logic designs, high-speed computing designs, and high-performance demand applications.

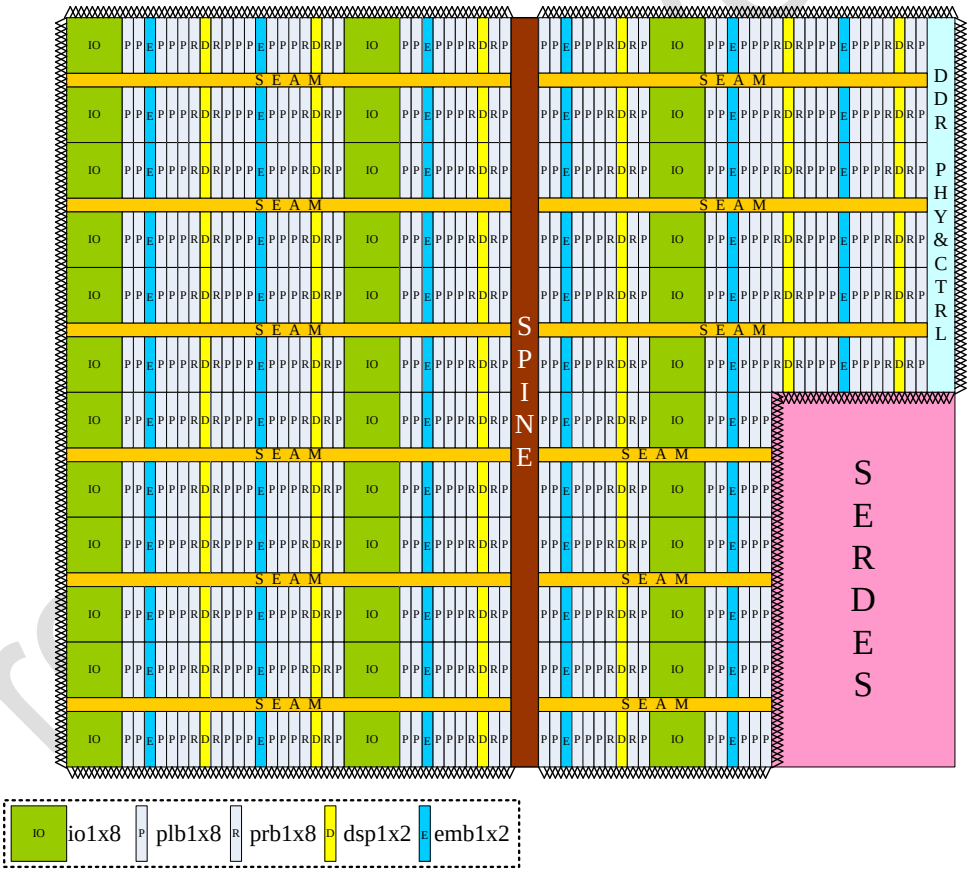


Figure 1 HME-Pegasus FAMILY FPGA Architecture

Feature

- **SRAM-based FPGA Fabric**
  - 36,864 6-input LUTs
  - 73,728 DFF-based registers
  - Fast carry chain and multiplexer
  - Up to 576Kb LRAM
- **Embedded RAM Block Memory**
  - Dual-port memory 18 Kb EMB blocks
  - One 18K EMB block can be configured to 2*9 Kbits or 4*4.5 Kbits EMB blocks independently
  - Support hard FIFO
  - Support ECC
- **Embedded DSP Blocks**
  - One 36x18 or two 18x18 Multipliers
  - Flexible Pre-adder
  - Dedicated Pipeline Registers and Cascading Wires
  - Arithmetic Logic Operations
  - Overflow/Underflow and Equality Detection
- **Clock Resources**
  - Differential or single-end clock input
  - 32 global clock sources
  - 4xPLLs support frequency multiplication, frequency division, phase-shifting, and de-skew
- **Multi-voltage, multi-standard, multi-bank I/O**
  - Support LVTTL / LVCMOS 33/25/18/15/ 12 IO standards
  - Support PCI/PCI-X IO standards
  - Support LVDS, RSDS, PPDS, TMDS, Mini-LVDS, LVPECL differential IO standards
  - Up to 1.3 Gb/s data transfer rate per differential LVDS I/O
  - Support MIPI D-PHY emulated
  - Support hot swap
- **Hardened Memory Controller and PHY**
  - Support 32/16-bit DDR2/3
  - Data rates up to 1333 Mb/s
  - Two SDII/AXI bus
  - Support ECC
- **High-speed Serial Transceiver**
  - Integrate universal PCS function
  - Support 8b/10b,64/66b codec
  - Data rates from 300M ~ 6.5Gb/s
  - Dynamic reconfiguration
  - Support PCI-E/SGMII/XAUI/Serial Rapid IO/CPRI (1-10X)/JESD204B protocol
- **Hard PCI Express**
  - Gen1/2 End Point, Root Complex
  - 2.5G/5G x1/2/4 channels Transceiver
- **Dual 12-bit 1MSPS ADC**
  - Up to 14 channels
  - Monitor chip temperature and voltage
- **Configuration**
  - JTAG mode
  - Active serial mode(x1/2/4 wire)
  - Passive serial mode(x1/8/x16 wire)
  - Support bitstream compression
  - Support SEU detection
- **Security**
  - Encrypted bitstream with 256-bit AES
  - One-time program EFUSE for 256-bit AES key

Feature Summary

Table 1 Feature Summary by Device

Part Number		P1P060
Programmable Logic Block (PLB)	Logic cells	58,982
	LUT6	36,864
	Register (DFF-based)	73,728
Embedded Memory Block (EMB)	LRAM	576 Kb
	18Kb EMB	144
	9Kb EMB	288
	Total EMB	2,592 Kb
Clock & PLL	PLL	4
	Global Clock	32
DSP	DSP Slice (DSP56V1)	144
	18 x 18 Multiplier	288
Hard IP	PCI Express Gen1/2	1
	DDR2/3 (PHY & controller) (1)	1
	Transceiver | Configurable 300M~6.5G	4
	XADC(1MSPS) (2)	2
Package(unit: mm)		Max User I/O (LVDS pair)
FBGA784(29x29x0.5)		477 (144)
VFBGA324(15x15x0.5)		209 (64)

Table 2 Device-Package Combinations and Available I/Os

Package	Dimensions (mm*mm)	Transceiver	DDR
VFBGA324	15*15	0	16b
FBGA784	29*29	4	32b

Notes:

(1) All the DDR pin can't be used as I/O if the DDR IP is used.

(2) The ADC can be used to monitor the internal chip temperature and voltage.

This part introduces the Pegasus family with its PLB, EMB, DSP, clock resources, PLL, DLL, and I/Os

2. FPGA

Programmable Logic Block (PLB)

The Programmable Logic Block (PLB) is the fabric basic logic tile that is composed of Logic Element (LE) and Xbar. The PLB is the basic tile of the fabric. Their organization is shown in the figure below. One Logic Element (LE) contains eight interconnected Logic Parcels (LP). The Logic Element (LE) constitutes the main logic resource for implementing synchronous as well as combinatorial circuits.

The Xbar switches and passes the signals between the tile elements.

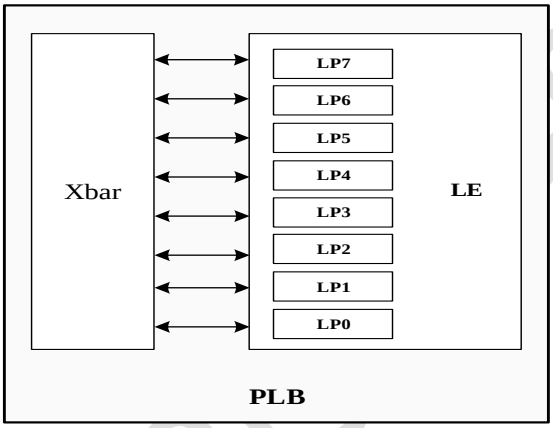


Figure 2 PLB Schematic Diagram

The LP is the basic programmable logic element, and has the following elements in common to provide logic and arithmetic functions:

- **One 6-input LUT**
- **Two register elements**
- **Carry, cascade, shift and arithmetic logic**
- **Fast wide multiplexer**

LRAM Block

The LRAM is a distributed embedded RAM which can be used as 32b or 64b memory. The features are shown below:

- **One LRAM used as one LRAM64**
- **One LRAM used as two LRAM32**
- **One LRAM used as one SR32**
- **One LRAM used as two SR16**
- **Support single/dual port write/read operation**

Embedded Memory Block

HME-Pegasus family device supports embedded memory block (EMB), which is organized as one column of EMB18K. EMB18K module is a true dual-port memory that permits independent access to the common EMB block. Each port has its own dedicated set of data, control, and clock lines for synchronous read and write operations.

EMB18K provides the features as below:

- **18 Kbits**
- **EMB18K can be used as four 4.5 Kb or two 9 Kb EMB independently**
- **Mixed clock mode**
- **A, B data width configured independently**
- **Support write/read first or through output mode**
- **Bypass or register output**
- **Configurable normal RAM or FIFO mode**
- **One 64-bit Error Correction Coding block is provided per EMB18K**
- **Initialization file to pre-load memory content in RAM and ROM modes**
- **Three Memory Modes available(tdp、sdp、sp)**

EMB18K Port Definitions

The dual-port primitive EMB18K signals are defined in the following table.

Table 3 EMB18K Port Definition

Port Name	Type	Width	Description
clka	I	1	Input clock for port A
cea	I	1	Chip enable for port A
wea	I	1	Write enable for port A
aa	I	12	Address line for port A
da	I	18	Data input for port A
clkb	I	1	Input clock for port B
ceb	I	1	Chip enable for port B
web	I	1	Wire enable for port B
ab	I	12	Address line for port B
db	I	18	Data input for port B
q	O	18	Memory data q output
wq_in	I	9	Input from paired EMB5K for wide true dual port mode

Port Name	Type	Width	Description
wq_out	O	9	Output to paired EMB5K for wide true dual port mode

Table 4 *EMB18K Parameters*

Parameters	Type	Description
modea_sel	string	Port a usage mode setting: 256x18, 512x9, 1kx4, 2kx2, 4kx1, wtdp (wide true dual port) Default: 256x18
modeb_sel	string	Port b usage mode setting: 256x18, 512x9, 1kx4, 2kx2, 4kx1, wtdp (wide true dual port) Default: 256x18
porta_wr_through	string	Bypassing of write data from write port to read port enable for port a, true or false Default: false
portb_wr_through	string	Bypassing of write data from write port to read port enable for port b, true or false Default: false
init_file	string	EMB initial file Default: “” (No initial file)
operation_mode	string	EMB working mode, just for simulation true_dual_port, single_port, simple_dual_port
porta_data_width	string	EMB port a data width
portb_data_width	string	EMB port b data width

EMB18K Operations

Writing data to and accessing data from the EMB18K are synchronous operations that take place independently on each of the two ports.

When the we and ce signals enable the active edge of clk, data at the d input bus is written to the EMB5K location addressed by the a lines. There are two write actions which are selected by wr_through parameter. The write data is also passed to q output bus if the wr_through is true during the writing process. The q output bus value will be the previous read output value during the writing process if the wr_through is false. The two operation waveforms are shown in ***Figure 3*** and ***Figure 4***.

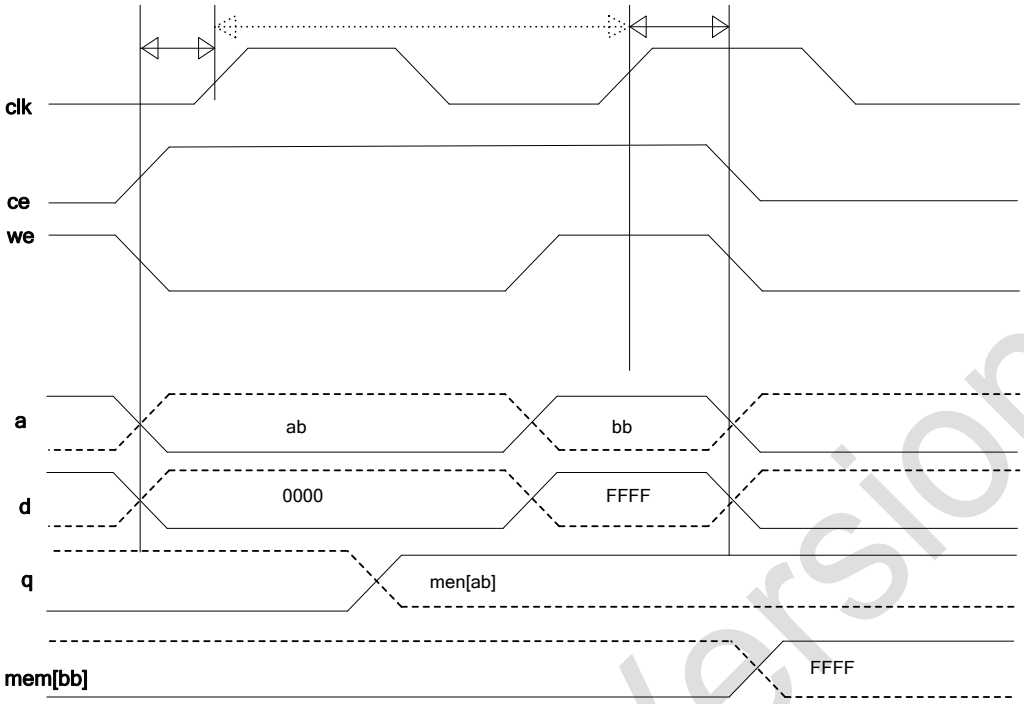


Figure 3 wr_through is false Waveform

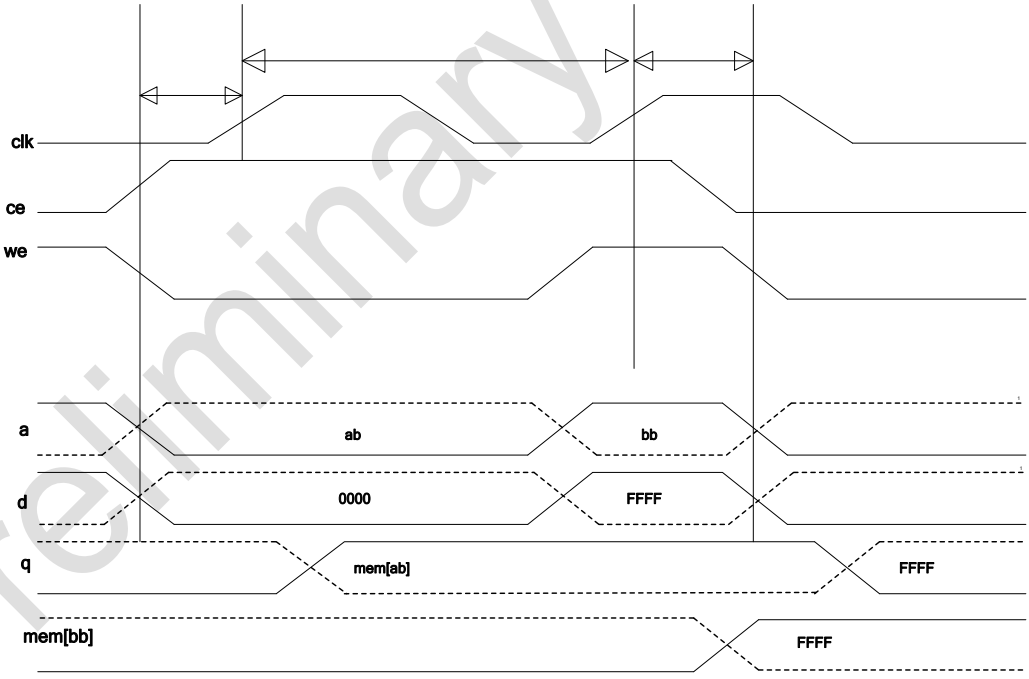


Figure 4 wr_through is true Waveform

EMB18K Operation Mode

EMB18K True Dual-port

EMB18K supports any combination of dual-port operation: two read ports, two write ports, or one read and one write at different clock frequencies. The following figure shows true dual-port memory configuration.

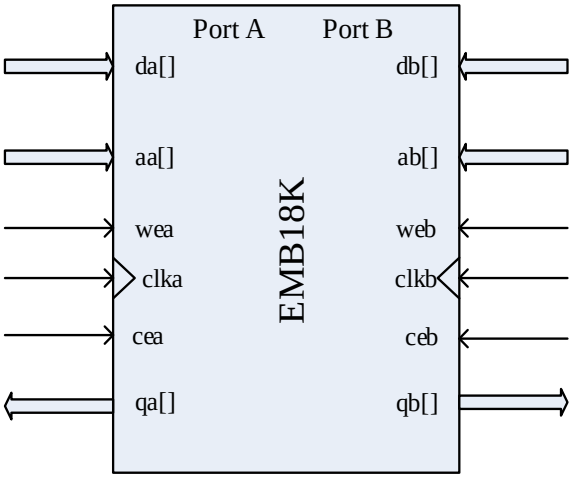


Figure 5 True Dual-port Memory Mode

Table 5 Port Descriptions of True Dual-port Memory Mode

Port Name	Type	Description
aa (b)	Input	Port A (B) Address.
da (b)	Input	Port A (B) Data Input.
qa (b)	Output	Port A (B) Data Output.
wea (b)	Input	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both wea (b) and cea (b) are high.
cea (b)	Input	Port A (B) Enable. When cea (b) is high and wea (a) is low, data read from the dual-port SRAM address aa (b). If cea (b) is low, qa (b) retains its value.
clka (b)	Input	Port Clock.

EMB18K Simple Dual-port

EMB18K also supports simple dual-port memory mode: one read port while one write port. The following figure shows simple dual-port memory configuration.

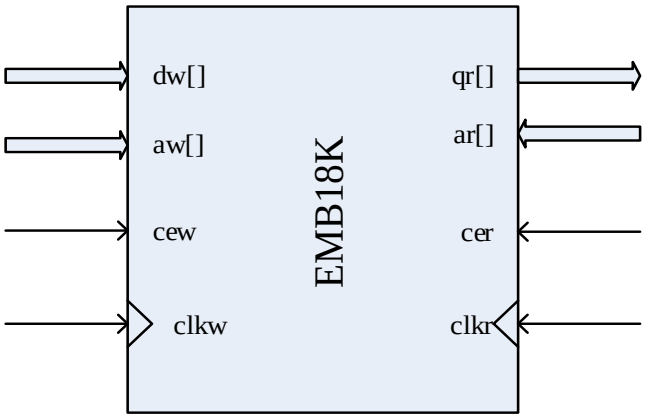


Figure 6 Simple Dual-port Memory Mode

Table 6 Port Descriptions of Simple Dual-port Memory Mode

Port Name	Type	Description
dw	Input	Write Data
aw	Input	Write Address
clkw	Input	Write Clock
cew	Input	Write Port Enable. Active high.
qr	Output	Read Data
ar	Input	Read Address
cer	Input	Read Enable. Active high
clkr	Input	Read Clock

Table 7 Simple Dual-port Configurations

W Port	Read Port						
	4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18
4K × 1	√	√	√	√			
2K × 2	√	√	√	√			
1K × 4	√	√	√	√			
512 × 8	√	√	√	√			
512 × 9					√		
256 × 16	√	√	√	√		√	
256 × 18							√

EMB18K Single-port

EMB18K also supports single-port memory mode as shown in the figure below.

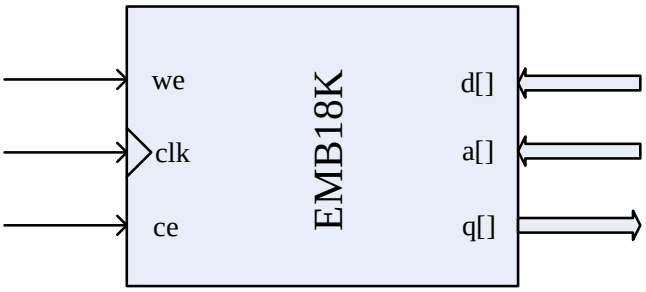


Figure 7 Single-port Memory Mode

Table 8 Pin Description of Single-port Memory Mode

Port Name	Type	Description
d	Input	Write Data
a	Input	Write Address.
we	Input	Write Enable. Active high.
clk	Input	Write Clock.
ce	Input	Port Enable. Active high.
q	Output	Read Data

Table 9 Single-port Configuration

Port						
4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18

Conflict Avoidance

In the dual-port memory mode, both ports can access any memory address at any time. When both ports access the same address, the read and write behavior should observe certain clock timing restrictions. These restrictions are applicable to both synchronous and asynchronous clocks.

DSP Block

The HME-Pegasus family devices have DSP MAC tiles that can implement DSP applications such as many binary multipliers and accumulators.

DSP tile contains one 36 x 18 bit two's complement multiplier and a 56-bit sign-extended accumulator, which is a function that is widely used in digital signal processing (DSP). Programmable pipelining of input operands, intermediate products, and accumulator outputs enhances throughput.

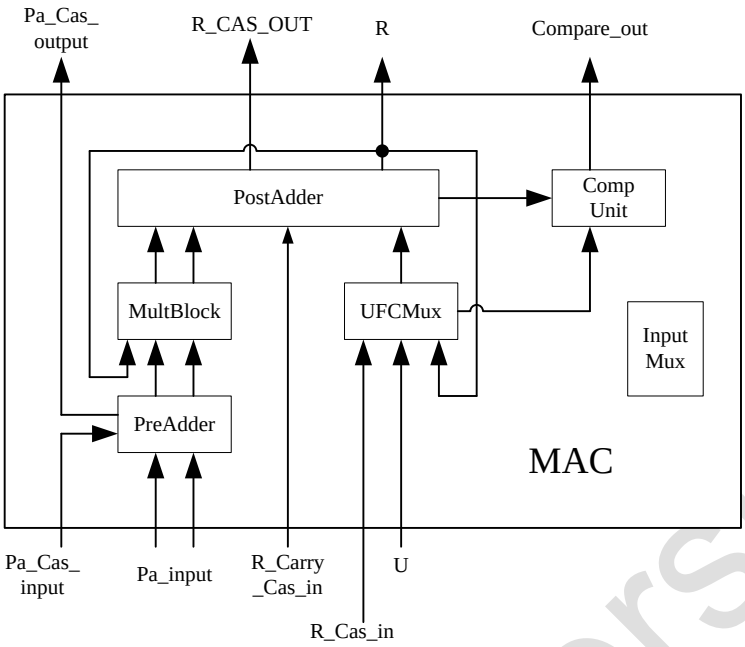


Figure 8 DSP block diagram

DSP provides features as below:

- **36 x 18 bit, two's complement multiplier with a full-precision 56-bit result**
- **One DSP supports two independent 18x18 multipliers**
- **Flexible pre-adder with optional registered input**
- **Flexible 56-bit post-accumulator/subtraction with optional registered feedback**
- **Registers, ensuring maximum clock performance and highest possible sample rates with no area cost**
- **Comparison Unit to check Equality**

Clock Resources

The HME-Pegasus family devices provide abundant clock lines to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew. Global clocks are often driven from the PLLs and clock input pins.

PLL

The PLL is a general-purpose, high-performance PLL-based clock generator, which serves as a frequency synthesizer for a wider frequency range. It can also be used as a clock buffer through a bypass mode. The PLL has programmable output frequency configured using an 8-bit input divider (DIVN), an 8-bit feedback divider (DIVM), a 1-bit VCO-post divider (DIVFB) and six 8-bit output dividers (DIVCx).

The PLL provides the features as below:

- **PFD comparison frequency: 10MHz~450MHz**
- **VCO operation frequency: 600MHz~1400MHz**

- Output frequency: 1.17MHz~700MHz
- Clock switchover support(Manual or Automatic mode)
- Internal center spread spectrum clock generating(SSCG), also support a spread spectrum input with typical modulation frequencies
- 6 single-ended output clocks
- A fractional divisor (non-integer) divider support
- Support dynamic phase shift
- Deskew mode
- Lock detector
- Power-down mode
- Bypass mode

Input/Output (I/O)

The Input/output Block (IOB) provides a programmable, bidirectional interface between the I/O pin and the FPGA internal logic.

All I/O pins are organized into banks that include the general I/O banks, LVDS I/O banks, DDR I/O banks, configuration I/O banks, and ADC analog bank. Each bank has several common VDDIO output supply-voltage pins, which also powers certain input buffers.

I/O provides the features as below:

- Support LVTTL/ LVCMOS 33/25/18/15/12 IO standards
- Support PCI/PCI-X IO standards
- Support LVDS, RSDS, PPDS, TMDS, Mini-LVDS differential IO standards
- Up to 1.3 Gb/s data transfer rate per differential LVDS I/O
- Support MIPI D-PHY standards emulated
- Support LVPECL differential IO standards
- Support SSTL 18/15 Class I, II single-end/differential IO standards
- Programmable slew rate controlled
- Programmable driving strength
- Programmable pull-up/down bus-keeper
- Programmable input/output delay
- Programmable 1:N(2/4/6/8/10/12/14/16) DDR serializer
- Programmable 1:N(2/3/4/5/6/7/8) SDR serializer
- Support Fast IO
- Inserting PCI clamping diode in
- Support hot socketing

3. System Resources

High-speed Serial Transceiver

All HME-Pegasus P1P060 family devices have gigabit transceiver circuits. Each transceiver is a combined transmitter and receiver, which is capable of operating at data rates from 300 M ~ 6.5 Gb/s. The transmitter and receiver are independent circuits that use PLL to multiply the reference frequency input to become the bit-serial data clock.

The features of Transceiver are shown as below

- **Integrate universal PCS function (8b/10b, 64/66b)**
- **Data rates from 300M ~ 6.5 Gb/s**
- **Dynamic reconfiguration (Change protocol and speed on-the-fly)**
- **Support PCI-E/SGMII/XAUI/Serial Rapid IO/CPRI (1-10X)/JESD204B protocol**

Integrated PCI Express Endpoint Block

The PCI Express standard is a packet-based, point-to-point serial interface standard. The differential signal transmission uses an embedded clock, which eliminates the clock-to-data skew problems of traditional wide parallel buses.

The PCI Express Base Specification 3.0 Specification, revision 2.0 defines bit rate of 5 Gb/s per lane, per direction (transmit and receive). When using 8B/10B encoding, this supports a data rate of 5 Gb/s per lane.

The HME-Pegasus P1P060 Pfamily devices include one integrated Endpoint block for PCI Express that is compliant with the PCI Express Base Specification 3.0 Specification, revision 1.0. The PCIe block implements three PCI Express protocol layers (Transaction layer, Data Link Layer, and the MAC portion of the Physical Layer). It also implements your application dependent functionality of the PCI Express Transaction Layer for packet transmission, which is located between your application logic and the PCI Express protocol layers.

The Physical Layer is split across the PIPE such that the MAC functionality (LTSSM, lane-to-lane deskew) is in the core and the PHY functionality is implemented in the PIPE-compliant PHY.

The PIPE interface is internal to the core. The external interface for the PHY consists of one or more transmits, and receives differential pairs.

Hardened DDR2/3 Memory Controller and PHY

The DDR memory PHY provides control features to ease the customer implementation of digitally controlled features of the PHY, such as initialization, DQS gate training delay line calibration and VT

compensation, write leveling, and programmable configuration controls. Customers access the external DDR2/3 memory as only a memory via the hard DDR memory controller through the PHY.

- **DDR2-400 to 1066 Mbps, DDR3-800 to 1333 Mbps**
- **DDR2 controller function compliance to JEDEC standard JESD79-2E**
- **DDR3 controller function compliance to JEDEC standard JESD79-3C**
- **Support ECC function**
- **Support BIST (built-in-self-test) function**
- **2 SDII/AXI port**

Dual 12-bit 1MSPS ADC

The 12-bit ADC is a successive approximation analog-to-digital converter. It has up to 16 multiplexed channels that allow to measure signals from 14 external sources and two internal sources which are the power and temperature sensor. The A/D conversion of the channels can be performed in single, continuous, scan or discontinuous mode.

The analog watchdog feature allows the application to detect if the input voltage goes beyond the user-defined, higher or lower thresholds.

- **Supports Dual 12-bit 1MSPS ADC**
- **Operation mode: Consecutive, continuous, single-scan, offset calibration, gain calibration conversion**
- **Monitor internal power supply voltage and temperature sensor**
- **Dedicated 2 pairs analog inputs for eliminating the noise rejection**
- **12 general analog inputs**

Configuration

The HME-Pegasus SRAM devices can be configured as follows:

- **AS (Active Serial) mode with SPI(x1/2/4) interface to external SPI Flash**
- **PS (Passive Serial) mode, the external master configure the device via the SPI interface.**
- **PP (Passive Parallel) mode, the external master can configure the device via the parallel interface.**
- **JTAG mode, the external master can configure the device via the standard JTAG interface.**

In addition to the flexible configuration modes, the Pegasus configuration engine supports the following special features:

- **Bitstream compression**
- **Bitstream AES encryption and decryption**
- **SEU detection**

4. DC & Switching Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

DC Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed in table below: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods adversely affects device reliability.

Table 10 Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Units
VDD_CORE	Internal supply voltage		-0.5	1.1	V
VDDIO	I/O driver supply voltage		-0.5	3.75	V
VIN	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	GND-0.2		V
	Voltage applied to all Dedicated pins		GND-0.2		V
VESD	Electrostatic Discharge Voltage	Human body model(1)	0	±2000	V
		Charged device model(2)	-	±500	V
		Machine model	-	±200	V
TJ	Junction temperature		-40	125	°C
TSTG	Storage temperature		–65	150	°C

Notes:

(1) For DDR SerDes, the maximum rating is ±1000V.

(2) For DDR SerDes, the maximum rating is ±250V.

Power Supply Specifications

Table 11 Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
VDDT	Threshold for the VDD core supply		0.75	V
VDDIO33T	Threshold for the VDDIO33 supply		2.1	V

Table 12 Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
VDDR	Ramp rate from GND to valid VDD supply level	10		us
VDDIO33R	Ramp rate from GND to valid VDDIO33 supply level	10		us

General Recommended Operating Conditions

Table 13 Recommended Basic Operating Conditions

Symbol	Parameter	Min	Typ	Max
TJ	Junction temperature	-40°C	25°C	125°C
VDD	Core power	0.855V	0.9V	0.945V
DDR_AVDD_PLL	DDR PLL power	2.25V	2.5V	2.75V
VDDIO33	Internal supply power	2.25V	3.3V	3.465V
VDDADC	ADC Power @ 3.3V	3.135V	3.3V	3.465V
	@2.5V	2.375V	2.5V	2.625V
VDDIO_x(1), (2)	I/O supply voltage @ 3.3V(1)	2.97V	3.3V	3.63V
	@2.5V	2.375V	2.5V	2.625V
	@1.8V	1.71V	1.8V	1.89V
	@1.5V	1.425V	1.5V	1.575V
	@1.2V	1.14V	1.2V	1.26V
V_I	Input Voltage	-0.5	-	VDDIO +0.3
V_O	Output Voltage	-0.3	-	VDDIO
I_L	Input Leakage Current	±1μA		

Notes:

(1) VDDIO_301,302,303 must be not above 2.5V if these banks are used as single-end I/O.

(2) DDR I/O banks can only be used as one bank if DDR I/O are used as general I/O, and the DDR I/O can be used as general I/O even the DDR is used as 8/16 bit mode.

General Core Leakage Current

Table 14 General Leakage Current

Symbol	Parameter	Min	Typ	Max
I_{slc}	Static leakage core supply current		150mA	

General DC Characteristics for I/O Pins

Table 15 I/O Pin Leakage Current

Symbol	Parameter	Min	Typ	Max
I_{ozl}	Tri-stated I/O pin leakage Current	-10uA	-	10uA
I_{IL}	Input Leakage Current	-10uA	-	10uA
I_{IOL}	VCC I/O leakage current(@3.3V)		TBD	

Table 16 Single-ended I/O Pin Driving Strength

Supported Voltage and Current Capabilities	Attributes	Value
Drive strength	I/O supply voltage @ 3.3V	2mA
		4mA
		8mA
		12mA
		16mA
		24mA
	I/O supply voltage @ 2.5V	2mA
		4mA
		8mA
		12mA
		16mA
	I/O supply voltage @ 1.8V	2mA
		4mA
		8mA
		12mA
	I/O supply voltage @ 1.5V	2mA
		4mA
		8mA
	I/O supply voltage @ 1.2V	2mA
		4mA

Table 17 Single-ended I/O Pull-Up and Pull-Down Resistor

Symbol	Parameter	Min	Typ	Max	Units
R_{PU}	Value of the I/O pin pull-up resistor		75		kΩ
R_{pd}			50		kΩ

Table 18 Hot-Swapping

Symbol	Parameter	Min	Typ	Max	Units
I_{HSDC}	DC current per I/O pin		TBD		uA
I_{HSAC}	AC current per I/O pin		TBD		mA

I/O Standard Specifications

Table 19 Single-ended I/O Standard Input DC Specifications

I/O Standard	VDDIO (V)			Vil (V)	Vih (V)
	Min	Typ	Max	Max	Min
3.3V LVTTL and LVCMOS	3.135	3.3	3.465	0.8	1.7
2.5V LVTTL and LVCMOS	2.375	2.5	2.625	0.7	1.7
1.8V LVTTL and LVCMOS	1.710	1.8	1.890	0.35 x VDDIO	0.65 x VDDIO
1.5V LVTTL and LVCMOS	1.425	1.5	1.575	0.35 x VDDIO	0.65 x VDDIO
1.2V LVTTL and LVCMOS	1.14	1.2	1.26	0.35 x VDDIO	0.65 x VDDIO

Table 20 Single-ended I/O Standard Output DC Specifications

I/O Standard	Test Conditions		Voltage Threshold	
	Iol (mA)	Ioh (mA)	Maximum Vol (V)	Minimum Voh (V)
3.3V LVTTL	4	-4	0.4	2.4
3.3V LVCMOS	0.1	-0.1	0.4	VDDIO – 0.4
2.5V LVTTL and LVCMOS	1	-1	0.4	VDDIO – 0.4
1.8V LVTTL and LVCMOS	2	-2	0.45	VDDIO – 0.45
1.5V LVTTL and LVCMOS	2	-2	25%VDDIO	75%VDDIO
1.2vLVTTL and LVCMOS			25%VDDIO	75%VDDIO

Table 21 Differential I/O Standard Input DC Specifications

I/O Standard	VDDIO (V)			Vid (V)			Vicm (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	2.375	2.5	2.625	0.1	0.35	0.6	0.1		2.0
Mini-LVDS	2.375	2.5	2.625	-	-	-	-	-	-
RSDS	2.375	2.5	2.625	-	-	-	-	-	-

Table 22 Differential I/O Standard Output DC Specifications

I/O Standard	Vod (mV)			Delta(Vod) (mV)			Vocm (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
LVDS	250	350	600			50	1.075	1.25	1.425
Mini-LVDS	300	450	600	-	-	50	1.0	1.2	1.4
RSDS	100	200	600	-	-	50	0.5	1.2	1.5
BLVDS		600					1.075	1.25	1.425
TMDS	350	425	550					VDDIO - 0.36	VDDIO + 0.2

DDR DC Specifications

Table 23 DDR3 Recommended Operation Voltages

Symbol	Parameter	Min	Nom	Max
DDR_VDDP	DDR3 IO post-driver	1.425V	1.5V	1.575V
DDR_VDD	DDR3 pre-driver and core logic power	0.855V (1)	0.9V	0.945V
DDR_VREF	DDR3 IO reference voltage	$0.49*V_{DDR\_VDDP}$	$0.5*V_{DDR\_VDDP}$	$0.51*V_{DDR\_VDDP}$
DDR_AVDD_PLL	PLL analog power	2.25V	2.5V	2.75V
V_I	Input voltage	0V		1.575V
V_O	Output voltage	0V		1.575V
V_{IC}	Core input voltage	0V		1.0V
V_{OC}	Core output voltage	0V		1.0V
T_J	Junction temperature	-40°C	25°C	125°C

Table 24 DDR2 Recommended Operation Voltages

Symbol	Parameter	Min	Nom	Max
DDR_VDDP	DDR2 IO post-driver power	1.7V	1.8V	1.9V
DDR_VDD	DDR2 pre-driver and core logic power	0.855V (1)	0.9V	0.945V
DDR_VREF	DDR3 IO reference voltage	$0.49*V_{DDR\_VDDP}$	$0.5*V_{DDR\_VDDP}$	$0.51*V_{DDR\_VDDP}$
AVDD_PLL	PLL analog power	2.25V	2.5V	2.75V
V_I	Pad input voltage	0V		1.9V
V_O	Pad output voltage	0V		1.9V
V_{IC}	Core input voltage	0V		1.0V

Symbol	Parameter	Min	Nom	Max
V_{OC}	Core output voltage	0V		1.0V
T_J	Junction temperature	-40°C	25°C	125°C

Notes:

(1) The power spec. is the supply voltage and related ground difference, which is measured on the ball when the DDRPHY is in operation. System designers should make sure the PDS (power delivery system) can deliver high enough power into the DDRPHY. Generally, power delivery from system should be normal voltage, and leave 10% voltage IR drop in PCB and package. DDRPHY does not guarantee the operation when power and ground difference drops below the minimum power spec. It does not cover the detrimental IR drop caused by the package or PCB design. The system designer should add enough margins to power for the IR drop when defining the system power specification.

Table 25 DC Electrical Specifications for DDR3

Symbol	Parameter	Conditions	Min	Nom	Max
DDR_V_{DDP}	SSTL_15 IO voltage		1.425V	1.5V	1.575V
DDR_V_{REF}	SSTL_15 reference voltage		0.49*DDR_ V_{DDP}	0.5* DDR_ V_{DDP}	0.51* DDR_ V_{DDP}
V_{TT}	SSTL_15 termination voltage	0.5* DDR_V_{DDP}	0.49* DDR_ V_{DDP}	0.5* DDR_ V_{DDP}	0.51* DDR_ V_{DDP}
$V_{IH(DC)}$	DC logic input high		DDR_ V_{REF}+0.1V		DDR_ V_{DDP}
$V_{IL(DC)}$	DC logic input low		0		DDR_ V_{REF}- 0.1V
$V_{OH(DC)}$	DC logic output high			0.8* DDR_ V_{DDP}	
$V_{OL(DC)}$	DC logic output low			0.2* DDR_ V_{DDP}	
RON_{34PU}	Driver DC pull-up resistance (34 Ω)	VOUT=0.5*V_{DDR_VDDP}	30.6 Ω	34 Ω	37.4 Ω
RON_{34PD}	Driver DC pull-down resistance (34 Ω)	VOUT=0.5*V_{DDR_VDDP}	30.6 Ω	34 Ω	37.4 Ω
RON_{40PU}	Driver DC pull-up resistance (40 Ω)	VOUT=0.5*V_{DDR_VDDP}	36 Ω	40 Ω	44 Ω
RON_{40PD}	Driver DC pull-down resistance (40 Ω)	VOUT=0.5*V_{DDR_VDDP}	36 Ω	40 Ω	44 Ω

Table 26 DC Electrical Specifications for DDR2

Symbol	Parameter	Conditions	Min	Nom	Max
DDR_V_{DDP}	SSTL_18 IO voltage		1.7V	1.8V	1.9V
DDR_V_{REF}	SSTL_18 reference voltage		0.49* DDR_ V_{DDP}	0.5* DDR_ V_{DDP}	0.51* DDR_ V_{DDP}
V_{TT}	SSTL_18 termination voltage	0.5*V_{DDR_VDDP}	DDR_ V_{REF}-40mV	DDR_ V_{REF}	DDR_ V_{REF}+40mV
$V_{IH(DC)}$	DC logic input high		DDR_ V_{REF}+0.125 V		DDR_ V_{DDP}
$V_{IL(DC)}$	DC logic input low		0		DDR_V_{REF}-0.125V
$V_{OH(DC)}$	DC logic output high		2		
$V_{OL(DC)}$	DC logic output low				2
RON_{PU}	Driver DC pull-up resistance		33.75Ω(1)	37.5Ω(1)	41.25Ω(1)
RON_{PD}	Driver DC pull-down resistance		33.75Ω(1)	37.5Ω(1)	41.25Ω(1)

Notes:

(1) The RON_{Pu} and RON_{PD} in DDR2 IO cascade a 20Ω serial resistor internally, so the RON_{Pu} and RON_{PD} = (17.5Ω+20Ω) = 37.5Ω. There is no Rs (serial resistor) needed in PCB design when using DDR2 application.

*(2) The maximum VOH (DC) and minimum VOL (DC) value depends on the driver RON, terminator voltage and terminator resistor value, the requirement of the VOH (DC) and VOL (DC) is to make sure that the input voltage of receiver could meet the VIH (DC) and VIL (DC) specification. For example, if terminator is 25Ω and V_{TT} = 0.793v, DDR_Vref = 0.833v and DDR_VDDP = 1.7v, the VOH (DC) min = (1.7v- 0.793v)*25Ω/(25Ω+41.25Ω)+0.793v = 1.1352v. VIN – DDR_Vref= 0.302v, which is larger than VIH (DC) = 0.125v and if terminator is 25Ω and V_{TT} = 0.873v, DDR_Vref = 0.833v and DDR_VDDP =1.7v, the VOL (DC) max = 0.873v-0.873v*25Ω/(25Ω+41.25Ω) = 0.5435v.DDR_Vref – VIN= 0.2895v which is larger than VIL (DC) = 0.125v.*

ADC Specifications

Table 27 ADC Specifications

Conditions: VDDADC=2.5V, CEXT=0.1uF, SYSCLK= 32Mhz, 25°C, unless other specified.

Symbol	Description	Min	Typ	Max
VDDADC	Analog power	2.375V	2.5V	2.625V
		3.135V	3.3V	3.465V
VREFP			1.0V	
VREFN			0	
Input voltage range (Vinp-Vinn)		-1V		1V
Input capacitance				
ENOB			10	
SNDR			62dB	
SFDR	Differential input		69dB	
DNL			+/-0.7LSB	
INL			+/-1LSB	
Conversion Speed			1MSPS	
Conversion time	Number of clk cycle			32
ADC clock frequency				32 MHz
Channel Crosstalk			-60dB	
On-chip supply monitor error	With calibration			1.0%
On-chip temperature monitor error	With calibration			±4°C
Supply current	Operating Current@3.3V		3.6mA	

Transceiver Specifications

Table 28 Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
DC Power Supply Pin Requirements					
AVCCR	0.9V power supply for Rx analog circuits	0.855	0.90	0.945	V
AVCCT	0.9V power supply for Tx analog circuits	0.855	0.90	0.945	V
DVDD	0.9V power supply of PCS digital circuits	0.855	0.90	0.945	V

Symbol	Description	Min	Typ	Max	Unit
AVTTRX	1.2V power supply for Transceiver Rx analog circuits	1.14	1.2	1.26	V
AVTTTX	1.2V power supply for Transceiver Tx analog circuits	1.14	1.2	1.26	V
AVCCRPI	1.2V power supply for Rx analog circuits	1.14	1.2	1.26	V
AVCCTPI	1.2V power supply for Tx analog circuits	1.14	1.2	1.26	V
AVCCPLL	1.2V power supply for PLL analog circuits	1.14	1.2	1.26	V
AVCCVCO	1.2V power supply for PLL analog circuits	1.14	1.2	1.26	V
AVCCBIAS	1.2V power supply for BG analog circuits.	1.14	1.2	1.26	V
AVCCAUX	1.2V power supply for Aux analog circuits	1.14	1.2	1.26	V
AVCCBG	2.5V power supply for BG analog circuits	2.25	2.5	2.75	V
AC Power Supply Pin Requirements					
VDD_0.9V	0.9V analog core supply voltage maximum AC power supply noise Total Integrated Peak-Peak noise for frequencies from 1KHz to 10MHz			0.03	Vpk-pk
VDD_1.2V	1.2V analog core supply voltage maximum AC power supply noise Total Integrated Peak-Peak noise for frequencies from 1KHz to 10MHz			0.03	Vpk-pk
VDD_2.5V	2.5V analog core supply voltage maximum AC power supply noise Total Integrated Peak-Peak noise for frequencies from 1KHz to 10MHz			0.03	Vpk-pk

Switching Characteristics

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics.

Clock Performance

Table 29 Global Clock Performance

Symbol	Max Frequency	Units
GCLK	550	MHz

PLL Specifications

Table 30 PLL Specifications

Symbol	Description	Min	Typ	Max	Unit
VDDIO	Analog power voltage	2.25	3.3	3.63	V
DVDD	Digital power voltage	0.855	0.9	0.945	V
Fin	Input clock freq.	10		700	MHz
Fpfd	PFD input freq.	10		450	MHz
Fvco	VCO operation freq.	600		1400	MHz
Fout	Output freq.	1.17		700	MHz
Tlock	Lock time			200	us
Duty	Output clock duty cycle	45	50	55	%
N	Input divider	1		256	--
M	Loop divider	1		256	--
C0~C5	Output divider	1		256	--
Ndly	Output clock delay	0		255	--
Terr	Static phase error	-10		10	Degree
Trst	External reset time		50	100	ns
Tjit	Peak-to-Peak period Jitter		150		ps

I/O Timing

Table 31 LVDS I/O Performance

IO Standard	Attribute	Min	Typ	Max
LVDS	Duty	45		55
	Frequency			650MHz

Table 32 DDR I/O Performance

IO Standard	Attribute	Min	Typ	Max
DDR	Duty			
	Jitter			
	Frequency			667MHz

DDR AC Specifications

Table 33 AC Electrical Specifications of SSTL_15 Transmitter and Receiver

Symbol	Parameter	Conditions	Min	Nom	Max
$V_{IH(AC)}$	AC logic input high		DDR_ V_{REF}+0.15V		DDR_ V_{DDP}
$V_{IL(AC)}$	AC logic input low		0		DDR_ V_{REF}-0.15V
$V_{OH(AC)}$	AC logic output high			V_{TT} +0.1* DDR_V_{DDP}	
$V_{OL(AC)}$	AC logic output low			V_{TT} -0.1* DDR_V_{DDP}	

Table 34 AC Electrical Specifications of SSTL_18 Transmitter and Receiver

Symbol	Parameter	Conditions	Min	Nom	Max
$V_{IH(AC)}$	AC logic input high		DDR_ V_{REF}+0.25V		
$V_{IL(AC)}$	AC logic input low				DDR_ V_{REF}-0.25V
$V_{OH(AC)}$	AC logic output high		(1)		
$V_{OL(AC)}$	AC logic output low				(1)

Notes:

*(1) The maximum VOH (AC) and minimum VOL (AC) value depends on the driver RON, terminator voltage and terminator resistor value, the requirement of the VOH (AC) and VOL (AC) is to make sure that the input voltage of receiver could meet the VIH (AC) and VIL (AC) specification. For example, if terminator is 25Ω and V_{TT} = 0.793v, DDR_Vref = 0.833v and DDR_VDDP = 1.7v, the VOH (AC) min = (1.7v- 0.793v)*25Ω/(25Ω+41.25Ω)+0.793v = 1.1352v. VIN – DDR_Vref= 0.302v, which is larger than VIH (AC) = 0.25v and if terminator is 25Ω and V_{TT} = 0.873v, DDR_Vref = 0.833v and DDR_VDDP = 1.7v, the VOL (AC) max = 0.873v-0.873v*25Ω/(25Ω+41.25Ω) = 0.5435v. DDR_Vref – VIN= 0.2895v which is larger than VIL (AC) = 0.25v. System designers should be aware of that.*

Table 35 Hard Macro Clock Timing Specification

Symbol	Description	Input Clock Frequency (MHz)	Operation Frequency (mbps)	Min (ps)	Typ (ps)	Max (ps)
t_{IPERJ}	Input clock period jitter of DDR PHY	333	1333			±55
		266	1066			±62.5

Symbol	Description	Input Clock Frequency (MHz)	Operation Frequency (mbps)	Min (ps)	Typ (ps)	Max (ps)
	hard macro	200	800			±75
		166	667			±87.5
t_{ICCJ}	Input clock cycle to cycle jitter of DDR PHY hard macro	333	1333			110
		266	1066			125
		200	800			150
		166	667			175
t_{OCCJ}	ut clock cycle to cycle jitter of PLL		1333			±30
			1066			±40
			800			±50
			667			±60
t_{ψ}	Static phase error when PLL lock					±50
t_{IR}	Input clock rising time					100
t_{IF}	Input clock falling time					100

PLB Performance

Table 36 PLB Performance

Symbol	Description	Min	Max	Units
ADD16	16-bit adder performance @ recommended operating condition.		350	MHz
ADD32	32-bit adder performance @ recommended operating condition.		300	MHz
ADD64	64-bit adder performance @ recommended operating condition.		280	MHz
CNT8	8-bit counter performance @ recommended operating condition.		500	MHz
CNT16	16-bit counter performance @recommended operating condition.		480	MHz
CNT32	32-bit counter performance @ recommended operating condition.		460	MHz

EMB Performance

Table 37 EMB Performance

Symbol	Description	Min	Max	Units
EMB9K	Using register path.		-	MHz
	Not using the register path.		-	MHz
EMB18K	Using register path.		260	MHz
	Not using the register path.		250	MHz

DSP Performance

Table 38 DSP Performance

Symbol	Description	Min	Max	Units
DSP 18x18-bit multiplier	DSP using register path.		320	MHz
	DSP not using the register path.		300	MHz
DSP 36x36-bit multiplier	DSP using register path.		300	MHz
	DSP not using the register path.		280	MHz

This part lists the pin definitions and rules as well as available package information. For the detailed pin list, please see the Pin List doc.

5. Pins and Package

Pins Definitions and Rules

Table 39 Pins Definitions and Rules

Pin Name	Direction	Description
User I/O Pins		
IOXX_# IO_XXY_#	Inout	General-purpose user-I/O pin. XX represents the I/O number in the bank. Y represents p or n for the differential I/O pairs.
Multi-Function Pins		
IOXXX/ZZZ_# IO_XXY/ZZZ_#	-	Multi-function pins are labeled IOXXX/YYY_# and IO_XXY/ZZZ_#, where YYY represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Multi-Function Pins: Passive configuration Pins		
SCK	Input/Output	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCLK is a clock output from device. The pin can be used as regular user I/Os after configuration.
SDI	Output	Dedicated configuration data output pin in AS mode. The pin can be used as regular user I/Os after configuration in AS mode
SDO	Input	Serial data input from spi flash in AS mode. The pin can be used as regular user I/Os after configuration.
SS	Output or Input	Chip select output to enable a SPI Flash in AS mode or input as a HME device select. This output is used during AS mode. The pin can be used as regular user I/Os after configuration in AS mode. It is used as chip selection control (input) during PS. The pin can be used as regular user I/Os after configuration in

Pin Name	Direction	Description
		PS mode.
HOLD	Output	SPI Flash hold signal.
WP	Output	SPI Flash write protect signal.
PS_BUSY	Output	Device busy in PP mode, high active.
PS_D[15:0]	Input	Input data from master in Passive mode.
Multi-Function Pins: Configuraiton		
CONF_DONE	Output	This is a dedicated configuration status pin, the pin will output high during configuration. The pin can be used as regular user I/Os after configuration.
CRST_N	Input	Chip global reset input. Active low.
Dedicated Pins: JTAG		
TCK	Input	TCK Input Boundary-Scan Clock.
TDI	Input	TDI Input Boundary-Scan Data Input.
TDO	Output	TDO Output Boundary-Scan Data Output.
TMS	Input	TMS Input Boundary-Scan Mode Select.
Multi-Function Pins: Clock Pins		
CC/GC	Input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
Dedicated Pins: DDR Pins		
DQ[31:0]	Inout	Data input/output
ECC_DQ[7:0]	Inout	ECC Data input/output
DM[3:0]	Output	Input data mask
DQS0/1, DQS0/1N	Inout	Data strobe
VREF0, VREF1	N/A	Reference voltage
CKE	Output	Clock enable
BA[2:0]	Output	Bank address inputs
A[14:0]	Output	Address inputs
CLK, CLKN	Output	DDR Clock
RASN	Output	Command inputs
CASN	Output	Command inputs
WEN	Output	Command inputs
RESETN	Output	DDR Reset. low active
ODT	Output	On-die termination
CSN	Output	Chip select, low active
DDR_AVDD_PLL	N/A	DDR PLL power, 2.5V
DDR_VDDP	N/A	DDR3 IO post-driver power,1.5V for DDR3,1.8V for DDR2
DDR_VREF	N/A	0.5*VDDR_VDDP
DDR_VDD		DDR3 pre-driver and core logic power,0.9V
Dedicated Pins: Transceiver Pins		
RXP0/RXN0	Input	Lane 0 Differential data input pins, high speed 10 Gb/s

Pin Name	Direction	Description
		and potential ESD hazards
RXP1/RXN1	Input	Lane 1 Differential data input pins, high speed 10 Gb/s and potential ESD hazards.
RXP2/RXN2	Input	Lane 2 Differential data input pins, high speed 10 Gb/s and potential ESD hazards.
RXP3/RXN3	Input	Lane 3 Differential data input pins, high speed 10 Gb/s and potential ESD hazards.
TXP0/TXN0	Output	Lane 0 Differential data output pins, high speed 10 Gb/s and potential ESD hazards.
TXP1/TXN1	Output	Lane 1 Differential data output pins, high speed 10 Gb/s and potential ESD hazards.
TXP2/TXN2	Output	Lane 2 Differential data output pins, high speed 10 Gb/s and potential ESD hazards.
TXP3/TXN3	Output	Lane 3 Differential data output pins, high speed 10 Gb/s and potential ESD hazards.
REFCLKP/ REFCLKN	Input	Reference Clock Differential Input pins, 650 MHz maximum.
RREF	N/A	Accurate Reference Resistor Pins for Calibration.
AVTTRX0/1/2/3	N/A	1.2V power supply for Rx analog circuits.
AVTTTX0/1/2/3	N/A	1.2V power supply for Rx analog circuits.
AVSSA	N/A	1.2V Ground for Tx/Rx analog circuits.
AVCCRPI1/2	N/A	1.2V power supply for Rx analog circuits.
AVSSRPI1/2	N/A	1.2V ground for Rx analog circuits.
AVCCR1/2	N/A	0.9V power supply for Rx analog circuits.
AVSSR1/2	N/A	0.9V ground for Rx analog circuits.
AVCCTPI1/2	N/A	1.2V power supply for Tx analog circuits.
AVSSTPI1/2	N/A	1.2V ground for Tx analog circuits.
AVCCT1/2	N/A	0.9V power supply for Tx analog circuits.
AVSST1/2	N/A	0.9V ground for Tx analog circuits.
AVCCPLL1	N/A	1.2V power supply for PLL analog circuits.
AVSSPLL1	N/A	1.2V ground for PLL analog circuits.

Pin Name	Direction	Description
AVCCVCO	N/A	1.2V power supply for PLL analog circuits.
AVSSVCO	N/A	1.2V ground for PLL analog circuits.
AVCCPLL2	N/A	1.2V power supply for PLL analog circuits.
AVSSPLL2	N/A	1.2V ground for PLL analog circuits.
AVCCBG	N/A	2.5V power supply for BG analog circuits.
AVSSBG	N/A	2.5V ground for BG analog circuits.
AVCCBIAS	N/A	1.2V power supply for BG analog circuits.
AVSSBIAS	N/A	1.2V ground for BG analog circuits.
AVCCAUX	N/A	1.2V power supply for Aux analog circuits.
DVDD	N/A	0.9V power supply of PCS digital circuits, should supply PMA blocks from PCS side.
DGND	N/A	0.9V PCS Digital circuits Ground, should supply PMA blocks from PCS side.
ATST	I/O	Analog Test I/O pin, 2.5V domain.
GREFCLK	Input	Transceiver Phy Reference clock source from user logic, single end, 0.9V TTL, clock should be less than 650MHz
TSTCK0	Output	Digital Test output interfaces, 0.9V TTL buffer, internal test signals can be accessed through this interface, for test and debug purpose.
TSTCK1	Output	Digital Test output interfaces, 0.9V TTL buffer, internal test signals can be accessed through this interface, for test and debug purpose.
TSTCK2	Output	Digital Test output interfaces, 0.9V TTL buffer, internal test signals can be accessed through this interface, for test and debug purpose.
TSTCK3	Output	Digital Test output interfaces, 0.9V TTL buffer, internal test signals can be accessed through this interface, for test and debug purpose.
ESD_RAIL	In/Out	ESD Bus can be shorted with the common ESD ground plane in the rest of the chip via back-to-back diodes instantiated within the PHY
Dedicated Pins: ADC Pins		
ADCI0-11P, ADCI0-11N	Input	ADC input pin, can be used as general IO if not used
ADC_VIPP, ADC_VIPN	Input	Dedicated ADC input
ADC_VINP, ADC_VINN	Input	Dedicated ADC input

Pin Name	Direction	Description
ADC_VREFP, ADC_VREFN	Input	Dedicated ADC reference. When the external 1v accurate reference voltage source (+/-0.25%) is tied to the pin of VREFP, the ADC can be worked at the best performance. When VREFP is floating, On-chip Bandgap Reference (1.00V+/-3%) is activated. VREFP and VREFN must be treated as analog signal. To properly operate, CEXT (1uF~10uF) external capacitor is needed to be placed between this PIN and VREFN pin.
VDD_ADC	N/A	ADC power supply, 3.3V or 2.5V.
Dedicated Pins: Power		
VDDIO33	N/A	Digital power for Configuration which also supply all the PLLs power, 3.3V.
VDDIO_X	N/A	Digital power for IO,1.5/1.8/2.5/3.3V. VDDIO_301,302,303 must be not above 2.5V if these banks are used as single-end I/O.
VDD_CORE	N/A	Digital power for core, 1.1V.
VSS	N/A	Digital ground.

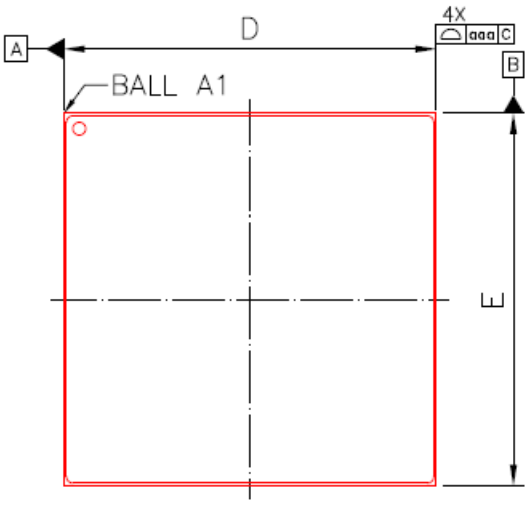
Notes:

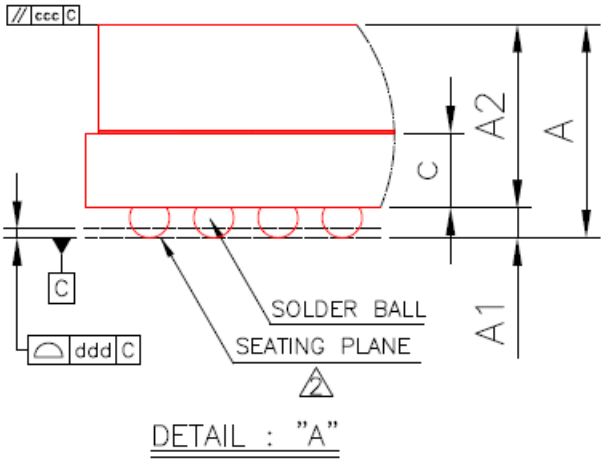
(1) VDDIO33 is the power for JTAG/SPI Flash that must be above 2.5V.

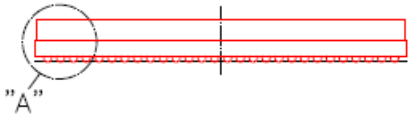
(2) There is a power sequence requirement: The VDD_CORE must be power on before the VDDIO33.

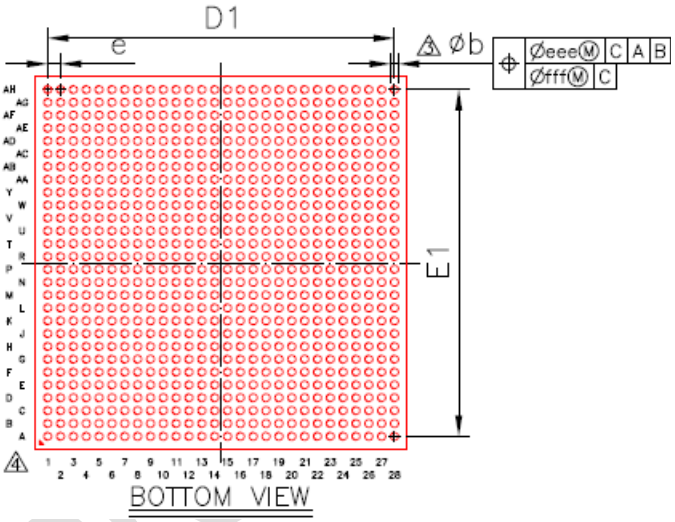
Package Information

FBGA784 Fineline BGA Package Specifications







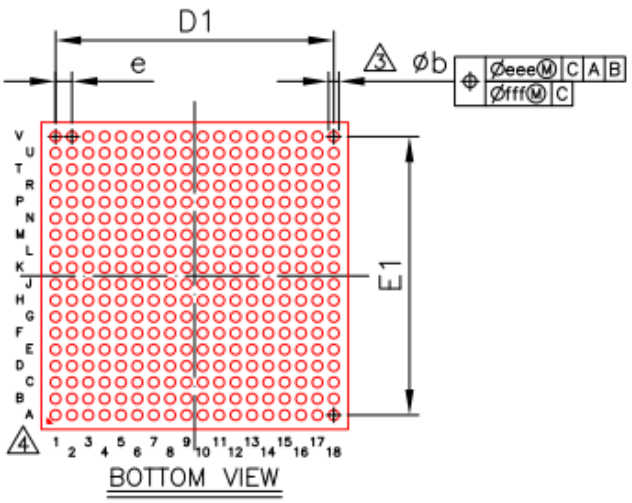


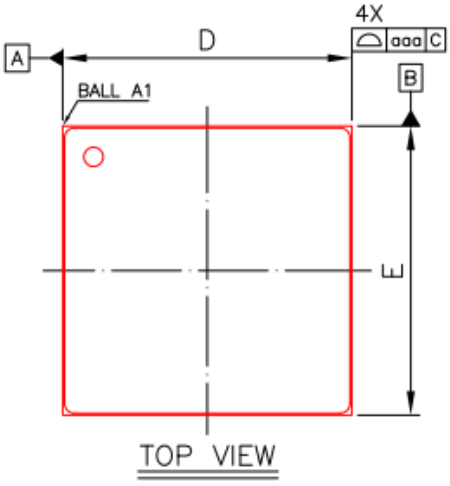
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.14	3.32	3.50	0.124	0.131	0.138
A1	0.37	0.47	0.57	0.015	0.019	0.022
A2	2.70	2.85	3.00	0.106	0.112	0.118
c	1.05	1.15	1.25	0.041	0.045	0.049
D	28.80	29.00	29.20	1.134	1.142	1.150
E	28.80	29.00	29.20	1.134	1.142	1.150
D1	---	27.00	---	---	1.063	---
E1	---	27.00	---	---	1.063	---
e	---	1.00	---	---	0.039	---
b	0.52	0.62	0.72	0.021	0.024	0.028
aaa		0.20			0.008	
ccc		0.35			0.014	
ddd		0.20			0.008	
eee		0.25			0.010	
fff		0.10			0.004	
MD/ME		28/28				

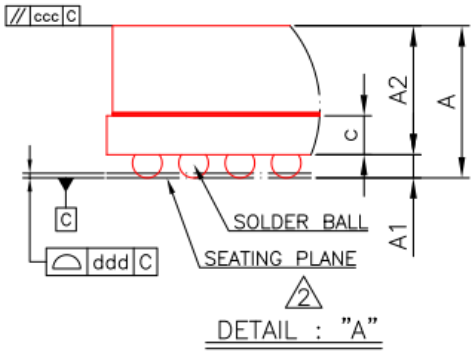
NOTE :

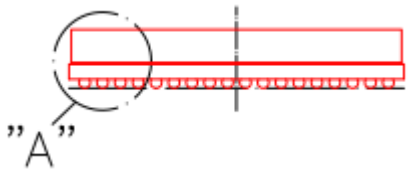
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
5. BALL PLACEMENT USE 0.60 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.50 mm

VFBGA324 Package Specifications









Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.44	2.62	2.80	0.096	0.103	0.110
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	2.05	2.22	2.39	0.081	0.087	0.094
c	0.57	0.67	0.77	0.022	0.026	0.030
D	14.80	15.00	15.20	0.583	0.591	0.598
E	14.80	15.00	15.20	0.583	0.591	0.598
D1	---	13.60	---	---	0.535	---
E1	---	13.60	---	---	0.535	---
e	---	0.80	---	---	0.032	---
b	0.46	0.51	0.56	0.018	0.020	0.022
aaa		0.15			0.006	
ccc		0.35			0.014	
ddd		0.20			0.008	
eee		0.20			0.008	
fff		0.08			0.003	
MD/ME		18/18				

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.50 mm SOLDER BALL.
   BGA PAD SOLDER MASK OPENING = 0.40 mm.

This appendix describes the ordering information about Pegasus family.

Ordering Information

All part numbers have the following conventions:

Table 40 Part number conventions

Vendor	Product Family	Device Type	LUT Density	Flash	Transceiver	Package Type	Temperature	Speed Grade
HME-	P1	P	060	N0	T	F784	C	7

Product Series

- ❒ **P1 Pegasus family**

Device Type

- ❒ **P FPGA**

LUT Density

- ❒ **060 60K LUTs**

Configuration NVM (SPI-flash) Option

- ❒ **N0 Without internal SPI-flash**

Transceiver:

- ❒ **T Transceiver**

Package Type: <type><#>

- ❒ **V VFBGA**
- ❒ **F Fineline BGA**
- ❒ **# Pin number (784 for 784 pin…)**

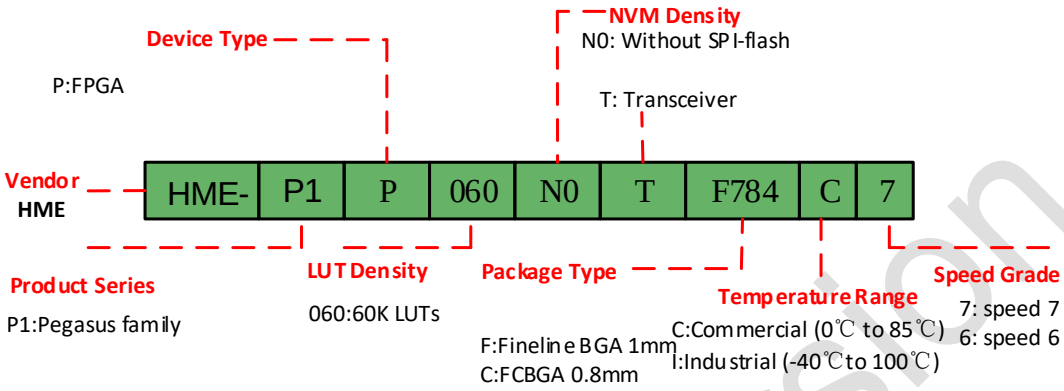
Temperature Range

- ❒ **C Commercial (0°C to 85°C)**
- ❒ **I Industrial (-40°C to 100°C)**

Speed Grade

- ❒ **# Speed (7 for speed 7, 6 for speed 6, …)**

Example: **HME-P1P060N0TF784C7**



Order information

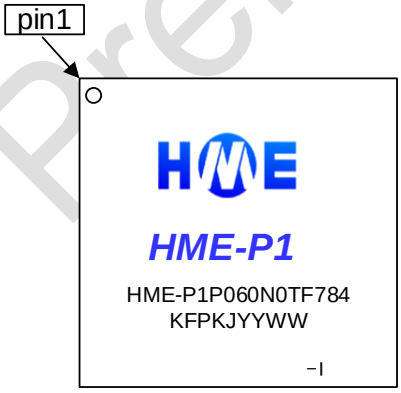
Product	Order P/N	Grade
P1P060N0TF784C7	P1P060N0TF784	Commercial
P1P060N0TF784I7	P1P060N0TF784I	Industrial
P1P060N0V324C7	P1P060N0V324	Commercial
P1P060N0V324I7	P1P060N0V324I	Industrial

Chip Marking Spec notice:

1) "C7" will not be marked. That default is commercial grade.

2) If "-I" is marked on the chip, that means industrial grade.

Sample Marking:



Line 4: Wafer Lot Number(first 5 bits) + Date Code
KFPKJYYWW
YYWW(Actual Assembly Work Week)
Ex: YY(Yearly 2015)---15
WW(Weekly 18) ---18

Line 5: Temperature Range

- -I: Industrial
- Empty for Commercial

This appendix lists the heart revisions of this doc for your reference.

Revision History

The table below shows the revision history for this document.

Release Date	Doc Version	Revision
Feb. 2020	HME-P1(P060)DSE01	Initial release.
Arg. 2020	HME-P1(P060)DSE01	C324 change to V324. VDDIO_301,302,303 power must be not above 2.5V.