SUBJECT NO-EC60204, SUBJECT NAME- DIGITAL VLSI CIRCUITS

LTP- 3-1-0,CRD- 4

SYLLABUS :-

Pre-requisites: EC31003 and EC30004Issues of Digital IC Design : General overview of design hierarchy, layers of abstraction, integration density and MooreÃÂ¢ÃÂÃÂs law, VLSI design styles, packaging styles, design automation principles; Logic Design : switch logic, gate restoring logic, Programmable Logic Array (PLAs), Finite State Machine (FSM) as a PLA, personality matrix of a PLA, PLA folding, pseudo-nmos logic, BiCMOS logic gates; Basic Circuit Concepts : sheet resistance and area capacitances of layers, driving large capacitive loads, super-buffers, propagation delay models of cascaded pass transistors, wiring capacitances, switching delay in BiCMOS logic circuits; Bipolar ECL Inverter : features of ECL gate, robustness and noise immunity, logic design in ECL, single-ended and differential ECL gates; Dynamic CMOS design : steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, np-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme, different logic families like CPL, DCVSL etc.; Sequential CMOS Logic Circuits : basic regenerative circuits, digital phase-locked loop (DPLL); Low-power CMOS Logic Circuits : low-power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance, adiabatic logic circuits; Subsystem Design : design of arithmetic building blocks like adders and multipliers, barrel and logarithmic shifters, area-time tradeoff, power consumption issues; Semiconductor Memories : Dynamic Random Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory; Case Study (instructor may choose any suitable digital system; in the following, an example is suggested) : A RISC Processor - Instruction Set, Pipeline Architecture, Major Logic Blocks, Layout, Functional Verification.