SUBJECT NO-EC60202, SUBJECT NAME- VLSI CAD

LTP- 3-1-0,CRD- 4

SYLLABUS :-

Pre-requisites: EC30004 Introduction: Basic design flow, concept of design automation; High level Synthesis: Role of hardware description language, behavioral and structural models, synthesis flow. Functional simulation at architectural level; Logic Design: Logic optimization techniques, logic hazards and their remedies. Power and delay minimization at logic level. Logic simulation at structural level; Circuit Design: Mapping of logic designs into transistor level circuits, optimized ordering of the input signals. Power and delay considerations. Fan-in and fanout issues. Circuit simulation; Physical design automation: Partitioning, floorplanning, placement, routing. Layout and design rules, DRC etc. Parasitic extraction, delay and power estimation through post layout simulation; CAD for analog and mixed signal designs. Memory synthesis. Clock and power routing. Testability, insertion of scan chain.