SUBJECT NO-EC60297, SUBJECT NAME- VLSI INTERCONNECTS

LTP- 3-0-0,CRD- 3

SYLLABUS :-

Pre-requisites: EC30004 Introduction: Moores law, Technological trends, Interconnect scaling, 3D-interconnect view; Interconnect delay modeling: Typical interconnect structure, Extraction of interconnect parameters, modeling interconnect drivers, switch-level RC model, effective capacitance modeling; Interconnection Length Prediction: Rents rule and parameter, Technology extrapolation, performance prediction, Interconnect-power and power modeling; Inductance of Interconnects: Increasing the effects of inductance, skin effect and its influence on resistance and inductance, Partial element equivalent circuit (PEEC) method; Driving interconnect for circuit speed optimization: Evolution of the speed optimization problem, logical effort method, Wire sizing, spacing. Driving RC trees; Crosstalk noise: Crosstalk configuration, DC noise margins, Reasons for high delay uncertainty, switch factor modeling of delay uncertainty, Buffer insertion for noise; Routing topology generation for speed optimization: New approaches in routing topology generation. Width optimization based on separability /monotonicity properties;