SUBJECT NO-EC39004, SUBJECT NAME- VLSI LABORATORY

LTP- 0-0-3,CRD- 2

SYLLABUS :-

Transistor-level Circuit Design using Cadence Design Flow1. Circuit design (paper-pencil design w/o cadence)2. Schematic capture and simulation3. Circuit layout and layout vs. schematic check4. Parameter extraction from layout and post-layout simulationÃ´ÂÂÂ Design experiments:o Familiarization with Cadence schematic-to-layout flow using inverter designo A cascode amplifier designo A differential amplifier designo A current source designo An operational transconductance amplifier designÃ¢ÂÂ¢ Logic-level Circuit Design using Xilinx FPGA Design Flow1. Architectural level design (paper-pencil design w/o Xilinx)2. HDL coding of the design and logic simulation3. Synthesis and post-synthesis logic simulation4. Implementation (placement and routing)5. Downloading to FPGA and verification of designÃ´ÂÂÂ Design experiments:o Familiarization with Xilinx HDL-to-implementation flow using ripple-carry adder designo Carry Look Ahead addero Arithmetic Multipliero Carry Bypass addero Barrel shiftero Logarithmic shiftero Sequence detectoro Left/right shiftero Synchronous up/down countero Linear feedback shift register