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Lab 1: Revisiting Digital Logic and Verilog Simulation

**Section 1: Introduction**

Purpose. Progress. Summary. (.5 pg)

**Section 2: Baseline Design**

Baseline design and implementation. Figures (FSM). How figure works. (<1pg)

**Section 3: Design**

Overview of Design. Why you chose to implement that way

**Section 4: Testing Strategy**

Tb. What happened in tb. Table with test results. Explain why it proves design works

**Section 5: Evaluation**

Simulation results. Explain them. Big picture summary.