Jaci Reichenberger

A20131719

Stephen Potter

A11341625

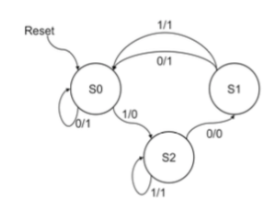
8 February 2021

Lab 1: Revisiting Digital Logic and Verilog Simulation

**Section 1: Introduction**

The purpose of this lab is to introduce the Verilog tools that will be utilized in this class. Using code already provided, this lab introduced how to use ModelSim to view the output waveforms of an FSM. Students were able to read through the code and learn how to utilize a DO file in order to see the waveform inputs and outputs in the application. The second part of this lab introduced how to write code, a testbench, and modify a DO file in ModelSim in order to show both the input and the output waveforms for a register. The code for the register was created following guidelines given for this lab. The testbench code was written to test the various guidelines given, and the DO file was only slightly changed from the FSM’s DO file. All in all, this lab introduced students to ModelSim and reminded students how to code in Verilog.

**Section 2: Baseline Design**

Part 1: FSM Simulation

Part 2: Register File and Simulation

Baseline design and implementation. Figures (FSM). How figure works. (<1pg)

**Section 3: Design**

Overview of Design. Why you chose to implement that way

**Section 4: Testing Strategy**

Tb. What happened in tb. Table with test results. Explain why it proves design works

**Section 5: Evaluation**

Simulation results. Explain them. Big picture summary.