DIGITAL CIRCUITS LAB
Experiment-10
Asynchronous Counters

Shashi Prabha
200020043

Aim:- To design and implement a circuit for a mod-8 Asynchronous up-counter and a mod-6 Asynchronous up-counter, using NAND gates(if required)

Summary: Implementation of the mod-8 Asynchronous up-counter and a mod-6 Asynchronous up-counter with JK filp flop and NAND gate which is require In mod-6 .

Components used: SN-5476(JK Flip-flop),NAND gate IC (DM7400), LED Display,switch, Breadboard, Power supply, Arbitrary Function Generator, 1k ohm resistor.

Procedure:

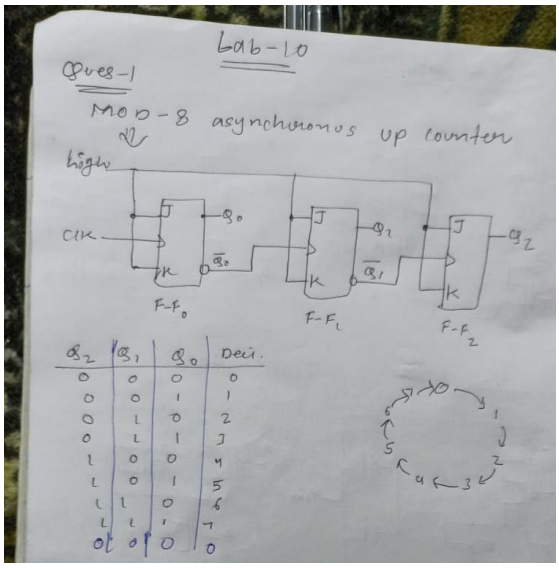
- Connect the circuit as shown in diagrams and give it power input.
- Give Clock signal to the circuit using the AFG with frequency between 1Hz and 1Vp-p.
- To see the output of clock signal you can connect clk to oscilloscope.
- Glowing LED implies that output was 1, otherwise 0.
- For MOD-8 total states are 8 i.e from 0-7 then again 0.
- For MOD-6 total states are 8 i.e from 0-6 then again 0,And for 6,7 it will reset to 0
- In whole experiment preset and clear will be 1 for j-k FF
- Verify if the simulation matches with the expected values.

Logic Design:

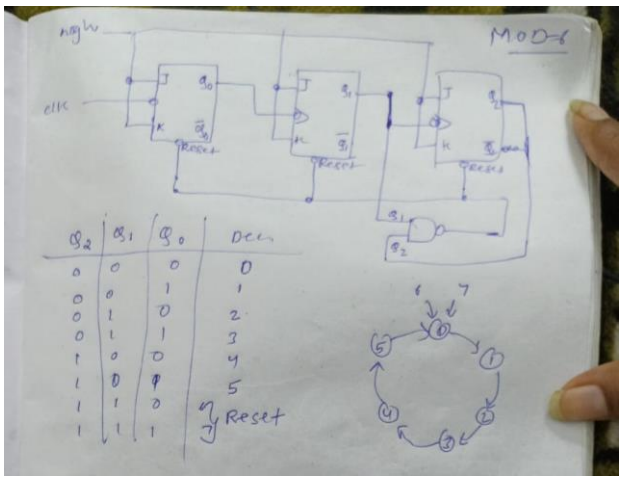
- Mod-8 design = asynchronous up-counter consisting of 3 JK Flip-flops.
- Mod-6 design= asynchronous up-counter consisting of 3 JK Flip-flops that has a clear activation at 6(110), so we connect Q1 and Q2 to an AND gate, and then pass that through CLR of the IC, so that 6,7 can be cleared to 0.

Circuit Design:

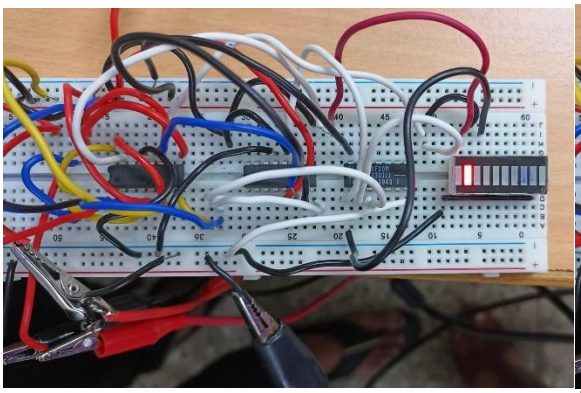
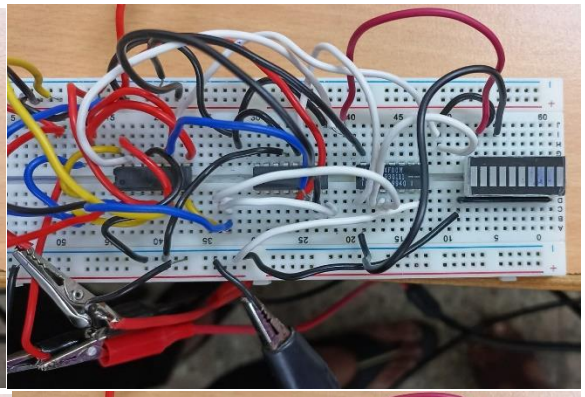
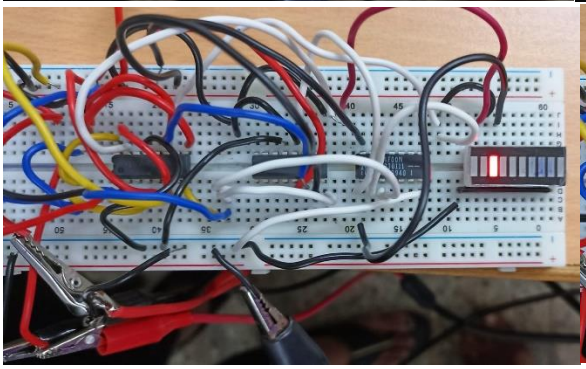
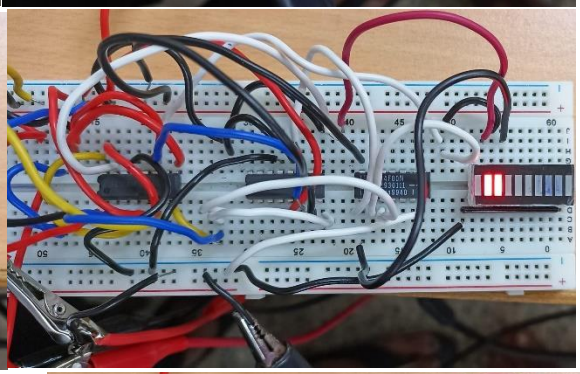
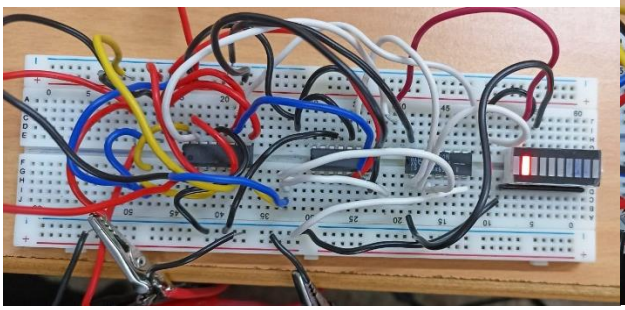
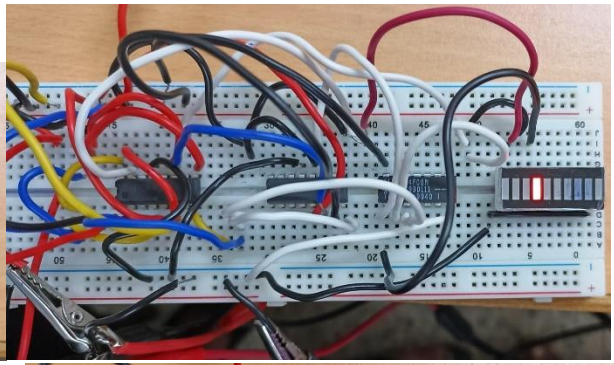
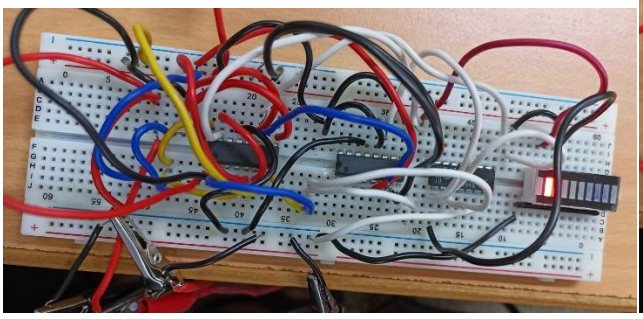
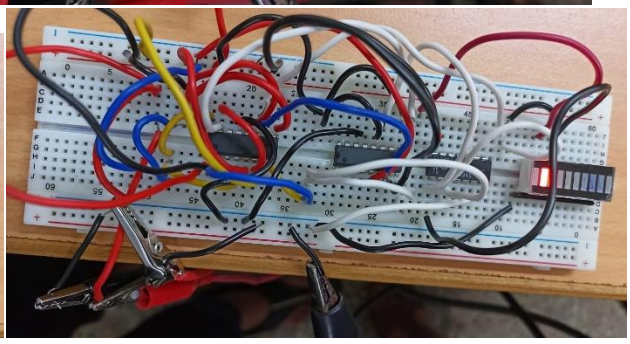
Mod-8 Asynchronous up-counter:

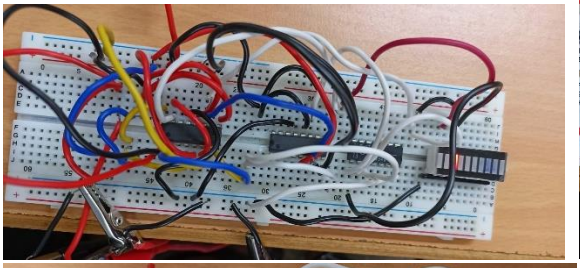


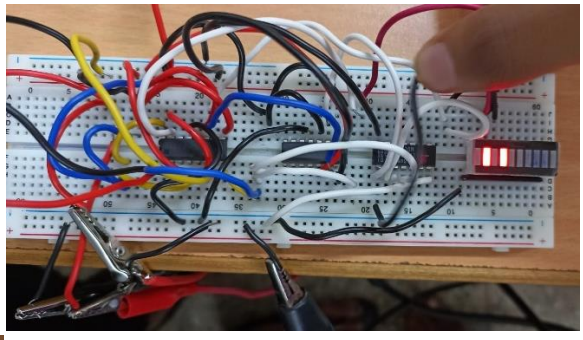
Mod-6 Asynchronous up-counter:

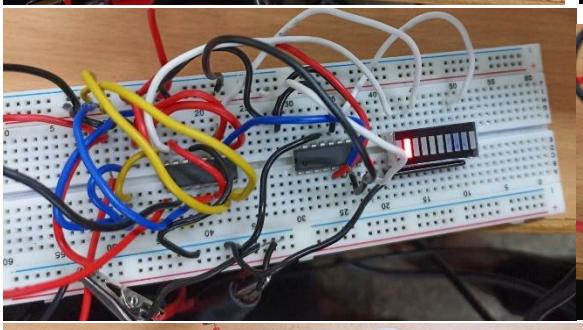


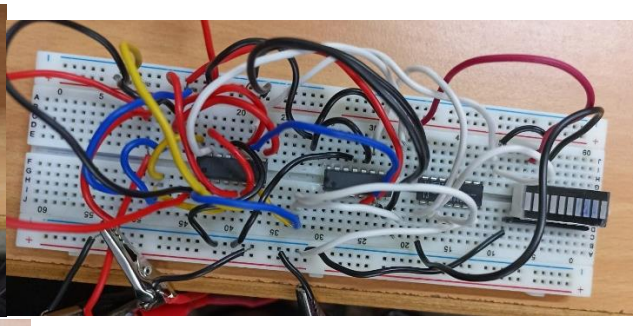
Hardware Implementation:

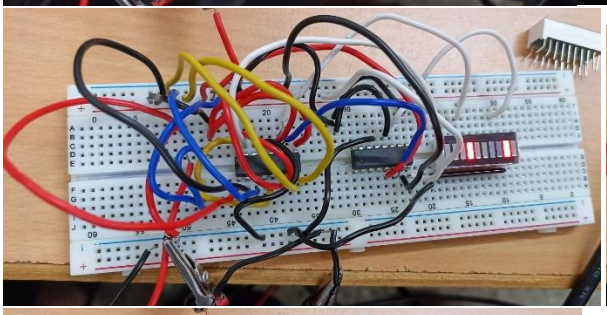









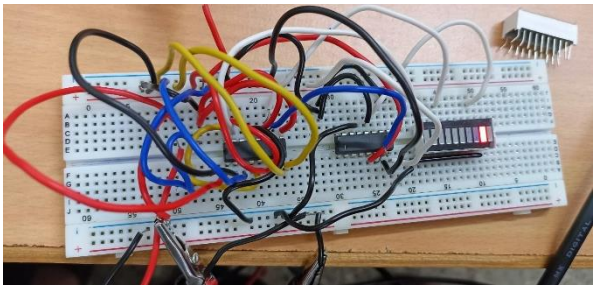


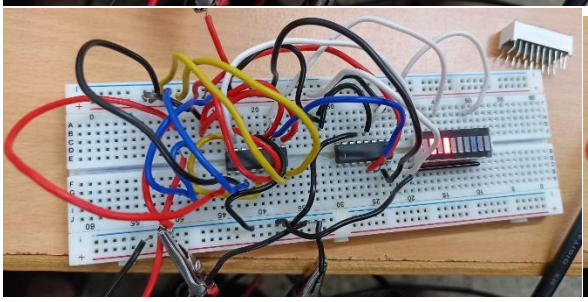


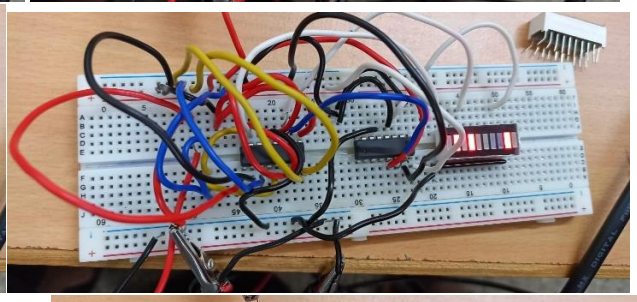


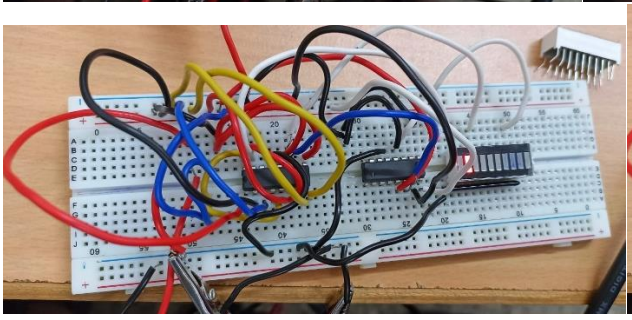


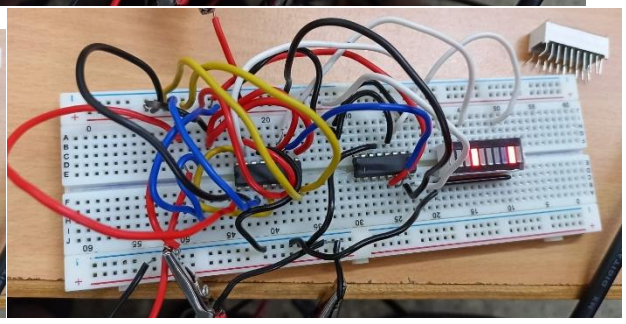












Results and Discussions: In this experiment, we constructed mod-8 and mod - 6 asynchronous up counters, where mod-8 counter was of 3 JK flip flops and in mod-6 it had to reset 6, states to 0 which was done by setting output of NAND gate to reset of all JK flip flops with inputs as Q1 and Q2.

Overall this expermiment was nice experience as we learned to construct MOD8 and MOD6 asynchronus up counters.