

## EE 212 (Electronic Devices Lab)

### Experiment-4

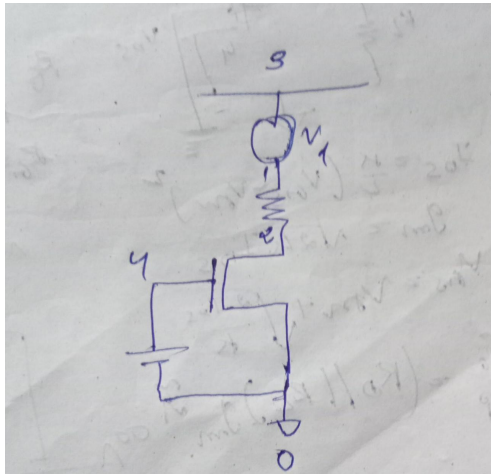
#### NMOS Common Source Amplifier Characteristics

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NGSPICE Code:

#### Question 2.3



\*ques. 2 :- NMOS CHARACTERISTICS

vdd 3 0 dc 5v

vd 3 2 dc 0v

vgs 1 0 dc 5v

m1 2 1 0 0 MN4007

\* N4007 (NMOS on CD4007 CMOS integrated circuit)

.model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6

+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p  
Is=16.64p N=1)

.dc vdd 0.1 5 0.2 vgs 0 5 0.2

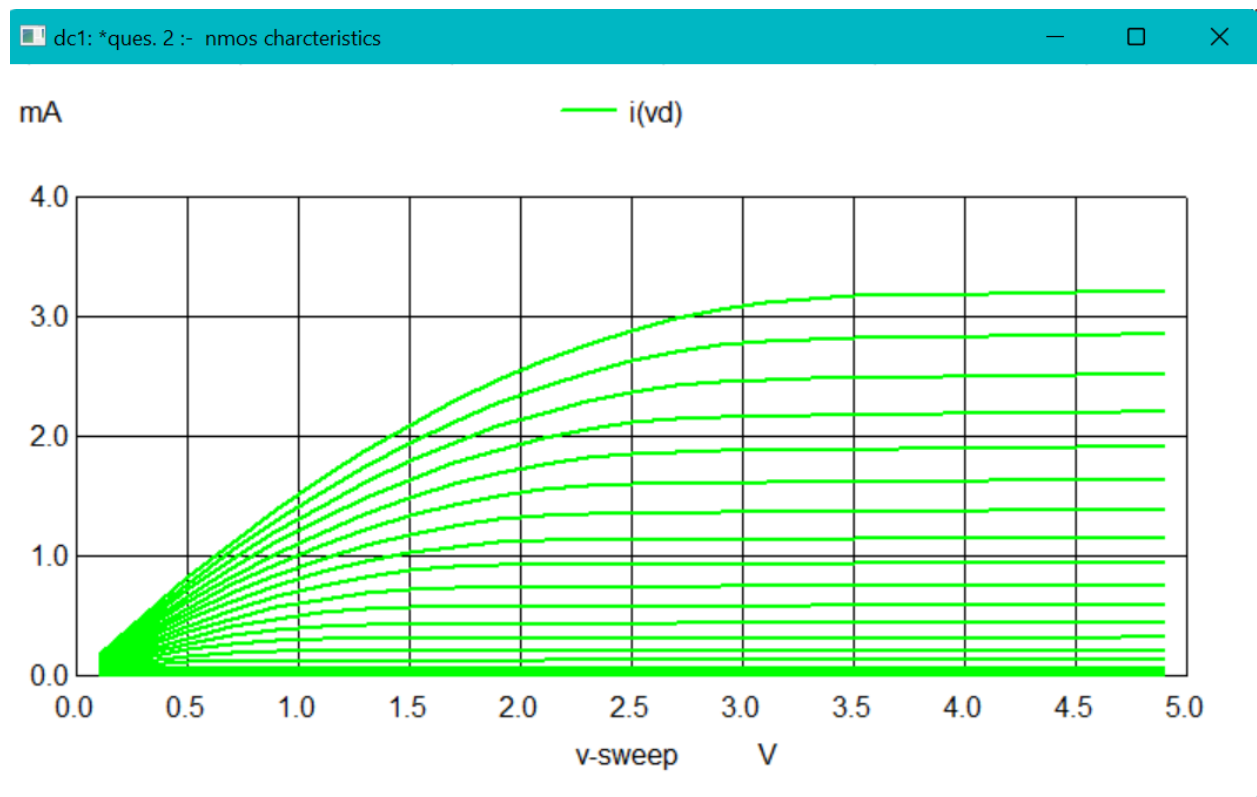
\* Control Statements

```
.control  
run
```

```
set color0=white  
set color1=black  
set xbrushwidth=2
```

```
plot i(vd)
```

```
.endc  
.end
```



#### Question 4

Vgs(V)	Rds(k-ohm)
1.1	750
1.2	1163
1.4	1774

1.6	1887
1.7	2341

Vgs(V)	r0(M-ohm)
1.1	7.2
1.2	11.3
1.4	17.3
1.6	18.3
1.7	24.5

### **Question 5**

\*ques5:- estimation of threshold voltage

vdd 3 0 dc 5v

vd 3 2 dc 0v

vgs 1 0 dc 5v

m1 2 1 0 0 MN4007

\* N4007 (NMOS on CD4007 CMOS integrated circuit)

.model MN4007 NMOS (Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6

+ Xj=0 Tox=1200n Phi=.6 Rs=0 Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p

Is=16.64p N=1)

.dc vgs 0 5 0.2

\*.dc vdd 0.1 5 0.2

.control

run

set color0=white

set color1=black

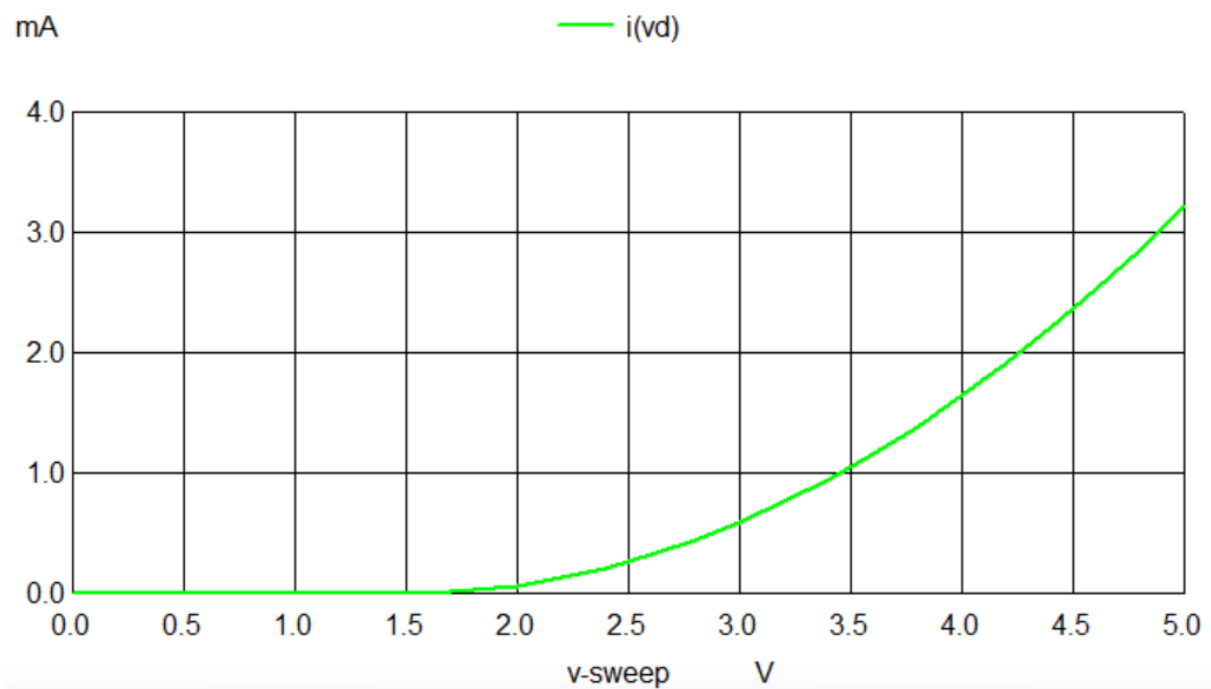
```
set xbrushwidth=2
```

```
plot i(vd)
```

```
.endc
```

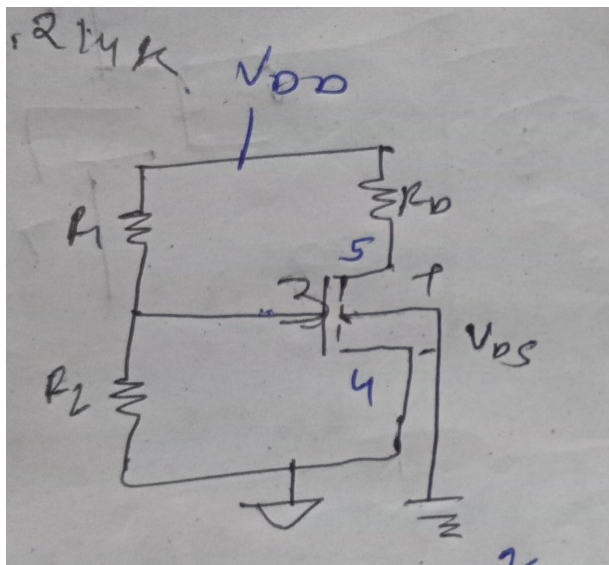
```
.end
```

dc2: \*ques5:- estimation of threshold voltage



**Threshold voltage = 1.7**

**Question 6.7**



Circuit: ques6:- nmos common source amplifier  
 Doing analysis at TEMP = 27.000000 and TNOM = 27.000000  
 No. of Data Rows : 1  
 Doing analysis at TEMP = 27.000000 and TNOM = 27.000000  
 i(vd) = 5.977808e-04  
 v(3) = 7.608877e+00  
 v(4) = 2.990654e+00  
 i(vd1) = 9.345794e-04  
 ngspice 3 ->

```
Vdd 1 0 10
vd 1 2 0
rd 2 3 4k
vd1 1 5 0
r1 5 4 7.5k
r2 4 0 3.2k
M1 3 4 0 0 MN4007
```

```
.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)
```

\* Control Statements

.control

op

run

set color0=white

set color1=black

set xbrushwidth=2

print i(vd) v(3) v(4) i(vd1)

.endc

.end

### Question 8

Handwritten calculations and circuit diagram for Question 8:

Top left:  $I_D R_D + V_{DS} = V_{DD}$

Top right:  $R_D = \frac{10 - 4}{1.5 \text{ mA}}$   
 $R_D = \frac{60}{1.5} = 40 \text{ k}\Omega$

Center:  $V_{GS} = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD}$

Below center:  $\frac{3}{10} = \frac{R_2}{R_1 + R_2}$

Left of center:  $3.214 \text{ k}\Omega$

Right of center:  $3R_1 + 3R_2 = 10R_2$   
 $3R_1 = 7R_2$   
 $R_1 = \frac{7}{3} R_2$

Bottom right:  $R_2 = 3.214 \text{ k}\Omega$   
 $R_D = 4 \text{ k}\Omega$

Bottom center:  $\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} = \frac{R_1 + R_2}{R_1 R_2}$   
 $R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{10.714}{2} = 5.357 \text{ k}\Omega$

Bottom left:  $R_{eq} = 2.24 \text{ k}\Omega$

Circuit diagram: A MOSFET circuit with a drain resistor  $R_D$  connected to  $V_{DD}$  and a source resistor  $R_S$  connected to ground. The gate is connected to a voltage divider consisting of  $R_1$  and  $R_2$  connected to  $V_{DD}$  and ground. The MOSFET is labeled with '3' on the gate, '4' on the source, and '5' on the drain. The output voltage  $V_{DS}$  is indicated across the drain and source.

### Question 9

Q9

```
Vdd 1 0 10
vd 1 2 0
vd1 1 5 0
vin 7 0 sin (0 100m 1k 0 0 0)
rg 6 7 1k
c1 4 6 2.2u
r1 5 4 7.5k
r2 4 0 3.2k
rd 2 3 4k
c2 3 8 2.2u
rl 8 0 100k
M1 3 4 0 0 MN4007
```

```
.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)
```

```
.tran 0.01ms 10ms 0.1ms
```

```
.control
```

```
op
```

```
run
```

```
set color0=black
```

```
set color1=white
```

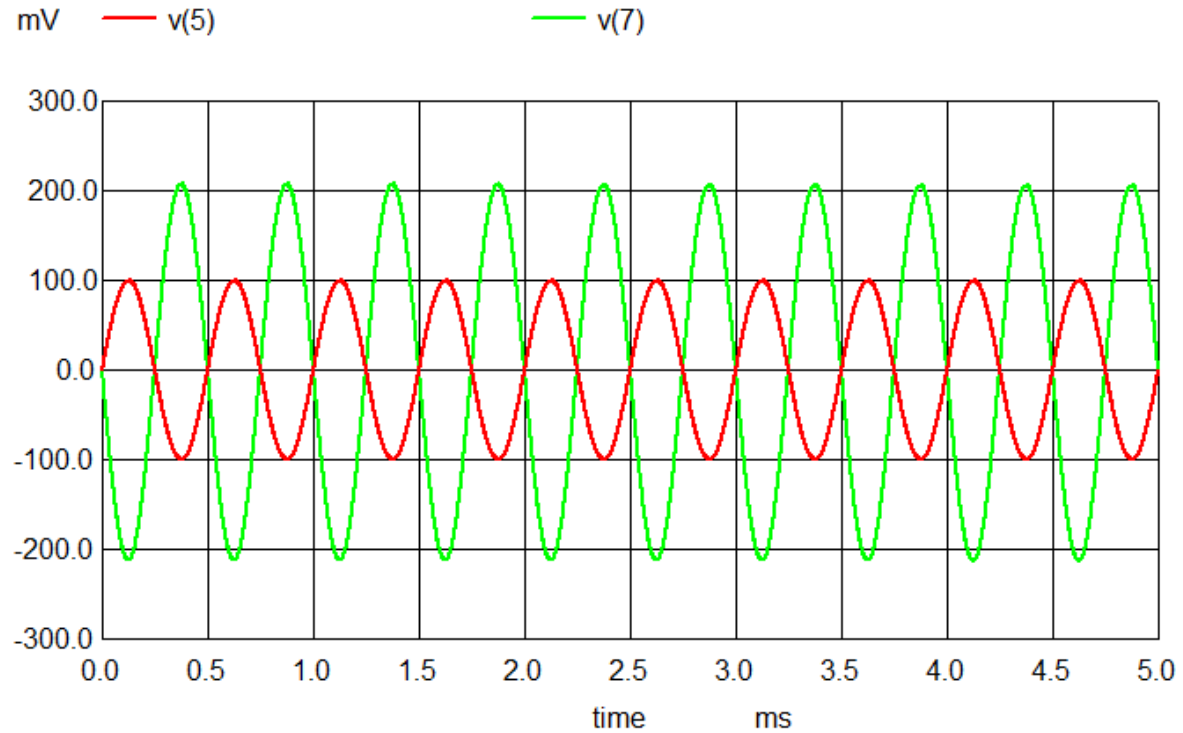
```
set xbrushwidth=2
```

```
*print i(vd) v(3) v(4) i(vd1)
```

```
plot v(7) v(8)
```

```
.endc
```

```
.end
```



### **Question 10**

Q10

```
.model MN4007 NMOS(Kp=500u Vto=1.5 Lambda=0.01 Gamma=0.6 Tox=1200n Phi=.6 Rs=0
Rd=0 Cbd=2.0p Cbs=2.0p Pb=.8 Cgso=0.1p Cgdo=0.1p Is=16.64p)
```

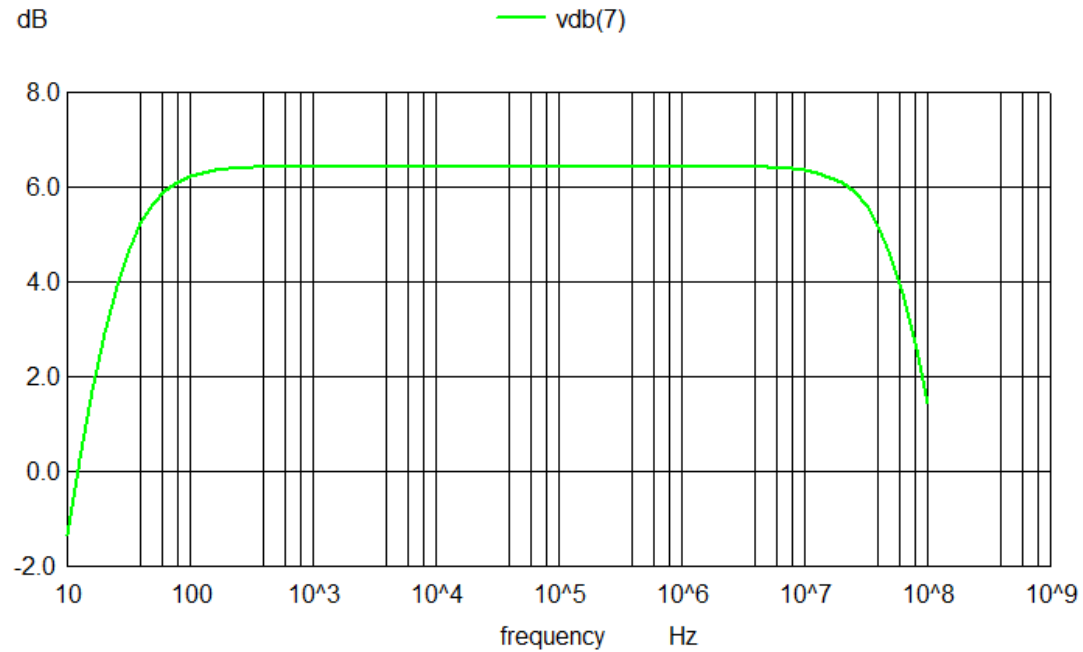
```
Vin 5 0 dc 0 ac 1
Rg 5 6 1k
C1 6 1 2.2u
R2 0 1 3.21k
R1 1 2 7.5K
Vdd 2 0 10V
Vd 2 3 0
Rd 3 4 4k
M1 4 1 0 0 MN4007
C2 4 7 2.2u
RI 7 0 100k
```

```
.ac dec 10 10 100000k
.control
run
*tran 1u 5m
```

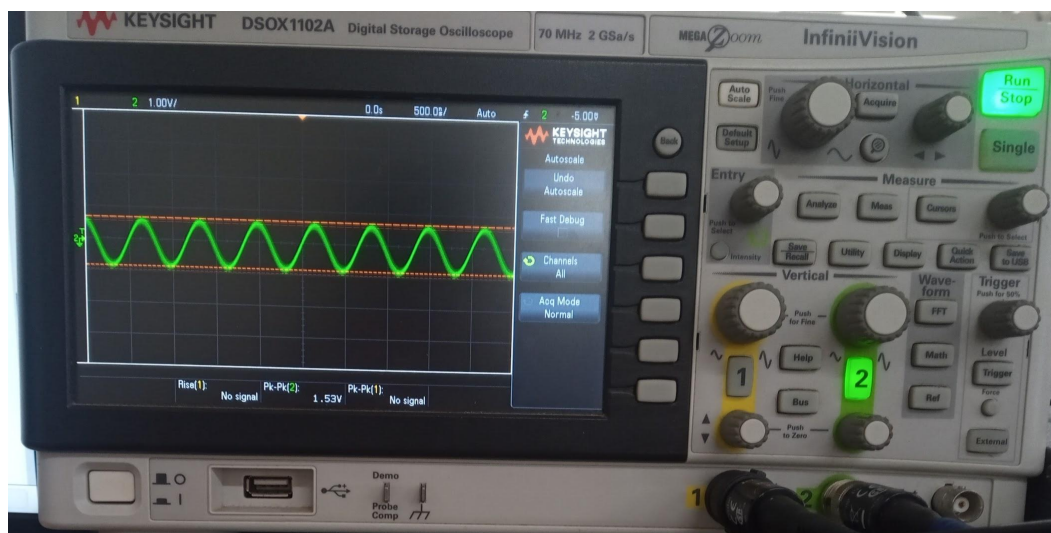


```
*plot v(7),v(5)
plot vdb(7) xlog
```

```
.endc
.end
```

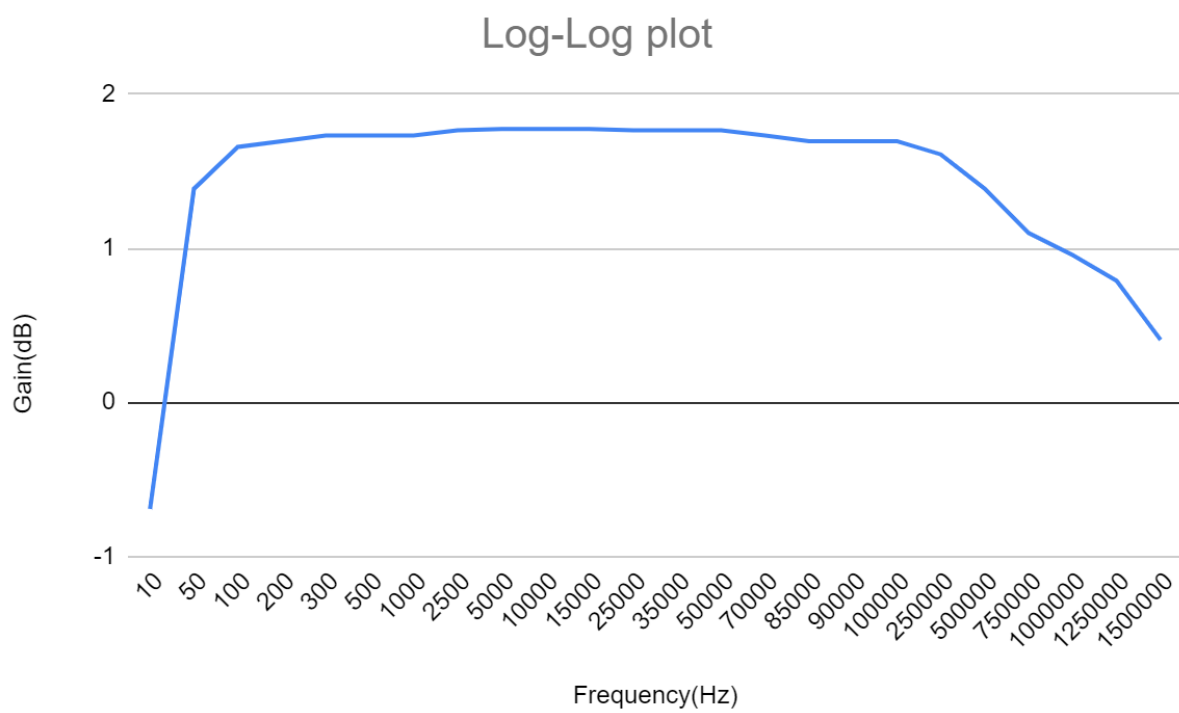


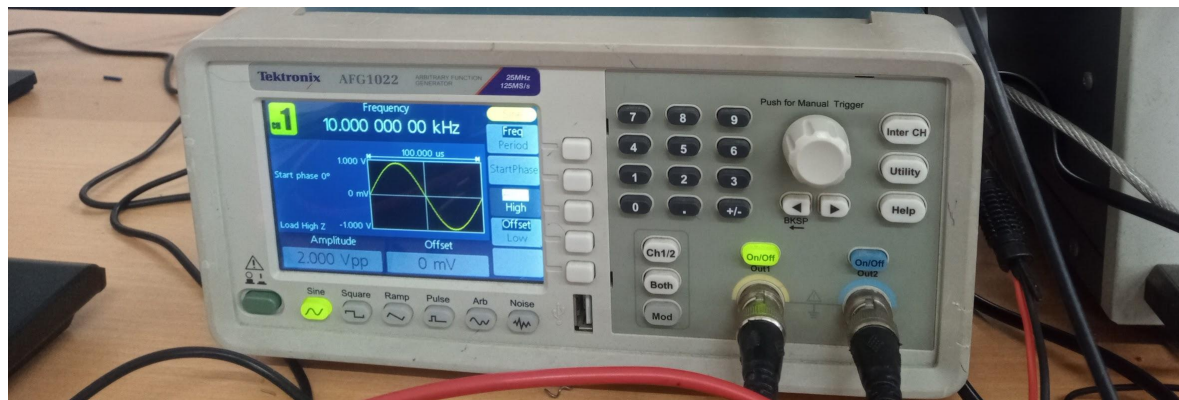
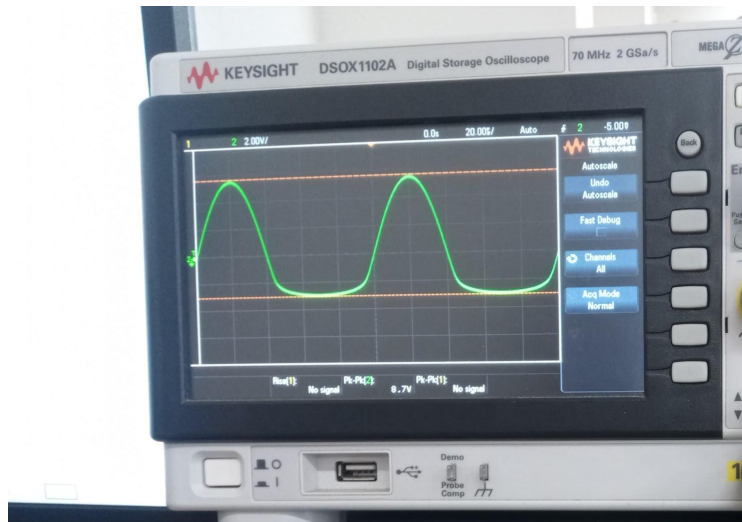
## Hardware



Input(V)	Output(V)	Frequency(Hz)	Gain
0.2	0.11	10	0.55
0.2	0.82	50	4.1
0.2	1.03	100	5.15
0.2	1.11	500	5.55
0.2	1.11	1k	5.55
0.2	1.19	5k	5.95
0.2	1.19	10k	5.95
0.2	1.15	25k	5.75
0.2	1.14	50k	5.7
0.2	1.08	100k	5.4
0.2	1.01	250k	5.05
0.2	0.8	500k	4
0.2	0.58	750k	2.9
0.2	0.51	1M	2.55
0.2	0.47	1.25M	2.35
0.2	0.33	1.5M	1.65







## Discussion

Manvi Baghel :

We learnt how to use the oscilloscope more efficiently. We wrote netlist of nmos for the first time. We also got a hand on designing common source amplifier. Also, finding the appropriate values of resistance and capacitors boosted our thinking capacity.

Shashi Prabha :

In this experiment we got to learn about how NMOS logic work and we saw it's proper biasing on the performance of NMOS Common Source amplifier and plotted it's  $I_D$  vs  $V_{DS}$  characteristics by varying voltage  $V_{GS}$ . We also plotted frequency responses of the amplifier for different values of frequency.