DIGITAL CIRCUITS LAB

EXPERIMENT-9

4 BIT UNIVERSAL SHIFT REGISTER

Shashi prabha
200020043

Aim: Design a circuit for 4-bit universal shift register controlled by a 2 bit control input and performs the following required operation.

Input		Operation
A	B	
0	0	Parallel Loading
0	1	Left Shift
1	0	Right Shift

Components used:

- IC (DM54153) 4:1 MUX
- IC (DM7474) Dual Positive-Edge-Triggered D-Type Flip-Flops with Preset, Clear and Complementary Outputs
- Switches
- LED
- Breadboard
- power supply

Summary of the experiment:

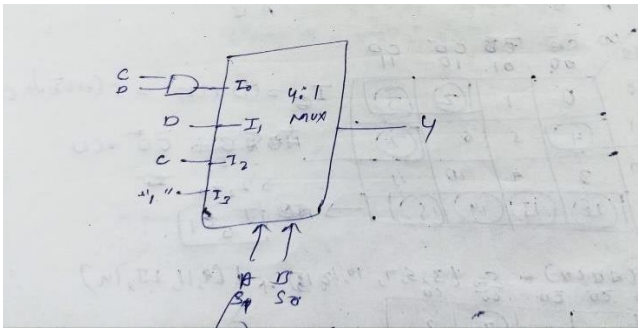
In this experiment we have to design a 4-bit universal shift register controlled by a 2 bit controller input and performs the above operation.

Steps :-

- The operation given to us is opposite of the we studied in class.
- So we made circuit according to given conditions.
- Since this is 4-bit universal shift register it will perform sift in both direction and we required 4 MUX and 4-D-Flip Flop.
- Since there are 2 MUX and 2 FF one IC so we used 2 MUX IC and 2 FF IC .
- In this we used S_1 ,S_2 for right and left shift.
- Inputs for the circuit are S_1,S_2,I_0,I_1,I_2,I_3 which we gav from switch.
- And there are 4 outputs Q_0,Q_1,Q_2,Q_3 these we connected to LED.
- We gave clock from AFG(arbitrary function generator) and saw clock output on oscilloscope.
- Where we saw the right sift, left shift on LED according to clk movement
- **SOME PROPERTIES OF UNIVERSAL SIFT REGISTER**
- Data I0, I1, I2, and I3 are stored in the D-FF
- Parallel input Parallel Output
- Clear is used for resetting
- S0 and S1 are selectors
- They are also used to select the mode of the register, Left shifting, right shifting or parallel loading

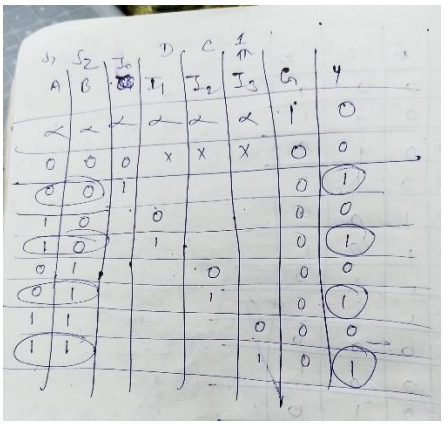
Design Procedure:

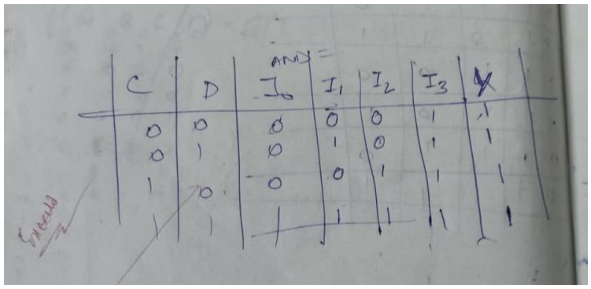
4:1 MUX



Truth table of 4:1 MUX

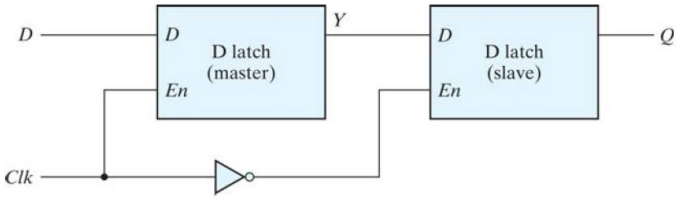
According to which we manipulated MUX





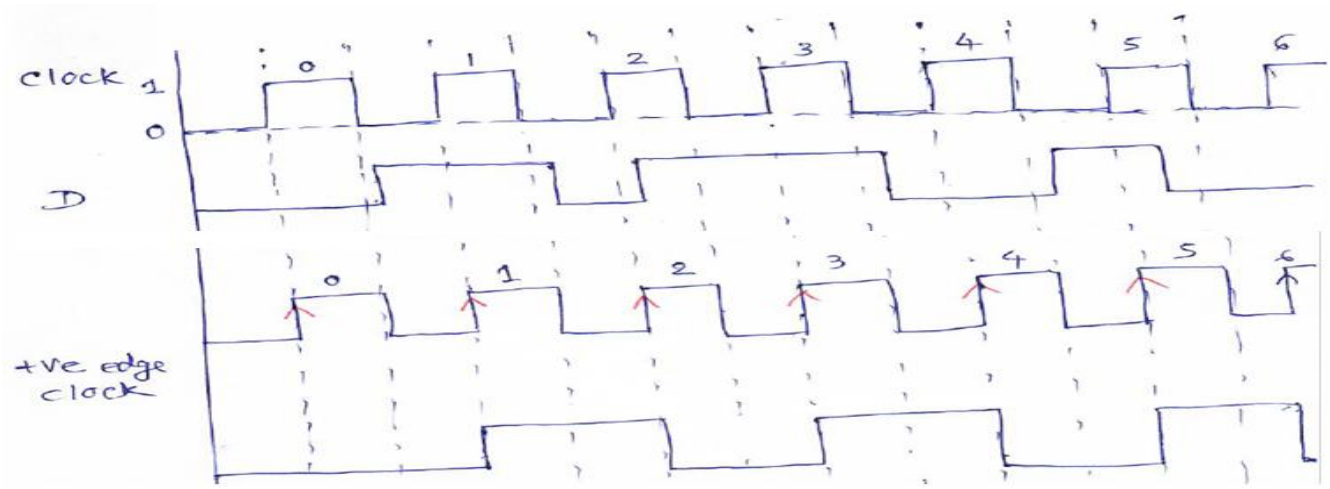
D-type positive-edge-triggered flip-flop:

since we used IC of D type positive-edge-triggered flip-flop



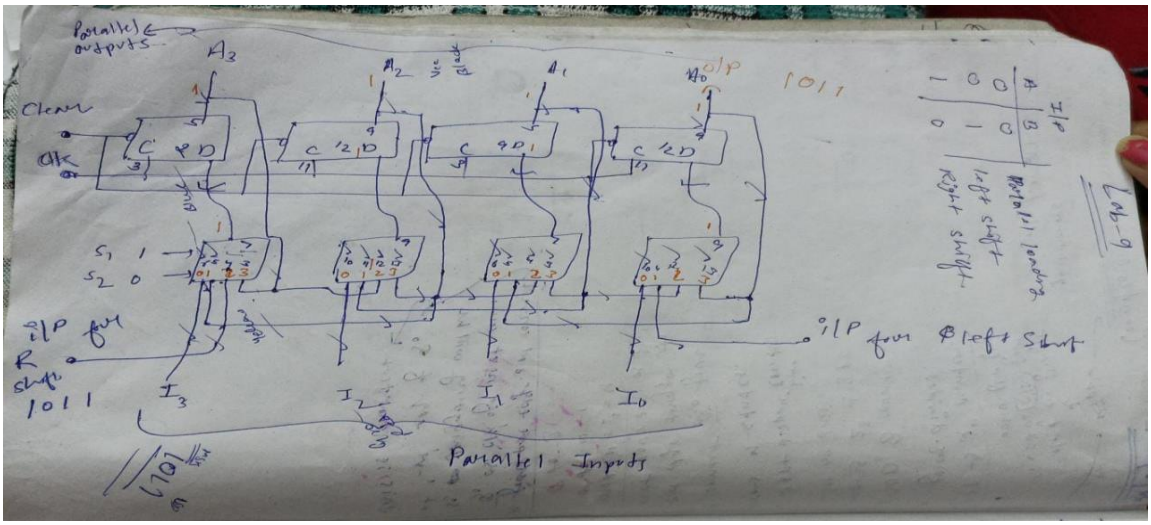
D	C	Q	Q'
0	↑	0	1
1	↑	1	0
X	0	Q_0	Q_0'

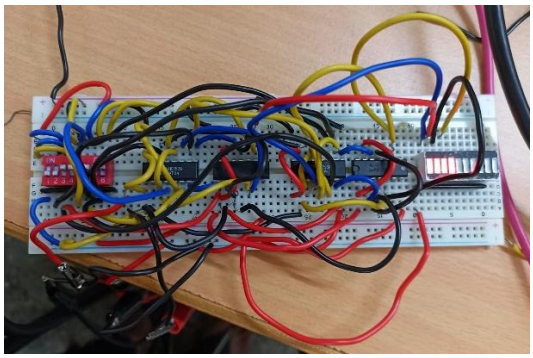
How D-type positive-edge-triggered flip-flop works with clk

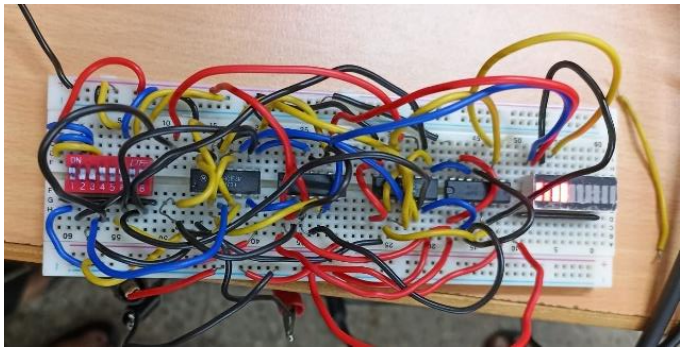


Clk	D	Q(t+1)
0	X	Q(t)
1	0	0
1	1	1

S1	S0	Register output
1	**1**	**No change**
1	0	Shift Right
0	1	Shift Left
0	0	Parallel load







Results and Discussions:

Throughout the experiment we discussed many things like this was opposite to what sir taught us we need to decide many things, like how right shift will work how left , what input should we give, clock, clear ,selectors ,etc. how to give clock in circuit was discussed. Overall it was a nice and very learn full lab we learned a lot.

Conclusion:

In this lab we learned to Design circuit for 4-bit universal shift register controlled by a 2-bit control input which will perform the required operation.