LAB-2 REPORT

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Aim: Designing combinational logic circuits based on CMOS logic families.

Summary of the experiment: Study of CMOS ICs and verifying their functionality.
We got two questions which are as follows:

1A:- bulb in a staircase has two switches, one on the ground floor and the other on the first floor. The bulb can be turned ON and also can be turned OFF only if both the switches are at different states. Design the CMOS circuit for this logic.

ANSWER: XOR

TRUTH TABLE OF XOR:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

1B:- A commercial building a powered by two renewable sources of energy – solar energy and wind energy. There are two alarms associated with both the generation stations that get HIGH if the power generation on any day is below the threshold values. Design the CMOS circuit that implements the logic of a third alarm switched ON if the generation by both the sources is below the threshold on any given day.

ANSWER: AND

TRUTH TABLE OF AND:

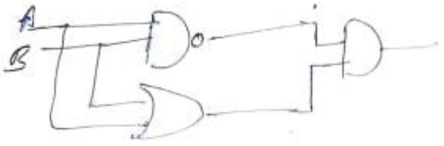
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

By seeing these question we have to find which gates are these and have to make them with CMOS.

Components used: IC **HCF4007UB** switches, 1Kohm resistor array, LED displays, breadboard, power supply.

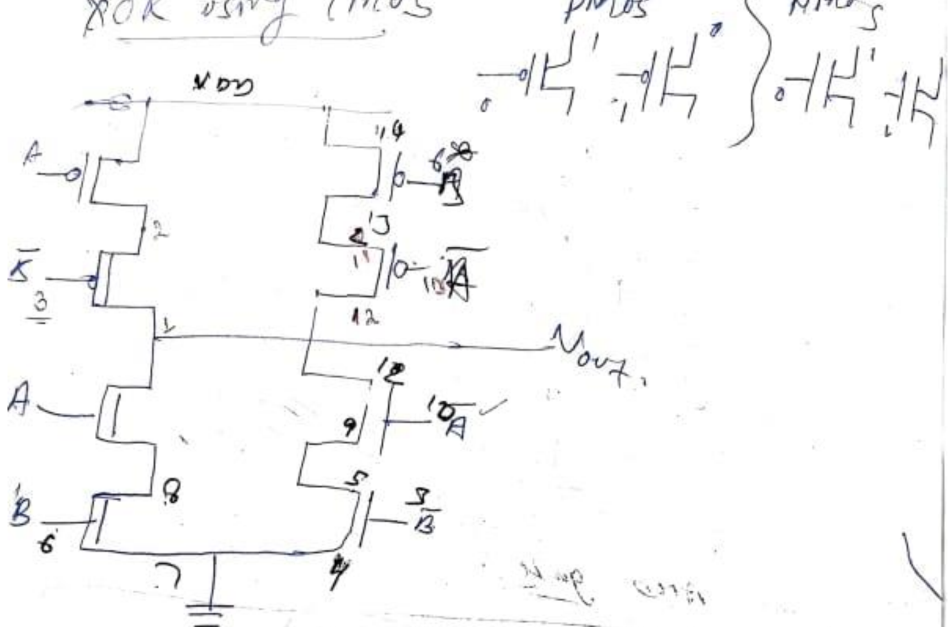
Circuit diagram: Logic circuits of gates.

1) XOR



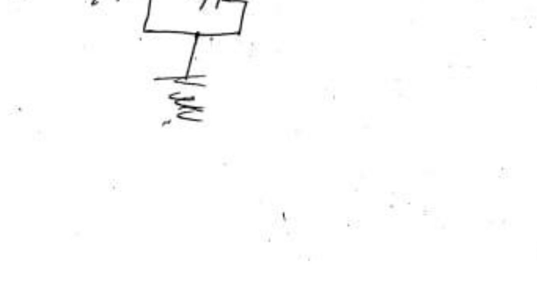
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR using CMOS

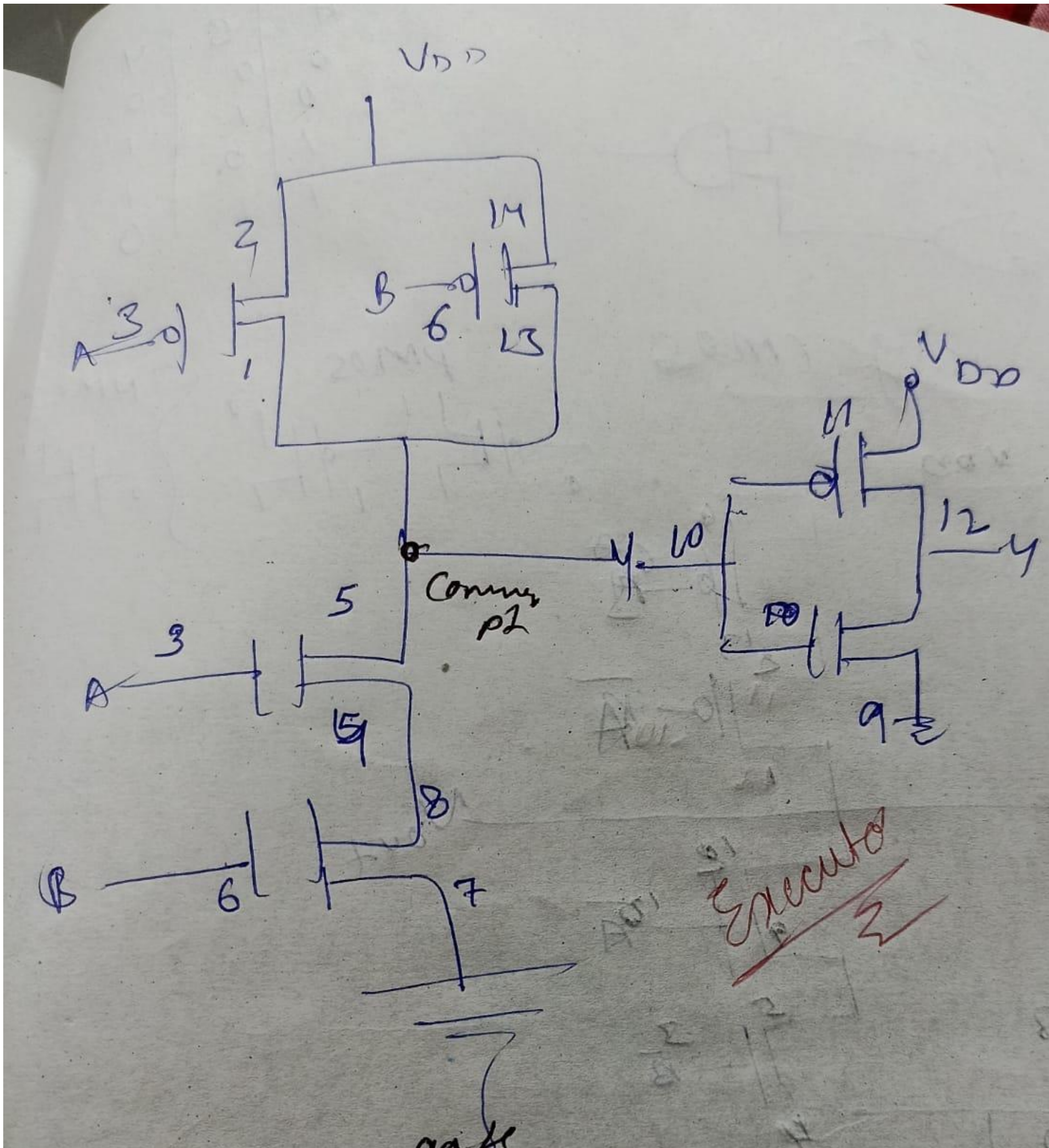


2 i/p XOR gate

2) AND Gate



A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

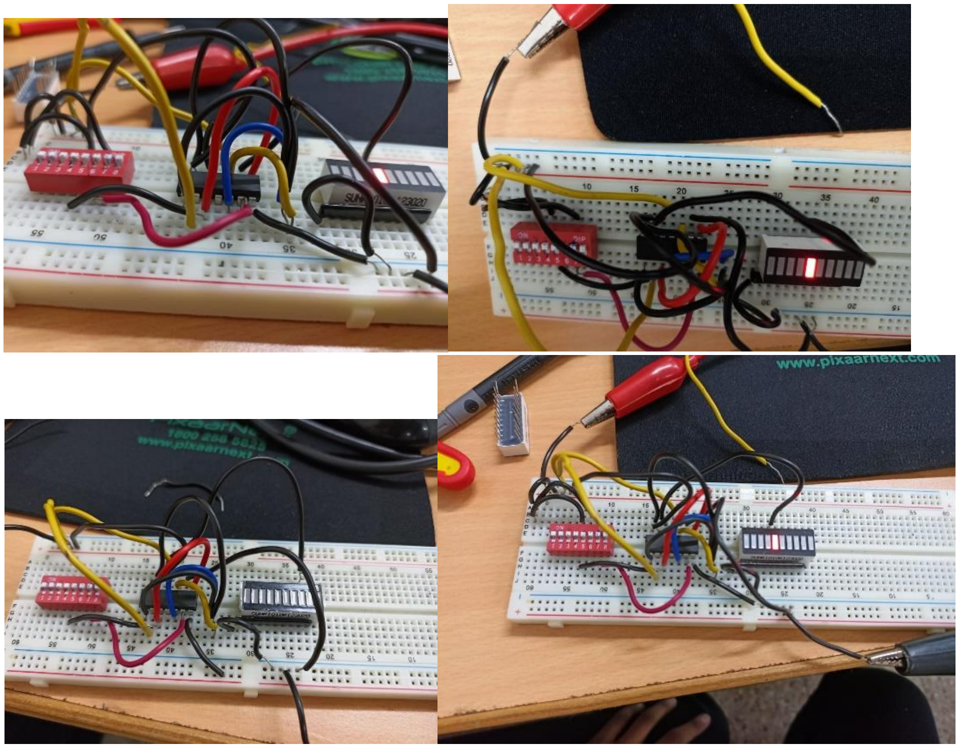


Execute

AND gate

Circuit and Simulation (for CPLD experiments) Snapshots :

Snaps of AND gate.



Results and Discussions:

At the end of the lab , we got to know about functional(internal) structure of CMOS and how it works. There is very important role of numbering in the internal structure of CMOS. There are equal number of PMOS and NMOS in CMOS .

Conclusion:

Study of CMOS ICs and verifying their functionality.

We got two questions ,By seeing the questions we have to find which gates are these and have to make them with CMOS.so in first question gate was XOR and in second AND.

We got the results for AND gate at the end of lab. Pictures are inserted above.