

LAB-3 REPORT

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Aim: Designing combinational logic circuits based on CMOS logic families.

Summary of the experiment: Study of CMOS ICs and verifying their functionality.

In this experiment we made NAND, NOR, OR, XOR, XNOR gates using CMOS static logic

TRUTH TABLE OF XNOR:

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

TRUTH TABLE OF XOR:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE OF AND:

A	B	X
0	0	0

0	1	0
1	0	0
1	1	1

TRUTH TABLE OF NOT GATE:

A	X
0	1
1	0

TRUTH TABLE OF NAND GATE:

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE OF OR GATE:

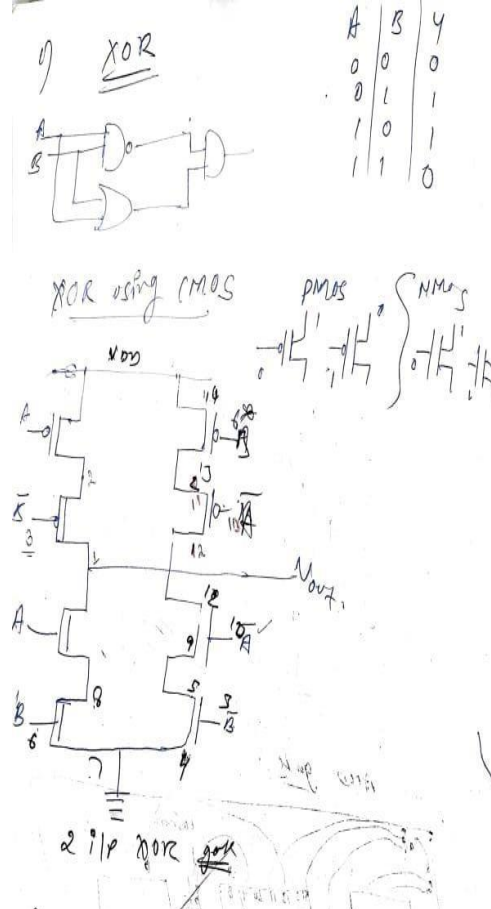
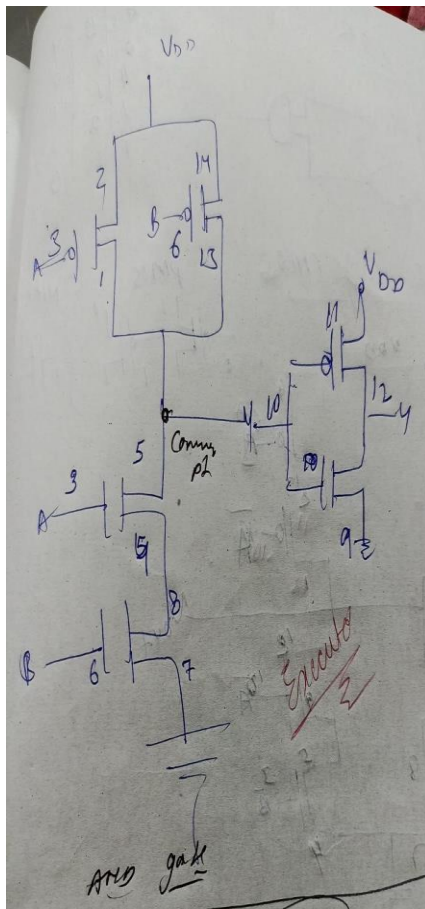
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

TRUTH TABLE OF NOR GATE:

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

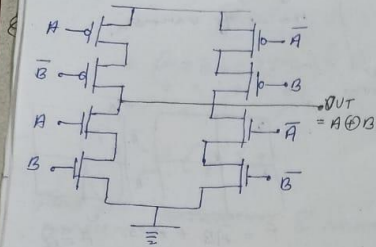
Components used: IC **HCF4007UB** switches, 1Kohm resistor array, LED displays, breadboard, power supply.

Circuit diagram: Logic circuits of gates.

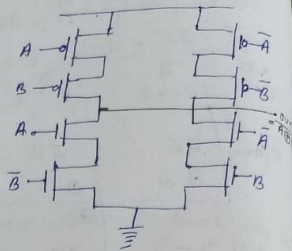


2 Input CMOS static logic

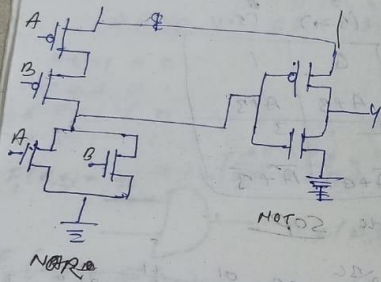
2 input XOR gate



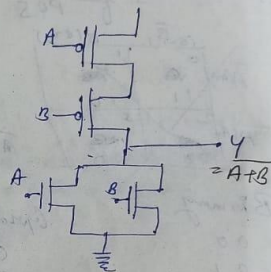
2 input XNOR gate



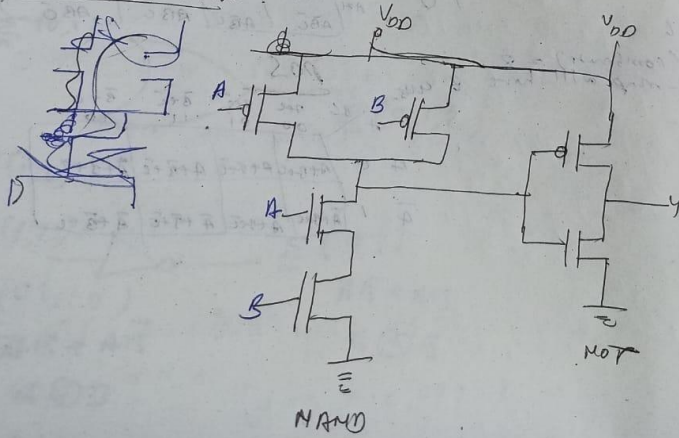
2 input ~~NOR~~ gate :-



2 input ~~NAND~~ gate

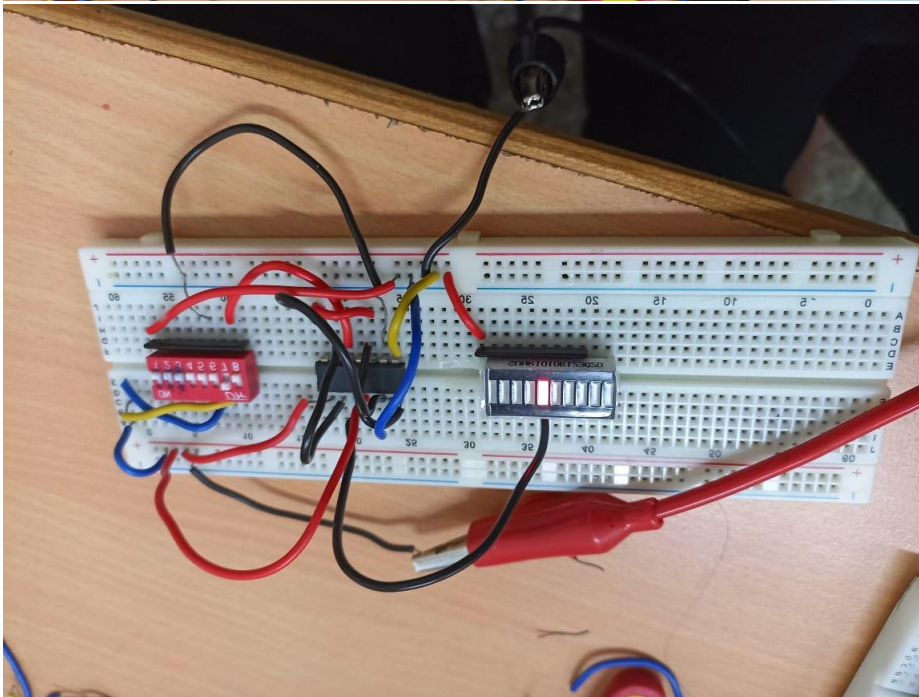
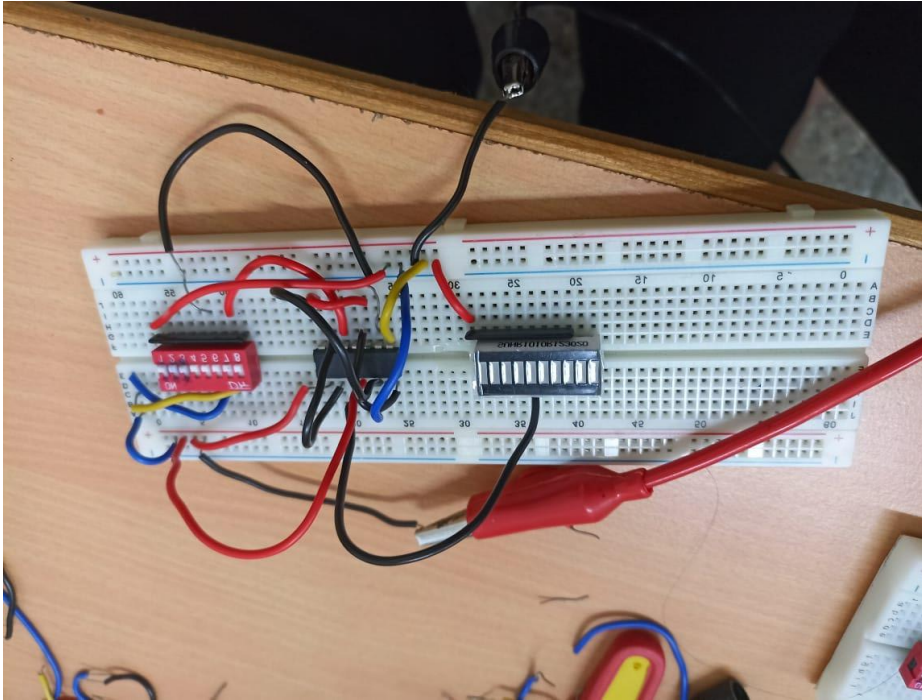


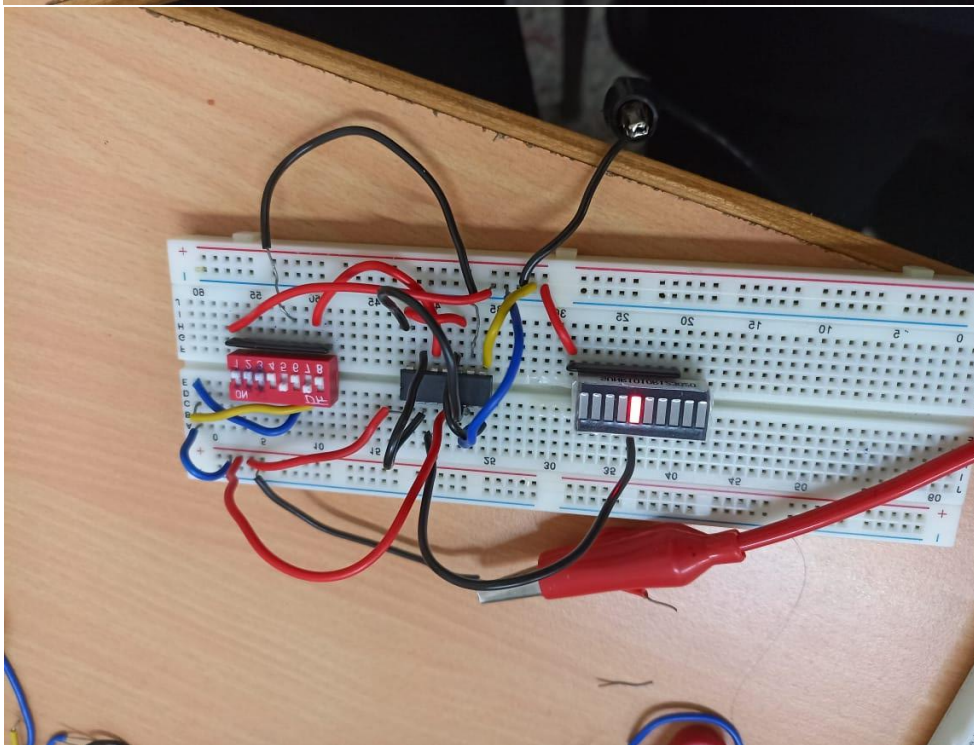
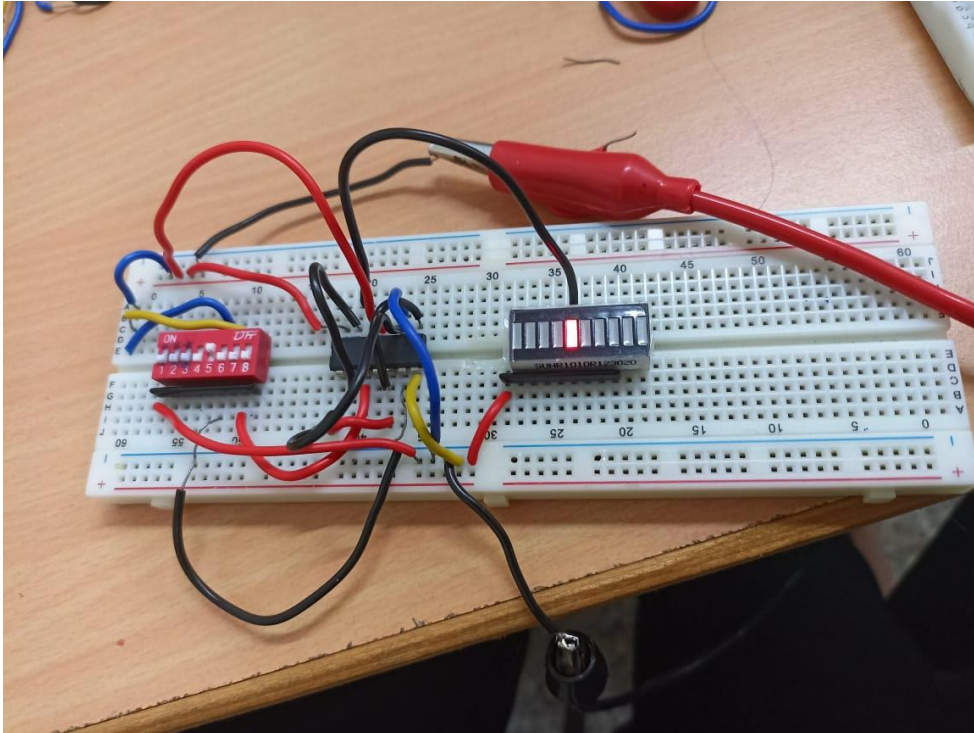
2 input ~~AND~~ Gate :



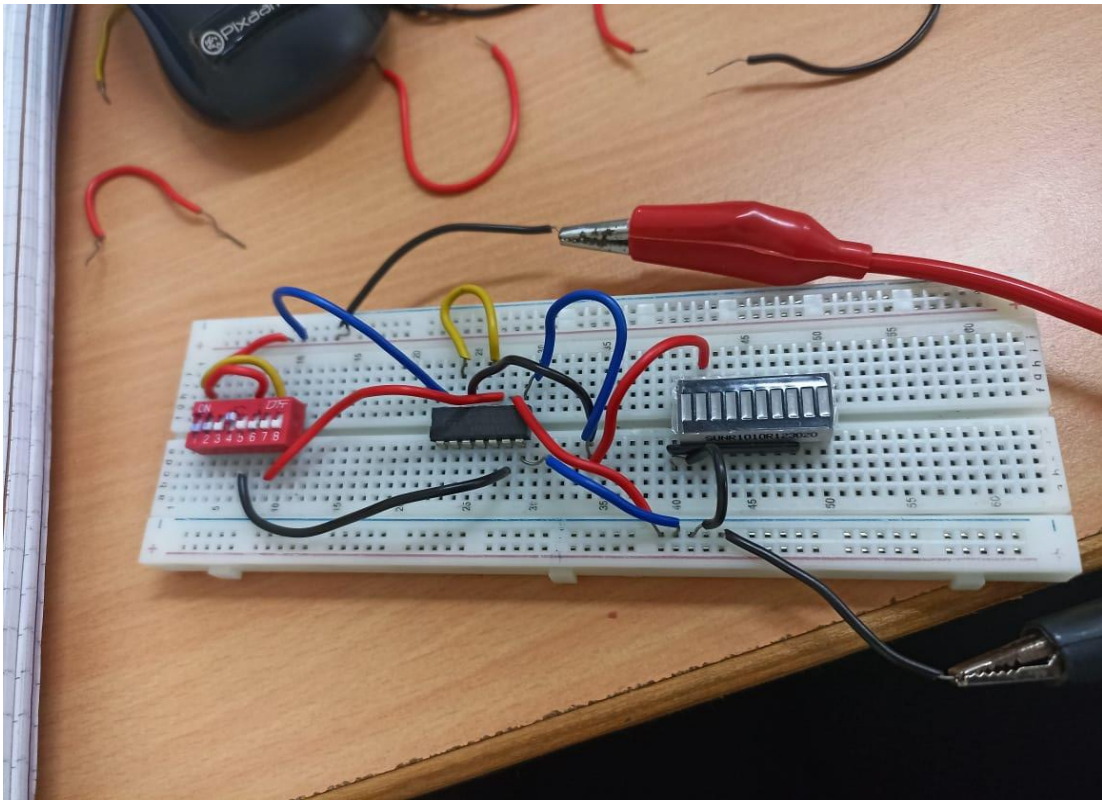
Circuit and Simulation (for CPLD experiments) Snapshots :
Snaps of AND ,NAND,OR,NOR,NOTgate.

OR:

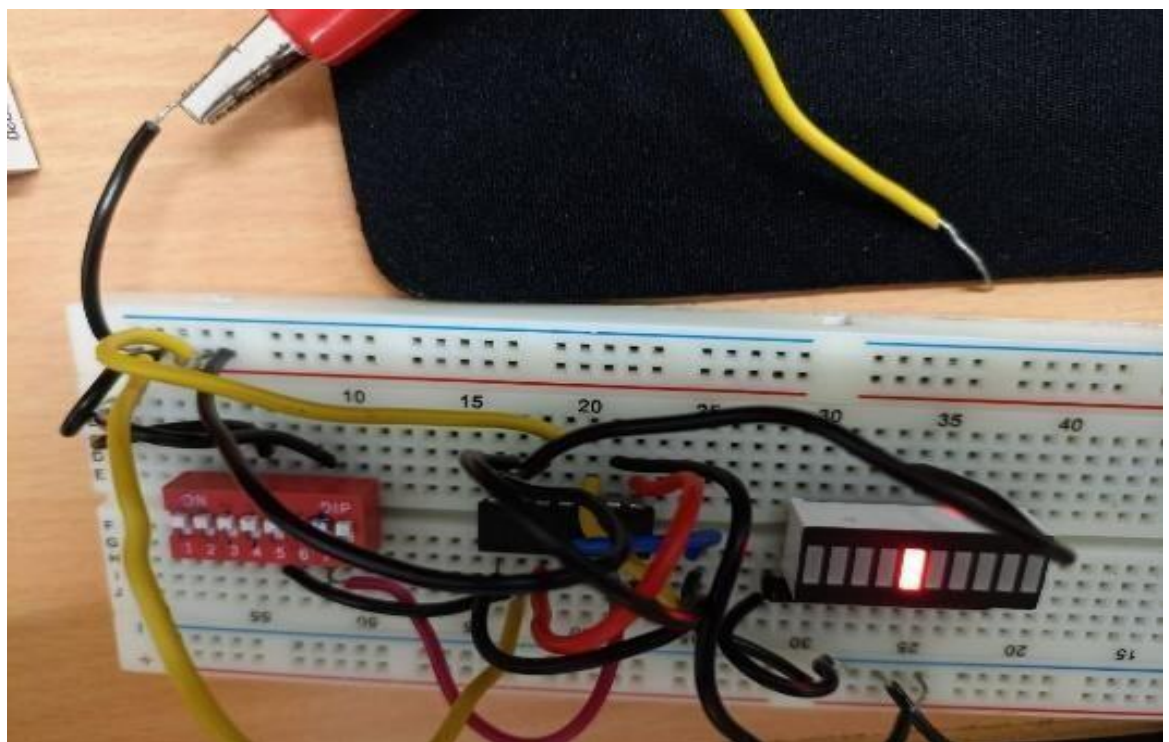
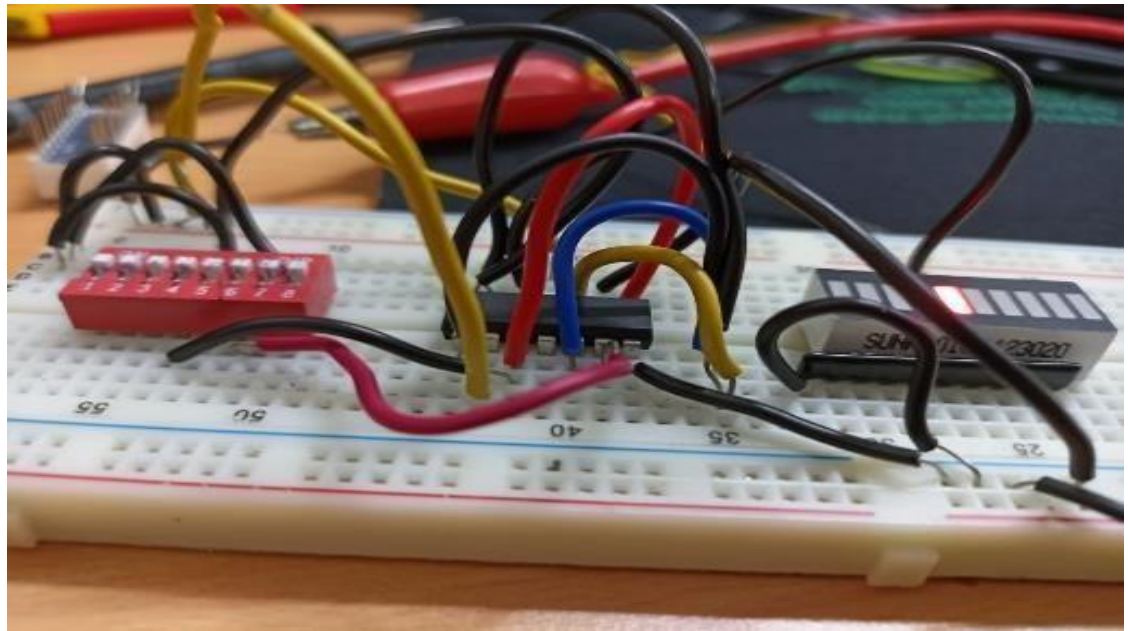


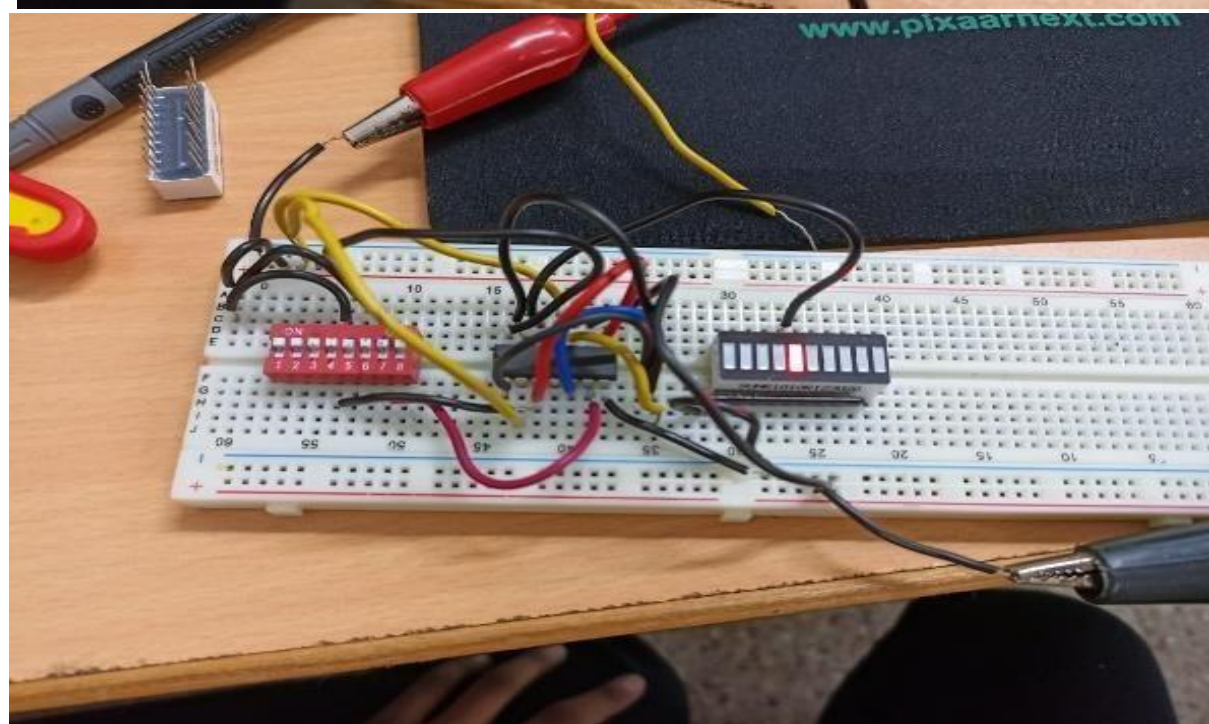
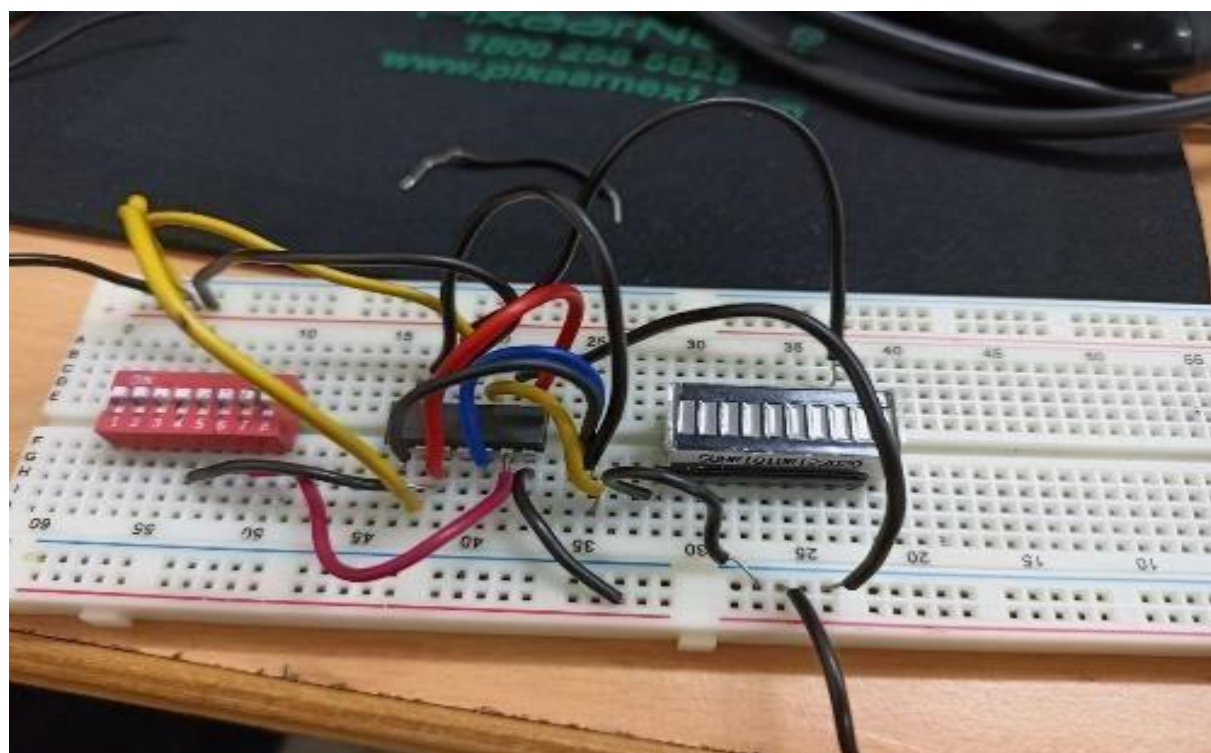


A breadboard circuit featuring a 741 op-amp, a 10k potentiometer, and a 100k resistor. The op-amp is configured with its non-inverting input to ground, its inverting input to a voltage divider, and its output to a potentiometer. A red probe is connected to the output.



AND gate:





Results and Discussions:

At the end of the lab, we got to know about functional(internal) structure of CMOS and how it works. There is very important role of numbering in the internal structure of CMOS. There are equal number of PMOS and NMOS in CMOS, we made 2 input CMOS static logic gates of AND, NAND, NOR, OR, NOT.

we can make AND, OR by putting NOT in the output of NAND and NOR gates.

For XOR gates we need two HC4007

Conclusion:

Study of CMOS ICs and verifying their functionality.

We got the results for AND, NAND, OR, NOR, NOT gate at the end of lab.

Pictures are inserted above.
