

Development of a Differential Voltage Probe for Measurements in Automotive Electric Drives

Michael Grubmüller, *Student Member, IEEE*, Bernhard Schweighofer and Hannes Wiegler

Abstract—Accurate efficiency determination is very important in the field of electric drive research and development. Modern inverters generate pulselength modulated signals with short rise times and high frequencies. Thus, high-accuracy power measurements under non-sinusoidal conditions have to be performed. This requires high precision voltage and current probes, including frequency response flatness over a wide bandwidth and a high linearity up to a few hundred volts. This paper describes the development and characterization of a high voltage differential probe, suitable for precise measurements in automotive electric drives. The main parts of the probe are two input voltage dividers with a further frequency compensation circuit and a difference amplifier. The complete circuit design and the compensation of parasitic effects is explained in detail. Final experiments show, that the developed probe outperforms commercially available probes. The probe has a very flat frequency response up to 1 MHz, a bandwidth of 20 MHz and a linearity better than 250 ppm up to the maximum differential input voltage of 1 kV.

Index Terms—Voltage measurement, power measurement, instruments - probes, automotive electronics, electric machines - AC machines, electric motors, differential amplifiers.

I. INTRODUCTION

ROAD transportation contributed more than 10 % to the worldwide greenhouse gas emissions in 2010 [1]. To reach a significant reduction of these emissions by 2050, new technologies for vehicles will be a key [2]. Although inverter driven motors have already been used in industrial and commercial applications for many decades, a huge progress has been made in the field of power electronics and electric motors regarding cost reduction and efficiency improvement [3], [4], since the automotive industry focused on electric and hybrid vehicles. Due to the fact that efficiency improvement means an advance in driving range, it is one of the keys for the success of electric vehicles; thus accurate power and efficiency measurements are very important for electric drive research and development.

A typical automotive electric drive consists of a high voltage DC source (battery), an inverter and the motor, see Fig. 1. The inverter converts the DC voltage into a 3-phase AC voltage and vice versa. To minimize the power losses in the inverter,

Manuscript received June 21, 2016; revised September 16, 2016; accepted September 29, 2016.

The authors are with the Institute of Electrical Measurement and Measurement Signal Processing, Graz University of Technology, Graz 8010, Austria (e-mail: michael.grubmueller@tugraz.at; schweighofer@tugraz.at; wegler@tugraz.at).

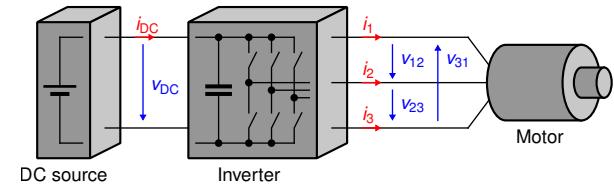


Fig. 1. Components of a typical electric drive. A DC source (battery) provides the power by means of v_{DC} and i_{DC} , the inverter generates a 3-phase system with the phase-to-phase voltages v_{12} , v_{23} and v_{31} to power the motor.

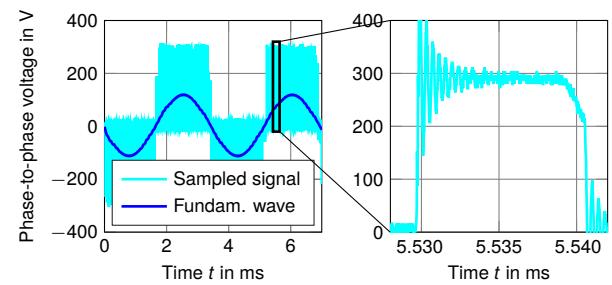


Fig. 2. Measured phase-to-phase voltage of an automotive electric drive. A PWM signal (Sampled signal) is used to approximate a sinusoidal motor voltage (Fundamental wave).

the conversion is done via pulselength modulated (PWM) signals with high switching frequency and short rise times, see Fig. 2. Thus, current and voltage contain high frequency harmonics, which makes the accurate power measurement to a challenging task [5]. In many publications, dealing with power measurements of non-sinusoidal signals, the lack of adequate voltage probes is discussed [6], [7].

This paper describes the development of a superb voltage probe for highly accurate measurements in automotive electric drives. Section II defines the requirements for a voltage probe for measurements in electric drives. Section III compares some commercially available probes and research projects in this field and points out their insufficient performance. This yields to the development of a novel voltage probe, which is described in Section IV. Further, the experiments in Section V show the superb performance of the developed probe.

II. REQUIREMENTS

In a typical automotive drive, only the phase-to-phase voltages are accessible, which makes it necessary to use a differential probe. As a rule of thumb, the sampling frequency should be at least ten times higher than the most significant

harmonic [8]. Thus, a probe for differential amplitudes up to 1 kV and a frequency range from DC to 10 MHz should be sufficient for a modern drive [9]. A more precise formulation is given in [10], where the authors claim a gain accuracy of $\pm 0.1\%$ up to the switching frequency, $\pm 0.25\%$ up to four times the switching frequency and $\pm 1\%$ up to 100 kHz (for a switching frequency of 5 kHz) to achieve a precise power measurement. Considering all these statements, the requirements for voltage measurements in a modern automotive drive (20 to 30 kHz switching frequency) are:

- Differential input voltage range up to 1 kV
- Common mode input range greater than 1 kV
- DC input impedance at least $4 M\Omega$
- Attenuation of 40 dB (100x probe)
- Attenuation flatness
 - $\pm 0.1\%$ up to 1 kHz
 - $\pm 0.2\%$ up to 100 kHz
 - $\pm 1\%$ up to 1 MHz
 - -3 dB bandwidth of at least 10 MHz

III. STATE OF THE ART

A. Commercially available differential high voltage probes

There are many differential high voltage probes on the market. Nearly every manufacturer of oscilloscopes and electrical measurement equipment offers a few different types. It is nearly impossible to select an adequate probe for highly precise measurements in electric drives, because virtually none of the datasheets contain any information about the frequency response flatness and linearity of the probes. Only Keysight [11] and LeCroy [12] provide a frequency response plot to show an overview of the "overall" frequency response and give a graphical proof of the advertised -3 dB bandwidth. Nevertheless, it is not possible to read out a deviation in the (sub-)percent range. Additionally, it may be seen that the manufacturers of the probes allow some peaking in the frequency response to achieve a higher bandwidth.

For an overview, some probes of Testec [13]–[16] are evaluated. These probes are widely used - they are manufactured by Sapphire Instruments and sold by many different vendors (e.g. Testec). Because all these probes are rather low-cost devices, a high-quality probe from Tektronix [17] is also evaluated. The datasheet information of the evaluated probes is summarized in Table I.

For high-accuracy measurements under non-sinusoidal conditions, the gain flatness is a very important information, which is not given in any datasheet. A measurement of the probes' small signal behavior shows, that they have a gain flatness of 1% up to only 50 kHz, see Fig. 3. Therefore it can be assumed that the given value for "Accuracy" is meant to be the accuracy at DC. A second measurement shows the strong non-linearity of the probes, see Fig. 4. Against expectation, the SI-51 which is classified as a high-accuracy probe, shows the worst behavior; the probe's gain changes about 0.5% over the whole input voltage range. The high-quality probe of Tektronix shows the best frequency response flatness but also has a gain error of 1% at 50 kHz and a non-linearity of 0.3% up to 1 kV.

TABLE I
 KEY FACTS OF EVALUATED COMMERCIALLY AVAILABLE PROBES

		Testec SI-9001	Testec SI-9002	Testec SI-51	Testec SI-9110	Tektronix P5205A
Bandwidth	MHz	25	25	50	100	100
Attenuation	%	10x, 100x	20x, 200x	100x	100x, 1000x	50x, 500x
Accuracy	%	2	2	1	2	- ^a 4
Rise time	ns	14	14	7	3.5	- ^a 4
Input impedance ¹	M Ω pF	4 5.5	4 5.5	4 7	4 7	5 4
Input voltage ²	V	70 , 700	140, 1400	700	140, 1400	130, 1300
- Differential	V	700	1400	1400	1400	1300
- Common-mode	V	700	700	300	900	- ^a 4
Output noise	μ V	77	77	84.3	60.8	- ^a 4
SNR ³	dBFs	77	77	84.3	60.8	- ^a 4
CMRR						
- Low frequency	dB@Hz	86@50	80@50	90@60	80@60	80@DC
- High frequency	dB@Hz	66@20k	60@20k	55@1M	50@1M	60@100k
Price	\$	350	350	400	500	1500

¹ Input to ground

² DC + AC peak

³ Calculated value, not stated in the datasheet

^a Not stated in the datasheet

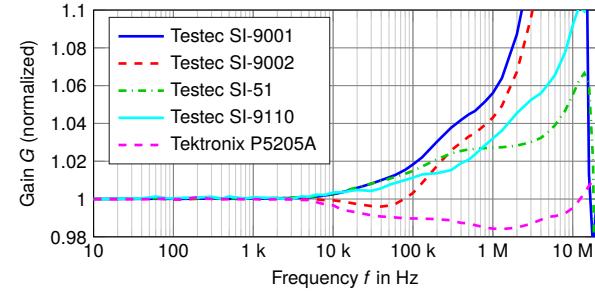


Fig. 3. Frequency response of different commercially available probes. The measurement is done with an input signal of 1 V amplitude.

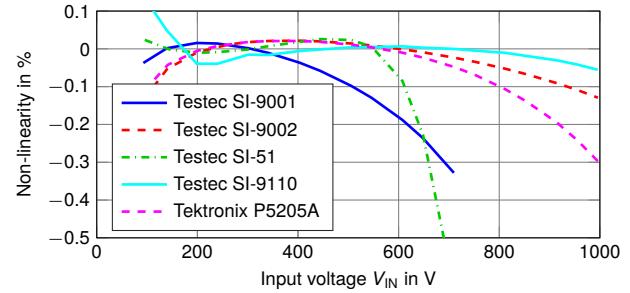


Fig. 4. Non-linearity of commercially available high voltage differential probes. The measurement is done with DC input signals.

B. Research projects

In [18] the authors explain their development of a high voltage differential probe. Their probe is built for differential input voltages up to $\pm 3\text{ kV}$, has a bandwidth of 10 MHz and is able to follow voltage edges up to 75 V/ns. Despite this promising specifications, they reach a gain flatness of only 2% to 3%, which makes it unfeasible for high-accuracy measurements over a wide frequency range.

Further, there are some metrological institutes which also work on voltage dividers, suitable for power measurements; [19] describes a divider which is "built for voltages up to 1 kV and frequencies to 20 kHz"; [20] "focuses on the design of a resistive voltage divider for voltages up to 240 V

(...) with minimal amplitude and phase errors at frequencies up to 100 kHz"; [21], [22] describe the characterization of resistive dividers for a power analyzer which is designed for voltages up to 600 V. All these works cover the design of high-accuracy dividers, but none of them meets the previously given requirements regarding maximum voltage and bandwidth. Also these designs only include single ended voltage dividers which make them unusable for measurements on electric machines where the voltages are not ground related. Although these dividers cannot be used for measurements in automotive electric drives directly, their design-thoughts are a great support towards the development of a new high voltage differential probe.

IV. DEVELOPMENT OF A DIFFERENTIAL PROBE

Fig. 5 shows the schematic of the developed probe. The first stage (A) consists of two identical voltage dividers. The high input voltages on both input terminals are attenuated to a small ground related voltage. To reach a superb frequency response flatness, an additional frequency response correction circuit (B) is used. Finally, a wide bandwidth difference amplifier (C) subtracts the two input voltages to create the ground related difference voltage on the output.

A. Input voltage divider

Each divider consists of $N_1 = 4$ identical blocks containing R_1 , C_1 and R_{DAMP} in the high voltage branch, the components R_2 and C_2 on the low voltage side, some diodes D_1 and D_2 for over-voltage protection and an additional low-pass filter with R_{LP} and C_{LP} at the output. The low-pass filter and the damping resistors R_{DAMP} are inserted to block high frequency disturbances greater than 50 MHz. The protection diodes are low capacitance types to avoid any additional capacitive loading of the voltage divider.

For DC and low frequency signals the circuit acts as a resistive voltage divider built with R_1 and R_2 . Although the attenuation of the probe should be 40 dB, the divider is designed with an attenuation of 54 dB to match the allowed input voltage levels of the following difference amplifier. For the divider, through-hole metal film resistors $R_1 = 1 \text{ M}\Omega$ with a very low temperature coefficient (TC) of $\pm 5 \text{ ppm/K}$ are used. This results in a maximum linearity error of 81 ppm due to self-heating at the maximum input voltage.

For rising frequencies the capacitive divider built with C_1 and C_2 starts dominating. To avoid any changes of the capacitance due to voltage or temperature, ceramic capacitors with a NP0 dielectric material are used. For a flat transfer function

$$G_A(f) \stackrel{!}{=} G_A(0) = \frac{1}{500} \quad (1)$$

has to be valid. For the circuit shown in Fig. 5 (A), this dependence can be approximated by choosing

$$\frac{R_2}{N_1 R_1 + R_2} \stackrel{!}{=} \frac{C_1 / N_1}{C_1 / N_1 + C_2 + C_{\text{LP}}}, \quad (2)$$

where the adjustment is done by changing the capacitor C_2 . Additionally, the non-ideal behavior of the components has

to be considered. Hence, for further simulation the equivalent circuit diagrams for resistors and capacitors shown in Fig. 7 are used. In the resistor equivalent circuit, R represents the nominal resistor. The capacitance C_{PAR} combines all parasitic capacitors, like the internal shunt capacitance and the pad-to-pad capacitance due to the printed circuit board (PCB) mounting. The determination of this value is done by an impedance measurement at high frequencies; for high value resistors like R_1 , the series inductance L_{SER} may be neglected [23]. In the capacitor equivalent circuit, C represents the nominal capacitance. The series elements R_{SER} and L_{SER} represent internal (component itself) and external (leads) parasitic behavior; values for internal elements may be found in the datasheet, values for the external elements strongly depend on the PCB design. To avoid additional external parasitic elements, leads and PCB traces are kept short. Both, the resistors and the capacitors, have a further parasitic capacitance C_{STRAY} . This capacitance occurs between the elements and the surrounding, which are other conductors, the housing of the PCB or even the environment of the probe if there is no conductive housing. Thus it is very difficult to predict a value for C_{STRAY} . To reach a constant and predictable capacitance C_{STRAY} a metal shield, which is connected to ground, is assembled around the divider. An exact calculation of C_{STRAY} is still only possible with a detailed electric field simulation like in [24]. A good approximation may be done by simplifying the geometry to a rectangular coaxial conductor, see Fig. 8. The analytic calculation of the specific capacitance is done in [25] and ends up with

$$C' = 2\varepsilon \cdot \left(\frac{w}{h} + \frac{b}{g} \right) + \frac{4\varepsilon}{\pi} \cdot \left[\log \left(\frac{g^2 + h^2}{4h^2} \right) + 2 \frac{h}{g} \arctan \left(\frac{g}{h} \right) \right] + \frac{4\varepsilon}{\pi} \cdot \left[\log \left(\frac{g^2 + h^2}{4g^2} \right) + 2 \frac{g}{h} \arctan \left(\frac{h}{g} \right) \right], \quad (3)$$

where b , g , h and w are the physical dimensions and ε is the dielectric permittivity of air. For the assembled geometry, a specific stray capacitance C' of 105 pF/m is calculated.

To avoid any loading of the input divider circuit, a unity gain amplifier is attached at the output. A dual supply, field effect transistor (FET) op-amp with high input resistance, low input capacitance and very low input bias current is used for this purpose.

Fig. 9 shows the results for the AC circuit simulation of the voltage divider. The Bode plots for an uncompensated, an undercompensated, a compensated and an overcompensated divider are shown. It can be seen that there is still a deviation of -0.1 dB (approximately 1% gain flatness) at 10 kHz in case of compensation. To reach a frequency response with a better gain flatness, an additional frequency response correction is introduced.

B. Frequency response correction

For the frequency response correction, the input divider is left undercompensated by about 2 dB, see G_A in Fig. 6. This

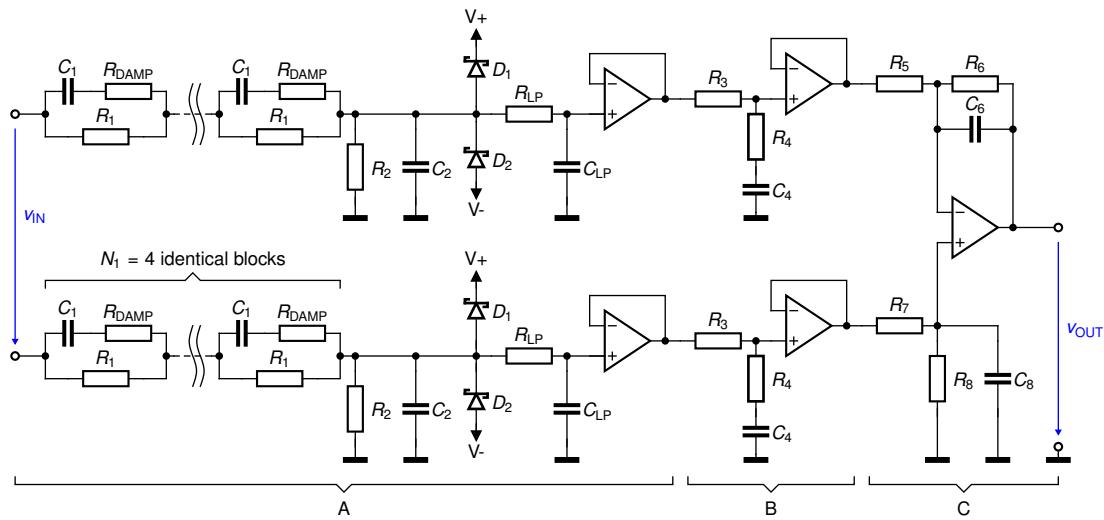


Fig. 5. Schematic of the developed differential probe. It consists of two identical voltage dividers (A), a lag circuit for frequency response correction (B) and a difference amplifier (C).

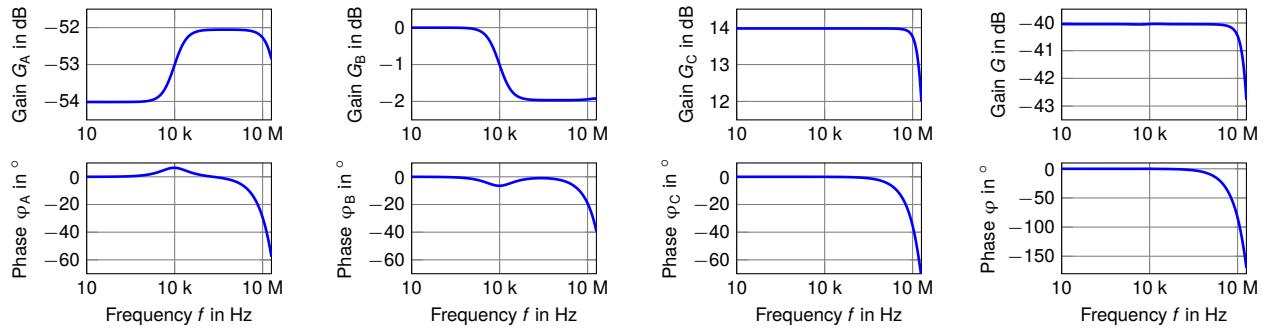


Fig. 6. Simulated Bode plot of the input voltage divider (G_A), the lag circuit for frequency response correction (G_B), the difference amplifier (G_C) and the resulting transfer function of the whole probe ($G = G_A \cdot G_B \cdot G_C$).

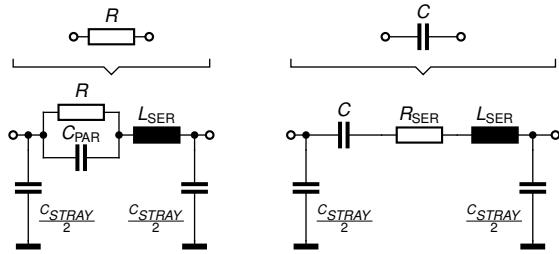


Fig. 7. Equivalent circuit diagrams for real life resistors and capacitors. R and C are the nominal parts, R_{SER} , L_{SER} , C_{PAR} and C_{STRAV} describe the non-ideal behavior.

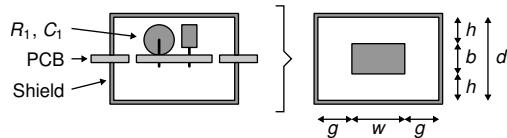


Fig. 8. Assembly of the high voltage branch on the PCB with surrounding copper shield (left) and simplified geometry for approximation of the stray capacitance (right).

is reached by choosing

$$C_2 = 0.7 \cdot C_1 \cdot \frac{R_1}{R_2}, \quad (4)$$

which is empirically determined and confirmed by a circuit simulation. The input divider is then followed by a lag circuit, see (B) in Fig. 5. This circuit has a DC gain of one and attenuates signals at high frequencies due to the resistive divider built with R_3 and R_4 , see G_B in Fig. 6. Choosing values for R_3 , R_4 and C_4 to reach

$$G_B(f) = \frac{G_A(0)}{G_A(f)}, \quad (5)$$

(see also section V, "B. AC gain" for detailed explanation of the calculation) results in a flat overall gain up to a few MHz, see G in Fig. 6.

C. Difference amplifier

To get the difference of the input voltages at the output, a difference amplifier is used, see (C) in Fig. 5. The amplifier is designed with a gain $G_C = 5$ to reach the overall attenuation of 100 for the probe.

The wide bandwidth, combined with the large output voltage swing of ± 10 V requires a high slew rate at the output. Therefore, an externally compensated op-amp is used, which maximizes the slew rate for the desired closed loop gain.

To reach a high common-mode rejection ratio (CMRR), a quad resistor array with a very low matching tolerance ($t_R =$

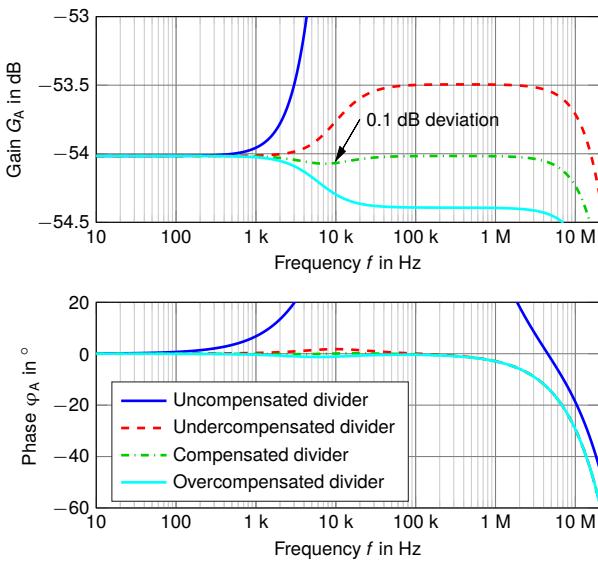


Fig. 9. Bode plot of the input voltage divider. The uncompensated divider (circuit without C_2) can be compensated by adjusting the capacitance C_2 . A too small capacitance results in an undercompensated; a too big capacitance in an overcompensated divider. The compensated divider still shows a 0.1 dB deviation at 10 kHz.

0.025 %) is used for the resistors R_5 to R_8 ; the capacitors are standard $t_C = 5\%$ tolerance types. The contribution of the resistor mismatch to the CMRR of the amplifier is calculated with

$$\text{CMRR}_R = \frac{1}{2} \cdot \frac{2 R_6 R_8 + R_6 R_7 + R_5 R_8}{R_5 R_8 - R_6 R_7} \quad (6)$$

which is derived in [26]. To consider the capacitors, R_6 is substituted by \underline{Z}_6 , which is the parallel circuit of R_6 and C_6 ; R_8 is substituted by \underline{Z}_8 , which is the parallel circuit of R_8 and C_8 . This results in the CMRR

$$\text{CMRR}_{RC} = \left| \frac{1}{2} \cdot \frac{2 \underline{Z}_6 \underline{Z}_8 + \underline{Z}_6 R_7 + R_5 \underline{Z}_8}{R_5 \underline{Z}_8 - \underline{Z}_6 R_7} \right| \quad (7)$$

contributed by the resistors and capacitors. For a worst case calculation $R_5 = R_{50}(1+t_R/2)$, $R_6 = R_{60}(1-t_R/2)$, $C_6 = C_{60}(1-t_C)$, $R_7 = R_{70}(1-t_R/2)$, $R_8 = R_{80}(1+t_R/2)$ and $C_8 = C_{80}(1+t_C)$ has to be chosen. R_{50} to R_{80} , C_{60} and C_{80} are the nominal values, t_R is the net matching tolerance of the resistor array and t_C is the tolerance of the capacitors. Because of using a resistor array, $t_R/2$ is used to guarantee a deviation of maximum t_r from one resistor to all others. Further the op-amp CMRR is considered to get the overall CMRR of the whole amplifier circuit [26], which is done with

$$\begin{aligned} \text{CMRR} &\approx \frac{1}{\text{CMRR}_{RC}} + \frac{1}{\text{CMRR}_{\text{OPAMP}}(0)} \\ &+ \frac{1}{\text{CMRR}_{\text{OPAMP}}(0)} \cdot \frac{f}{f_c}, \end{aligned} \quad (8)$$

where $\text{CMRR}_{\text{OPAMP}}(0)$ is the low frequency CMRR of the op-amp and f_c is the frequency where the CMRR has decreased by 3 dB. The calculation results in a worst case CMRR for the difference amplifier of 80 dB up to 10 kHz. Further the CMRR decreases to 77 dB at 100 kHz, 64 dB at 1 MHz and 44 dB at 10 MHz.



Fig. 10. Ready assembled voltage probe for measurements in automotive electric drives.

V. EXPERIMENTS

All experiments shown in this section are done with the ready assembled voltage probe which is shown in Fig. 10. The probe already contains 4 differential voltage channels, which makes it suitable to measure all voltage signals of an automotive electric drive (3 phase-to-phase voltages and 1 battery voltage). The cost of material for a single probe is about 600 \$ (20 % passive components, 20 % semiconductors, 20 % mechanic components and 40 % PCB).

A. DC gain

A Philips PE-4839 stabilized high voltage source (200 to 2000 V DC output voltage) is used to provide the high input voltage; for voltages below 200 V, a voltage divider is installed between the source and the probe. The input voltage is measured with a Keithley 2100 6 1/2-digit desk voltmeter (100 V and 1000 V DC range); for measuring the output voltage of the probe, a further Keithley 2100 is used (1 V and 10 V DC range). The measurement is iterated in 50 V steps from 100 V up to 50 % of the full-scale range (FSR) (500 V). Afterwards the nominal gain G is defined by approximating the slope of $V_{\text{OUT}}(V_{\text{IN}})$ by using a linear least squares curve fitting.

To calibrate the DC gain, the resistor R_2 of every divider is adjusted. To achieve a good long term stability this is not done via potentiometers. Instead, a resistor with a larger value than nominally required is assembled initially. After a gain measurement, R_2 gets adjusted by placing a further resistor in parallel.

To determine the gain non-linearity, the same setup as for calibrating the DC gain is used. The measurement of input and output voltage is done for voltages from 50 V up to FSR (1000 V), which results in an input voltage dependent gain curve $G(V_{\text{IN}})$. The non-linearity is then defined by the deviation of $G(V_{\text{IN}})$ from the nominal gain G , see Fig. 11. The developed probe has a maximum non-linearity of 250 ppm up to the maximum input voltage.

B. AC gain

A common method for measuring the AC gain is to measure the forward voltage gain S_{21} with a network analyzer [27]. As already mentioned in [28], this method is only applicable down to a few kHz due to the network analyzer's frequency

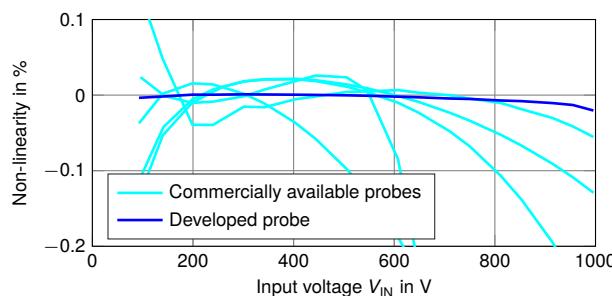


Fig. 11. Non-linearity of the developed probe, compared to the reviewed commercially available probes. The developed probe has a non-linearity of 250 ppm up to the maximum input voltage.

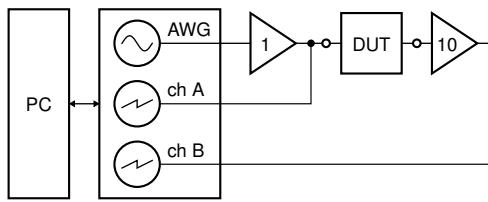


Fig. 12. Experimental setup for measuring the transfer function. The measurement is done with a high resolution USB oscilloscope with an integrated arbitrary waveform generator (AWG).

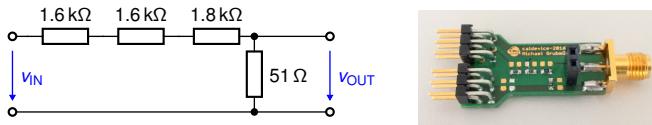


Fig. 13. Calibration device for the transfer function measurement setup. All resistors are surface mount devices in a 0603 package.

range. A further drawback is the insufficient accuracy of network analyzers. Thus, the measurements for this work are done with a Picoscope 5444B USB oscilloscope (200 MHz bandwidth, 125 MS/s sampling rate in 15 bit resolution and 2 channel mode) with an integrated arbitrary waveform generator (AWG). The measurement setup is shown in Fig. 12. To get the transfer function the waveform generator frequency is swept from 10 Hz to 20 MHz and the fast Fourier transformation (FFT) of in- and output voltage at the desired frequency is evaluated. An advantage of using an oscilloscope with an integrated AWG is that both use the same internal clock. Thus it is possible to set the sampling frequency exactly to an integral multiple of the signal frequency, which avoids leakage of the FFT.

Since the gain flatness has to be determined over a wide bandwidth in the sub-percent range, the setup has to be calibrated. For that reason, the device under test (DUT) in Fig. 12 is replaced by the calibration device shown in Fig. 13. To minimize the influence of the parasitic capacitance of the resistors in the calibration device, three resistors in series are used instead of a single $5\text{ k}\Omega$ part in the upper branch. A circuit simulation for the calibration device, using the lumped circuit diagram of Fig. 7, verifies that this device has a 60 ppm gain flatness and less than 1° phase shift up to 20 MHz. Thus it is ideal for calibrating the setup in the range up to the desired

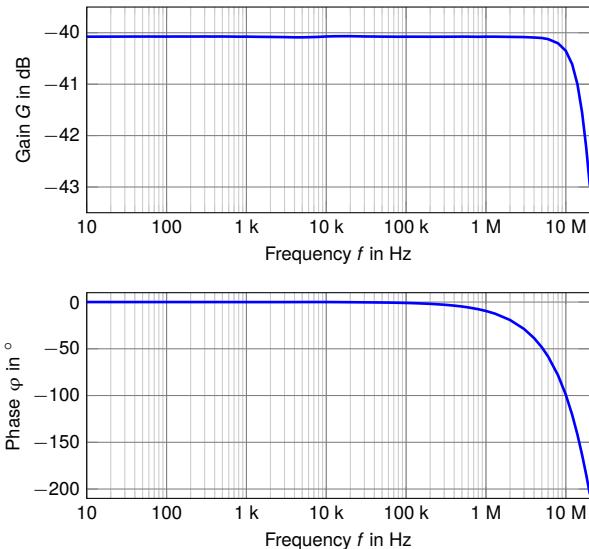


Fig. 14. Bode plot of the calibrated high voltage differential probe, showing the nominal attenuation of 40 dB (100x) and the bandwidth of 20 MHz.

20 MHz.

To calibrate the AC gain of the developed probe, an initial measurement of the undercompensated input divider gain G_A has to be done. In a next step the values for R_4 and C_4 in

$$G_B(f) = \frac{\sqrt{(2\pi f)^2 R_4^2 C_4^2 + 1}}{\sqrt{(2\pi f)^2 (R_3 + R_4)^2 C_4^2 + 1}}, \quad (9)$$

are calculated, so that

$$G_B(f) \stackrel{!}{=} \frac{G_A(0)}{G_A(f)}, \quad (10)$$

by solving the optimization problem

$$\min \left\| G_B(f, R_4, C_4) - \frac{G_A(0)}{G_A(f)} \right\|, \quad (11)$$

in which G_B is the transfer function of the compensation circuit. Since standard ceramic capacitors have a tolerance of 5 %, the capacitors for C_4 have to be handpicked by measuring their value with a LCR meter. Fig. 14 shows the resulting Bode plot of the calibrated probe. It shows the nominal attenuation of 40 dB and the bandwidth of 20 MHz. Fig. 15 shows the normalized magnitude of the Bode plot in a linear scale to point out the very flat frequency response. The probe has a frequency response flatness of $\pm 0.1\%$ up to 1 kHz and $\pm 0.2\%$ up to 2 MHz.

C. Rise time

The rise time of the developed probe is measured by applying a 0 to 500 V voltage step at the probe's input. The output voltage is sampled with a Tektronix TDS7154B 1.5 GHz 20 GS/s digital oscilloscope, see Fig. 16. To get the rise time t_R of the input step, the input signal is also measured with the 100 MHz Testec SI9110 probe. The rise time of the input is then calculated with

$$t_R = \sqrt{t_{R,\text{SI9110}}^2 - t_{R,\text{SI9110}}^2} = 14.1 \text{ ns}, \quad (12)$$

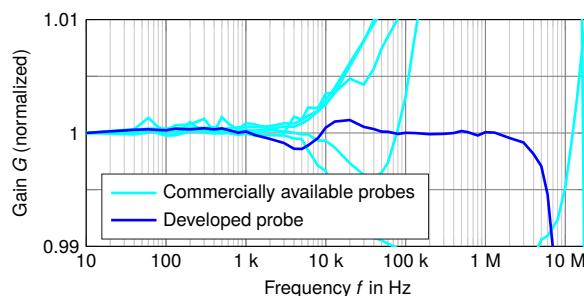


Fig. 15. Normalized gain of the developed differential probe. The probe has a frequency response flatness of $\pm 0.1\%$ up to 1 kHz and $\pm 0.2\%$ up to 2 MHz.

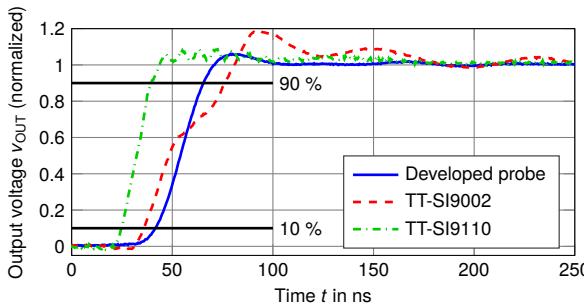


Fig. 16. Step response for a 0 to 500 V input step. For a comparison the normalized output voltages of the developed probe, the Testec SI9002 25 MHz probe and the Testec SI9110 100 MHz probe are shown.

where $t'_{R,SI9110} = 15.6\text{ ns}$ is the measured rise time with the Testec device and $t_{R,SI9110} = 3.5\text{ ns}$ is the true rise time of the Testec device which is given in the datasheet. In a similar way the rise time $t_{R,\text{PROBE}}$ of the developed probe is calculated by

$$t_{R,\text{PROBE}} = \sqrt{t_{R,\text{PROBE}}^2 - t_R^2} = 19\text{ ns}, \quad (13)$$

with a measured rise time $t'_{R,\text{PROBE}} = 23.7\text{ ns}$.

D. Input voltage derating

For DC and low frequency input signals, the input impedance of the probe is dominated by R_1 , which limits the maximum allowable input voltage (input to ground) to 1.5 kV. With increasing frequencies, the input impedance decreases due to capacitor C_1 , which is parallel to R_1 . The resulting increase of the input current causes increasing power losses at the capacitor's C_1 series resistance and the damping resistor R_{DAMP} . To avoid any damages to C_1 and R_{DAMP} the input current has to be limited, which is done by derating the maximum allowable input voltage over frequency. The derating is calculated to limit the temperature rise of C_1 to 20 K and to limit the power loss of R_{DAMP} to 0.25 W. The resulting derating curve is shown in Fig. 17. It shows that the maximum input voltage of 1.5 kV may be applied up to 700 kHz, 1 kV may be applied at 1 MHz and finally a 20 MHz signal must not exceed 80 V.

E. Signal-to-noise ratio

To calculate the signal-to-noise ratio (SNR) of the probe, the RMS output noise E_{PROBE} has to be measured for a

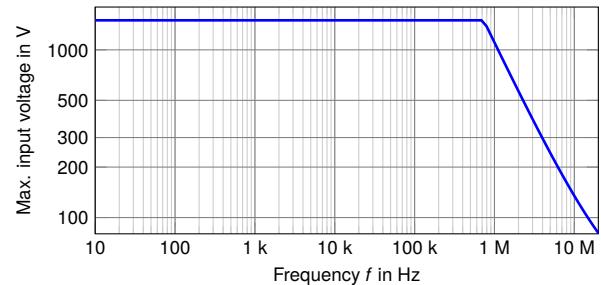


Fig. 17. Derating of the maximum allowable input voltage (DC + AC peak) over frequency.

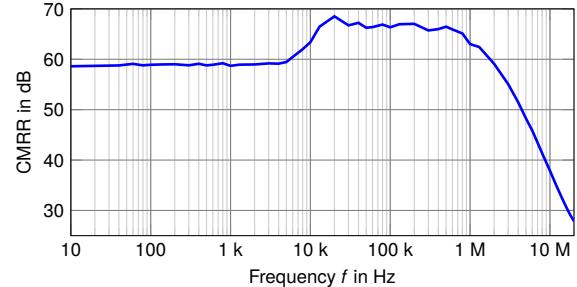


Fig. 18. Common-mode rejection ratio of the developed probe.

bandwidth of 20 MHz. At first, the output voltage of the probe with short-circuited inputs is sampled with an oscilloscope at a rate of 40 MS/s. Calculating the standard deviation of these samples delivers $E'_{\text{PROBE}} = 593.5\text{ }\mu\text{V}$, the combined noise of the probe and the oscilloscope. At second, the inherent noise of the oscilloscope $E_{\text{SCOPE}} = 115.6\text{ }\mu\text{V}$ is measured by taking samples with a short-circuited oscilloscope input. Finally, the output noise of the developed probe is calculated by

$$E_{\text{PROBE}} = \sqrt{E_{\text{PROBE}}'^2 - E_{\text{SCOPE}}^2} = 582.1\text{ }\mu\text{V}, \quad (14)$$

which leads to

$$\text{SNR} = 20 \log \left(\frac{\hat{v}_{\text{OUT},\text{MAX}}/\sqrt{2}}{E_{\text{PROBE}}} \right) = 81.7\text{ dBFS}, \quad (15)$$

where $\hat{v}_{\text{OUT},\text{MAX}}$ is the full-scale output voltage of 10 V.

F. Common-mode rejection ratio

The measurement of the CMRR is done with the same setup as used for measuring the transfer function, see Fig. 12, with the difference that the input signal is now provided to both input terminals of the developed probe. Fig. 18 shows the resulting CMRR of the probe. It can be seen that the CMRR has a constant value of 59 dB up to 10 kHz, increases by a few dB and stays constant up to 1 MHz before it rolls off to 28 dB at 20 MHz. The change of the CMRR at 10 kHz is caused by the two-step calibration procedure; the CMRR up to 10 kHz is dominated by the DC gain calibration, the CMRR at higher frequencies is dominated by the AC gain calibration.

VI. SUMMARY

Accurate power and efficiency measurements are very important for automotive electric drive research and development.

This requires high-accuracy voltage probes for measuring the inverter voltage signals. This paper demonstrates that commercially available probes do not fulfill the requirements regarding gain flatness and linearity. Further the development of a high voltage differential probe is presented. By showing circuit simulation results and rough calculations, the importance of considering the parasitic effects of the circuit components and the PCB assembly is shown. The experimental results confirm the superb performance of the probe, regarding frequency response flatness, non-linearity, rise time, SNR and CMRR.

ACKNOWLEDGMENT

The authors would like to thank the staff of the Instrumentation and Test System Department of the AVL List GmbH for their valuable comments and discussions about measurements in automotive electric drives.

REFERENCES

- [1] Intergovernmental Panel on Climate Change, *Climate Change 2014: Mitigation of Climate Change: Working Group III Contribution to the IPCC Fifth Assessment Report*. Cambridge University Press, 2014. [Online]. Available: <http://mitigation2014.org>
- [2] European Commission, "Roadmap to a single european transport area – towards a competitive and resource efficient transport system," White Paper, 2011. [Online]. Available: http://ec.europa.eu/transport/themes-strategies/2011_white_paper_en.htm
- [3] C. Chan, "An overview of electric vehicle technology," *Proc. IEEE*, vol. 81, no. 9, pp. 1202–1213, Sep. 1993.
- [4] A. Emadi and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in-hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.
- [5] L. Aarniovuori, A. Kosonen, P. Sillanpää, and M. Niemelä, "High-power solar inverter efficiency measurements by calorimetric and electric methods," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2798–2805, Jun. 2013.
- [6] E. Houtzager, G. Rietveld, and H. E. van den Brom, "Switching sampling power meter for frequencies up to 1 MHz," *IEEE Trans. Instrum. Meas.*, vol. 62, no. 6, pp. 1423–1427, Jun. 2013.
- [7] U. Pogliano, B. Trinchera, and D. Serazio, "Development of a system for the accurate measurement of power with distorted signals," in *Proc. IMEKO TC4 Symp.*, Jul. 2013, pp. 538–542.
- [8] A. Domijan, D. Czarkowski, and J. Johnson, "Power measurements of variable speed motors," in *Proc. IEEE Ind. Appl. Conf. (IAS)*, Oct. 1997, pp. 89–96.
- [9] D. Lindenthaler and G. Brasseur, "Signal-bandwidth evaluation for power measurements in electric automotive drives," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 6, pp. 1336–1343, Jun. 2015.
- [10] S. Mukherjee, R. Hoft, and J. McCormick, "Digital measurements of the efficiency of inverter-induction machines," *IEEE Trans. Ind. Appl.*, vol. 26, no. 5, pp. 872–879, Sep./Oct. 1990.
- [11] N2790A 100 MHz, N2791A 25 MHz and N2891A 70 MHz High-voltage Differential Probes, Keysight Technologies, Aug. 2015. [Online]. Available: <http://www.keysight.com>
- [12] HVD3000 Series High-Voltage Differential Probes, Teledyne LeCroy, Inc., Sep. 2015. [Online]. Available: <http://www.teledynelecroy.com>
- [13] SI-9001 25 MHz High Voltage Differential Probe, User Manual, Sapphire Instruments Co. Ltd., May. 2009. [Online]. Available: <http://www.sapphire.com.tw>
- [14] SI-9002 25 MHz High Voltage Differential Probe, User Manual, Sapphire Instruments Co. Ltd., May. 2009. [Online]. Available: <http://www.sapphire.com.tw>
- [15] SI-9110 100 MHz High Voltage Differential Probe, User Manual, Sapphire Instruments Co. Ltd., May. 2009. [Online]. Available: <http://www.sapphire.com.tw>
- [16] SI-51 50 MHz High Voltage Differential Probe, User Manual, Sapphire Instruments Co. Ltd., Apr. 2013. [Online]. Available: <http://www.sapphire.com.tw>
- [17] High-voltage Differential Probes, Datasheet, Tektronix, Jan. 2016. [Online]. Available: <http://www.tek.com>
- [18] A. Van den Bossche and D. Bozalakov, "Two channel high voltage differential probe for power electronics applications," in *Proc. Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–6.
- [19] K.-E. Rydler, S. Svensson, and V. Tarasso, "Voltage dividers with low phase angle errors for a wideband power measuring system," in *Proc. Conf. Precis. Electromagn. Meas. (CPMEM)*, Jun. 2002, pp. 382–383.
- [20] T. Hagen and I. Budovsky, "Development of a precision resistive voltage divider for frequencies up to 100 kHz," in *Proc. Conf. Precis. Electromagn. Meas. (CPMEM)*, Jun. 2010, pp. 195–196.
- [21] U. Pogliano, B. Trinchera, M. Lanzillotti, and D. Serazio, "Characterization of resistive dividers for a wideband power analyzer," in *Proc. Conf. Precis. Electromagn. Meas. (CPMEM)*, Aug. 2014, pp. 130–131.
- [22] U. Pogliano, B. Trinchera, and D. Serazio, "Traceability for accurate resistive dividers," in *Proc. IMEKO TC4 Int. Symp.*, Sep. 2014, pp. 937–941.
- [23] M. Grubmüller, B. Schweighofer, and H. Wegleiter, "Characterization of a resistive voltage divider design for wideband power measurements," in *Proc. IEEE SENSORS*, Nov. 2014, pp. 1332–1335.
- [24] M. Zucca, M. Modarres, D. Giordano, and G. Crotti, "Accurate numerical modelling of MV and HV resistive dividers," *IEEE Trans. Power Del.*, vol. PP, no. 99, pp. 1–1, 2015.
- [25] T. S. Chen, "Determination of the capacitance, inductance, and characteristic impedance of rectangular lines," *IEEE Trans. Microw. Theory Tech.*, vol. 8, no. 5, pp. 510–519, Sep. 1960.
- [26] R. Pallas-Areny and J. Webster, "Common mode rejection ratio in differential amplifiers," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 4, pp. 669–676, Aug. 1991.
- [27] *IEEE Standard for Terminology and Test Methods for Circuit Probes*, IEEE Std. 1696-2013, Feb. 2014.
- [28] K. Loudiere, A. Breard, C. Vollaire, F. Costa, H. Moussa, and R. Meuret, "Wide band measurements in time domain with current and voltage probes for power losses evaluation and EMC measurements on power converters," in *Proc. IEEE Int. Symp. Electromagn. Compat. (EMC)*, Aug. 2015, pp. 1266–1271.



Michael Grubmüller (S'14) received the B.Sc. and Dipl.-Ing. degrees from Graz University of Technology, Graz, Austria in 2011 and 2013, respectively, where he is currently pursuing the Ph.D. degree.

He is currently a Research and Teaching Assistant with the Institute of Electrical Measurement and Measurement Signal Processing, Graz University of Technology. His research interests include electrical measurement technology, circuit design and power electronics.



Bernhard Schweighofer received the Dipl.-Ing. and Dr.techn. degrees from Graz University of Technology, Graz, Austria, in 1998 and 2007, respectively.

He is currently a Research Assistant with the Institute of Electrical Measurement and Measurement Signal Processing, Graz University of Technology. His research interests include analog circuit design and computer engineering.



Hannes Wegleiter received the Dipl.-Ing. and Dr.techn. degrees from Graz University of Technology, Graz, Austria, in 2004 and 2006, respectively.

He has been an Assistant Professor with the Institute of Electrical Measurement and Measurement Signal Processing, Graz University of Technology, since 2014. His research interests include electrical measurement technology, circuit design and electrical energy storage systems.