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Application note

Migrating microcontroller applications from STM32F427/437 and STM32F429/439 to STM32H573/563 and STM32H562 MCUs

Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type by another in the same product family or products from a different family.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate from an existing design based on the STM32F427/437 or STM32F429/439 MCUs, to the STM32H573/563 and STM32H562 MCUs.

This document lists the full set of features available for the STM32F427/437 and STM32F429/439 devices, and the equivalent features on the STM32H573/563 and STM32H562 product lines. This application note also provides a guideline on both hardware and peripheral migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562 datasheets and reference manuals. For additional information, refer to the product datasheets and reference manuals.

1 General information

STM32F427/437, STM32F429/439, STM32H573/563 and STM32H562 MCUs are STM32 32-bit devices based on Arm® Cortex® processors.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The following table presents a non-exhaustive list of terms and acronyms used in this document.

Table 1. Terms and acronyms

Acronym	Definition
A/C	Addresses and commands
DDR3 SDRAM	Double data rate of third generation SDRAM
DDR3L SDRAM	Double data rate of third generation low-voltage SDRAM
DQ	Data
DQMx	Data mask
DQSx_N/DQSx_P	Data strobe N/Data strobe P
GND	Ground
HF	High frequency
LPDDR2 SDRAM	Low-power double data rate 2 SDRAM
LPDDR3 SDRAM	Low-power double data rate 3 SDRAM
MT/s	Mega transfers per second
PCB	Printed circuit board
SDRAM	Synchronous dynamic random access memory
STPMIC	Highly integrated power-management device for microprocessors
VTT	Termination voltage

Table 2. Reference documents

Document number	Title
[1]	Reference manual *STM32MP13xx advanced Arm®-based 32-bit MPUs* (RM0475)
[2]	STPMIC1 datasheet (DS12792)

2 STM32H573/563 and STM32H562 MCUs overview

2.1 Main features

The STM32H573/563 and STM32H562 cryptographic include a larger set of peripherals and with more advanced features, compared to the STM32F427/437 and STM32F429/439.

Some of the improved peripherals for STM32H573/563 and STM32H562 are:

- Security
  - TrustZone®-aware and securable peripherals
  - Active tamper, secure firmware installation, secure firmware upgrade support, secure data storage with hardware unique key
  - Preconfigured immutable root of trust (ST-iROT)
  - Flexible life cycle scheme with secure debug authentication
  - Up to eight configurable SAU regions
  - Additional encryption accelerator engine
    - Advanced encryption hardware accelerator (AES)
    - Public key accelerator (PKA)
    - Secure AES coprocessor (SAES)
    - On-the-fly decryption engine on OCTOSPI (OTFDEC)
- Performance
  - Frequency up to 250 MHz
  - Direct access to flash interface through ICACHE
  - ICACHE for internal and external memories
  - DCACHE for external memories
- Power supply
  - Embedded regulator (LDO)
  - SMPS step-down converter
    - Depending on the package configuration (SMPS or LDO), the regulator is selected by hardware. SMPS and LDO regulator are exclusively selected
    - Both regulators can provide four different voltages (voltage scaling) and can operate in Stop modes
- New peripherals
  - Filter mathematical accelerator (FMAC)
  - CORDIC coprocessor
  - New communication interface: I3C, FDCAN, LPUART, USB Type-C® connector/USB power delivery interface (UCPD), PSSI

Note: This document only manages the differences between STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 for the common features. The new features of STM32H573/563 and STM32H562, mainly linked to the TrustZone® support, are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

The table below summarizes the memory availability of the STM32F427/437, STM32F429/439, STM32H573/563 and STM32H562 deviceMCUs.

Table 3. Memory availability

Products	Flash memory		RAM size (Kbytes)				Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	BKPSRAM	
STM32H573	2 Mbytes	Dual	256	64	320	4	With hardware crypto: AES, PKA, SAES, and OTFDEC
STM32H563	2 Mbytes	Dual	256	64	320	4	NA
STM32H562	2 Mbytes	dual	256	64	320	4	Without Ethernet

Products	Flash memory		RAM size (Kbytes)				Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	BKPSRAM	
STM32F427/ STM32F429	2 Mbytes	Dual	112	16	64	4	NA
STM32F437/ STM32F439	2 Mbytes	Dual	112	16	64	4	With cryptographic processor (CRYP)

2.2 System architecture

The STM32H573/563 and STM32H562 MCUs embed:

- High-speed memories (2 Mbytes of dual-bank flash memory and 640 Kbytes of SRAM)
- a flexible external memory controller (FMC) for devices with packages of 100 pins and more
- one Octo-SPI memory interface (at least one Octo-SPI available on all packages) and an extensive range of enhanced I/Os and peripherals connected to three APB buses,
- three AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562.

Table 4. Bus matrix

Bus type	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
AHB bus matrix masters	**Up to 8 masters**: CPU I-bus, D-bus, and S-bus, DMA1 memory bus, DMA2 memory bus, DMA2 peripheral bus, Ethernet DMA bus, USB OTG HS, DMA bus	**Up to 13 masters**: Fast C-bus, Slow C-bus, CPU S-bus for internal memories, CPU S-bus for external memories, GPDMA1 (featuring two master ports), GPDMA2 (featuring two master ports), SDMMC1, SDMMC2, Ethernet MAC(1)
AHB bus matrix slaves	**Up to 7 slaves**: Internal flash memory ICode bus, Internal flash memory DCode bus, SRAM1, SRAM2, AHB1 peripherals (including AHB to APB bridges and APB peripherals), AHB2 peripherals, FSMC	**Up to 10 slaves**: Internal flash memory, SRAM1, SRAM2, SRAM3, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, FMC, OCTOSPI, AHB3 peripherals, AHB4 peripherals

1. *Not available on STM32H562 devices.*

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The figures below show the system architectures of STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562.

Figure 1. STM32F427/437 and STM32F429/439 devices system architecture

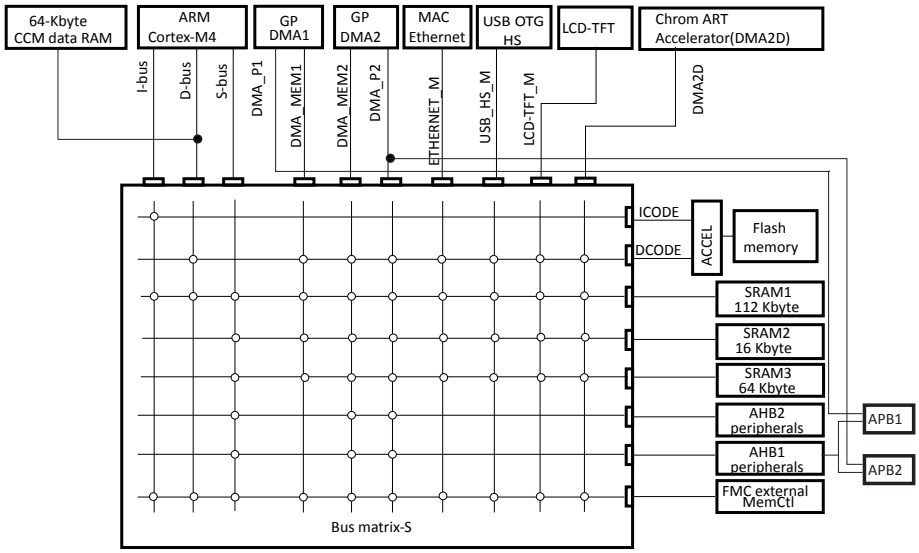
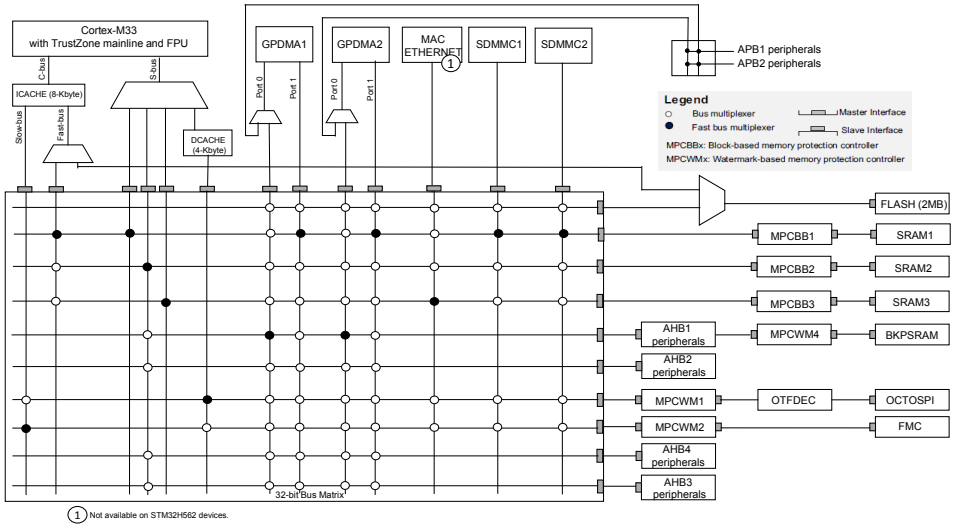


Figure 2. STM32H573/563 and STM32H562 devices system architecture



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3 Hardware migration

This section presents the package and pinout compatibility details for the hardware migration.

3.1 Package availability

The STM32H573/563 and STM32H562 devices offer eight packages from 64 to 176 pins, and two options of pinout:

- LDO option, without internal SMPS: most packages are partial compatible with STM32F427/437 and STM32F429/439 devices
- Internal SMPS option: versions with internal SMPS, fully new packages. For this pinout version, the SMPS step-down converter and the LDO are embedded in parallel to provide the VCORE supply.

All STM32H573/563 and STM32H562 packages are available with two options LDO or SMPS supply for the VCORE (except for LQFP64, WLCSP and VFQFPN68 packages).

For more details on the pinout, refer to the product datasheets.

The table below lists the available packages on the STM32H573/563 and STM32H562 compared to STM32F427/437 and STM32F429/439.

Table 5. Packages available

Package (Size in mm x mm)	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562 (LDO version)	STM32H573/563 and STM32H562 (SMPS version)
LQFP208 (28 x 28 mm)	X(2)	NA	NA
LQFP176 (24 x 24 mm)	X	X	X
LQFP144 (20 x 20 mm)	X	X	X
LQFP100 (14 x 14 mm)	X	X	X
LQFP64 (10 x 10 mm)	NA	X	NA
TFBGA216 (13 x 13 mm)	X(2)	NA	NA
UFBGA176 (10 x 10 mm)	X	X	X
UFBGA169 (7 x 7 mm)	X	X	X
VFQFPN68 (8 x 8 mm)	NA	X	NA
WLCSP	WLCSP143	NA	WLCSP80

1. *X = available, NA = not available*
2. *Not available for STM32F437 devices.*

3.2 Pinout compatibility

The STM32F427/437 and STM32F429/439 devices are not identical with the STM32H573/563 and STM32H562 devices in term of MCU port assignment to package terminals, that is, in term of pinout or ballout. This holds for all common package types of the package listed in Table 5. Packages available .

For the LQFP176 and UFBGA176 packages, the BYPASS_REG pin is replaced in the STM32H573/563 and STM32H562 with a VSS pin.

For the STM32F427/437 and STM32F429/439 devices, the BYPASS_REG pin connected to VDD permits to select the mode where the internal regulator is switched off and the core supply is externally provided.

For the STM32H573/563 and STM32H562 devices, there is no dedicated pin that defines if the regulator is in bypass mode or which regulator(s) is used. Both LDO and SMPS regulators are enabled by hardware depending on package configuration. The regulator is enabled on power-on reset. To supply the VCORE from external source, it is possible to disable the regulator by setting the BYPASS bit.

For the LQFP100 and LQFP144 packages, the VCAP_1 and VCAP_2 pins are replaced in the STM32H573/563 and STM32H562 with a VSS and VDDUSB pin, respectively.

The following sections show the packages pinout figures and the packages pinout differences tables.

3.2.1 LQFP100 package

Figure 3. **STM32H573/563 and STM32H562 LQFP100 pinout**

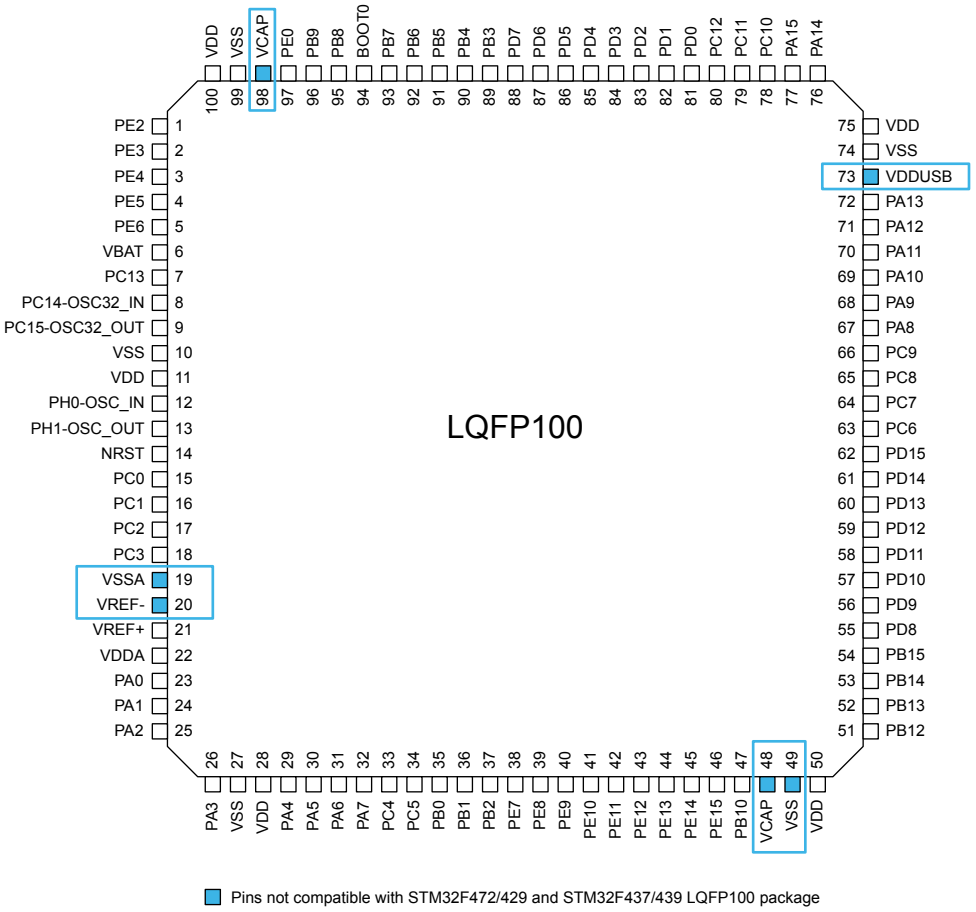


Table 6. **LQFP100 pinout differences**

LQFP100 pin number	STM32F427/437 and STM32F429/439 pinout	STM32H573/563 and STM32H562 pinout
19	VDD	VSSA
20	VSSA	VREF-
48	PB11	VCAP
49	VCAP_1	VSS
73	VCAP_2	VDDUSB
98	PE1	VCAP

3.2.2 LQFP144 package

Figure 4. **STM32H573/563 and STM32H562 LQFP144 pinout**

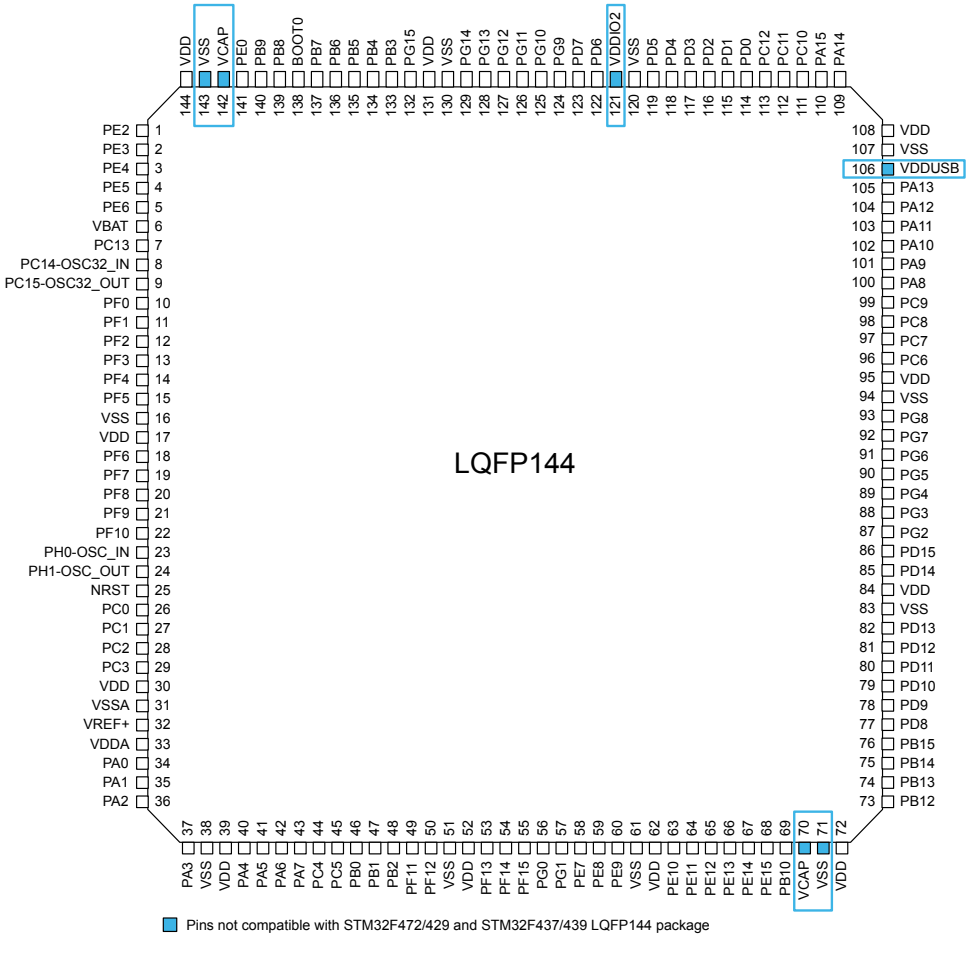


Table 7. **LQFP144 pinout differences**

LQFP144 pin number	STM32F427/437 and STM32F429/439 pinout	STM32H573/563 and STM32H562 pinout
70	PB11	VCAP
71	VCAP_1	VSS
106	VCAP_2	VDDUSB
121	VDD	VDDIO2
142	PE1	VCAP
143	PDR_ON	VSS

3.2.3 LQFP176 package

Figure 5. **STM32H573/563 and STM32H562 LQFP176 pinout**

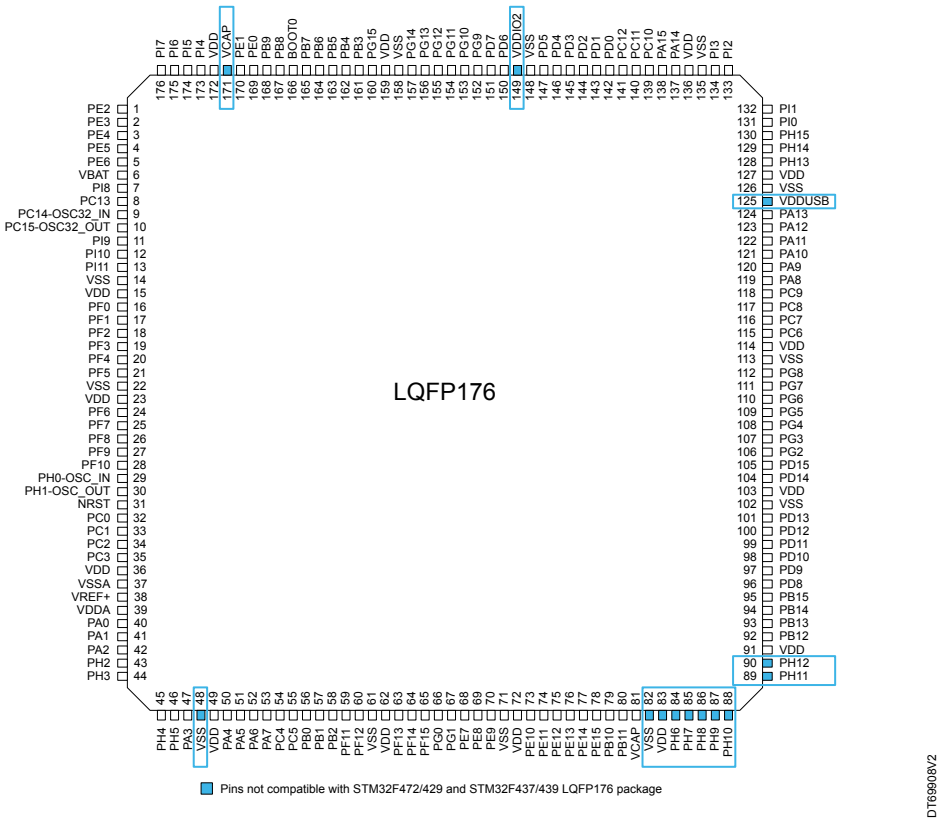


Table 8. **LQFP176 pinout differences**

LQFP176 pin number	STM32F427/437 and STM32F429/439 pinout	STM32H573/563 and STM32H562 pinout
48	BYPASS_REG	VSS
82	VDD	VSS
83	PH6	VDD
84	PH7	PH6
85	PH8	PH7
86	PH9	PH8
87	PH10	PH9
88	PH11	PH10
89	PH12	PH11
90	VSS	PH12
125	VCAP_2	VDDUSB
149	VDD	VDDIO2
171	PDR_ON	VCAP

3.2.4 UFBGA176 + 25 package

Figure 6. STM32H573/563 and STM32H562 UFBGA176 + 25 ballout

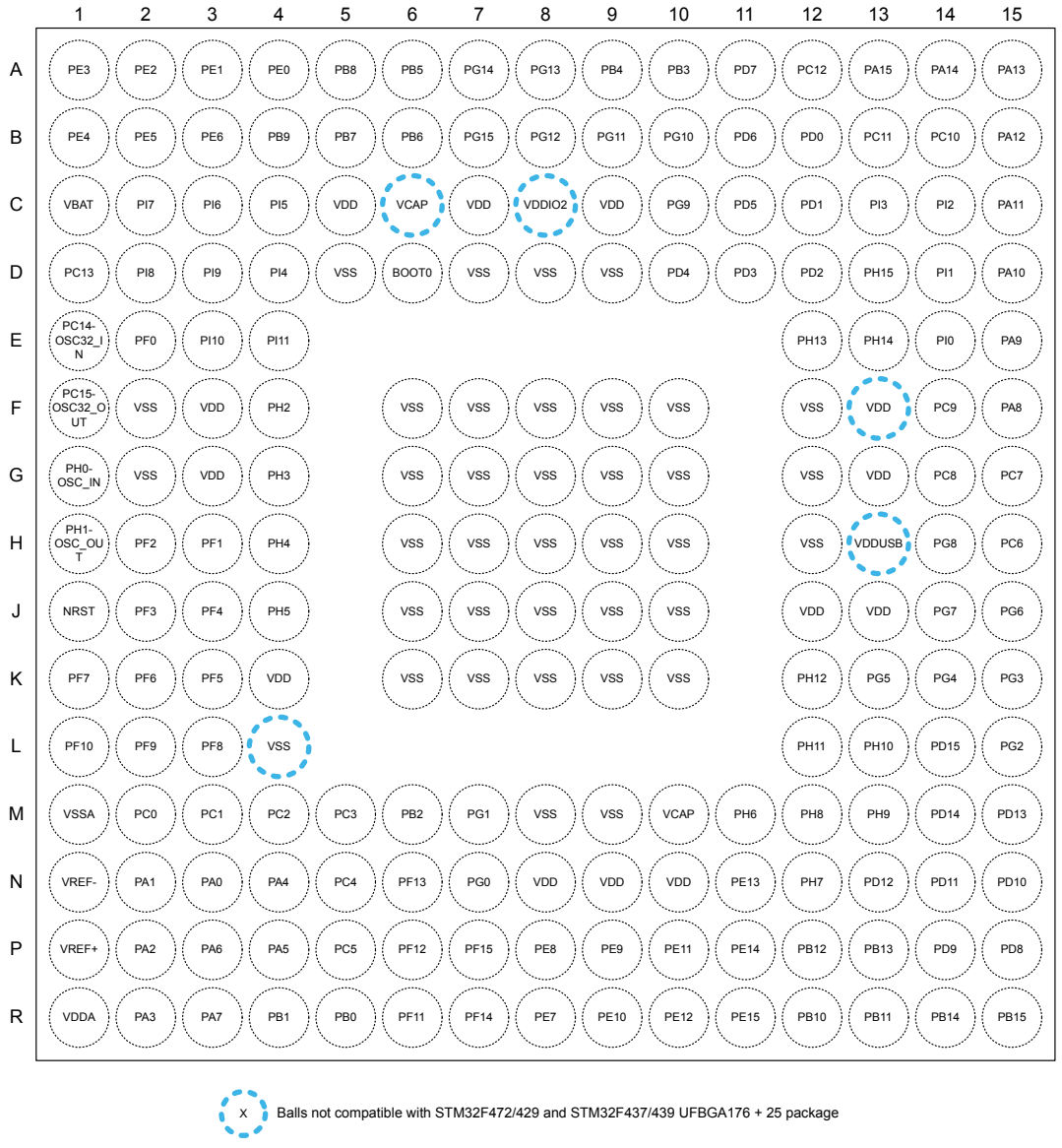


Table 9. UFBGA176 + 25 ballout differences

UFBGA176 + 25 ball number	STM32F427/437 and STM32F429/439 ballout	STM32H573/563 and STM32H562 ballout
C6	PDR_ON	VCAP
C8	VDD	VDDIO2
F13	VCAP_2	VDD
H13	VDD	VDDUSB
L4	BYPASS_REG	VSS

3.2.5 UFBGA169 package

For UFBGA169 package, STM32F427/437 and STM32F429/439 devices are not compatible with the STM32H573/563 and STM32H562 devices.

4 Boot mode compatibility

4.1 Boot mode selection

In STM32F427/437 and STM32F429/439, three different boot modes can be selected through the BOOT[1:0] pins as shown in the table below.

Table 10. Boot modes for STM32F427/437 and STM32F429/439

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main flash memory	Main flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

STM32H573/563 and STM32H562 embed an SBS peripheral that controls boot and security features. For these devices, the main boot control actions are listed below:

- Run the product with or without TrustZone® enabled.
- Select between ST-iROT or OEM-iROT (refer to the reference manual for more details).
- Boot when launching a debug authentication sequence.
- Select boot between the bootloader or the user flash memory boot.
- Initialize the HDPL boot value.

For STM32H573/563 and STM32H562 devices, the boot configurations are selected considering the product settings:

- **BOOT0**: to select booting on user flash memory or RSS (root secure services).
- **BOOT_UBE**: option byte to select the iROT between ST-iROT and OEM-iROT.
- **TZEN**: option byte to activate/deactivate the TrustZone®.
- **sbs_boot_addresses**: list of addresses defined by the flash memory:
  - NSBOOTADD: nonsecure boot address
  - SECBOOTADD: secure boot address
- **PRODUCT_STATE**: option byte to activate the different security mechanisms depending on the product use.
- **sbs_dbg_req:** used to launch the debug authentication protocol when booting.

The tables below present the STM32H573 boot modes, when TrustZone® is disabled or enabled.

Table 11. STM32H573 Boot modes when TrustZone® is disabled (TZEN=0xC3)

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	NA	Bootloader	Bootloader
Provisioning	x	NA	NA	RSS	RSS
Provisioned, Closed, Locked	x	NA	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 12. **STM32H573 Boot modes when TrustZone® is enabled (TZEN=0xB4)**

PRODUCT_STATE	BOOT0 pin	BOOT_UBE FLASH_OPTSR[29:22]	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	0xB4	NA	Bootloader	Bootloader
	1	0xC3	NA	ST-iROT	ST-iROT
Provisioning	x	NA	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	0xC3	ST-iROT	ST-iROT	ST-iROT
	x	0xB4	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

The tables below illustrate the STM32H56x boot modes, when TrustZone® is disabled or enabled.

Table 13. **STM32H563 Boot mode when TrustZone® is disabled (TZEN=0xC3)**

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, Closed, Locked	x	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

Table 14. **STM32H563 Boot mode when TrustZone® is enabled (TZEN=0xB4)**

PRODUCT_STATE	BOOT0 pin	Boot address option-byte selection	Boot area	ST programmed default value
Open	0	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000
	1	NA	Bootloader	Bootloader
Provisioning	x	NA	RSS	RSS
Provisioned, TZ_Closed, Closed, Locked	x	SECBOOTADD[31:8]	Boot address defined by user option byte SECBOOTADD[31:8]	Flash: 0x0C00 0000

4.2 System bootloader

The system bootloader is in the system memory, programmed by STMicroelectronics during the production.

It is used to reprogram the flash memory using one of the following serial interfaces.

The following table shows the supported communication peripherals by the system bootloader. For more details, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

Table 15. Bootloader communication peripherals

System bootloader peripherals	STM32F42xxx/F43xxx I/O pin	STM32H573/563 and STM32H562 I/O pin
DFU[1]	PA11/PA12	
USART1	PA10/PA9	
USART2	NA	PA3/PA2
USART3	PB10 / PB11 and PC10 / PC11	PD9/PD8
CAN	CAN2 (PB5/PB13 PB8/PB9)	FDCAN2(PB5/PB13) [2]
I2C3	NA	PA8/PC9
I2C4	NA	PD12/PD13
I3C1	NA	PB6/PB7
SPI1	NA	PA7/PA6/PA5/PA4
SPI2	NA	PC1/PB14/PB10/ PB12
SPI3	NA	PC12/PC11/PC10/PA15

1. *On STM32H5, USB DFU bootloader does not need an external quartz. It uses internal HSI48.*
2. *On STM32H5xx, FDCAN bootloader does not use an external quartz. It uses HSI and PLL.*

5 Peripheral migration

5.1 Cross-compatibility between STM32 products

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals by definition common to all products
  Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Group2: peripherals shared by all products but with only minor differences (in general to support new features)
  The migration from one product to another is very easy and does not need any significant new development effort.
- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example)
  For this group of peripherals, the migration requires a new development at application level.

For STM32H563/573 and STM32H562, all of the following can be configured as trusted or untrusted: each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, DCACHE, and every small part of flash memory or SRAM. The following table summarizes the available peripherals in STM32F427/437 and STM32F429/439 compared to STM32H573/563 and STM32H562.

Table 16. STM32 peripheral compatibility between products

Peripherals		STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Core		Cortex®-M4	Cortex®-M33
Maximum CPU frequency		Up to 180 MHz	Up to 250 MHz
Flash memory		2 Mbytes	2 Mbytes
SRAMs	System	256 Kbytes (112+16+64+64)	640 Kbytes (256+64+320)
	Backup	4 Kbytes	4 Kbytes
Timers	General purpose	2 (32 bits) and 8 (16 bits)	2 (32 bits) and 8 (16 bits)
	Advanced control	2(16 bits)	2 (16 bits)
	Basic	2 (16 bits)	2 (16 bits)
	Low power(1)	No	6 (16 bits)
	SysTick timer	1	2
	Watchdog timers (independent, window)	2	2
Communication interfaces	**SPI/I2S**	Up to 6 SPIs, 2 with muxed full-duplex I2S	Up to 6x SPIs. Including three muxed with full-duplex I2S and up to 5x additional SPI from 5x USART when configured in Synchronous mode (one additional SPI with OctoSPI)
	I2C	3 (Sm and Fm interfaces (SMBus/PMBus)	4 (Sm, Fm, and FM+ interfaces (SMBus/PMBus)
	I3C(1)	No	1
	USART/UART	4 / 4	6 / 6
	LPUART(1)	No	1
	USB	USB OTG FS and USB OTG HS	USB FS
	UCPD (1)	No	Yes

Peripherals		STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Communication interfaces	CAN	2	2 FDCAN(1)
	SAI	1	2
	SDIO/SDMMC	1	2
	DCMI	Yes	Yes
	PSSI(1)	No	Yes
	Ethernet	Yes	Yes (not available on STM32H562)
Flexible memory controller (FMC)		Yes (8,16,32-bit data bus width)	Yes (8,16-bit data bus width)
OCTOSPI(1)		No	1
HDMI-CEC(1)		No	Yes
CRC		Yes	Yes
LCD-TFT display controller		Yes	No
Chrom-ART Accelerator DMA2D		Yes	No
DMA		2	2 GPDMA (1)(featuring two master ports) TrustZone® support/linked-list
CORDIC coprocessor(1)		No	Yes
Filter mathematical accelerator (1)(FMAC)		No	Yes
Real-time clock (RTC)		Yes	Yes
Random number generator (RNG)		Yes	Yes
SAES, AES(1)		No	Yes
Public key accelerator(1) (PKA)		No	Yes
HASH (SHA-512)		Yes	Yes
Cryptographic processor (CRYP)		Yes	No
On-the-fly decryption engine(1) (OTFDEC)		No	Yes
GPIOs		Up to 168	Up to 140
ADC (12 bits)	count	3 (12-bit ADC 2.4 MSPS and 7.2 MSPS in triple interleaved mode)	2 (12-bit ADC with up to 5 MSPS)
	Number of channels	16/24	20/20
DAC (12 bits)	Count	1	1
	Number of channels	2	2
RCC		Yes	Yes
Operating temperatures		Ambient temperature: : –40 to +85°C /–40 to +105°C Junction temperature: –40 to + 125°C	Ambient operating temperature: – 40 to 85°C/– 40 to 125°C Junction temperature: – 40 to 105°C/– 40 to 130°C
Operating voltage		1.7 to 3.6 V	1.71 to 3.6 V
Internal voltage reference buffer		No	Yes

1. *New versus STM32F427/437 and STM32F429/439.*

5.2 System peripherals

5.2.1 Embedded flash memory (FLASH)

The following table compares the flash memory interface on the STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices.

Table 17. FLASH features

Flash memory	STM32F427/429 and STM32F437/439	STM32H573/563 and STM32H562
Main / program memory	• Up to 2 Mbytes (dual bank) • 4 sectors of 16 Kbytes • 1 sector of 64 Kbytes • 6 sectors of 128 Kbytes	• Up to 2 Mbytes of nonvolatile memory (dual bank) • Flash memory read operations supporting multiple lengths: 128 bits, 64 bits, 32 bits, 16 bits, or one byte • 8 Kbytes sector erase, bank erase and dual-bank mass erase
Features	Read while write (RWW)	
Error code correction (ECC)	No	One error detection/correction or two error detections per 128-bit flash word using 9 ECC bits, on 16-bit words with 6 bits within configurable Flash high-cycle data area
Wait states	Up to 8 (depending on the supply voltage and frequency)	Up to 6 (depending on the supply voltage and frequency)
One time programmable (OTP) memory	512 bytes (OTP) for user data	2 Kbytes (OTP) area
FLASH security and protections	• Read protection (RDP) • Write protections • Proprietary code readout protection (PCROP)	• TrustZone® backed watermark and block security protection • HDP protection providing temporal isolation • Configuration protection • Write protection • Device nonvolatile security life cycle and application boot state management
User option bytes (1)	nRST_STDBY nRST_STOP WDG_SW BOR_LEV BFB2 OPTSTRT OPTLOCK DB1M nWRP RDP USER SPRMOD	NRST_STBY NRST_STOP IWDG_SW WWDG_SW IWDG_STBY, IWDG_STOP BOR_LEV BORH_EN BOOT_UBE OPTSTRT OPTLOCK WRPSG PRODUCT_STATE VDDIO_HSLV SWAP_BANK

1. *Refer to the "Option-byte organization" table in the Reference Manual that provides all user option bytes.*

5.2.2 SRAMs

In STM32F427/437 and STM32F429/439, the control of SRAM is integrated within the SYSCFG.

The RAMCFG controller, a new peripheral available on STM32H573/563 and STM32H562, is dedicated to control SRAM1, SRAM2, SRAM3, and BKPSRAM. Refer to section *RAMs configuration controller* section in the corresponding reference manual for more details.

Table 18. SRAM features

Features	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Size	• Up to 256 Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM • Main internal SRAM1 (112 KB) – Auxiliary internal SRAM2 (16 KB) – Auxiliary internal SRAM3 (64 KB) • 4 Kbytes of backup SRAM	Up to 644 Kbytes: 256-Kbyte SRAM1 64-Kbyte SRAM2 320-Kbyte SRAM3 4-Kbyte BKPSRAM
Access by DMA and CPU	• BKPSRAM (system bus) • Bytes, half-words (16 bits), or full words (32 bits) possible access	• Bytes, half-words (16 bits), or full words (32 bits) possible access
CPU access bus	• System bus or I-Code/D-ode buses • BKPSRAM (system bus)	• System bus or C-bus • BKPSRAM (only system bus)
Retention	BKPSRAM: Optional retention in Standby mode Optional retention in VBAT mode	
Security	NA	• When the TrustZone® security is enabled, all SRAMs are secure after reset • The SRAMs can be programmed as nonsecure, using the MPCBB with a block granularity of 512 bytes
Hardware and software erase conditions	The backup SRAM is not mass erased by a tamper event Backup SRAM is only erased when the RDP changes from level 1 to 0	SRAM1 and SRAM2 erase can be requested by executing a specific software sequence, detailed in section *RAMCFG* of the product reference manual SRAM2 and optionally backup SRAM are protected by the tamper detection circuit, and is erased by hardware in case of tamper detection SRAM2 is deleted in case of regression
System reset erase	NA	SRAM2 can be erased with a system reset using the option bit SRAM2_RST option bit in the Flash memory user option bytes SRAM1 and SRAM3 are erased when a system reset occurs if the SRAM13_RST option bit is selected in the Flash memory user option bytes
Error detection and correction	NA	• Single error detection and correction with interrupt generation • Double error detection with interrupt or NMI generation • The ECC is supported by SRAM2, SRAM3, and BKPSRAM when enabled with the SRAM2_ECC, SRAM3_ECC, and BKPRAM_ECC user option bits • ECC: 7 bits are added per 32 bits • Interrupts are generated when single- and/or double-ECC errors are detected: – Two ECC RAMCFG interrupts – One ECC NMI interrupt
Write protection	NA	SRAM2 can be write-protected with a page granularity of 1 Kbyte Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 63) bit in RAMCFG registers
Read access latency	NA	3-bit programmable wait-states depending on AHB clock frequency (HCLK) and voltage scaling range

5.2.3 System configuration controller

The table below illustrates the system configuration controller (SYSCFG) main differences between STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices.

Note: For STM32H5 series, the SYSCFG (system configuration controller) is integrated in the SBS (system configuration, boot, and security).

Table 19. System configuration features

STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
• Managing the I/O compensation cell • Select the Ethernet PHY interface	
• Remap the memory accessible in the code area • Manage the external interrupt line connection to the GPIOs	NA
NA	• Enabling/disabling the FMP high-drive mode of some I/Os and voltage booster for I/O analog switches • Configuring TrustZone® security register access • Tracking the PVT conditions to control the current slew-rate and output impedance in I/O buffer through compensations cells • Two compensation cells are embedded, one for the I/Os supplied by VDDIO power rail and one for the I/Os supplied by VDDIO2 power rail

5.2.4 Instruction and data caches (ICACHE/DCACHE)

The STM32H573/563 and STM32H562 embed an ICACHE (8 Kbytes) and a DCACHE (4 Kbytes) that allows more efficient use of the external memory through OCTOSPI and FMC ports.

The STM32F427/437 and STM32F429/439 devices do not embed these caches.

5.2.5 Direct memory access controller (DMA)

The STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 have different DMA architecture and features.

All devices embed two DMA controllers:

- DMA1 (8 channels) and DMA2 (8 channels) for STM32F427/437 and STM32F429/439
  Each channel is dedicated to manage the memory access requests from one or more peripherals. The devices embed also an arbiter for handling the priorities among the DMA requests
- GPDMA1 (8 channels) and GPDMA2 (8 channels) for STM32H573/563 and STM32H562
  Each GPDMA instance has the same channel-based implementation and is connected to the same requests and triggers

STM32F427/437 and STM32F429/439 embed also a Chrom-ART Accelerator (DMA2D) that is a specialized DMA dedicated to image manipulation. The following table illustrates the main differences between DMA requests in STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562.

Table 20. **DMA features**

Peripherals	STM32F427/437 and STM32F429/439		STM32H573/563 and STM32H562	
	DMA1	DMA2	GDMA1	GDMA2
Architecture	Each instance of DMA controllers can access memory and peripherals			
Number of instances	1	1	1	1
Number of masters	Dual AHB master bus	Dual AHB master bus	Dual bidirectional AHB master	
Number of channels	8	8	8	8
TrustZone® security	NA		Yes	
Privileged/unprivileged DMA				
Linked-List				

5.2.6 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between the STM32F427/437, STM32F429/439, STM32H573/563 and STM32H562 devices.

Table 21. **RCC features**

RCC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
HSI	16 MHz RC oscillator	64 MHz RC oscillator
CSI	NA	CSI: low-power RC oscillator that can be used directly as system clock, peripheral clock, or PLL input: low-cost clock source since no external crystal is required faster startup time than HSI (a few microseconds) very low-power consumption. The CSI provides a clock frequency of about 4 MHz.
HSI48	NA	48 MHz RC oscillator HSI48 can drive USB and RNG.
LSI	32 kHz RC Lower consumption, higher accuracy	
HSE	From 4 to 26 MHz	From 4 to 50 MHz
LSE	32.768 kHz	32.768 kHz Configurable drive/consumption
PLL	Three PLLs: • PLLI2S and PLLSAI generate an accurate clock • A main PLL (PLL) clocked by the HSE or HSI oscillator and featuring two different output clocks: – One output generates the high-speed system clock (up to 180 MHz) – One output for USB OTG FS, RNG, and SDIO	Three PLLs: • Main PLL (PLL1) provides clocks for CPU and some peripherals • PLL2 and PLL3 generate the kernel clock for peripherals Each PLL offers three outputs with postdividers. Input frequency range: • 2 to 16 MHz for the VCO in wide-range mode • 1 to 2 MHz for the VCO in low-range mode
AHB frequency	Up to 180 MHz	Up to 250 MHz
APB1 frequency	Up to 45 MHz	Up to 250 MHz
APB2 frequency	Up to 90 MHz	Up to 250 MHz

RCC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
RTC clock source	LSE, LSI, or HSE/ 32	
Kernel clock	NA	Independent kernel clock for each IP, allowing frequency scaling without impact on communication interfaces
System clock source	HSI, HSE, or PLL	HSI, CSI, HSE, or PLL1
Clock security system	CSS on HSE	CSS on HSE CSS on LSE
MCO clock source	• MCO1 pin (PA8): HSI, LSE, HSE, or PLL • MCO2 pin (PC9): HSE, PLL, SYSCLK, or PLLI2S	MCO1 pin (PA8): HSI,LSE,HSE, PLL1 or HSI48 MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1,CSI, or LSI

Peripheral clock configuration

The peripherals presented below have a dedicated clock source, that is used to generate the clock required for their operation. This section presents the difference between STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices, for peripherals with different clock sources.

Table 22. Peripherals with different clock sources

Peripherals	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
SAI	PLLI2S_Q PLLSAI_Q External clock mapped on the I2S_CKIN pin	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
U(S)ART	APB1 or APB2 clock (PCLK1 or PCLK2)	rcc_pclk1(1) rcc_pclk2(2) pll2_q_ck pll3_q_ck hsi_ker_ck csi_ker_ck lse_ck
I2Cs	APB1 clock (PCLK1)	rcc_pclk1(3) rcc_pclk3(4) pll3_r_ck hsi_ker_ck
SPI	APB clock (PCLK)	rcc_pclk2(5) rcc_pclk3(6) pll2_q_ck(7) pll3_q_ck(7) hsi_ker_ck(7) hse_ck(7) csi_ker_ck(7) pll1_q_ck(8) pll2_p_ck(8)

Peripherals	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
		pll3_p_ck(8) AUDIOCLK(8) per_ck(8)
I2S	PLLI2S External clock mapped on I2S_CKIN pin	pll1_q_ck pll2_p_ck pll3_p_ck AUDIOCLK per_ck
CAN	APB clock (PCLK)	hse_ck pll1_q_ck pll2_q_ck
ADC	APB2 clock (PCLK2)	rcc_hclk sys_ck pll2_r_ck hse_ck hsi_ker_ck csi_ker_ck
USB FS	PLL 48 MHz derived from main PLL VCO (PLLQ clock)	hsi48_ker_ck pll1_q_ck pll3_q_ck
RNG		hsi48_ker_ck pll1_q_ck lse_ck lsi_ker_ck
SDMMC	SDIO/SDMMC1: PLL48CLK	SDMMCx (x= 1,2): pll1_q_ck pll2_r_ck
IWDG	LSI	

1. *Only for UARTx (x=4,5,7,8,9,12) and USARTx (x=2,3,6,10,11).*
2. *Only for USART1.*
3. *Only for I2Cx (x=1,2).*
4. *Only for I2Cx (x=3,4).*
5. *Only for SPIx (x=4,6).*
6. *Only for SPI5.*
7. *Only for SPIx (x=4,5,6).*
8. *Only for SPIx (x=1,2,3).*

5.2.7 Power (PWR)

The table below presents the PWR controller differences between STM32F427/437, STM32F429/439 devices, and STM32H573/563 and STM32H562 devices. Both dynamic and static power-consumption were optimized for the STM32H573/563 and STM32H562 devices.

Table 23. **PWR features**

PWR	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Power supplies	**VDD = 1.7 to 3.6 V:** external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins	**VDD = 1.71 V to 3.6 V:** external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
	VSSA, VDDA = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs, and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.	VDDA = 1.62 V ADCs / 1.8 V (DAC), 2.1 V (VREFBUF) to 3.6 V external analog power supply for A/D converters, D/A converters, and voltage reference buffer. The VDDA voltage level is independent from the VDD voltage.
	V12: voltage source through VCAP_1 and VCAP_2 pins/ around **1.2 V**	**VCAP = 1.0 V to 1.35 V:** power supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory
	VBAT = 1.65 to 3.6 V: when VDD is not present, VBAT is power supply for RTC, external clock 32 kHz oscillator, and backup registers	**VBAT = 1.2 V to 3.6 V:** when VDD is not present, VBAT is the power supply for RTC, external clock 32 kHz oscillator, backup registers, and optionally backup SRAM
	NA	(1)(2) **VDDSMPS = 1.71 V to 3.6 V:** external power supply for the SMPS step-down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply as VDD pin. • VLXSMPS is the switched SMPS step-down converter output An external coil with typical value of 2.2 µH to be connected between the dedicated VLXSMPS pin to VSSSMPS, via a capacitor of 10 µF VSSSMPS is an isolated supply ground.
	NA	**VDDUSB = 3.0 V to 3.6 V**: external independent power supply for USB transceivers The VDDUSB voltage level is independent from the VDD voltage.
	NA	**VDDIO2 = 1.08 V to 3.6 V:** external power supply for 10 I/Os (PD6, PD7, PG9:14, PB8, PB9). This voltage is independent from the VDD voltage.
Battery backup domain	RTC with backup registers LSE Backup SRAM when the low-power backup regulator is enabled. PC13 to PC15 I/Os, plus PI8 I/O (when available)	RTC with backup registers (128 bytes) LSE PC13 to PC15 I/Os plus PI8 I/O (when available)
Power supply supervisor	POR, PDR, BOR, PVD	
	NA	AVD Backup domain voltage and temperature monitoring
Sleep mode wake-up sources	Any peripheral interrupt/wakeup event	
Standby mode, wake-up sources	WKUP pin PA0 on rising edge RTC event (RTC ALARM, Tamper event, Time stamp event) IWDG reset	WKUPx pin edge, RTC event, external reset in NRST pin, IWDG reset, BOR reset

PWR	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
	External reset in NRST pin	
Stop mode, wake-up sources	Any EXTI line (configured in the EXTI registers, internal and external lines)	Any EXTI line (configured in the EXTI registers) Specific peripherals events
Wakeup system clock	Stop: HSI RC oscillator	Stop: CSI when STOPWUCK = 1 in RCC_CFGR HSI with the frequency before entering the Stop mode, up to 64 MHz, when STOPWUCK Standby: HSI clock at 64 MHz
Low-power modes	Sleep mode	Sleep mode
	Stop mode	Stop mode: To further optimize the power consumption, the unused RAMs can be totally or partially Shut-off.
	Standby mode	Standby mode

1. *Supply for the SMPS power stage (available on SMPS packages)/The SMPS power supply pins are available only on a specific package with SMPS step-down converter option.*
2. *VDDSMPS, VLXSMPS only available for STM32H563/H573 devices.*

The STM32H573/563 and STM32H562 devices embed two regulators: one LDO or one SMPS to provide the VCORE supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory. These regulators can provide four different voltages (voltage scaling) and can operate in Stop modes. Depending on the package configuration (SMPS or LDO), the regulator is selected by hardware. SMPS and LDO regulator are exclusively selected.

The following figures present the power supply for the STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices. The differences are summarized in the previous table.

Figure 7. STM32H573/563 and STM32H562 power supply overview with (a) LDO (b) SMPS

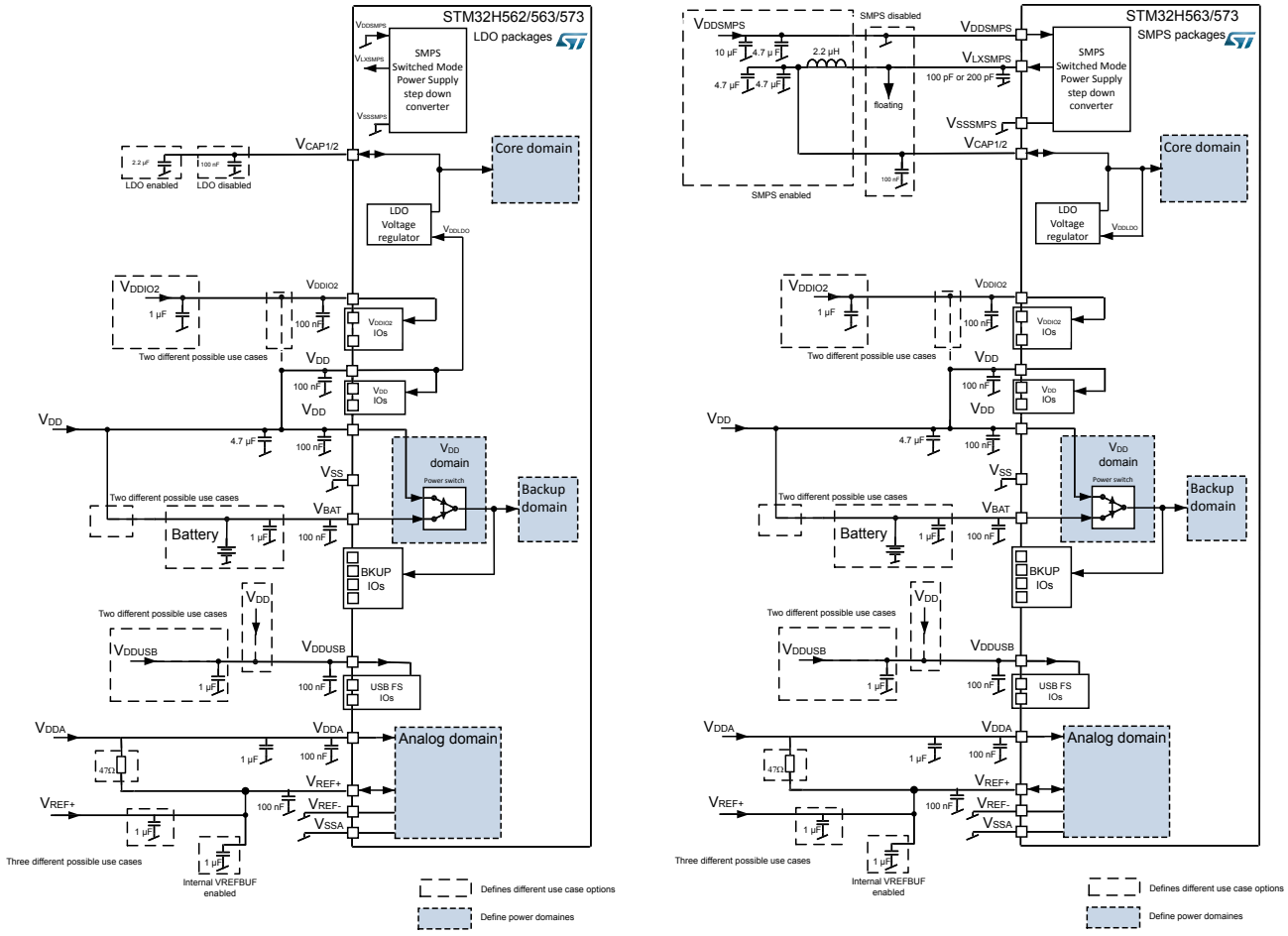
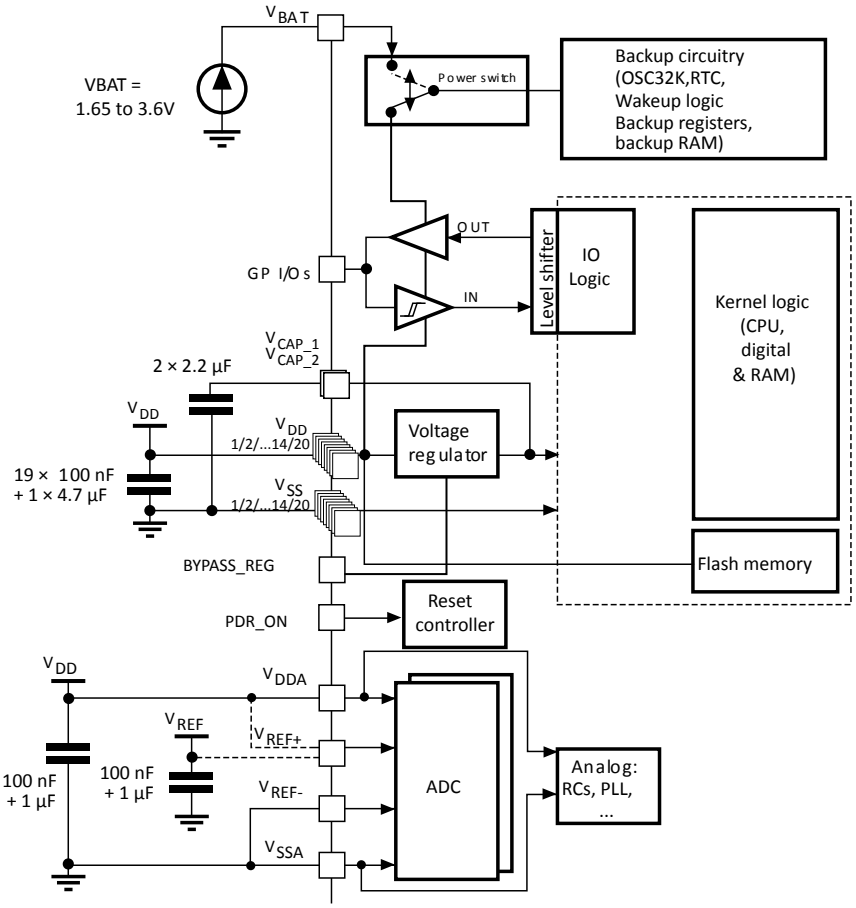


Figure 8. **Power supply overview for STM32F42xxx and STM32F43xxx**



5.2.8 General-purpose I/Os (GPIO)

STM32H573/563 and STM32H562 implement the same GPIO features than STM32F427/437, STM32F429/439, but with main differences.

For STM32H573/563 and STM32H562, each GPIO port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 16 bits reset register (GPIOx_BRR) and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR), two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL), a secure configuration register (GPIOx_SECCFGR) and a high-speed low-voltage register (GPIOx_HSLVR).

Each general-purpose I/O pin of GPIO port in STM32H573/563 and STM32H562 can be individually configured as secure through the GPIOx_SECCFGR register. After reset, all GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state secure or nonsecure.

- Additional TrustZone® security support.
  The TrustZone® security is activated by the TZEN option byte in the Flash Option Byte register. When the TrustZone® is active (TZEN = 0xB4), each I/O pin of GPIO port can be individually configured as secure through the GPIOx_SECCFGR register.
- I/Os state retention during Standby mode.
  In the Standby mode, the I/Os in STM32H573/563 and STM32H562 are by default in floating state. If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during standby entry. The state of I/Os is applied to the pin via pull-up and pull-down resistors. The pull-up and pull-down resistors remains applied after Standby wake-up until software clears the IORETEN bit in the PWR_IORETR register.

- High-speed low-voltage mode (HSLV)
  Some I/Os have the capability to increase their maximum speed at low voltage by configuring them in HSLV mode. The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

For more information about the STM32H573/563 and STM32H562 GPIO and TrustZone® security, refer to the *General-purpose I/Os (GPIO)* section of the reference manual and to the product datasheet for detailed description of the pinout and alternate function mapping.

5.2.9 Extended interrupt and event controller (EXTI)

5.2.9.1 EXTI main features in STM32H573/563 and STM32H562

The extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable event inputs. It provides wakeup requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The STM32H573/563 and STM32H562 feature TrustZone® security support and privileged/unprivileged mode selection and do not feature direct event inputs.

EXTI security protection

When security is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a secure access. A nonsecure write access is discarded and a read returns 0.

EXTI privilege protection

When privilege is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a privileged access. An unprivileged write access is discarded and a read returns 0.

The table below describes the difference of EXTI features between STM32F427/437, STM32F429/439 devices, and STM32H573/563 and STM32H562 devices.

Table 24. EXTI features

EXTI	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Features	Generation of up to 23 software event/interrupt requests	• 58 input events supported • TrustZone® support • Privileged/unprivileged mode

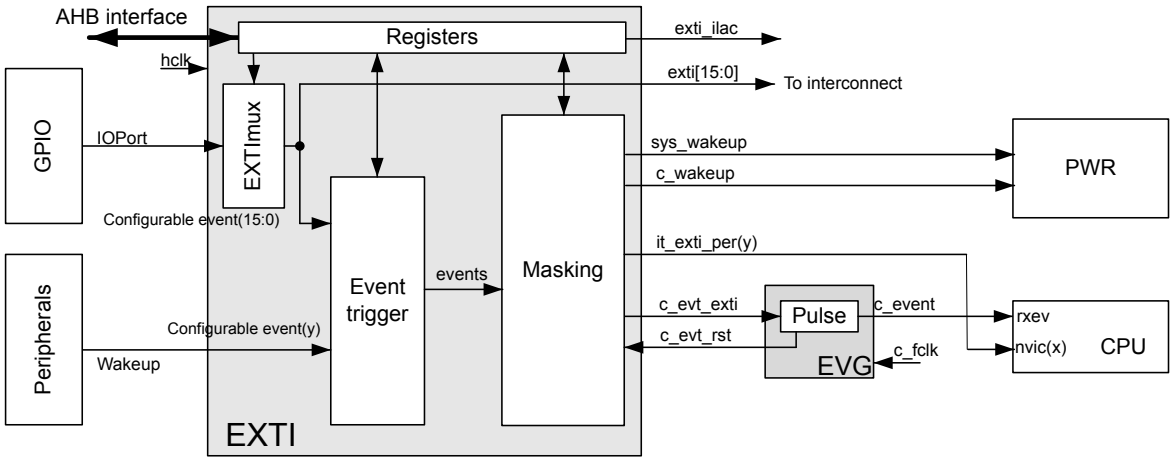
5.2.9.2 EXTI block diagram in STM32H573/563 and STM32H562

As shown in the figure below, the EXTI consists of

- a register block accessed via an AHB interface
- an event input trigger block
- a masking block, and EXTI mux as shown in the figure below.

The register block contains all the EXTI registers. The event input trigger block provides event input edge trigger logic.

Figure 9. **EXTI block diagram on STM32H573/563 and STM32H562**



The table below presents the EXTI line differences between STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices.

Table 25. **EXTI line differences**

EXTI line	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
0-15	16 external interrupt lines	GPIO
16	PVD output	PVD/AVD output
17	RTC alarm event	RTC nonsecure
18	USB OTG FS wakeup event	RTC secure
19	Ethernet wakeup event	TAMP nonsecure
20	USB OTG HS (configured in FS) wakeup event	TAMP secure
21	RTC tamper and TimeStamp events.	I2C1 wakeup
22	RTC wakeup event	I2C2 wakeup
23	NA	I2C3 wakeup
24		I3C wakeup
25		USART1 wakeup
26		USART2 wakeup
27		USART3 wakeup
28		UART4 wakeup
29		UART5 wakeup
30		USART6 wakeup
31		UART7 wakeup
32		UART8 wakeup
33		UART9 wakeup
34		USART10 wakeup
35		USART11 wakeup
36		UART12 wakeup
37		LPUART1 wakeup
38		LPTIM1

EXTI line	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
39	NA	LPTIM2
40		SPI1 wakeup
41		SPI2 wakeup
42		SPI3 wakeup
43		SPI4 wakeup
44		SPI5 wakeup
45		SPI6 wakeup
46	NA	ETH wakeup
47		USB FS wakeup
48		USBPD1 wakeup
49		LPTIM2 CH1
50		DTS wakeup
51		HDMI-CEC wakeup
52		I2C4 wakeup
53		UVM output
54		LPTIM3
55		LPTIM4
56		LPTIM5
57		LPTIM6

5.2.10 CRC calculation unit

The table below presents the CRC differences between the STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562 devices.

Table 26. CRC features

CRC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Features	• Uses CRC-32 (Ethernet) polynomial • Single input/output 32-bit data register • CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size • General-purpose 8-bit register (can be used for temporary storage)	
	Handles 32-bit data size	• Handles 8-,16-, 32-bit data size fully programmable polynomial with programmable size (7, 8, 16, 32 bits) • Programmable CRC initial value • Input buffer to avoid bus stall during calculation • Reversibility option on I/O data • Accessed through AHB slave peripheral by 32-bit words only, with the exception of CRC_DR register that can be accessed by words, right-aligned half-words and right-aligned bytes
CRC registers	CRC data register (CRC_DR) CRC independent data register (CRC_IDR) CRC control register (CRC_CR) CRC register map	
	-	CRC initial value (CRC_INIT) CRC polynomial (CRC_POL)

5.3 Security peripherals

5.3.1 Random number generator (RNG)

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The table below presents the RNG features of STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439.

Table 27. RNG features

RNG	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Features	• RNG delivers 32-bit random numbers • 40 periods of the RNG_CLK clock signal between two consecutive random numbers • RNG passed the FIPS PUB 140-2 tests with a success ratio of 99% • Monitoring of the RNG entropy to flag abnormal behavior	• RNG delivers 32-bit true random numbers • Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG) • Tested using German BSI statistical tests of AIS-31 (T0 to T8) • Embeds start-up and NIST SP800-90B approved continuous health tests • AHB slave peripheral, accessible through 32-bit word single accesses only • RNG internal tamper event signal to TAMP • Can be enabled with an automatic low-power mode (default configuration)
	Can be disabled to reduce power consumption	

In STM32H573/563 and STM32H562, the RNG is transparently used by SAES and PKA.

When an unexpected error is found by the RNG an internal tamper event is triggered in TAMP peripheral, and the RNG stops delivering random data. When this event occurs, secure application needs to reset the RNG peripheral either using the central reset management or the global SoC reset. Then a proper initialization of the RNG is required, again.

5.3.2 Hash processor (HASH)

The following table illustrates the differences between HASH features in STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562.

Table 28. **HASH features**

HASH	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Features	• Secure HASH algorithm (SHA-1, SHA-224, SHA-256) • MD5 (message-digest algorithm 5) hash algorithm • HMAC (keyed-hash message authentication code)	• Secure HASH algorithm (SHA-1, SHA-2 family) • HMAC (keyed-hash message authentication code) algorithm
	• FIPS PUB 180-2 • Secure HASH standard specifications (SHA-1, SHA-224 and SHA-256) • IETF RFC 1321 (internet engineering task force request for comments number 1321) specifications (MD5)	• FIPS PUB 180-4 • Secure HASH standard (SHA-1 and SHA-2 family) • FIPS PUB 186-4, digital signature standard (DSS) • Internet engineering task force (IETF) request for comments RFC 2104,
	Fast computation of SHA-1, SHA-224 and SHA-256, and MD5 (SHA-224 and SHA-256 are available on STM32F43xxx only)	Fast computation of SHA-1, SHA2-224, SHA2-256, SHA2-384, and SHA2-512
	8x 32-bit words (H0 to H7) on STM32F43xxx for output message digest	8x 32-bit words (H0 to H15) for output message digest
	32-bit data words for input data, supporting word, half-word, byte and bit bit-string representations, with little-endian data representation only	Single 32-bit, write-only, input register associated to an internal input FIFO, corresponding to a 64-byte block size (16 x 32 bits)
	Automatic data flow control supporting direct memory access (DMA)	• Automatic data flow control supporting direct memory access (DMA) • Support for both single and fixed DMA burst transfers of four words
	• AHB slave peripheral • Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message • Automatic padding to complete the input bit string	

5.3.3 On-the-fly decryption engine (OTFDEC)

The OTFDEC decrypts in real-time the encrypted content stored in the external OCTOSPI memories used in Memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

The STM32H573/563 and STM32H562 embed one OTFDEC peripheral. While in STM32F427/437 and STM32F429/439, this peripheral is not supported.

5.3.4 Public key accelerator (PKA)

The STM32H573/563 and STM32H562 devices embed one PKA peripheral intended for the computation of cryptographic public key primitives within the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The STM32F427/437 and STM32F429/439 devices do not support a PKA peripheral.

5.3.5 AES and SAES hardware accelerators

The STM32H573/563 and STM32H562 embed two AES accelerators: one secure AES (SAES) and a faster AES. The SAES is a new feature in STM32H573/563 and STM32H562. The AES is replacing the cryptographic processor (CRYP) that is available in STM32F427/429 and STM32F437/439 devices.

In STM32H573/563 and STM32H562, the SAES with hardware-unique key embeds protection against differential power analysis (DPA) and related side channel attacks.

When an unexpected hardware fault occurs, an output tamper event is triggered, and the AES automatically clears key registers. A reset is required for the AES to be usable again.

The AES peripheral can use the SAES peripheral as security coprocessor. In this case, the secure application performs two actions:

- prepares the key in the robust SAES peripheral
- when they key is ready, the AES can load this prepared key through a dedicated hardware key bus.

5.3.6 Global TrustZone controller (GTZC)

The security architecture of STM32H573/563 and STM32H562 is based on Arm® TrustZone® with the Armv8-M mainline extension.

Each GPIO or peripheral, DMA channel, clock configuration register, DCACHE/ICACHE, or small part of Flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in the STM32H573/563 and STM32H562 is used to configure secure TrustZone® and privileged attributes within the full system. All details about GTZC are described in the product reference manual.

This controller is a new feature of STM32H573/563 and STM32H562 and is not embedded in STM32F427/437 and STM32F429/439.

5.4 Communication peripherals

5.4.1 Serial peripheral interface (SPI)

This section highlights the SPI features(1) implemented on STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices.

Table 29. SPI features

SPI	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	6x SPIs	6x SPIs
Speed	Up to 45 Mbit/s	Max 50 Mbps
Features	SPI + I2S	
	2 with muxed full-duplex	Including 3 muxed with full-duplex I2S
Full-duplex synchronous transfer on three lines	X	X
Half-duplex	X	X
Simplex synchronous transfer on two lines	With or without a bidirectional data line	With unidirectional data line
Data size	8- or 16-bit transfer frame format selection	From 4-bit up to 32-bit data size selection or fixed to multiply of 8-bit
Multimaster mode capability	X	X
Baudrate prescalers	8 master mode baud rate prescalers (fPCLK/2 max.)	Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
Protection of configuration and settings	NA	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Configurable SS signal polarity and timing	NA	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable transaction data	NA	Programmable number of data within a transaction to control SS and CRC
Programmable data order with MSB-first or LSB-first shifting	X	X

SPI	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Programmable clock polarity and phase	X	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and TI formats support	X	X
Hardware CRC feature for reliable communication: • **CRC value can be transmitted as last byte in Tx mode** • **Automatic CRC error checking for last-received byte**	X	X
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit buffer-empty flag • Receive buffer not empty flag • Master mode fault event • Overrun error • CRC error flag • TI frame format error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP active • Transmission transfer filled • Overrun error • Underrun error • TI frame format error • CRC error • Mode fault • End of transfer • Master mode suspended • TxFIFO transmission complete All the interrupt events are capable to wakeup system from Sleep mode at each instance
Configurable behavior at slave-underrun condition	NA	X (support of cascaded circular buffers)
FIFOs	NA	• Two multiply of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance) • Configurable FIFO thresholds (data packing)
RDY status pin	NA	Optional status pin RDY signalizing the slave device ready to handle the data flow

1. *X = available, NA = not available.*

5.4.2 Inter-integrated circuit (I2C)

The STM32H573/563 and STM32H562 devices implement the same I2C features than the STM32F427/437 and STM32F429/439 devices but with some enhancements. The main differences are stated in the table below.

Table 30. I2C differences

I2C	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	x3 (I2C1, I2C2, I2C3)	x4(I2C1, I2C2, I2C3, and I2C4)
Features	• 7-bit and 10-bit addressing mode • SMBus/PMBus • Standard mode (up to 100 kbit/s) • Fast mode (up to 400 kbit/s)	
	Single clock source	• Fast-mode plus (up to 1 MHz) I2C bus • Wakeup from stop mode only (no autonomous mode) • Independent clock

5.4.3 Improved inter-integrated circuit (I3C)

The STM32H573/563 and STM32H562 devices implement a new feature compared to the STM32F427/437 and STM32F429/439 devices, which is the I3C peripherals.

5.4.4 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H573/563 and STM32H562 devices implement several new features on the U(S)ART compared to the STM32F427/437 and STM32F429/439 devices. The following table shows the U(S)ART differences.

Table 31. U(S)ART features

USART	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	• 4 USARTs • 4 UARTs	• 6 USARTs • 6 UARTs • LPUART
Baud rate	Up to 4x 11.25 Mbit/s	Depends on the frequency (oversampling by 16 or by 8)(1)
Clock	Single clock domain	Dual clock domain and Wakeup from low-power mode
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	23 interrupt sources with flags
Others features	Hardware flow control (CTS/RTS)	• RS232 hardware flow control • RS485 hardware control mode
	• LIN mode • IrDA SIR encoder block • Continuous communication using DMA • Multiprocessor communications • Single-wire half-duplex communication	
	NA	• Modbus communication: Timeout feature, CR/LF character recognition • Two internal FIFOs for transmit and receive data • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • Wakeup from Stop mode
	• Smartcard mode: has to be implemented by software • Number of stop bits: 0.5, 1, 1.5, 2	• Smartcard mode : Support the T=0 and T=1 asynchronous protocols • Number of stop bits: 0.5, 1, 1.5, 2

1. *Refer to the USART section in the reference manual.*

5.4.5 Serial audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations(1). Many stereo or mono audio applications may be targeted (such as I2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols).

Table 32. SAI features

SAI	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	SAI1	SAI1 and SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	Same features on all available instances	
Mute mode		
Stereo/mono audio frame capability		
16 slots with configurable size		
Data size configurable : 8-, 10-, 16-, 20-, 24-, 32-bit		
FIFO size	8 words	
SPDIF	-	X
PDM	-	Available only on SAI1

1. *'X' = supported, '-' = not supported.*

5.4.6 Digital camera interface (DCMI)

The DCMI is available on STM32F427/437, STM32F429/439, and STM32H573/563 and STM32H562 devices.

The DCMI main features are the following:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature

Data formats supported:

- 8-, 10-, 12-, and 14-bit progressive video (either monochrome or raw Bayer)
- YCbCr 4:2:2 progressive video
- RGB 565 progressive video
- Compressed data JPEG

5.4.7 Parallel synchronous slave interface (PSSI)

The PSSI is only available on STM32H573/563 and STM32H562 devices.

DCMI and PSSI use the same circuitry and then, when they are both implemented on a device, they cannot be used at the same time: when using the PSSI, DCMI registers cannot be accessed, and vice-versa. In addition, PSSI and DCMI share the same alternate functions and interrupt vector.

The PSSI peripheral main features are listed below:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte)
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output.

5.4.8 Controller area network (CAN)

The main differences related to CAN between STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562 are presented in the table below.

Table 33. **CAN features**

CAN	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	x2	x2 FDCAN (only 1x FDCAN on STM32H562)
Features	• Supports CAN protocol version 2.0 A, B Active • Bit rates up to 1 Mbit/s • Supports the time triggered communication option • Tx :3 transmit mailboxes, configurable transmit priority, time stamp on SOF transmission • Rx:2 receive FIFOs with three stages, scalable filter banks, identifier list feature, configurable FIFO overrun, time stamp on SOF reception • Time-triggered communication option: disable automatic retransmission mode,16-bit free running timer, time stamp sent in last two data bytes • Management: – Maskable interrupts – Software-efficient mailbox mapping at a unique address space • Dual CAN: • – CAN1: master bxCAN for managing the communication between a slave bxCAN and the 512-byte SRAM memory – CAN2: slave bxCAN, with no direct access to the SRAM memory	• Conform with CAN protocol version 2.0-part A, B and ISO 11898-1: 2015, -4 • CAN FD with maximum 64 data bytes supported • CAN error logging • AUTOSAR and J1939 support • Improved acceptance filtering • Two receive FIFOs of three payloads each (up to 64 bytes per payload) • Separate signaling on reception of high priority messages • Configurable transmit FIFO / queue of three payload (up to 64 bytes per payload) • Transmit event FIFO • Programmable loop-back test mode • Maskable module interrupts • Two clock domains: APB bus interface and CAN core kernel clock • Power down support

5.4.9 Universal serial-bus interface (USB)

The STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562 devices have different USB peripherals:

- The STM32F427/437 and STM32F429/439 devices implement an USB FS only instead of an USB OTG FS
- The STM32H573/563 and STM32H562 devices implement an USB FS and USB Type-C® connector/USB power delivery interface (UCPD)

Most features supported by the STM32F427/437 and STM32F429/439 devices are also supported by the STM32H5 Series. The main USB differences between the STM32F427/437 and STM32F429/439 and STM32H573/563 and STM32H562 devices are listed in the table below.

Table 34. USB differences

USB	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
General	Full support for the USB on-the-go (USB OTG FS)	USB FS with clock recovery
	FS mode: • One bidirectional control endpoint • Three IN endpoints (bulk, interrupt, isochronous) • Three OUT endpoints (bulk, interrupt, isochronous) **HS mode:** • 6 bidirectional endpoints (including EP0) • 12 host mode channels	Up to 8 bidirectional endpoints
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
	NA	Battery charging detection (BCD) support for device
		Independent VDDUSB power supply
Buffer memory	**FS mode:** • 1.25-Kbyte data FIFOs • Management of up to 4 Tx FIFOs (one for each IN end point) + one Rx FIFO **HS mode:** • 4 Kbytes of total RAM	2048 bytes of dedicated packet buffer memory SRAM
Low-power modes	**FS mode:** • USB suspend and resume **HS mode:** • No LPM supported	USB revision 2.0 including link power management (LPM) support

5.5 Analog peripherals

5.5.1 Analog-to-digital converter (ADC)

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 embed:

- Two ADCs: ADC1 and ADC2 for STM32H573/563 and STM32H562, both consist of a 12-bit successive approximation ADC that are tightly coupled and can operate in dual mode (ADC1 is master).
- Three ADCs: ADC1, ADC2 and ADC3 (12-bit resolution) for STM32F427/437 and STM32F429/439.

Table 35. ADC differences between devices

ADC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	x3	x2
Resolution	12-bit	
Number of channels	16 / 24	20 / 20
Configurable resolution	12-bit, 10-bit, 8-bit or 6-bit	
Maximum sampling speed	2.4 MSPS 7.2 MSPS in triple interleaved mode	5 MSPS
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual mode	
DMA support	Yes	
Data register	16-bit data register	
Analog watchdog feature	This feature allows the application to detect if the input voltage goes outside the user-defined high or low threshold	
ADC input range:	VREF– ≤ VIN ≤ VREF+	VSSA ≤ VIN ≤ VREF+
New features	NA	• ADC conversion time independent from the AHB bus clock frequency • Manage single-ended or differential inputs • Low-power features • Three analog watchdogs per ADC • Self-calibration • Oversampling ratio adjustable from 2 to 256 • Programmable data shift up to 8 bits

5.5.2 Digital-to-analog converter (DAC)

The STM32H573/563 and STM32H562 devices implement some enhanced DAC compared to the STM32F4 Series devices. Refer to the table below for the main DAC differences between them.

Table 36. DAC differences

DAC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Instances	x2 with one output channel each	x1 with maximum two output channels
Resolution	12 bits	
Output buffer	Yes	
Dual DAC channel	For independent or simultaneous conversions	
New features	NA	• Double-data DMA • Buffer offset calibration • Sample and hold mode for low-power operation in Stop mode

5.6 Timer peripherals

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices include two advanced-control timers, up to ten general-purpose timers, two basic timers, two watchdog timers and two SysTick timers (one for STM32F427/437 and STM32F429/439).

Furthermore, the STM32H573/563 and STM32H562 devices include six low-power timers.

This section compares the features of the above listed timers and RTC in STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices.

5.6.1 Advanced-control timers (TIM1/TIM8)

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 include two advanced-control timers, TIM1 and TIM8, with almost identical features detailed in the table below.

Table 37. Advanced-control timer (TIM1/8) features

Feature	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Counter resolution and type	16-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (Edge and Center-aligned mode) • One-pulse mode output	Up to six independent channels for: • Input capture (channels 5 and 6) • Output compare • PWM generation (Edge and Center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time	
Synchronization with external signals and general-purpose timers	• Synchronization circuit to control the timer with external signals and to interconnect several timers together • The advanced-control (TIM1/TIM8) and general-purpose (TIMy) timers are completely independent, and do not share any resources	
Repetition counter	Repetition counter to update the timer registers only after a given number of cycles of the counter	
Break inputs	One break input to put the timer’s output signals in reset state or in a known state	Two break inputs to put the timer’s output signals in reset state or in a known state
Interrupt/DMA generation	Interrupt/DMA generation on the following events:	
	• Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare	
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

5.6.2 GP timers with up, down, up-down auto-reload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler.

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices include GP timers with up, down or up/down auto-reload counter (TIM2, TIM3, TIM4 and TIM5), with identical features.

Table 38. **GP timer (TIM2/3/4/5) features**

Feature	STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562
32-bit resolution	TIM2 and TIM5
16-bit resolution	TIM3 and TIM4
Counter resolution and type	16-bit or 32-bit up, down, up/down auto-reload counter
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (Edge- and Center-aligned modes) • One-pulse mode output
Synchronization with external signals and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (*input capture*) • Generating output waveforms (*output compare and PWM*)

5.6.3 GP timers with auto-reload up-counter

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices include 16-bit resolution GP timers with a 16-bit auto-reload up-counter:

- TIM15/TIM16/TIM17 for STM32H573/563 and STM32H562 devices
- TIM9 to TIM14 for STM32F427/437 and STM32F429/439 devices

Table 39. GP timer (with auto-reload up-counter) features

Feature	STM32F427/437 and STM32F429/439		STM32H573/563 and STM32H562	
16-bit resolution	TIM10/TIM11 and TIM13/TIM14	TIM9/TIM12	TIM15	TIM16/TIM17
Counter resolution and type	16-bit auto-reload up-counter			
Prescaler factor	16-bit programmable prescaler used to divide the counter clock frequency by any factor between 1 and 65535			
Channels	Independent channel for:	Up to two independent channels for:		One channel for:
	• Input capture • Output compare • PWM generation (Edge-aligned mode) • One-pulse mode output			
Complementary outputs	NA		Complementary outputs with programmable dead-time (for channel 1 only)	Complementary outputs with programmable dead-time
Break input	NA		Break input to put the timer's output signals in the reset state or a known state	
Synchronization with external circuits and other timers	NA	Synchronization circuit to control the timer with external signals and to interconnect several timers together		NA
Repetition counter	NA		Repetition counter to update the timer registers only after a given number of cycles of the counter	
Interrupt generation	Interrupt generation on the following events:		Interrupt/DMA generation on the following events:	
	• Update: counter overflow, counter initialization (by software) • Input capture • Output compare	• Update: counter overflow, counter initialization (by software or internal trigger) • Trigger event (counter start, stop, initialization or count by internal trigger) • Input capture • Output compare	• Update: counter overflow, counter initialization (by software or internal/ external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	• Update: counter overflow • Input capture • Output compare • Break input
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM).			

5.6.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist in a 16-bit auto-reload counter driven by a programmable prescaler.

These timers are completely independent, and do not share any resources.

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices have the same basic timers features.

Table 40. **Basic timers**

Feature	STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562
Counter resolution and type	16-bit auto-reload up-counter
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535
Synchronization signals	Synchronization circuit to trigger the DAC
Interrupt/DMA generation	Interrupt/DMA generation on the update event: counter overflow

5.6.5 Low-power timers (LPTIM1/2/3/4)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. This is a new feature in STM32H573/563 and STM32H562, that is not available in STM32F427/437 and STM32F429/439. The next table describes LPTIM features on STM32H573/563 and STM32H562 devices.

Table 41. **LPTIM features**

Feature	STM32H573/563 and STM32H562
LPTIMx	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5 and LPTIM6
Counter resolution and type	16 bit up-counter
Prescaler factor	3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
Selectable clock	• Internal clock sources: configurable internal clock source (see RCC section) • External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)
Auto-reload	16 bit ARR auto reload register
Capture/compare	16 bit capture/compare register
Continuous mode	Continuous/one-shot mode
Trigger mode	Selectable software/hardware input trigger
Glitch filter	Programmable digital glitch filter
Configurable output	Configurable output: pulse, PWM
Polarity	Configurable I/O polarity
Encoder mode	Yes
Repetition counter	Yes
Input capture, PWM and one-pulse channels	Up to two independent channels for: • Input capture • PWM generation (Edge-aligned mode) • One-pulse mode output
DMA requests	DMA request generation on the following events: • Update event • Input capture

5.6.6 Watchdogs (WWDG/IWDG)

The STM32H573/563 and STM32H562, STM32F427/437 and STM32F429/439 devices embed two watchdogs:

- A system window watchdog (WWDG) with same features
- An independent watchdog (IWDG) with same differences

Table 42. IDWG features

Feature	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Clock	Clocked from an independent RC oscillator	• Independent clock • LSI used as IWDG kernel clock (iwdg_ker_ck)
Window option(1)	-	X
Early wakeup interrupt generation (1)	-	X
Reset generation(1)	X	
New features(1)	-	

1. *"X" = supported, "-" = not supported.*

5.6.7 Real-time clock (RTC)

The following table describes the difference of RTC features between STM32F427/437, STM32F429/439 devices and STM32H573/563 and STM32H562 devices. For more information about RTC, refer to the RTC section of the product reference manual.

Table 43. RTC features

RTC	STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
Feature	Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year	
	Two programmable alarms	
	Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision	
	Timestamp function	
	Daylight saving time	
	Automatic wakeup	
	Digital calibration circuit with 0.95 ppm resolution	
	Alarm A, Alarm B, wakeup interrupt, timestamp, tamper detection	Alarm A, alarm B, wakeup Timer and timestamp individual privilege protection
	NA	• Binary mode with 32-bit free-running counter • On-the-fly correction from 1 to 32767 RTC clock pulses • RTC TrustZone® support
Tamper and backup registers	• 20x 32-bit backup registers • 2x tamper pins/ 2 events • Edge or level detection with configurable filtering	• 32x 32-bit backup registers • Up to 11 tamper pins for 8 external tamper detection events • 13 internal tamper events • TrustZone® support

5.6.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems but can also be used as a standard down-counter.

The STM32H573/563 and STM32H562 Cortex®-M33 with TrustZone® embeds two SysTick timers. When TrustZone® is activated, the two SysTick timers are available, but when TrustZone® is disabled, only one SysTick timer is available.

STM32F427/437 and STM32F429/439 embed a Cortex®-M4 with just one SysTick timer.

5.7 External memory interface peripherals

5.7.1 Flexible memory controller (FMC)

The following table presents the FSMC interface differences between the STM32F427/437, STM32F429/439 and STM32H573/563 and STM32H562 devices.

Table 44. FMC features

FSMC		STM32F427/437 and STM32F429/439	STM32H573/563 and STM32H562
External memory interfaces		• SRAM • NOR Flash memory/one NAND Flash memory • PSRAM • 16-bit PC card compatible devices • Two banks of NAND Flash memory with ECC hardware to check up to 8 Kbytes of data	• SRAM • NOR Flash memory/one NAND Flash memory • PSRAM • Ferroelectric RAM (FRAM) • NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
Data bus width		8,16 or 32-bit	8 or 16-bit
FMC Bank memory mapping	**Bank 1 4x 64-Mbyte**	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank 2 4x 64-Mbyte	NAND Flash memory	Not used
	Bank 3 4x 64-Mbyte		NAND Flash memory
	Bank 4 4x 64-Mbyte	PC Ccrd	Not used
	SDRAM Bank 1 4x 64-Mbyte	SDRAM	SDRAM
	SDRAM Bank 2 4x 64 Mbyte		

For STM32H573/563 and STM32H562, FSMC registers can be configured as secure through the TZSC controller (refer to the reference manual for more details).

5.7.2 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as Flash memory, PSRAM, HyperRAM™, HyperFlash.

The Octo-SPI specialized communication interface targets single-, dual-, quad- or octal-SPI memories, and can be configured in three modes: Indirect, Status-polling and Memory-mapped.

The OCTOSPI peripheral is available on STM32H573/563 and STM32H562, with the following features:

- Functional modes: Indirect, Automatic status-polling, and Memory-mapped
- Read and write support in Memory-mapped mode
- Dual-quad configuration
- SDR (single-data rate) and DTR (double-transfer rate)
- Data strobe (DS, DQS)
- GPDMA interface

Note: OCTOSPI is not supported by STM32F427/437 and STM32F429/439.

Revision history

Table 45. **Document revision history**

Date	Version	Changes
08-Apr-2023	1	Initial release.

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