AN4982

Assembly guidelines for molded array process ball grid array package

Rev. 4 — 8 December 2020 Application note

1 Introduction

This application note provides guidelines for the handling and assembly of NXP Molded Array Process Ball Grid Array (MAPBGA), including Flip Chip Chip Scale Packages (FCCSP) during printed circuit board (PCB) assembly. PCB design and rework, package performance information such as moisture sensitivity level (MSL) rating, board level reliability, mechanical and thermal resistance data are included for reference.

2 Scope

This document contains generic information that encompasses various NXP MAPBGA packages assembled internally or at external subcontractors. Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.nxp.com or contact the appropriate product application team.

3 MAPBGA package

3.1 Package description

The MAPBGA package is a surface mount package that uses a grid of solder balls for electrical connections. The individual units are arranged in a matrix array on a substrate strip which are molded together, and then singulated by sawing. Singulated units are distinguished by mold compound completely covering the substrate.

Figure 1, Figure 2, and Figure 3 show example MAPBGA offerings from NXP. Figure 1 shows a typical NXP MAPBGA offering. Figure 2 is an example of a fully populated ball grid array (BGA) matrix and Figure 3 is an example of a depopulated BGA matrix. Different sizes and configurations of MAPBGA packages are available. Contact your NXP representative for specific size and BGA matrix configuration requirements.

Figure 1. Typical NXP MAPBGA

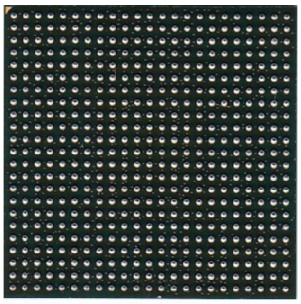

Figure 2. Fully populated BGA matrix

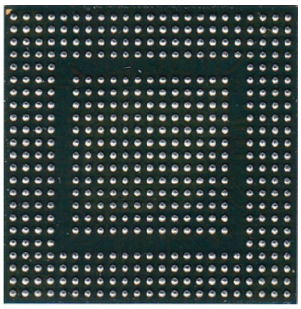

Figure 3. Depopulated BGA matrix

3.2 Package dimension

NXP offers industry standard MAPBGA sizes and thicknesses with various options of I/O (solder balls) quantity and pitch. Package sizes range from 3 mm x 3 mm to 27 mm x 27 mm with ball pitch ranging from 0.4 mm to 1.27 mm pitch. To obtain detailed dimensions and tolerances, refer to NXP package case outline drawings. Package size and ball pitch are continually in review, check with the NXP sales team for more information.

3.3 Package cross-section

The cross-section drawing in Figure 4 shows the representative internal layers of a typical MAPBGA package with a 2-layer substrate and wirebond interconnects. Figure 5 and Figure 6 shows the representative internal layers of a typical FCCSP overmolded with capillary underfill and overmolded underfill respectively with C4 bumps. The 2-layer substrate (typical) refers to the two conductive metal layers used to redistribute the I/O within the substrate. The standard configuration for a MAPBGA / FCCSP typically uses 2-layer substrates. High performance products may use 4-layer substrates.

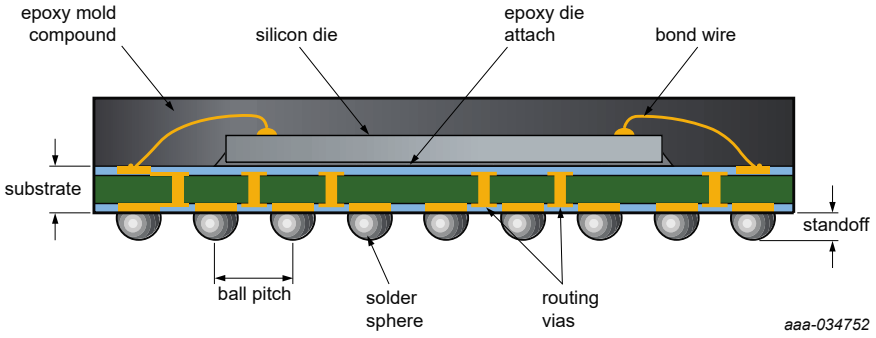

Figure 4. MAPBGA cross-section with 2-layer substrate configuration

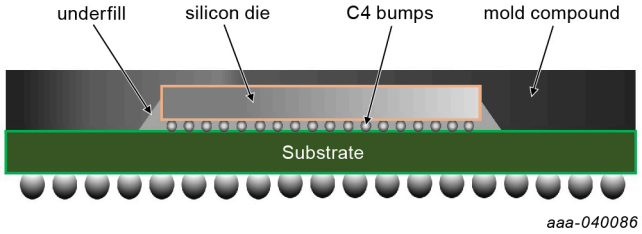

Figure 5. FCCSP overmolded with capillary underfill with HDI substrate

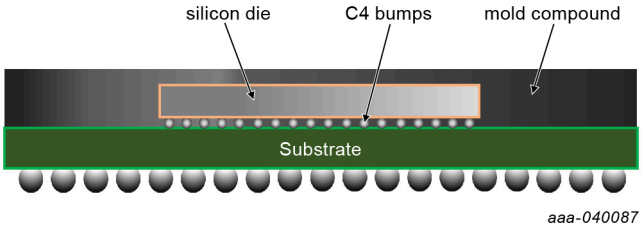

Figure 6. FCCSP overmolded underfill (MUF) with HDI substrate

4 Printed circuit board guidelines

4.1 PCB design guidelines

Proper PCB footprint and stencil designs are critical to ensure high surface mount assembly yields, and electrical and mechanical performance. The design starts with obtaining the correct package drawing. Package case outline drawings are available at www.nxp.com.

Follow the procedures in Section 9.1 "Downloading the information from NXP". Figure 7 shows an example of a 17 mm x 17 mm 364 MAPBGA case outline drawing. The goal is a well soldered MAPBGA as shown in Figure 8.

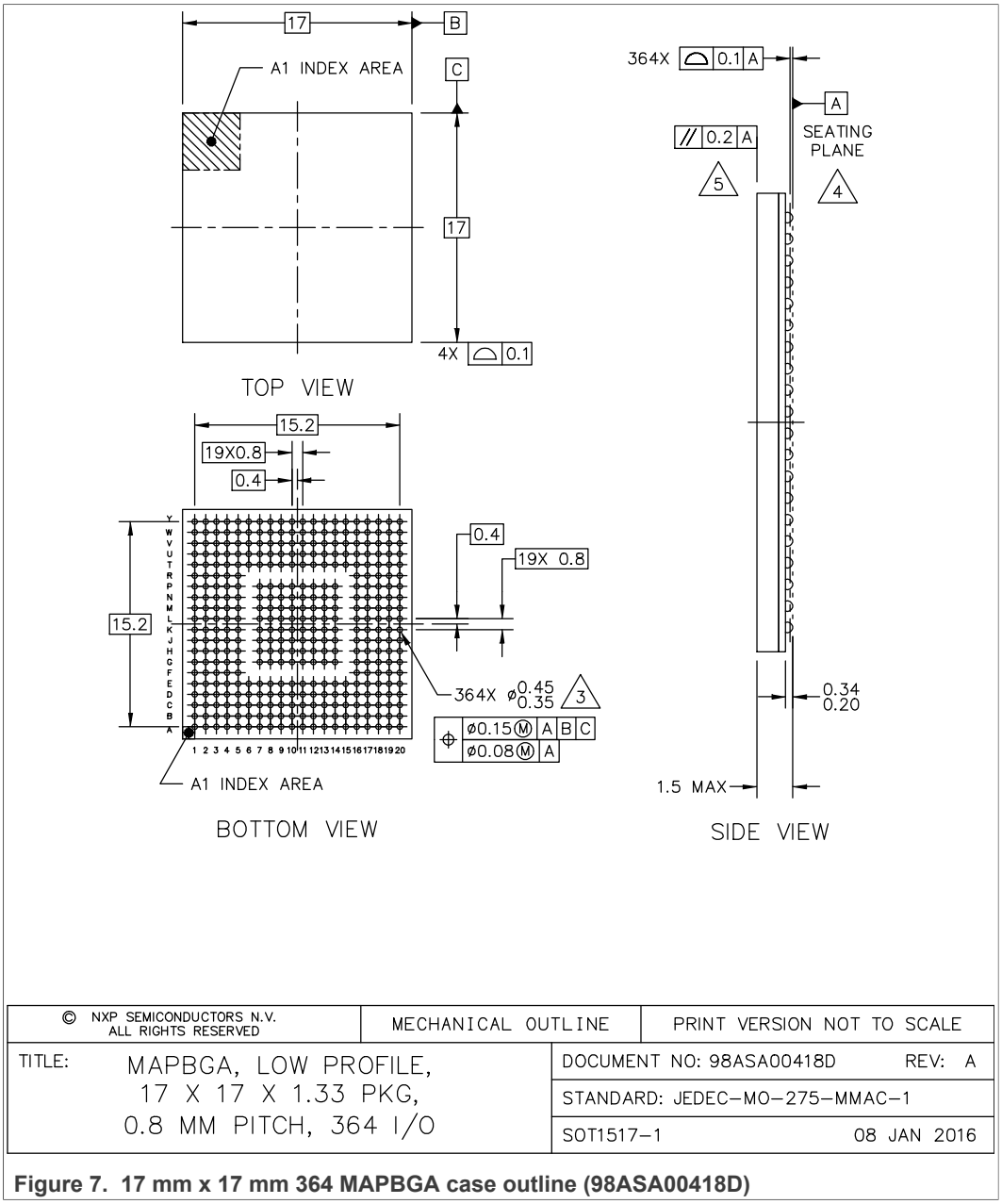

Figure 7. 17 mm x 17 mm 364 MAPBGA case outline (98ASA00418D)

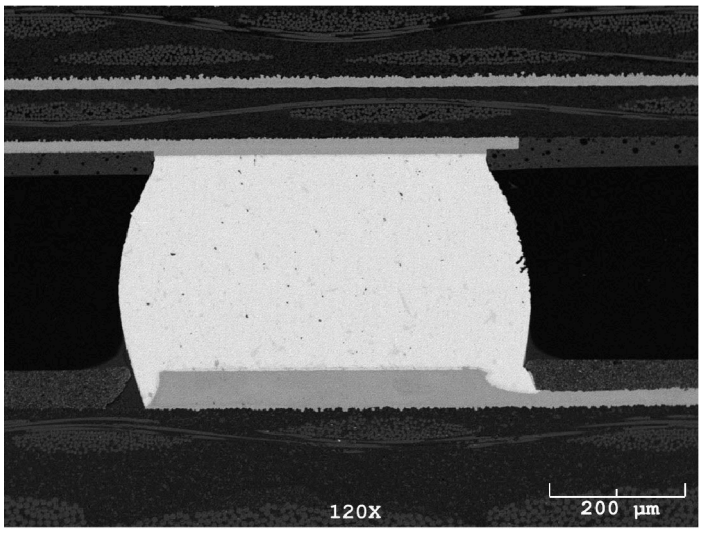

Figure 8. Scanning electron microscope (SEM) image of a well soldered 292 MAPBGA solder-joint (package top / PCB bottom)

4.2 PCB pad design

NXP follows the Institute for Printed Circuits (IPC) document, IPC-7351B[(12)], *Generic Requirements for Surface Mount Design and Land Pattern Standards*. This document and an accompanying land pattern calculator can be purchased from the IPC website and includes guidelines for BGAs based on assumed package dimensions.

Many MAPBGA products do not have fully populated arrays to allow for better PCB routing. PCB design must ensure that the final footprint matches the part.

4.2.1 Pad diameter

For pitches at or above 0.80 mm, the first estimate for PCB solderable diameter is one half the pitch. For pitches at or below 0.65 mm, the solderable diameter is generally larger than one-half pitch in diameter (See Table 1).

Table 1. Suggested PCB pad diameters by BGA pitch

BGA Pitch[1] (mm)	Suggested PCB Pad Diameter (mm)
1.00	0.500
0.80	0.400
0.65	0.325
0.50	0.300
0.40	0.225

[1] Some legacy products may have alternate pitches.

4.2.2 Pad surface finishes

Almost all PCB finishes are compatible with MAPBGAs including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn and Immersion Ag. NXP suggests monitoring the PCB surface

finish shelf life to ensure that the life has not “expired”. Surfaces should always be free of dirt and grease before PCB assembly.

4.2.3 Solder mask layer

NXP encourages customers to use Non-Solder Mask Defined (NSMD) PCB pad designs which typically provide better thermal fatigue life. Some field use conditions may require the use of Solder Mask Defined (SMD) pads for better drop/shock survivability. The difference between NSMD and SMD is shown in Figure 9.

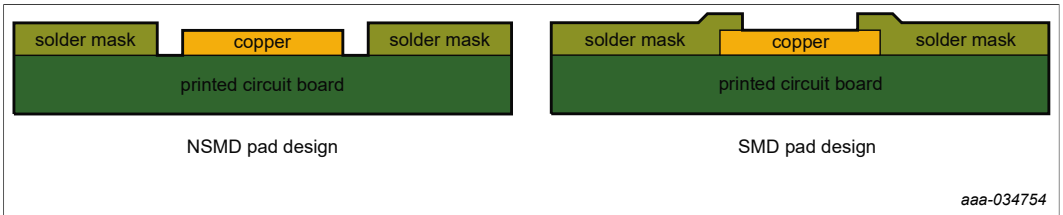

Figure 9. NSMD and SMD pad designs

The NSMD solder mask opening diameter is suggested to be 0.125 mm larger than the solderable area (i.e. Cu diameter). However, it is critical to understand the PCB fabrication capabilities of PCB suppliers. Also, finer BGA pitches may require < 0.125 mm in order to meet PCB routing requirements.

SMD pads (compared to NSMD) have a larger Cu diameter which means more Cu is joined to the PCB laminate. Copper diameter for SMD is 0.125 mm larger than solder mask opening diameter. This increased diameter makes pad cratering on the PCB more difficult, and therefore increases drop/shock life. For SMD at smaller pitches, a key factor of picking the Cu diameter and solder mask diameter is PCB vendor capabilities. Inspection of delivered PCBs for solder mask registration is encouraged.

5 Board assembly

5.1 Assembly process flow

A typical Surface Mount Technology (SMT) process flow is shown in Figure 10.

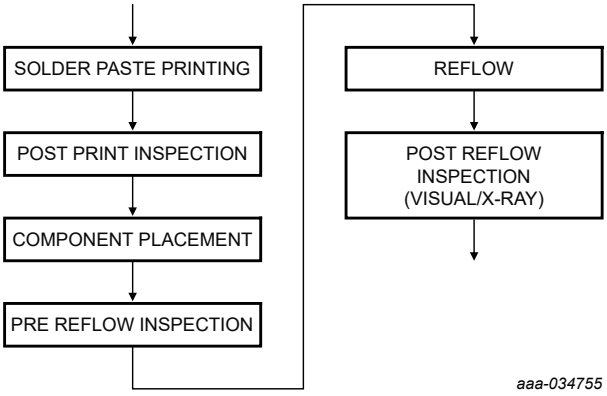

Figure 10. SMT process flow

5.2 Solder stencil / solder paste

5.2.1 Stencil thickness

Solder paste stencil design is critical for good solder joint formation, especially as the BGA pitch decreases. The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern.

For 1.0 mm pitch parts, a common stencil thickness is 0.125 mm (5 mils), while 0.100 mm thick stencils (4 mils) are also used. In high reliability applications, 0.150 mm (6 mils) thick stencils are preferred. For 0.80 mm pitch, the 0.100 mm thick stencil is common.

For these stencils, well cut openings created with a laser or by chemical etch is preferred. The opening walls should be polished and a nickel (Ni) finish is recommended. The goal is to have a stencil that properly releases a consistent volume of solder paste, print after print.

The stencils for BGA pitches at or below 0.65 mm have to consider other factors as well. Usually on a PCB, there may be other small size and small pitch components that prevent reduction of the stencil opening size. Instead, the total stencil thickness is decreased. Typically, stencils are from 0.075 mm to 0.125 mm thick.

At smaller pitches, it may help to use square openings in place of round as shown in Figure 11. Square openings allow a slightly larger volume of solder paste to be released. Generally, the opening length or diameter is 1:1 with the solderable PCB diameter. For additional solder paste volume, the opening length/diameter could be increased.

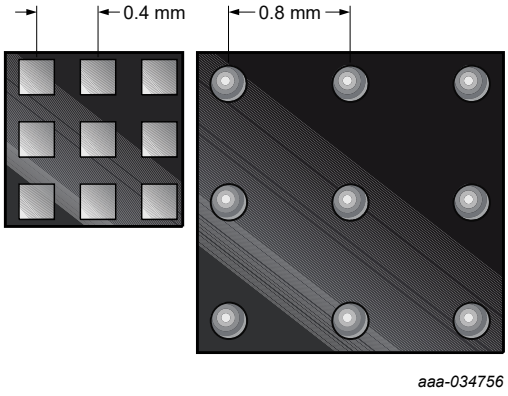

Figure 11. Square 0.4 mm and round 0.8 mm pitch stencil openings

Small pitch stencils frequently have specialized coatings to help with paste release. These coatings, frequently called nano-coatings, wear out. A monitoring program for stencil age (number of prints) may be needed.

5.2.2 Solder paste properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

There are two different flux systems commonly available:

- The first type of flux system requires cleaning such as standard rosin chemistries and water-soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions, or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
- The second type of flux system type requires no cleaning, but normally a little residue remains on the PCB after soldering.

Solder paste grain size can be useful to manipulate by pitch. For larger pitch parts, 0.80 mm and larger, Type 3 solder powder (25 micron to 45 micron grain size) is widely used. At the pitches, 0.65 mm and smaller, Type 4 solder (20 micron to 38 micron grain size) may provide a better solder joint.

5.3 Component Placement

The high lead interconnection and insertion density require precise and accurate placement tools. To meet this requirement, equip the placement machine with optical recognition systems, i.e., vision system, for centering the PCB and components during the pick and place motion. A placement accuracy study is recommended in order to calculate compensations required. NXP follows the EIA-481D[(5)] standard for tape and reel orientation as shown in Figure 12. See Section 10.3 "Packing of devices" for additional details.

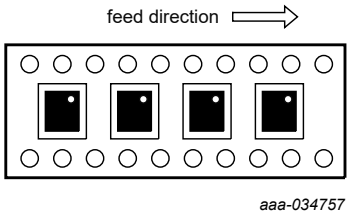

Figure 12. MAPBGA orientation in tape and reel

5.4 Soldering

A typical profile band is shown in Figure 13. The actual profile parameters depend on the solder paste used. The recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB reach reflow temperatures as well.

Dry air is a common reflow furnace atmosphere. Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balling). NXP recommends monitoring the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.

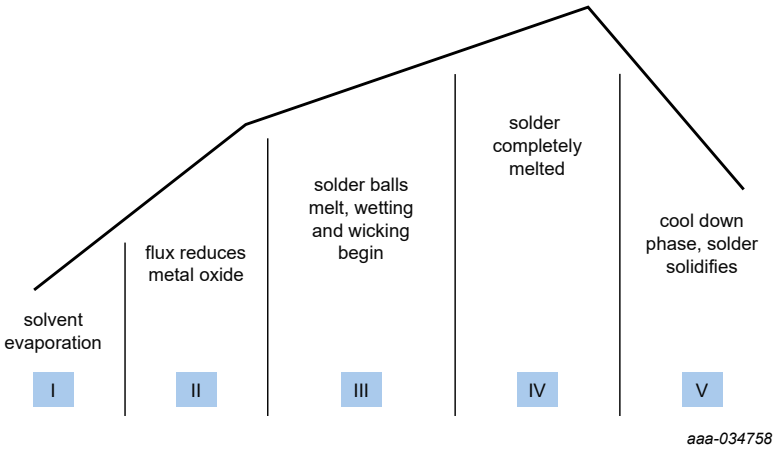

Figure 13. General solder reflow phases

For all devices on the PCB, take the solder paste into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a “safety” margin to ensure that all solder paste on the PCB reflows.

Deviation from the reflow profile recommended by the paste manufacturer should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as “x” and “y” lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or “x” and “y”. The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up. PCB should be rated for multiple reflow of MSL classification. Reference the device data sheet for any device specific board assembly guidelines.

At NXP.com, NXP provides application note AN3300[(1)] that contains general information on reflow profiles and is a useful starting point.

5.5 Inspection

The solder joints of MAPBGA parts are formed *underneath the package.* To verify any open or short circuits (bridging) after reflow, non-destructive vision/optical inspection and x-ray inspection are recommended after reflow soldering. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing).

Figure 14 shows the expected x-ray image of a soldered component.

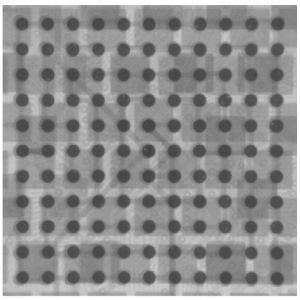

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Figure 14. Inspection x-ray of a MAPBGA package

5.6 Common MAPBGA solder-joint defects

Two common MAPBGA solder-joint defects are the head in pillow and solder bridge. Figure 15 shows a head in pillow defect. This defect occurs when the solder paste and solder ball melt, but fail to join. Figure 16 shows a solder bridge defect. The solder bridge defect occurs when the solder paste and solder ball merge during reflow from poor paste printing.

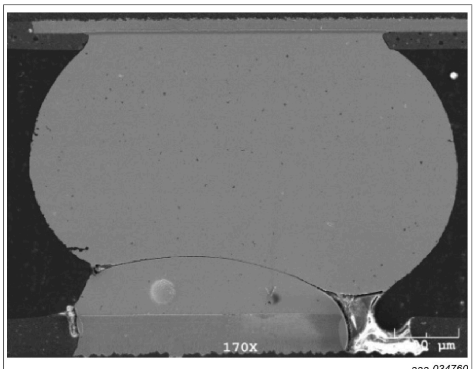

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Figure 15. Head in pillow

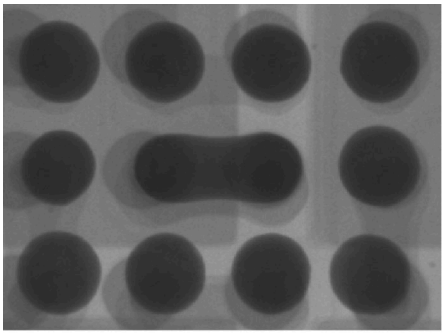

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Figure 16. Solder bridge

6 Repair and Rework Procedure

6.1 Repairing

Repairing a single solder joint of MAPBGA is not recommended because the joint is *underneath the package*.

6.2 Reworking

If a defective component is observed after board assembly, remove the device and replace it with a new one. This rework can be performed using the heating methods described in this section.

When performing the rework:

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent package.

- Heating conditions must be applied to correspond to the actual product and the mounted components. Heating conditions differ because of heat capacity differences of the PCB (board thickness, number of layers) and the mounted components used.
- NXP follows industry standard component level qualification requirements which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass. Removed packages should be properly disposed of so they are not mixed in with new components.

A typical package rework flow process is:

1. Section 6.2.1 "Tooling preparation"
2. Section 6.2.2 "Package removal"
3. Section 6.2.3 "Site redressing"
4. Section 6.2.4 "Solder paste printing"
5. Section 6.2.5 "Package remount"
6. Section 6.2.6 "Reflow soldering"

Note: *NXP product quality guaranty/warranty does not apply to products that have been removed. Component reuse should be avoided.*

In any rework, the PCB is heated. The thermal limits of PCB and components (e.g. MSL information) have to be followed. During heating, package cracking and/or delamination of critical interfaces within the components and PCB may result from the combination of rapid moisture expansion, materials mismatch, and material interface degradation. In order to prevent moisture induced failures, NXP recommends strict storage control for the PCBs and components in a controlled environment such as dry air or Nitrogen. When the maximum storage time out of dry pack (see packing material label) is exceeded after board assembly, a prebake is recommended to remove the moisture from the PCB and components prior to removal of the package. For example, with boards containing SMT components, prebake at 125 °C for 24 hours or with boards containing temperature sensitive components, prebake at 95 °C for 24 hours.

Individual process steps for reworking a package are found in Section 6.2.1 "Tooling preparation" through Section 6.2.6 "Reflow soldering".

6.2.1 Tooling preparation

Various rework systems are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing MAPBGA packages, a system should meet the following requirements:

- **Heating** – Controlled hot air transfer (temperature and air flow) to both the MAPBGA package and its mounted PCB is recommended. The heating must be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side. Nitrogen can be used instead of air. Additional information can be found in Section 6.2.2 "Package removal".
- **Vision System** – The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.

- **Moving and Additional Tools** – Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Package removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB. Any defects introduced during removal of the component from the PCB may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture Removal**: Dry bake components before removal at 125 °C for 16 – 24 hours for boards with SMT components. Dry bake boards with temperature sensitive components at 95 °C for 16 – 24 hours.
- **Temperature Profile**: During de-soldering, ensure that the package peak temperature is not higher and temperature ramps are not steeper than the standard assembly reflow process.
- **Mechanics**: Do not apply high mechanical forces for removal. High force can damage the component and/or the PCB which may limit failure analysis of the package. For large packages, vacuum wands can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. To properly remove the component using a vacuum pick-up tool, use an air nozzle of correct size to conduct heat to the MAPBGA package. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

With large PCBs, it is important to avoid bending the printed circuit material due to thermal stress. Place a bending prevention tool on the bottom of the printed circuit board, and install a bottom heater to heat the entire printed circuit board in order to raise work efficiency.

6.2.3 Site redressing

After the component is removed, the PCB pads must be cleaned to remove solder residue and prepare for the new component placement. After applying flux, clean by vacuum de-soldering, solder sucker, or solder wick braid, etc. Solder residue and projections prevent the solder stencil from adhering to the PCB during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean flux residue from the PCB. A de-soldering station can be used for solder dressing. Note that the applied temperature should not exceed 245 °C, which can contribute to PCB

pad peeling from the PCB. Site redressing is typically a manual operation requiring experience and skill.

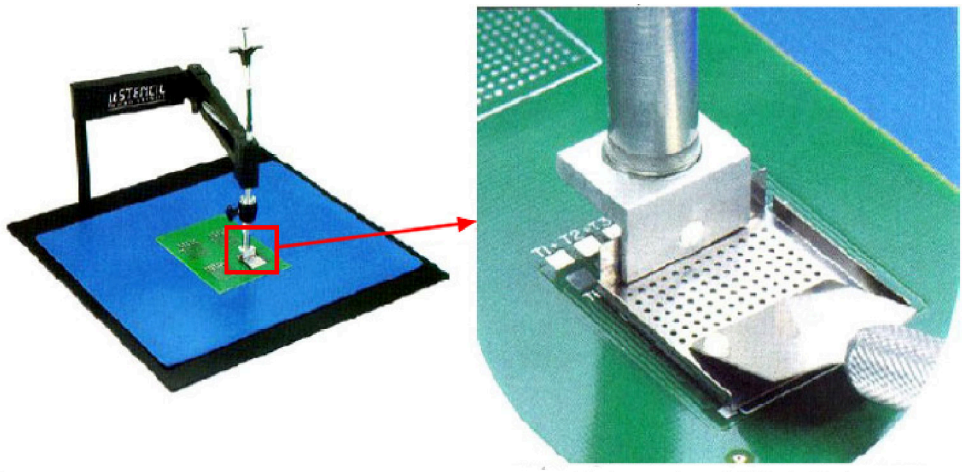
Non-abrasive or soft bristle brushes should be used. Abrasive brushes contribute to bad solder joints (e.g. steel brushes). Before placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini-stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini-metal squeegee blade deposits solder paste in the specific area. See Figure 17. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are near MAPBGA components and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

Depending on customer reliability standards, a flux only application to either the replacement part or to the reworked PCB may be sufficient for joining a MAPBGA part to the board. Flux choice is critical and should be of the same standards as for the original PCB assembly.



(photos courtesy of OK industries)

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Figure 17. Mini-stencil and mini-squeegee

6.2.5 Package remount

After preparing the site, the new package can be placed onto the PCB. Handling of the replacement package should follow the guidelines of Section 9.2 "Moisture sensitivity level". When remounting the package, NXP recommends using rework equipment that has good optical or video vision capability. A split light system displays images of both package balls and PCB pads by superimposing the two images. Alignment of the balls and pads is completed by adjusting the XY table.

Regular ball array MAPBGA exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Perfect placement is not required. At

least 50 % on solder ball on PCB pad for all pads is the minimum goal for part placement accuracy.

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in Section 5.4 "Soldering". Reflow furnaces are not typically used for rework. Instead, a dedicated rework station performs both part removal and new part joining. During soldering, the package peak temperature and temperature ramps cannot exceed the package peak temperature and temperature ramps of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PCB depending on the furnace type, size and mass of components, and the location of components on the assembly. Additionally, rework stations only apply heat locally, not to the entire PCB. If nozzles are used to direct the heat, the nozzle size must be sufficiently large to encompass the entire part. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, carefully attach thermocouples with very small amounts of thermally conductive grease, or epoxy, directly to the solder joint interface between the package and board.

The materials used in rework have a higher potential to create conductive traces, corrosion, etc. compared to standard materials. Residual solder and flux must be specific to the type of paste used in the original assembly. Follow the recommendations of the solder paste manufacturer. NXP recommends the use of low-residue and no-clean solder paste for soldering.

7 Board level reliability

7.1 Testing details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. There are several different names for board-level reliability (BLR) that customers may see. These include: second-level reliability (2^{nd} level reliability), solder-joint reliability (SJR), and temperature cycling on board (TCoB).

Information provided here is based on experiments executed on MAPBGA devices using a daisy chain BGA configuration. Actual surface mount process and design optimizations are recommended to develop an application-specific solution.

- For automotive grade product applications, the widely accepted temperature range for testing is -40 °C to +125 °C.
- Consumer SJR temperature cycling conditions may vary widely depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0 °C to +100 °C.

The preferred test method varies by market and industry. For automotive, the primary test is a version of IPC-9701A[(13)], air temperature cycling. For the consumer market, the JEDEC drop test is the primary test (JESD22-B111[(16)]). Telecommunications uses both IPC-9701A[(13)] and IPC/JEDEC-9702[(8)] (monotonic bend). NXP may not test an electronic package and may not have all tests for each market and industry.

Table 2 shows the NXP standard test set-up for performing automotive board level solder joint reliability testing. For consumer markets, the board stack-up found in JESD22-B111[16] is commonly used, 8 Cu layers, and 1 mm total thickness. Telecommunications market parts use IPC-9701A[13]/ IPC/JEDEC-9702[8] stack-ups of 8 Cu layers and 2.25 mm total thickness.

Table 2. Board level reliability setup

Board Level Reliability Testing: Material and Test Setup	
PCB board	• 1.58 mm thickness • 4 Cu layer • OSP surface finish
Test board assembly	• Pb-free solder paste SAC387 • Reflow peak temperature for SAC assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 mm thickness, Ni plated, laser cut and electro-polished stainless steel stencil
Cycling conditions	• Continuous in-situ daisy chain monitoring per IPC-9701A[13] and IPC-SM-785[14] • Air Temperature Cycling (ATC) for Automotive – –40 °C / +125 °C – 15 minute ramp / 15 minute dwell – 1 hour cycle time • Air Temperature Cycling (ATC) for Commercial & Industrial – 0 °C / +100 °C – 10 minute ramp / 10 minute dwell – 40 minute cycle time
Package test vehicle	• Production bill of materials (BOM) package including die (die mechanically present, without wire bond connection) • Daisy chain in the BGA pattern connecting pairs of solder balls.

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for various packages. To obtain results from these experiments (including Weibull plots), contact the NXP sales team. Customers should interpret the NXP solder joint reliability data to determine how well the solder joint reliability data meets the final application requirements.

8 Thermal characteristics

8.1 General thermal performance

The thermal package properties provided by NXP serve only as a guideline for the thermal application design. Thermal package performance in the final application depends on a number of factors. These factors include board design, power dissipation of other components on the same board, and ambient temperature. In applications where the thermal performance is critical, NXP recommends that customers perform application-specific thermal calculations during the design phase to confirm the onboard thermal performance.

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors that need be considered in PCB design and thermal rating of the final application are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path, solder joints that may reduce the effective solder area)

The thermal characteristics of the package indicate the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are stated in the NXP product data sheets as appropriate. Product data sheets are available at NXP.com. Customers may request more detailed thermal properties.

8.3 Package thermal properties – definition

The definition of thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W) typically specify the thermal performance of a MAPBGA package. Thermal characterization is performed by physical measurement and running complex simulation models under the following conditions:

- Two thermal board types:
  - Single layer board (1s) per JEDEC JESD51-3 & JESD51-5 (exposed pad packages only)
  - Four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only).
- Four boundary conditions:
  - Natural convection (still air) per JEDEC JESD51-2[(2)]
  - Forced convection per JEDEC JESD51-6[(3)]
  - Thermal test board on ring style cold plate method per JEDEC JESD51-8[(4)]
  - Cold plate method per MIL SPEC-883[(18)] method 1012.1

8.3.1 RθJA: Theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2[(2)]) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into and through the test board followed by convection and radiation off the exposed board surfaces.

8.3.2 RθJMA: Theta junction-to-moving-air forced convection

Junction-to-Moving-Air (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6[(3)]) is similar to $R_{\theta JA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to a moving air (at 200 feet/minute) environment.

8.3.3 RθJB: Theta junction-to-board

Junction-to-board thermal resistance[1] measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four layer test board (2s2p) per JEDEC JESD51-7. $R_{\theta JB}$ is frequently used by customers to create thermal models that consider both package and application board thermal properties.

8.3.4 RθJC: Theta junction-to-case

Junction-to-Case thermal resistance[2] indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method[3] with the cold plate temperature used for the case temperature. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is performed.

8.3.5 ΨJT (Psi JT): Junction-to-package top

Junction-to-Package top[4] indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition[5] or forced convection environment[6]. Ψ_{JT} must not be confused with the parameter RθJC. RθJC is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature. Ψ_{JT} is the value of the temperature difference between package surface and junction temperature, usually in natural convection.

8.4 Package thermal properties – example

An example of the thermal characteristics as typically shown in the NXP product data sheet is shown in Table 3. The example applies to a package size 17 mm x 17 mm x 1.5 mm (max), pitch 0.8 mm, 364 I/O, die size ~ 4.9 mm x 5.9 mm (NXP case outline drawing SOT1517-1).

Table 3. Thermal resistance example

Rating			W/O HS, 0.7 mold	With HS, 0.7 mold	W/O HS, 0.8 mold	With HS, 0.8 mold	Unit	Notes
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	45	37	45	37	°C/W	[1], [2]

1 Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8[(4)]
2 Theta-JC or $R_{\theta JC}$ per MIL SPEC-883[(18)] Method 1012.1
3 per MIL SPEC-883[(18)] Method 1012.1
4 Psi JT or Ψ_{JT}
5 per JEDEC JESD51-2[(2)]
6 per JEDEC JESD51-6[(3)]

Table 3. Thermal resistance example...*continued*

Rating			W/O HS, 0.7 mold	With HS, 0.7 mold	W/O HS, 0.8 mold	With HS, 0.8 mold	Unit	Notes
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	28	22	28	23	°C/W	[1], [2], [3]
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	37	29	37	30	°C/W	[1], [3]
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	24	19	24	19	°C/W	[1], [3]
Junction to Board	—	$R_{\theta JB}$	17	11	17	12	°C/W	[4]
Junction to Case	—	$R_{\theta JC}$	8	8	10	9	°C/W	[5]
Junction to Package Top	Natural Convection	Ψ_{JT}	2	7	2	8	°C/W	[6]

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature, air flow, power dissipation of other components on the board, and the thermal resistance.

[2] Per JEDEC JESD51-2(2) with the single layer board horizontal. Board meets JESD51-9 specification.

[3] Per JEDEC JESD51-6(3) with the board horizontal.

[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8(4). Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL Spec-883(18) Method 1012.1).

[6] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2(2). When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9 Case outline drawing, MCDS, and MSL rating

9.1 Downloading the information from NXP

At NXP.com, NXP offers packaging, environmental, and compliance information in the parametric tables and in the device information details. Enter the part number in the search box and review the package information details for the specific part.

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752-A(11) reporting format, can be downloaded as a PDF file. Information on product-specific Moisture Sensitivity Level (MSL) is also available in the part details.

9.2 Moisture sensitivity level

The Moisture Sensitivity Level (MSL) indicates the component floor life, storage conditions, and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation[7] of the mold compound from the die or substrate, wire bond damage, die damage, and internal cracks. In the most severe cases, the component can bulge and pop, known as the "popcorn" effect.

7 Known as delamination

It is necessary to seal dry moisture-sensitive components in a moisture barrier antistatic bag with a desiccant and a moisture indicator card. Vacuum seal the bag according to IPC/JEDEC J-STD-033 and only remove immediately prior to assembly to the PCB.

Table 4 presents the MSL definitions per IPC/JEDEC J-STD-20. Refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of NXP products. Components must be mounted and reflowed within the allowable time period (floor life out of the bag). The maximum reflow temperature shall not be exceeded during board assembly at the customer’s facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card (HIC) indicates too much moisture after opening a moisture-barrier bag (MBB), baking the components is required prior to the assembly process. To determine allowable maximum temperature, refer to imprints/labels on the respective packing.

The higher the MSL value, more attention is required to store the components. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 4. MSL descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30 °C / 85 % RH
2	1 Year	30 °C / 60 % RH
2a	4 Weeks	30 °C / 60 % RH
3	168 Hours	30 °C / 60 % RH
4	72 Hours	30 °C / 60 % RH
5	48 Hours	30 °C / 60 % RH
5a	24 Hours	30 °C / 60 % RH
6	Time on Label (TOL)	30 °C / 60 % RH

10 Package handling

10.1 Handling ESD devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS). Proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs, and components. Comprehensive ESD controls to protect ESDS during handling and processing should be considered.

The following industry standards describe detailed requirements for proper ESD controls. NXP recommends users meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD615-B[17] – Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5[7] – Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling moisture-sensitive SMD devices

MAPBGA devices are moisture/reflow sensitive Surface Mount Devices (SMD) and proper precautions are required for handling, packing, shipping, and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in Section 9.2 "Moisture sensitivity level", during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concern. Proper handling of SMDs should be considered.

Dried moisture-sensitive SMDs are placed in trays or tape-and-reels, and dry-packed for proper transportation and storage. SMDs are sealed with desiccant material and a humidity indicator card (HIC) inside a Moisture-Barrier Bag (MBB). The shelf life of dry-packed SMDs is 12 months from the dry pack seal date when stored in ≤ 40 °C / 90 % RH environment.

Proper use and storage of moisture-sensitive SMDs are required after the MBB is opened. Improper use and storage increases various quality and reliability risks. SMDs subjected to reflow solder or other high temperature processes must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033D standard.

The baking of SMDs is required before mounting if any of following conditions is experienced:

- SMDs exposed to a specified floor environment greater than specified period
- Humidity Indicator Card (HIC) reading > 10 % for level 2a – 5a or > 60 % for level 2 devices when read at 23 °C ± –5 °C environment.
- SMDs not stored according to J-STD-033D standard

The baking procedure, and more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in the following industry standard:

- J-STD-033DB[(10)] – Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.3 Packing of devices

MAPBGA devices are contained in tray or tape-and-reel configuration. The trays and tape-and-reels are dry-packed for transportation and storage. Packing media is designed to protect devices from electrical, mechanical, and chemical damage as well as moisture absorption. However, proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C / 90 % RH environment, excessive stacking of dry packs, etc.) increase various quality and reliability risks.

- Tray
  - NXP complies with standard JEDEC tray design configuration, see Figure 18.
  - Pin 1 of the devices is oriented with lead 1 toward the chamfered corner of the tray.
  - Trays are designed to be baked for moisture sensitive SMDs, but the temperature rating of tray should NOT be exceeded when devices are baked. The temperature

rating can be found at the tray end-tab. Recommended baking temperature of trays is 125 °C.

– Trays are typically banded together with 5+1 (five fully loaded trays and one cover tray) stacking and dry-packed in a moisture barrier bag. Partial stacking (1+1, 2+1, etc.) is also available depending on individual requirements.

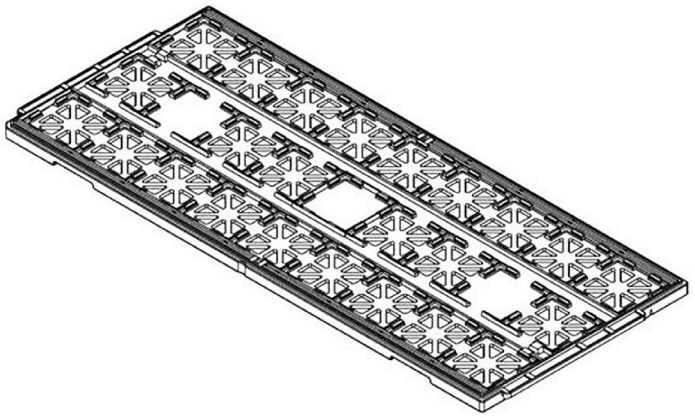

Figure 18. JEDEC tray example

- Tape and reel
  - NXP complies with EIA-481-E[(5)] for carrier tape and reel configuration, see Figure 19 and Figure 20.
  - NXP complies to pin 1 orientation of devices with EIA-481-E[(5)].
  - Tape-and-reels are NOT designed to be baked at high temperature.
  - Each tape-and-reel is typically dry-packed in a moisture barrier bag.

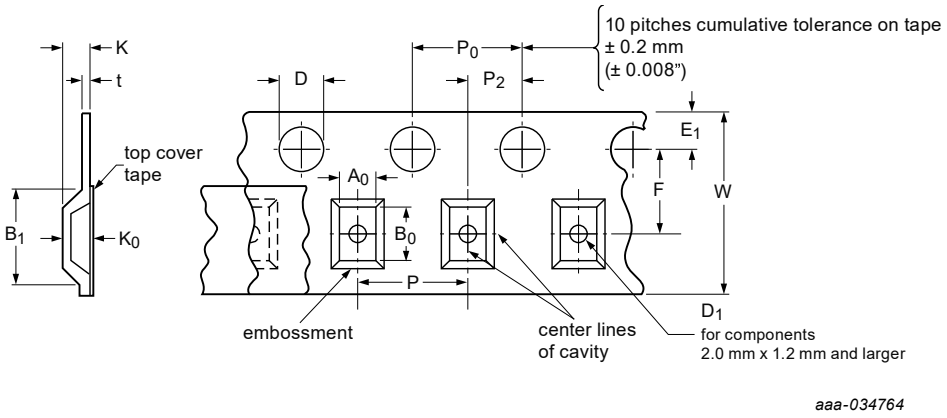

Figure 19. Carrier tape specifications

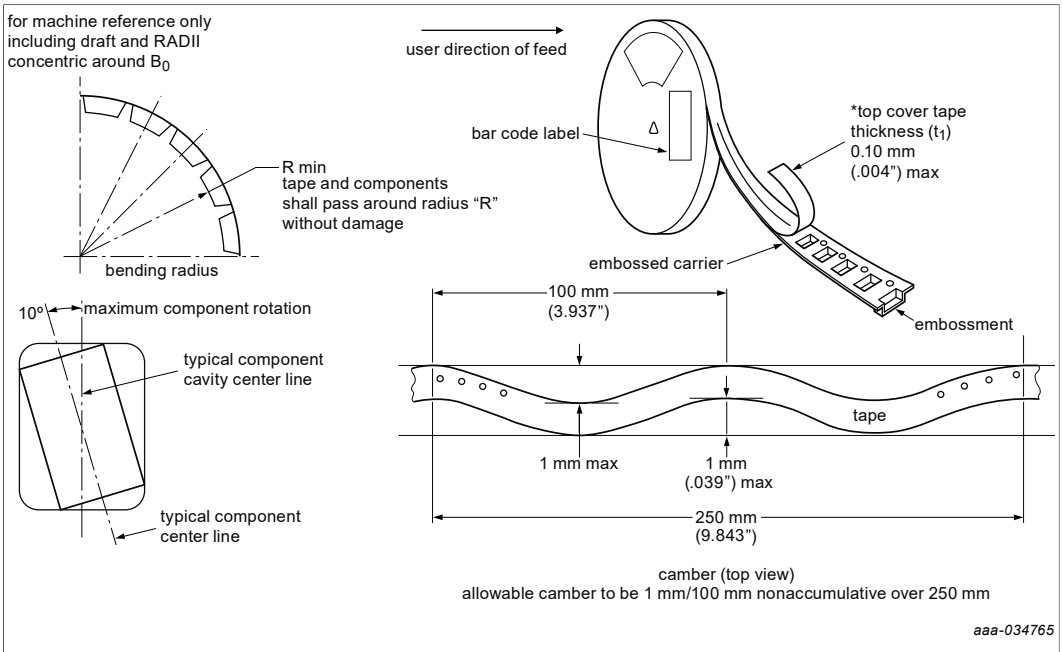

Figure 20. Tape and reel example

- Dry packing
  - Trays and tape-and-reels loaded with devices, are sealed in a moisture barrier bag, labeled, and packed in dedicated boxes with dunnage for the final shipment.
  - Each dry pack bag contains a desiccant pouch and a humidity indicator card (HIC).
  - NXP encourages the recycling and reuse of materials whenever possible.
  - NXP does not use packing media items processed with or containing Class 1 ozone depleting substances.
  - Whenever possible, NXP designs its packing configurations to optimize volumetric efficiency and package density to minimize the amount of packing material entering the industrial waste stream.

NXP complies with the following environmental standards conformance guidelines/ directives:

- ISPM 15[(15)], *Guidelines for Regulating Wood Packaging Material in International Trade*.
- EPCD 94/62/EC[(6)], *European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste*.

11 Abbreviations

Table 5. Abbreviations

Acronym	Description
1s	Single layer board
2s2p	Four layer board
Ag	Silver
BGA	Ball grid array
BLR	Board-level reliability
BOM	Bill of materials
Cu	Copper
ENIG	Electroless nickel immersion gold
ESD	Electrostatic discharge
ESDS	Electrostatic discharge sensitive
HASL	Hot air solder leveled
HIC	Humidity indicator card
IC	Integrated circuit
IPC	Institute for Printed Circuits
JEDEC	Joint Electron Device Engineering Council
MAPBGA	Molded array process ball grid array
MBB	Moisture-barrier bag
MCDS	Material composition declaration sheet
MSL	Moisture sensitivity level
Ni	Nickel
NSMD	Non-solder mask defined
OSP	Organic solderability protectant
Pb	Lead
PCB	Printed circuit board
SEM	Scanning electron microscope
SJR	Solder joint reliability
SMD	Solder mask defined
SMD	Surface mount devices
SMT	Surface mount technology
Sn	Tin
TCoB	Temperature cycling on board

12 References

(1) AN3300 — *General Soldering Temperature Process Guidelines*, Rev. 1, Aug 2017

(2) JESD51-2A — *Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)*, Jan 2007.

(3) EIA/JESD51-6 — *Integrated Circuits Thermal Test Method Environment Conditions – Forced Convection (Moving Air)*, Mar 1999.

(4) EIA/JESD51-8 — *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*, Oct 1999.

(5) EIA-481 — *8 mm Through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling*, Rev. E, Jan 2015.

(6) EPCD 94/62/EC — *European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste*, Dec 1994

(7) IEC-101/61340-5 — *Specification for the Protection of Electronic Devices from Electrostatic Phenomena*, Nov 2018

(8) IPC/JEDEC-9702 — *Monotonic Bend Characterization of Board-Level Interconnects*, Jun 2004.

(9) J-STD-020E — *Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Nonhermetic Surface-Mount Devices*, Dec 2014.

(10) J-STD-033D — *Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices*, Apr 2018

(11) IPC-1752-A — *Materials Declaration Management Standard*, Mar 2014.

(12) IPC-7351B — *Generic Requirements for Surface Mount Design and Land Pattern Standards*, Jun 2010.

(13) IPC-9701A — *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*, Feb 2006.

(14) IPC-SM-785 — *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, Nov 1992.

(15) ISPM 15 — *Regulation of wood packaging material in international trade*, May 2019.

(16) JESD22-B111 — *Board Level Drop Test Method of Components for Handheld Electronic Products*, Jul 2003.

(17) JESD625-B — *Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices*, Dec 2011.

(18) **MIL-STD-883** — *MIL-STD-883, Department of Defense Test Method Standard, Microcircuits, Method 1012.1 Thermal Characteristics*, Revision G, Feb 2006.

13 Revision history

Table 6. Revision history

REVISION	DATE	DESCRIPTION OF CHANGES
4	20201208	• Section 1, added ", including Flip Chip Chip Scale Package (FCCSP)" to the first paragraph. • Section 3.3, added Figure 5, Figure 6, and revised the paragraph to support the added figures.
3	20190822	• The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Performed the following global changes: – Updated all figures and images. – Performed spelling and grammar revisions. – Rephrased some passive voice sentences and paragraphs to active voice. • Section 3.1: Revised the second paragraph to describe associated figures. • Section 3.2, revised "Package sizes range from 4.0 x 4.0 to 27 x 27 mm..." to Package sizes range from 3 mm x 3 mm to 27 mm x 27 mm.…" • Section 4.1: Revised package drawing from SOT-1516-1 to SOT1517-1. • Added Section 11 "Abbreviations". • Section 12: Updated references.
2	9/2014	Updated Section 9.1.
1	8/2014	Initial release

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Tables

Figures

Assembly guidelines for molded array process ball grid array package

Contents

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