Chapter-7

80386

Limitations of 286

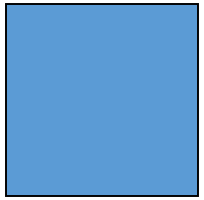
- 16-bit ALU
- 64K segment size
- cannot be easily switched back and forth between real and protected mode
  - to come back to the real mode from protected mode, you have to switched off the 286

386 was designed to overcome these limitations

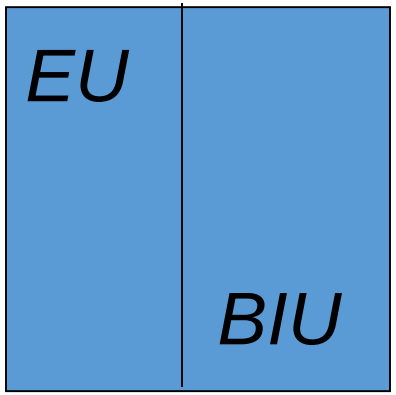
- 32 bit ALU
- segment size can be as large as 4G
  - a program can have as many as 16K segments.
  - So, a program has access to 4Gx16K=64TB of virtual memory
- 386 has a ***virtual 86*** mode which allows easy switching between real and protected modes.

80386 Features

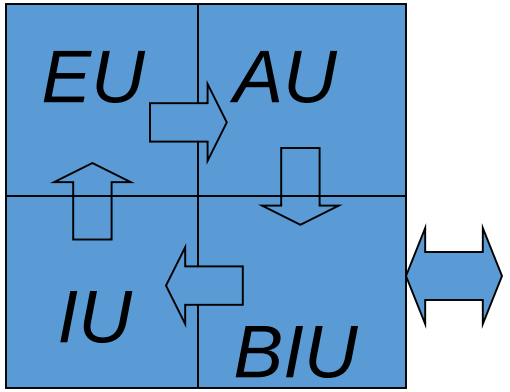
- Intel introduced the first 32-bit chip, 80386, in October 1985 as an upgrade to the 80286 processor
- Intel stopped producing 386 since September 2007.
- It operates in 3 different modes
  - **Real**
  - **Protected**
  - **Virtual .**
- MMU provides virtual memory, paging and 4 levels of protection
- Low cost & low power consumption.
- Clock Frequency : 20,25 and 33MHz
- 386 was capable of performing more than five million instructions every second (MIPS)



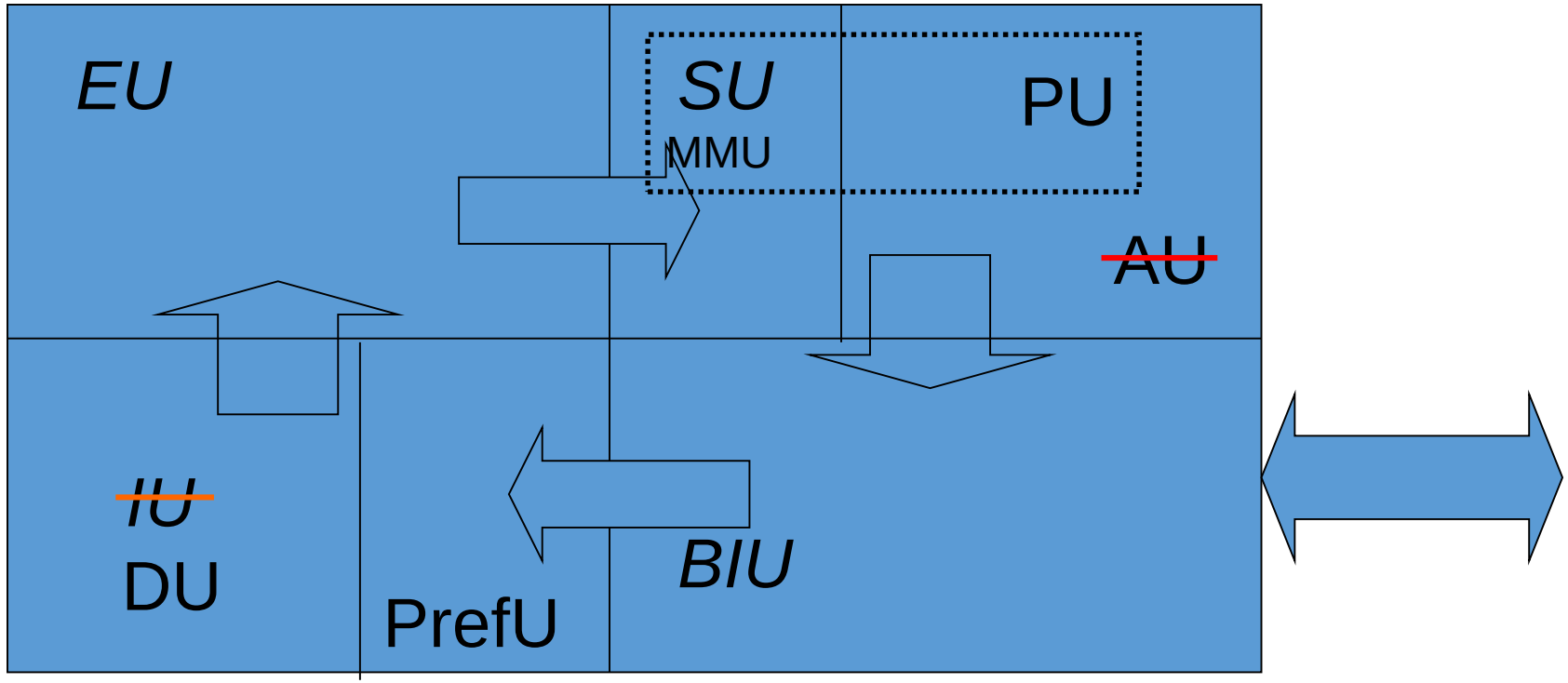
8085



8086



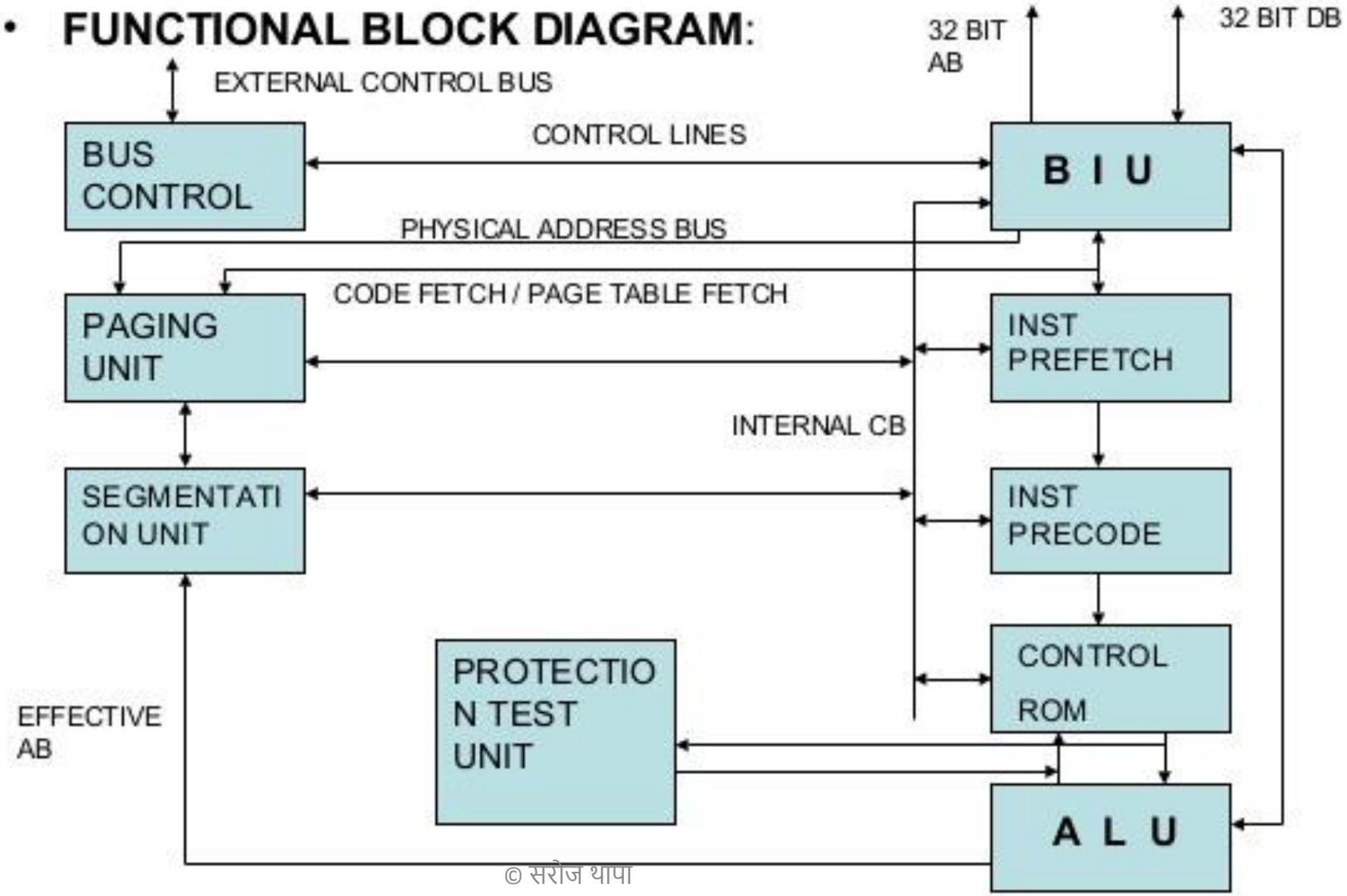
80286



80386

80386

- **FUNCTIONAL BLOCK DIAGRAM:**



Architecture of 80386

- The Internal Architecture of 80386 is divided into 3 sections:

i) Central processing unit (CPU)

- Execution unit (EU) and
- Instruction unit (IU)

ii) Memory management unit (MMU)

- Segmentation unit and
- Paging unit

iii) Bus interface unit (BIU)

Architecture of 80386...

CPU

i. Execution unit

- Execution unit has 8 General and Special purpose registers, which are either used for handling data or calculating offset addresses.
- The 64-bit barrel shifter increases the speed of all shift, rotate.
- Multiply/divide logic implements the bit-shift rotate algorithms to complete the operation in minimum time

ii. Instruction Unit:

- It decodes the opcode bytes received from the 16-byte instruction code queue and arrange them into a 3- decoded instruction queue.
- After decoding it is passed to control section for deriving necessary control signals

Memory Management Unit

MMU consists of a segmentation unit and paging unit.

Segmentation Unit:

- Uses of two address components - segment and offset – for relocability and sharing of data.
- It allows a maximum segment size of 4GB

Paging Unit

- It organizes physical memory in terms of pages of 4KB size.
- It works under the control of segmentation unit i.e. each segment is divided into pages.
- It converts linear addresses into physical addresses.

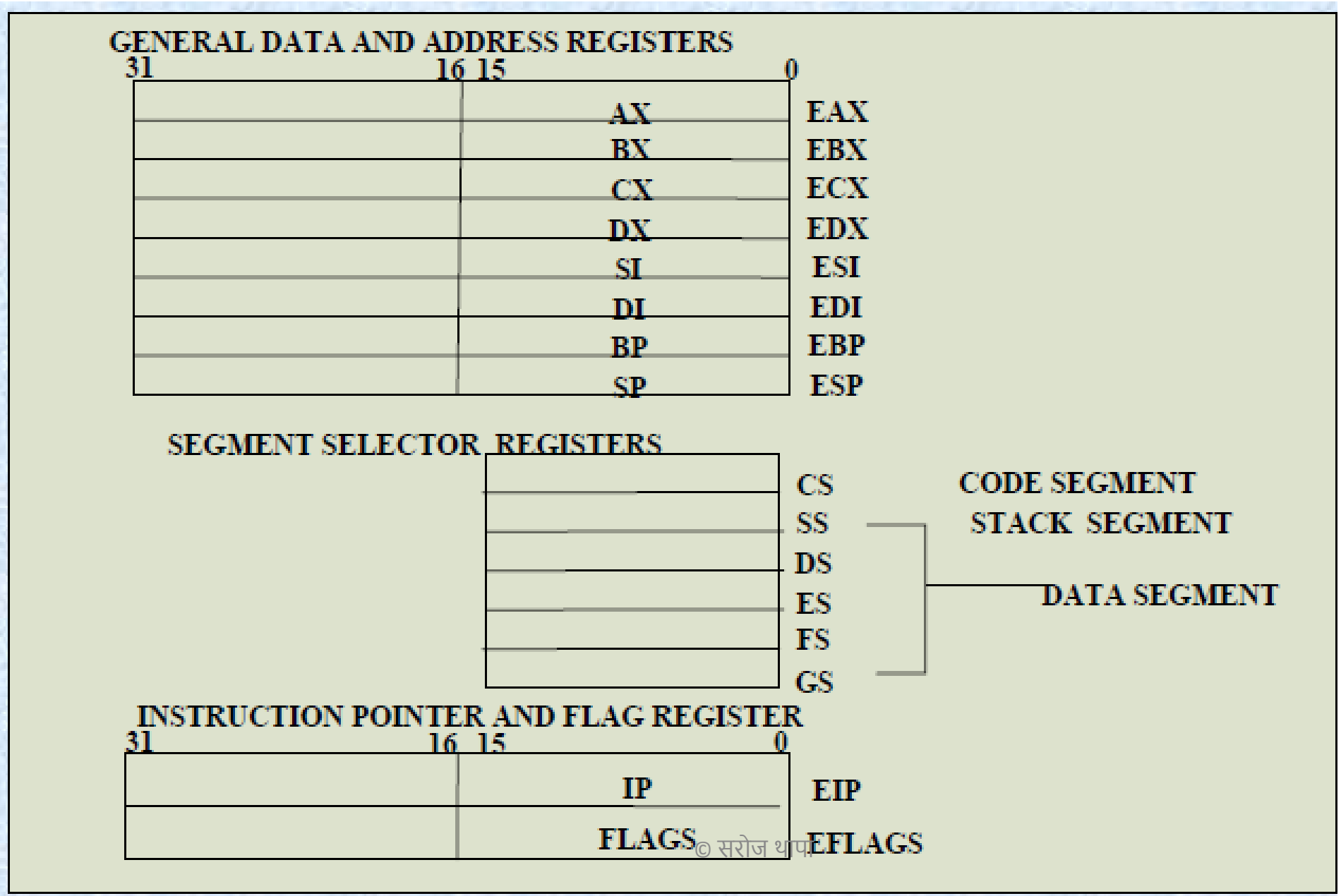
Bus Control Unit

- It has a prioritizer to resolve the priority of various bus requests.
- This controls the access of the bus.
- The address driver drives the bus enable and address signals A2 – A31.

Register Organisation in 80386

• The 80386 has eight 32 - bit general purpose registers which may be used as either 8 bit or 16 bit registers.
• A 32 - bit register known as an extended register, is represented by the register name with prefix E.
• Example : A 32 bit register corresponding to AX is EAX, similarly BX is EBX etc.
• The 16 bit registers BP, SP, SI and DI in 8086 are now available with their extended size of 32 bit and are names as **EBP,ESP,ESI and EDI**.
• AX represents the lower 16 bit of the 32 bit register EAX. BP, SP, SI, DI represents the lower 16 bit of their 32 bit counterparts, and can be used as independent 16 bit registers.

Register Organisation in 80386



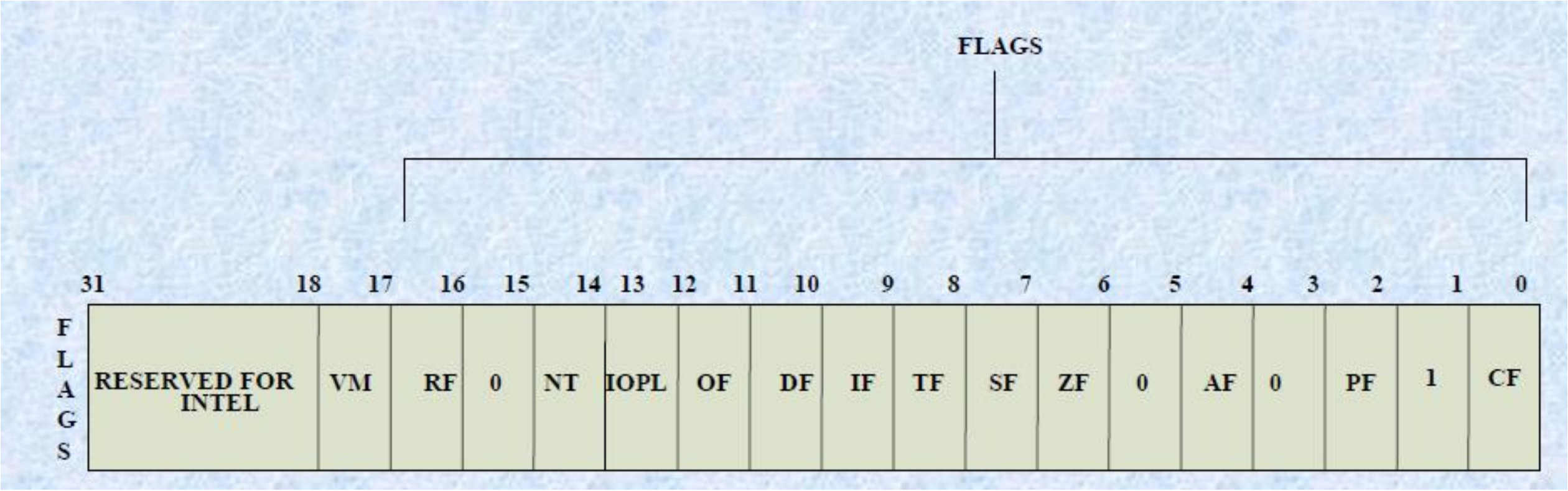
Register organization cont..

- The six segment registers available in 80386 are CS, SS, DS, ES, FS and GS.
- The CS and SS are the code and the stack segment registers respectively, while **DS, ES, FS, GS** are 4 data segment registers.
- A 16 bit instruction pointer IP is available along with 32 bit counterpart EIP.

Flag Register of 80386:

- The Flag register of 80386 is a **32 bit register**. Out of the 32 bits, Intel has reserved bits D18 to D31, D5 and D3, while D1 is always set at
- Two extra new flags are added to the 80286 flag to derive the flag register of 80386.
- They are **VM and RF flags**
- **VM - *Virtual Mode Flag***: If this flag is set, the 80386 enters the virtual 8086 mode within the protection mode.
- ***RF- Resume Flag***: This flag is used with the debug register breakpoints. It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle.

Flag Register of 80386:



Special Purpose registers

i.segment Descriptor Registers:

- This registers are not available for programmers, rather they are internally used to store the descriptor information, like attributes, limit and base addresses of segments.
- The six segment registers have **corresponding six 73 bit** descriptor registers.

ii. Debug and Test Registers:

- Intel has provide a set of 8 debug registers for hardware debugging.
- Out of these eight registers DR0 to DR7, two registers DR4 and DR5 are Intel reserved.

Registers cont..

iii. Control Registers:

- The 80386 has three 32 bit control registers **CR1, CR2 and CR3** to hold global machine status independent of the executed task.
- Load and store instructions are available to access these registers.

iv. System Address Registers:

- Four special registers are defined to refer to the descriptor tables supported by 80386.
- The 80386 supports four types of descriptor table, viz. **global descriptor table (GDT)**, **interrupt descriptor table (IDT), local descriptor table (LDT)** and task state segment descriptor (TSS).

Memory access in Protected Mode of 80386

- All the capabilities of 80386 are available for utilization in its protected mode of operation.
- The 80386 in protected mode support all the software written for 80286 and 8086 to be executed under the control of memory management and protection abilities of 80386.
- The protected mode allows the use of additional instruction, addressing modes and capabilities of 80386.

ADDRESSING IN PROTECTED MODE:

- In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment.

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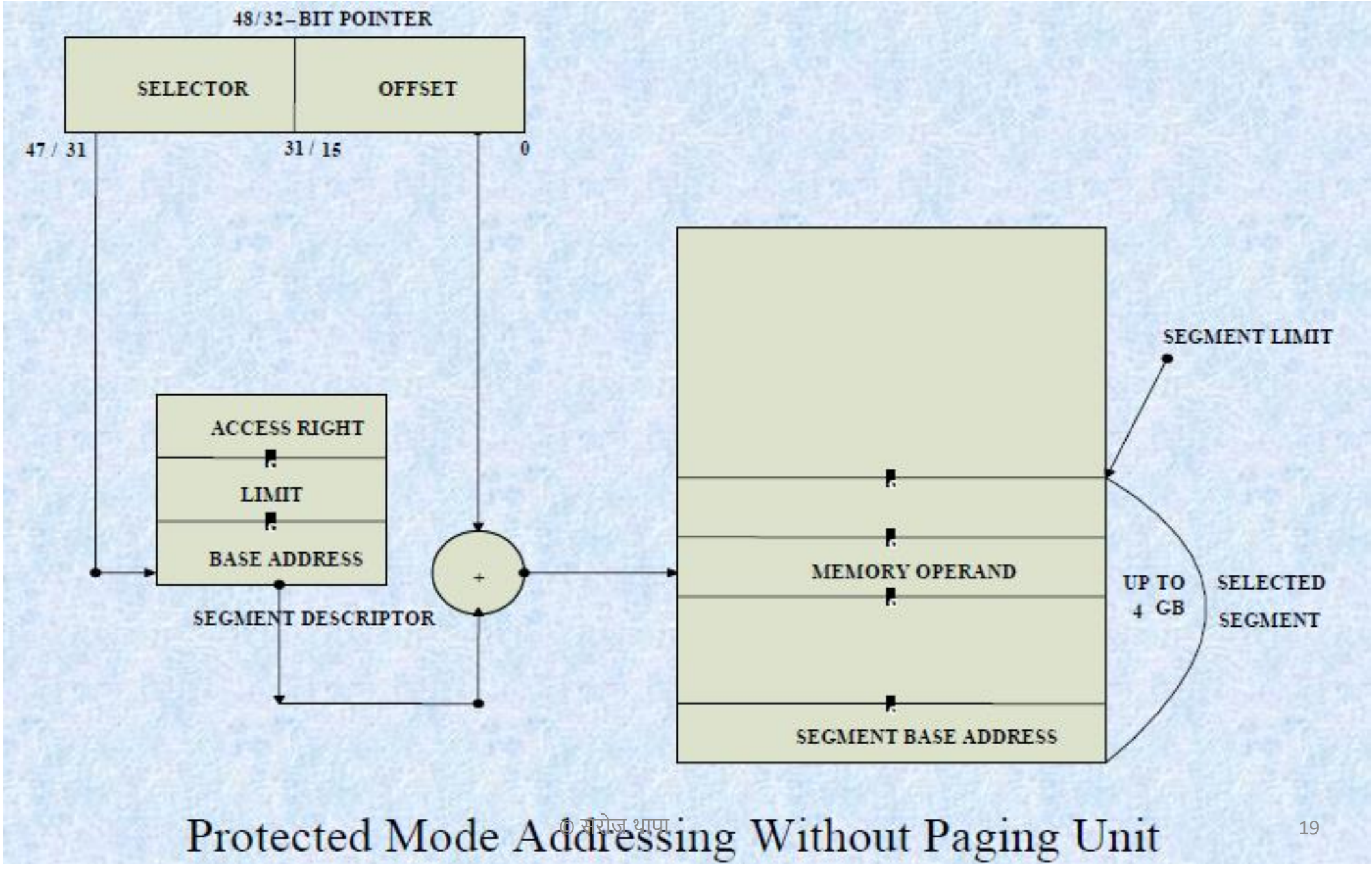


Protected Mode Addressing Without Paging Unit

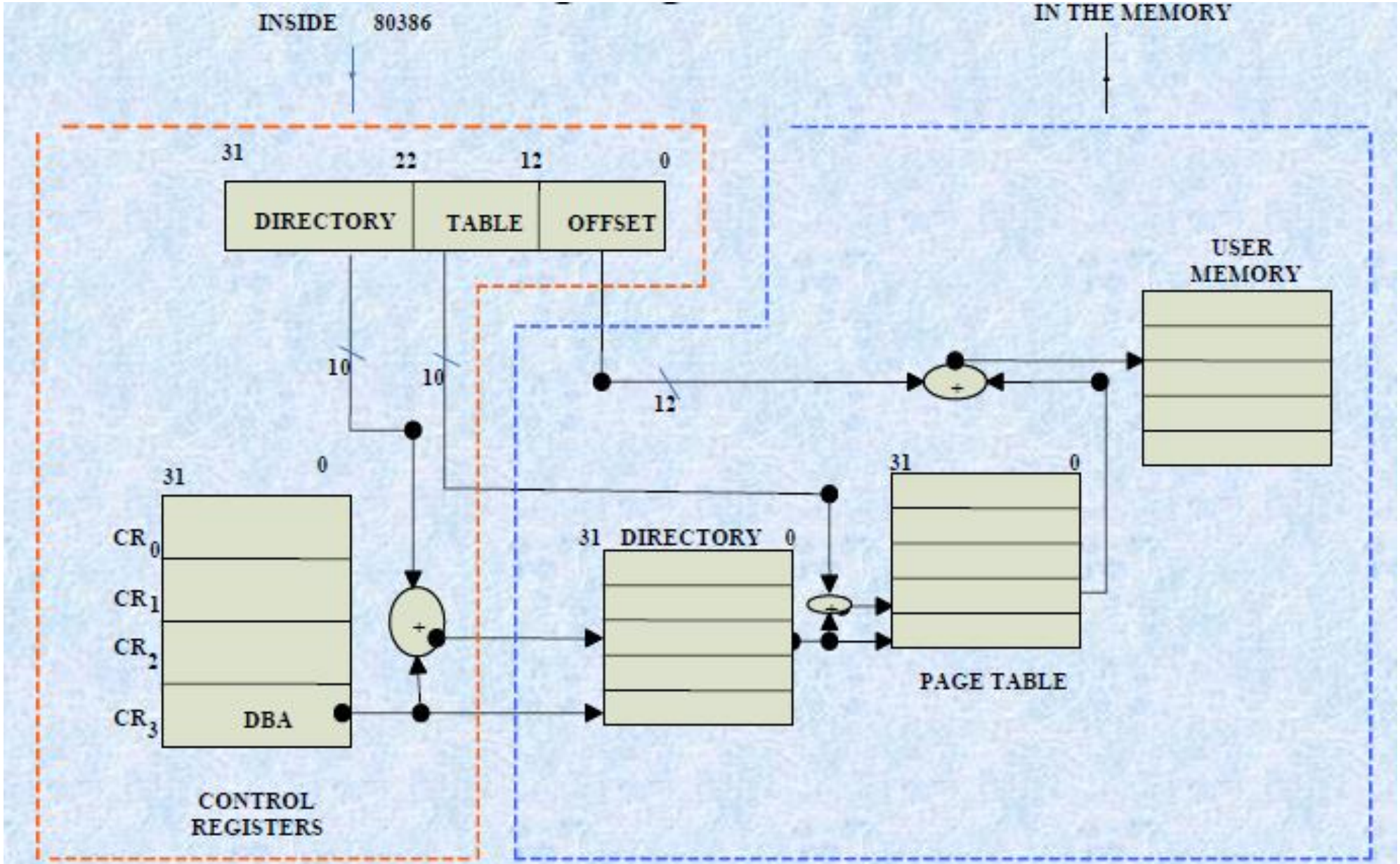
Paging

- Paging is one of the memory management techniques used for virtual memory multitasking operating system.
- The segmentation scheme may divide the physical memory into a variable size segments but the paging divides the memory into a fixed size pages.
- The segments are supposed to be the logical segments of the program, but the pages do not have any logical relation with the program.
- The **pages are just fixed size portions of the program module or data**.
- The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time.
- Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory.

Paging Unit:

- The paging unit of 80386 uses a two level table mechanism to convert a **linear address provided by segmentation unit into physical addresses.**
- The paging unit converts the complete map of a task into pages, each of size 4K. The task is further handled in terms of its page, rather than segments.
- The paging unit handles every task in terms of three components namely
  - page directory,
  - page tables and
  - page itself.

Cont..



DBA Physical directory base address

Cont..

Paging Descriptor Base Register:

- The control register CR2 is used to store the 32-bit linear address at which the previous page fault(Note it!!!) was detected.
- The CR3 is used as page directory physical base address register, to store the physical starting address of the page directory.
- The lower 12 bit of the CR3 are always zero to ensure the page size aligned directory.

Page Directory :

- This is at the most 4Kbytes in size. Each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory.
- The upper 10 bits of the linear address are used as an index to the corresponding page directory entry. The page directory entries point to page tables.

Cont..

Page Tables:

- Each page table is of **4Kbytes** in size and many contain a maximum of 1024 entries.
- The page table entries contain the **starting address of the page** and the **statistical information** about the page

END of this course