



nRF51822

Multiprotocol *Bluetooth*® 4.0 low energy/2.4 GHz RF SoC

Product Specification v1.3

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自我感觉不重要的地方就没有深究，加之水平有限，错误难免
译文非专业翻译，仅供学习参考，使用者自行承担使用之责

欢迎各位同行讨论、指点、批评、建议： mq-elec@foxmail.com

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主要特点

- 2.4 GHz 无线收发器
 - 低功耗模式下灵敏度 : -93 dBm
 - 数据传输速率 : 250 kbps, 1 Mbps, 2 Mbps
 - TX Power -20 to +4 dBm in 4 dB steps
 - 省电模式下发射功率 : -30 dBm
 - 峰值电流, 接收时 : 13 mA, 发射时(0 dBm) : 10.5 mA
 - RSSI (分辨率 : 1 dB) #接收信号的强度指示
- ARM® Cortex®-M0 32 bit processor
 - 275 µA/MHz running from flash memory
 - 150 µA/MHz running from RAM
 - Serial Wire Debug (SWD)
- 现成的软件包 : S100 系列
- 存储
 - 内置Flash : 256 kB /128 kB
 - 16 kB RAM
- 支持非并行多协议运行
 - 兼容 nRF24L 系列
- 灵活的电源管理
 - 工作电压 : 1.8 V - 3.6 V
 - 使用 16 MHz RC : 2.5 µs 唤醒
 - 关闭模式 : 0.4 µA @ 3 V
 - 关闭模式且保留一个区域 RAM : 0.5 µA @ 3 V
 - 运行模式, 所有模块空闲 : 2.3 µA @ 3 V
- 8/9/10 bit ADC - 8 个可配置通道
- 31 个通用 I/O
- 一个32位和两个16位带计数模式的定时器
- SPI 主端
- 2线主端 (兼容I2C)
- UART (CTS/RTS)
- 与 CPU 相互独立的可编程外设总线 (PPI)
- 正交解码 (QDEC)
- AES 硬件加密
- 实时计数器 (RTC)
- 封装类型
 - QFN48 封装, 6 x 6 mm
 - WLCSP 封装, 3.50 x 3.83 mm

应用场合

- 电脑外设和输入输出设备
 - 鼠标
 - 键盘
 - 多点触控板
- 娱乐互动设备
 - 遥控
 - 3D 眼镜
 - 游戏控制器
- 个人互联
 - 健康/健身的探测和监控设备
 - 医疗设备
 - 钥匙, 手表
 - 遥控玩具

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
May 2013	1.3	Updated schematics and BOMs in <i>Section 11.3 on page 61</i> .
April 2013	1.2	<p>Added chip variant nRF51822-CEAA. Updated feature list on front page.</p> <p>Updated</p> <p><i>Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 28, Section 10.4 on page 52, and Section 10.5.1 on page 53.</i></p> <p>Added</p> <p><i>Section 2.2.2 on page 10, Section 7.1 on page 29, Section 9.2 on page 50, and Section 11.3 on page 61.</i></p> <p>Removed PCB layouts in <i>Chapter 11 on page 54</i>.</p>
March 2013	1.1	<p>Added chip variant nRF51822-QFAB. Added 32 MHz crystal oscillator feature. Updated feature list on front page. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 8 to the nRF51 Reference Manual.</p> <p>Updated</p> <p><i>Chapter 1 on page 6, Section 2.2 on page 8, Section 3.2 on page 14, Section 3.5 on page 18, Section 3.5.1 on page 19, Section 4.2 on page 23, Chapter 5 on page 26, Section 8.1 on page 30, Section 8.1.2 on page 31, Section 8.1.5 on page 33, Section 8.2 on page 35, Section 8.3 on page 37, Section 8.5.3 on page 39, Section 8.8 on page 43, Section 8.9 on page 44, Section 8.10 on page 45, Section 8.14 on page 46, Chapter 10 on page 51, Section 11.2.3 on page 59, Section 11.2.1 on page 55, and Section 11.2.2 on page 57.</i></p> <p>Added</p> <p><i>Section 3.5.4 on page 21, Section 8.1.3 on page 32, and Section 11.1 on page 54.</i></p>
November 2012	1.0	<p>Changed from PPS to PS.</p> <p>Updated feature list on front page.</p> <p>Updated <i>Table 13 on page 28, Table 14 on page 29, Table 16 on page 31, Table 18 on page 33, Table 19 on page 33, Table 20 on page 34, Table 23 on page 36, Table 24 on page 37, Table 26 on page 38, Table 27 on page 38, Table 28 on page 39, Table 32 on page 42, Table 33 on page 43, Table 35 on page 44, Table 38 on page 45, Table 39 on page 46, Table 42 on page 47, Table 45 on page 48, Table 46 on page 48, Table 61 on page 53, and Figure 15 on page 59</i>.</p>

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1 简介

nRF51822 是一款集成nRF51x系列无线收发器的超低功耗的片上系统 (Soc) , 包含一个32位 ARM® Cortex®-M0 CPU , flash 存储器和模拟、数字外设。nRF51822 支持低功耗蓝牙和一系列专有 2.4 GHz 协议，例如 Nordic Semiconductor 公司的 Gazell。

完全适用于nRF51822的低功耗协议栈在 S100 系列软件包中实现。S100 系列软件包是免费的，可下载、安装到nRF51822上，独立于您的应用代码。

nRF51822 有不同的封装和内存类型 (variants)。本手册不适用于所有变量，这些适用的变量将会明示。例如 一个类型名是nRF518822-QFAA的，如果没有说明该类型，或者仅 nRF51822 被使用，那么该数据适用于 nRF51822 的所有版本。

1.1 推荐阅读

强烈建议阅读 nRF51 参考手册(*nRF51 Reference Manual*)。

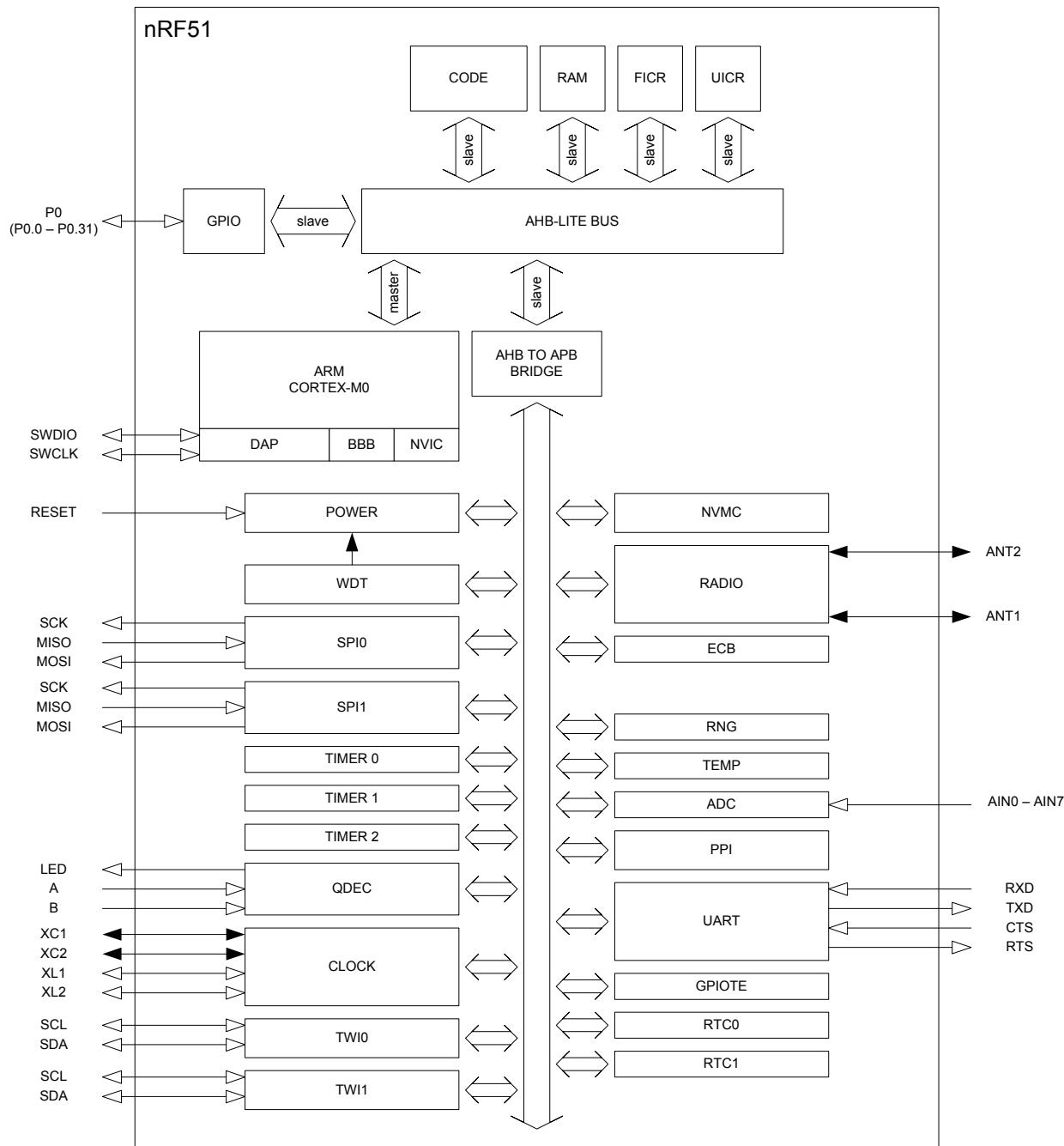
1.2 书写规范

本手册遵循一套印刷规范，确保这些文档是一致的，易于阅读的。规范如下：

- 命令，事件名称和位状态 使用 Lucida Console 样式。
- 引脚名称和引脚信号状态 使用 Consolas 样式。
- 文件名称和用户接口组件 使用粗体 **bold** 。
- 内部交叉引用是斜体，使用 *semi-bold*. 样式。
- 参数的占位符使用斜体、普通文本字体。例如，一种联结的语法描述写法如下：
Connect(TimeOut, AdvInterval).
- 常量写成普通文本字体。例如，一种联结的方法描述写法如下：
Connect will be written as:
Connect(0x00F0, Interval).

2 产品概述

2.1 模块框图



Note: 默认情况下RESET是无效的。

Figure 1 nRF51822 block diagram

2.2 引脚分配和功能

本节描述不同封装类型的引脚分配和引脚的功能。

2.2.1 nRF51822 QFN48

2.2.1.1 引脚分配

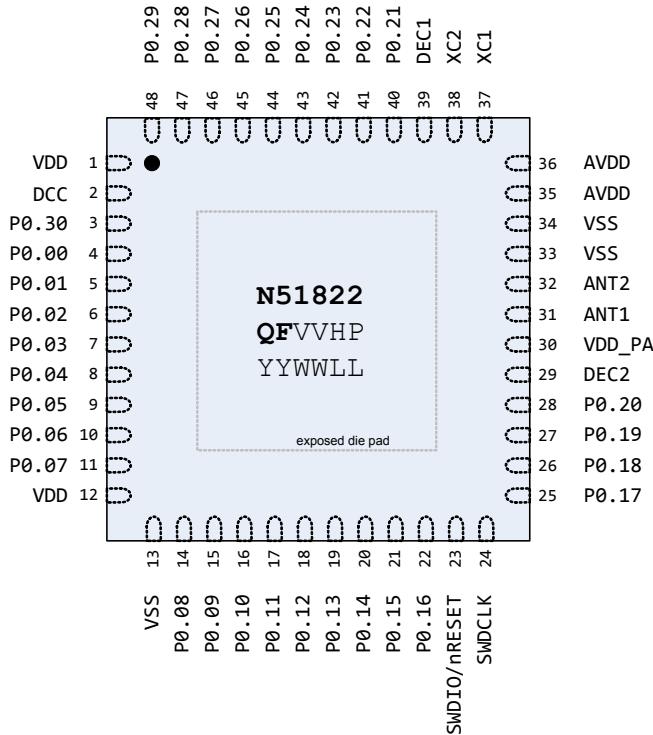


Figure 2 Pin assignment - nRF51822 QFN48 packet

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see [Section 10.4 on page 52](#).

2.2.1.2 Pin functions

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply
2	DCC	Power	DC/DC output voltage to external LC filter
3	P0.30	Digital I/O	General purpose I/O pin
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin ADC Reference voltage
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin ADC input 2
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin ADC input 3
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin ADC input 4
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin ADC input 5
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin ADC input 6
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin ADC input 7 ADC Reference voltage
11	P0.07	Digital I/O	General purpose I/O pin
12	VDD	Power	Power supply
13	VSS	Power	Ground (0 V) ¹
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin
23	SWDIO/nRESET	Digital I/O	System reset (active low). Also HW debug and flash programming I/O
24	SWDCLK	Digital input	HW debug and flash programming I/O
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin
29	DEC2	Power	Power supply decoupling
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp
31	ANT1	RF	Differential antenna connection (TX and RX)
32	ANT2	RF	Differential antenna connection (TX and RX)
33, 34	VSS	Power	Ground (0 V)
35, 36	AVDD	Power	Analog Power supply
37	XC1	Analog input	Connection for 16/32 MHz crystal or external 16 MHz clock reference
38	XC2	Analog output	Connection for 16/32 MHz crystal
39	DEC1	Power	Power supply decoupling

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin
45	P0.26	Digital I/O	General purpose I/O pin
	AIN0	Analog input	ADC input 0
	XL2	Analog output	Connection for 32.768 kHz crystal
46	P0.27	Digital I/O	General purpose I/O pin
	AIN1	Analog input	ADC input 1
	XL1	Analog input	Connection for 32.768 kHz crystal or external 32.768 kHz clock reference
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin

1. The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

Table 1 Pin functions nRF51822 QFN48 packet

2.2.2 nRF51822 WLCSP

2.2.2.1 Ball assignment

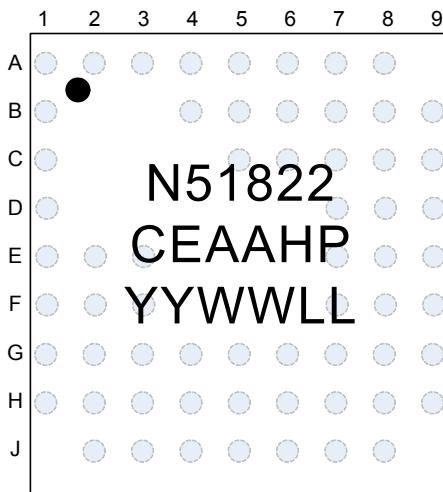


Figure 3 Ball assignment nRF51822-CEAA packet (top side view)

Note: HP = Buildcode, YYWWLL = Tracking code
Solder balls not visible on the top side. Dot denotes A1 corner.

2.2.2.2 Ball functions

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal
A4	DEC1	Power	Power supply decoupling
A5	P0.21	Digital I/O	General purpose I/O
A6	P0.24	Digital I/O	General purpose I/O
A7	P0.26	Digital I/O	General purpose I/O
	AIN0	Analog input	ADC input 0
	XL2	Analog output	Crystal connection for 32.768 kHz crystal oscillator
A8	P0.27	Digital I/O	General purpose I/O
	AIN1	Analog input	ADC input 1
	XL1	Analog input	Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference
B1	VSS	Power	Ground (0 V)
B4	VSS	Power	Ground (0 V)
B5	P0.22	Digital I/O	General purpose I/O
B6	P0.23	Digital I/O	General purpose I/O
B7	P0.28	Digital I/O	General purpose I/O
B8	VDD	Power	Power supply
B9	DCC	Power	DC/DC output voltage to external LC filter
C1	ANT2	RF	Differential antenna connection (TX and RX)
C5	P0.25	Digital I/O	General purpose I/O
C6	N.C.	No Connection	Must be soldered to PCB
C7	P0.29	Digital I/O	General purpose I/O
C8	VSS	Power	Ground (0 V)
C9	P0.00	Digital I/O	General purpose I/O
	AREF0	Analog input	ADC Reference voltage
D1	ANT1	RF	Differential antenna connection (TX and RX)
D7	VSS	Power	Ground (0 V)
D8	P0.30	Digital I/O	General purpose I/O
D9	P0.02	Digital I/O	General purpose I/O
	AIN3	Analog input	ADC input 3
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp
E2	N.C.	No Connection	Must be soldered to PCB
E3	N.C.	No Connection	Must be soldered to PCB
E7	N.C.	No Connection	Must be soldered to PCB
E8	P0.31	Digital I/O	General purpose I/O
E9	P0.01	Digital I/O	General purpose I/O
	AIN2	Analog input	ADC input 2

Ball	Name	Function	Description
F1	DEC2	Power	Power supply decoupling
F2	P0.19	Digital I/O	General purpose I/O
F3	N.C.	No Connection	Must be soldered to PCB
F7	N.C.	No Connection	Must be soldered to PCB
F8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O ADC input 5
F9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O ADC input 4
G1	P0.20	Digital I/O	General purpose I/O
G2	P0.17	Digital I/O	General purpose I/O
G3	N.C.	No Connection	Must be soldered to PCB
G4	N.C.	No Connection	Must be soldered to PCB
G5	N.C.	No Connection	Must be soldered to PCB
G6	VSS	Power	Ground (0 V)
G7	N.C.	No Connection	Must be soldered to PCB
G8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O ADC input 7 ADC Reference voltage
G9	VSS	Power	Ground (0 V)
H1	P0.18	Digital I/O	General purpose I/O
H2	SWDCLK	Digital input	HW debug and flash programming I/O
H3	VSS	Power	Ground (0 V)
H4	P0.14	Digital I/O	General purpose I/O
H5	P0.13	Digital I/O	General purpose I/O
H6	P0.10	Digital I/O	General purpose I/O
H7	P0.07	Digital I/O	General purpose I/O
H8	VDD	Power	Power supply
H9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O ADC input 6
J2	SWDIO/ nRESET	Digital I/O	System reset (active low). Also HW debug and flash programming I/O
J3	P0.16	Digital I/O	General purpose I/O
J4	P0.15	Digital I/O	General purpose I/O
J5	P0.12	Digital I/O	General purpose I/O
J6	P0.11	Digital I/O	General purpose I/O
J7	P0.09	Digital I/O	General purpose I/O
J8	P0.08	Digital I/O	General purpose I/O

Table 2 Ball functions for nRF51822-CEAA

3 系统模块

nRF51822 包含所有 nRF51 系列共有的系统级特征：时钟控制，电源和复位，中断系统，可编程外设总线（PPI），看门狗 和 GPIO。

System 系统模块例化在设备的地址空间中，有一个寄存器接口，并且（and/or）分配中断向量。系统模块的例化，它们的关联 ID（关于中断向量）和基地址请查阅 *Table 12 on page 26*。详细的功能描述，配置选项和寄存器接口可查阅 nRF51 参考手册（*nRF51 Reference Manual*）。

3.1 CPU

ARM® Cortex™-M0 CPU 拥有16位和32位扩展（[Thumb-2® technology](#)）指令集，实现高密度的代码和小内存占用。通过使用单周期32位乘法，3级流水线和嵌套向量控制器（NVIC），ARM Cortex-M0 CPU 使程序运行简单、高效。

ARM Cortex-M 系列处理器的 CMSIS 的硬件抽象层已经实现，也适用于 M0 CPU。代码是向前兼容 ARM Cortex M3 芯片的。

3.2 存储器

存储器和寄存器的映射参见 *Figure 4*。nRF51 系列芯片闪存的底部用作代码空间，FICR 和 UICR 区域。RAM 区域就是 SRAM。

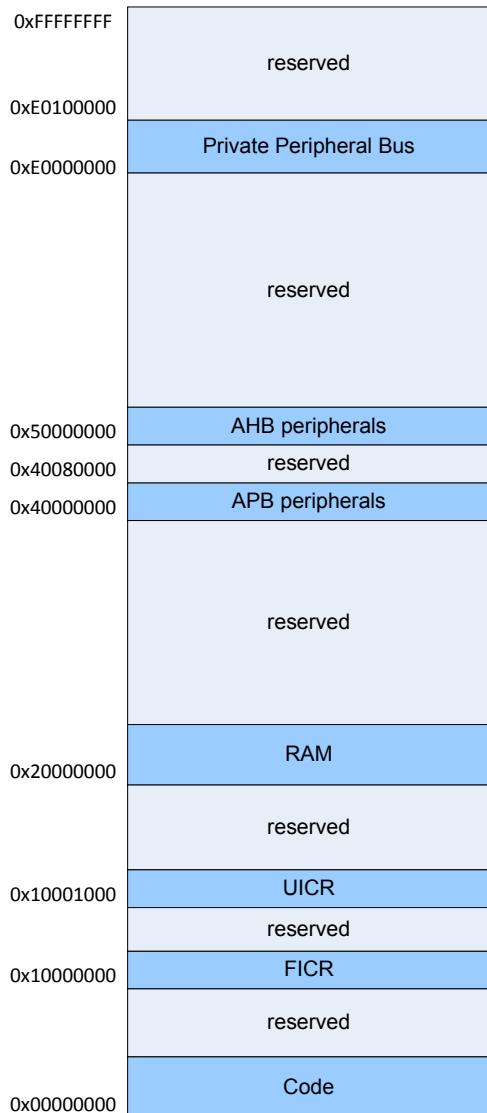


Figure 4 Device Memory Map

保存程序和静态数据的内嵌闪存空间可通过 SWD 接口从 RAM 使用 IAP 方式编程，或者通过在线从代码区域的一段可执行程序来编程。NVMC 用于烧写/擦除操作。也可能通过使能 UICR 中的读保护来设置所有或部分代码区域拥有读保护。

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51822-QFAA		256 kB	1024 byte
nRF51822-CEAA			256
nRF51822-QFAB	128 kB	1024 byte	128

Table 3 Code organization

3.2.2 RAM organization

如 nRF51 系列参考手册 (*nRF51 Series Reference Manual*) 中所述，RAM 被分块以便于独立管理电源。
RAM 的电源管理由 POWER 系统控制。

Chip variant	RAM size	Block	Start address	Size
nRF51822-QFAA				
nRF51822-QFAB	16 kB	Block0 Block1	0x20000000 0x20002000	8 kB 8 kB
nRF51822-CEAA				

Table 4 RAM organization

3.3 电源管理 (POWER)

电源管理系统是非常的灵活，除了整个系统的开关模式外，这些模块，如 CPU，无线收发器和外设还有独立的供电控制。在系统关闭模式，RAM 可以保留，并且通过复位或 GPIO 信号，芯片状态可以切换到系统打开模式。当系统处于打开模式，所有功能块可根据需要单独设为空闲 (IDLE) 或运行状态。

电源管理特点：

- 系统打开/关闭模式
- 局部供电限制
- 电源失效比较器
- 系统关闭模式下引脚唤醒
- 功能分块运行/空闲模式
- 系统关闭模式下 2 个区域 RAM 可保留

供电特点：

- Supervisor HW to manage power on reset, brownout, and power fail
- 使用内置 LDO 稳压，供电范围：1.8V - 3.6V
- 低电压模式必须使用外置稳压器，供电范围：1.75V - 1.95V
- 使用内部 DC/DC 降压，供电范围：2.1V - 3.6V

3.3.1 低电压模式

芯片可运行于低电压模式，外部使用稳定的 1.8V 电源供电。使用低电压模式时，电路必须修改为 *Section 11.2.2 on page 57*

3.3.2 DC/DC 转换器

nRF51 的 DC/DC 降压转换器将电池电压转换成低内部电压，功耗损失极小。转换后的电压作为线性稳压器的输入。当供电低于电压下限时，可以失能 DC/DC 转换器，这样 LDO 用于低电压供电。在启用的情况下，当内部只需要稳定低电流时，DC/DC 转换过程会自动暂停。

该特点特别有利于使用标称电压很高的电池供电设计。降压措施减少了电池的峰值功率耗散。使用 3V 纽扣电池时，电池的峰值电流耗散降了近 30%

注：使用 DC/DC 转换器需要外接三个无源器件。详细内容参见 *Section 11.2.3 on page 59* 的原理图。

3.4 可编程外设总线(PPI)

PPI 使外设可以独立于CPU，相互间通过任务、事件自由通讯。当应用程序有实时性约束存在时，该特点使外设间同步精确。并且，通过 PPI 预置，可以不需要 CPU 参与。

Instance	Number of channels	Number of groups
PPI	16	4

Table 5 PPI properties

3.5 Clock management (CLOCK)

时钟管理系统能从内部或外部高频、低频振荡器获得系统时钟，然后根据模块的各自需要给他们分配时钟。这样可避免激活庞大的时钟树，当系统模块不需要参考时钟被激活时能避免消耗能量。

如果应用程序使某个需要参考时钟的模块却没有相应的振荡器工作，时钟管理系统会自动使能 RC 振荡器来提供时钟源。当模块进入空闲状态，时钟管理系统同样会自动设置振荡器为空闲。为避免启动给定振荡器时的延时，或者需要一上特定的振荡器，应用程序可以改变自动管理，因此当没有系统模块需要参考时钟时也能使振荡器保持激活状态。

时钟只在系统打开模式有效，可以通过下面时钟源产生：

Clock	Source	Frequency options
High Frequency Clock (HFCLK) ¹	External Crystal (XOSC)	16/32 MHz ²
	External clock reference ³	16 MHz
	Internal RC Oscillator (RCOSC)	16 MHz
Low Frequency Clock (LFCLK)	External Crystal (XOSC)	32.768 kHz
	External clock reference ³	32.768 kHz
	Synthesized from HFCLK	32.768 kHz
	Internal RC Oscillator (RCOSC)	32.768 kHz

1. 外部晶振必须用于无线电工作
2. 使用16和32MHz晶振 HFCLK 都是 16MHz
3. 更多关于外部时钟参见 nRF51参考手册 (nRF51 reference manual)

Table 6 Clock properties

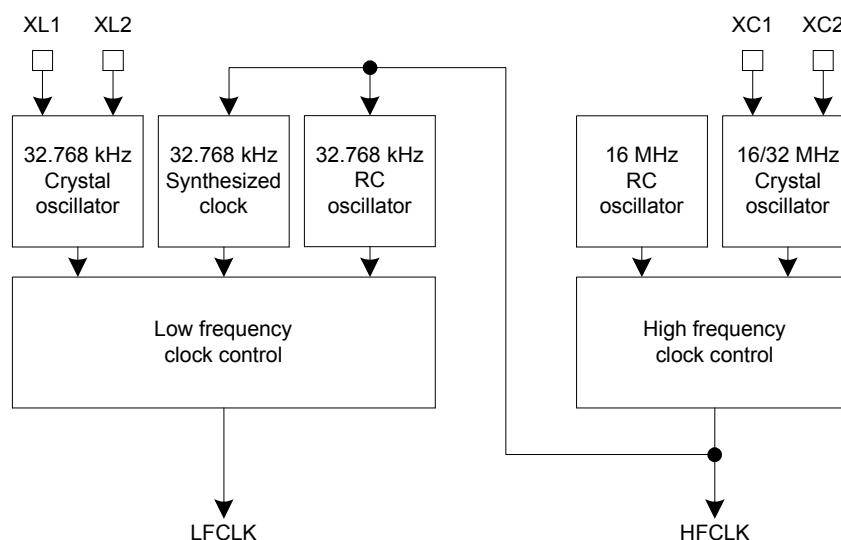


Figure 5 Clock management

3.5.1 16/32 MHz 晶体振荡器

(nRF51 Reference Manual)。晶体振荡器专为并联谐振方式下使用石英晶体 (AT-cut quartz) 设计。为得到正确的振荡频率，负载电容必须与晶体数据表中的参数匹配。Figure 6 显示晶何时如何连接到 16/32 MHz 的晶体振荡器。

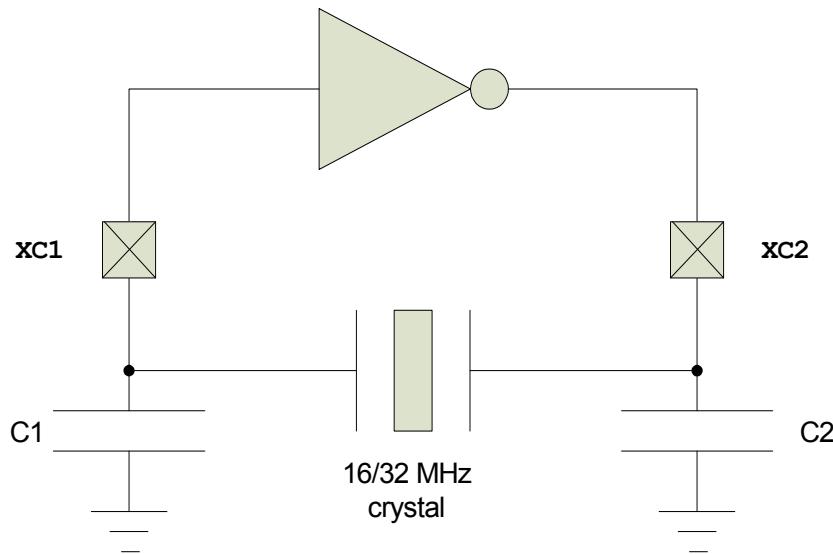


Figure 6 Circuit diagram of the 16/32 MHz crystal oscillator

负载电容 (C_L) 是由晶体两端看过去的总电容，公式如下：

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

$C1$ 和 $C2$ 是贴片式陶瓷电容。 C_{pcb1} 和 C_{pcb2} ¹ 是 PCB 的寄生电容。 C_{pin} 是 $XC1$ 和 $XC2$ 引脚上的引脚输入电容，参见 Table 16 on page 31 (16 MHz) 和 Table 17 on page 32 (32 MHz)。负载电容 $C1$ 和 $C2$ 的值应该相同。

为了可靠工作，晶体的负载电容，寄存电容，等效串联电阻 ($R_{S,X16M}/R_{S,X32M}$) 和驱动电平必须遵循 Table 16 on page 31 (16 MHz) 和 Table 17 on page 32 (32 MHz) 中参数说明。如果负载电容或寄存电容大，推荐使用比 $R_{S,X16M}/R_{S,X32M}$ 最大值小的晶体。这样启动速度更快，消耗电流更低。低负载电容将减小启动时间和电流消耗。

1. See Chapter 11 on page 54 for the capacitance value used for C_{pcb1} and C_{pcb2} in reference circuitry.

3.5.2 32.768 kHz 晶体振荡器

32.768 kHz 的晶体振荡器专为并联谐振方式下使用石英晶体设计。为得到正确的振荡频率，负载电容必须与晶体数据表中的参数匹配。*Figure 7* 显示晶何时如何连接到 32.768 kHz 的晶体振荡器。

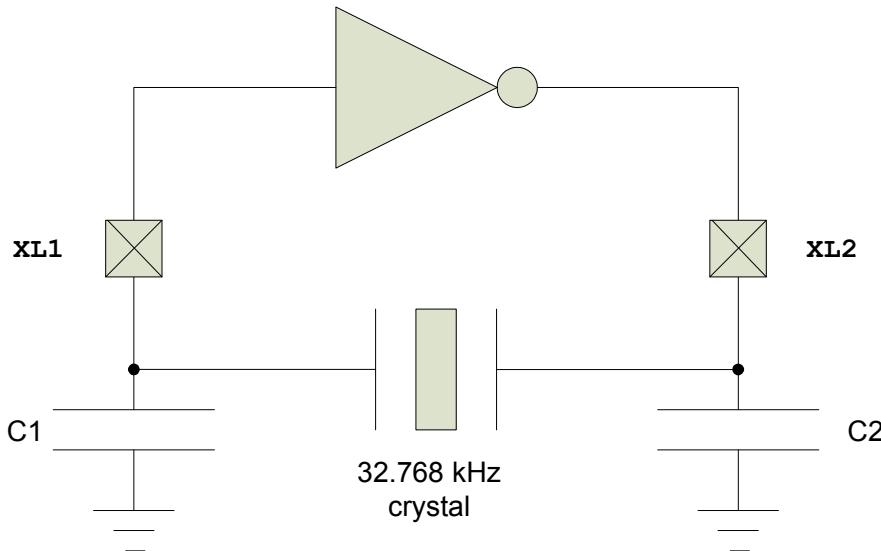


Figure 7 Circuit diagram of the 32.768 kHz crystal oscillator

负载电容 (C_L) 是由晶体两端看过去的总电容，公式如下：

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$

$$C2' = C2 + C_{pcb2} + C_{pin}$$

$C1$ 和 $C2$ 是贴片式陶瓷电容。 C_{pcb1} 和 C_{pcb2} ² 是 PCB 的寄生电容。 C_{pin} 是 $XC1$ 和 $XC2$ 引脚上的引脚输入电容，参见 *Table 19 on page 33*。负载电容 $C1$ 和 $C2$ 的值应该相同。

3.5.3 32.768 kHz RC 振荡器

低频率的 32.768 kHz RC 振荡器也可作为 32.768 kHz 晶体振荡器的备用选择。在温度稳定或者变化但定期校准的环境中，频率精度可达 ± 250 ppm。32.768 kHz RC 振荡器不需要外部器件。

2. See *Chapter 11 on page 54* for the capacitance value used for C_{pcb1} and C_{pcb2} in reference circuitry.

3.5.4 合成的 32.768 kHz 时钟

低频率时钟可以由高频率时钟合成。这样可节省晶体，但是因为需要激活高频率时钟，而会增加平均功耗。

3.6 GPIO

灵活的通用 I/O 被组织为一个可达 32(取决于封装) 个 I/O 的接口，这些多达 32 个 I/O 通过一个接口提供访问和控制功能。每个 GPIO 可独立访问，每个都如下的配置特点：

- 输入/输出方向
- 输出驱动能力
- 内部上拉/下拉电阻
- 所有引脚高电平唤醒，低电平触发
- 所有引脚触发中断
- 所有引脚可用于 PPI 任务/事件系统；同时可通过 PPI 系统连接的最大数量受 GPIO TE 模块的数量限制。
- 所有引脚可单独配置来传输串行接口或者正交解码信号。

3.7 调试支持

2线串行调试(SWD)接口作为调试访问端口 (DAP)，配合 NTB 为无干扰调试代码提供灵活有效的途径。支持断点，单步执行，指令跟踪捕获等。

4 外设模块

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, 例化的 ID (中断向量)、基地址位于 *Table 12 on page 26*。详细的功能描述，配置选项和寄存器接口可参考 nRF51 参考手册 (*nRF51 Reference Manual*)。

4.1 2.4 GHz 无线电 (RADIO)

nRF51 系列的 2.4 GHz RF 收发器设计工作在全球开放的 ISM 频段：2.4 - 2.4835 GHz。无线调制模式、配置包结构使无线收发器与 Bluetooth® low energy (BLE), ANT™, Enhanced ShockBurst™，还有其它的 2.4 GHz 协议共同使用。

无线收发直接从系统存储器收发数据，数据管理灵活且高效

- 通用调制特点
 - GFSK 调制
 - 数据简单
 - 7 位线性反馈移位寄存器 (可编程IV)
 - 数据速率
 - 250 kbps
 - 1 Mbps
 - 2 Mbps
- 可编程发射功率：+4 dBm - -20 dBm, in 4 dBm steps
- 省电模式发射功能：-30 dBm
- RSSI 功能(1 dB 分辨率, $\pm 6 \pm 6$ dB 精度)
- 集成通道滤波的接收器的最大灵敏度：
 - -96 dBm @ 250 kbps
 - -93 dBm @ 1 Mbps BLE
 - -90 dBm @ 1 Mbps
 - -85 dBm @ 2 Mbps
- RF Synthesizer
 - 1 MHz frequency programming resolution
 - 1 MHz non-overlapping channel spacing at 1 Mbps and 250 kbps
 - 2 MHz non-overlapping channel spacing at 2 Mbps
 - 使用低成本 ± 60 ppm 16 MHz 晶体振荡器工作
- 基带控制器
 - 从 RAM 直接收发 EasyDMA³ RX 和 TX 的数据包
 - 动态负载长度
 - 极速组合/拆散和AES CCM 负载加密
 - 8 位, 16 位 和 24 位CRC 检验(可编程多项式和初始值)

3. EasyDMA - 是一个集成 DMA，不需要配置就能使用灵活的数据管理系统，避免与 RAM 的拷贝操作。

4.2 定时器/计数器 (TIMER)

TIMER 工作于高频率时钟源 (HFCLK) , 包含一个对 HFCLK 分频的 4 位 ($1/2^X$) 预分频。

TIMER 的任务/事件和中断特点使得可以使用 PPI 系统用于对包括任一 GPIO 在内的系统外设的输入/输出任务进行计时/计数。PPI 系统也能使 TIMER 产生周期输出信号和 PWM 信号输出到任意 GPIO。同时输入/输出的数量受 GPIO TE 模块的数量限制。

Instance	Bit-width	Capture/Compare registers
TIMER0	32	4
TIMER1	16	4
TIMER2	16	4

Table 7 Timer / Counter properties

4.3 实时计数器(RTC)

RTC 工作于低频时钟源 (LFCLK) 下 , 提供一个通用的、低功耗的时钟。 RTC 功能特点 : 24 位计数器 , 12 位 ($1/X$) 预分频器 , 捕获/比较寄存器 , 还有低功耗的滴答事件发生器 , 为 RTOS 的实现提供 滴答时钟。

Instance	Capture/Compare registers
RTC0	4
RTC1	3

Table 8 RTC properties

4.4 AES-ECB 加密(ECB)

ECB 加密模块支持 128 位 AES 加密。它可以用一系列加密功能 , 如哈希生成 , 数字签名 , 数据加密/解密的密钥生成。

It operates with EasyDMA access to system RAM for in-place operations on cleartext and ciphertext during

4. 随机数发生器 (RNG)

随机数发生器 (RNG) 基于内部热噪声生成真正的非确定性随机数。这些随机数适用于加密的目的。RNG 不需要种子值。

4.6 看门狗 (WDT)

采用低频率时钟源 (LFCLK) 的倒计数看门狗提供可配置的、强大的保护防止应用程序锁死。CPU长时
间处于睡眠 (低功耗应用) 和调试器暂 CPU 的情况下 , 看门狗可以被暂停。

4.7 温度传感器

温度传感器，分辨率为 0.25 °C。

4.8 SPI (SPI)

SPI接口允许设备之间进行全双工同步通信。它支持 3线 (SCK, MISO, MOSI) 双向总线，与多个从设备快速传输数据。对于连接到总线的每个从设备，独立的片选信号是必须的，但是这些控制权是留给应用程序使用GPIO控制。I/O的数据是双缓冲。

用于每个 SPI 接口线的 GPIO可从芯片上的 GPIO 中任选，而且可独立配置。这使得芯片引线十分灵活，有效利用印制电路板空和信号通路。

SPI 外设支持 SPI 的 0, 1, 2, 3 模式。

Instance	Master/Slave
SPI0	Master
SPI1	Master

Table 9 SPI properties

4.9 两线接口 (TWI)

两线接口使用两根线 (SCL, SDA) 连接双向线和总线(wire-AND bus)。该协议可连接多达128个可单独寻址的设备。该接口兼容时钟拉伸，支持 100 kbps 和 400 kbps 传输速率。

用于每个 SPI 接口线的 GPIO可从芯片上的 GPIO 中任选，而且可独立配置。这使得芯片引线十分灵活，有效利用印制电路板空和信号通路。

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table 10 Two-wire properties

4.10 UART (UART)

通用异步接收器/发送器提供快速，全双工，内置流量控制的异步串行通信 (CTS, RTS)，在硬件方面支持高达1 Mbps波特率。 支持奇偶校验和第9位数据生成。

用于每个 SPI 接口线的 GPIO可从芯片上的 GPIO 中任选，而且可独立配置。这使得芯片引线十分灵活，有效利用印制电路板空和信号通路。

4.11 正交解码器 (QDEC)

正交解码器提供正交编码传感器信号的缓存解码。适用于带可选 LED输出信号和输入去抖滤波器的机械、光学传感器。采样周期和累积量是可配置的，以满足应用需要。

4.12 模拟 - 数字转换器 (ADC)

10位增量式模拟 - 数字转换器 (ADC) 通过前端多路复用使采样可达8路外部信号。ADC 拥有可配置的输入、参考预分频和 8/9/10位采样分辨率。

4.13 GPIO 任务事件模块 (GPIOTE)

在引脚状态改变时，GPIO TE 模块使端口 0 的GPIO 产生事件，这通过 PPI 系统可用于执行任务。使用 PPI 系统，在系统事件触发时 GPIO 也可被改变状态。

Instance	Number of GPIOs
GPIOTE	4

Table 11 GPIOTE properties

5 例化表

nRF51822 的外设例化表如下表所示

ID	Base address	Peripheral	Instance	Description
0	0x40000000	POWER	POWER	Power Control
0	0x40000000	CLOCK	CLOCK	Clock Control
1	0x40001000	RADIO	RADIO	2.4 GHz Radio
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/ Transmitter
3	0x40003000	SPI	SPIM0	SPI0
3	0x40003000	TWI	TWI0	I2C compatible Two-Wire Interface 0
4	0x40004000	SPI	SPI1	SPI1
4	0x40004000	TWI	TWI1	I2C compatible Two-Wire Interface 1
5				Unused
6	0x40006000	GPIOTE	Port 0 Task and events	GPIO Tasks and events
7	0x40007000	ADC	ADC	Analog-to-Digital Converter
8	0x40008000	TIMER	TIMER0	Timer/Counter 0
9	0x40009000	TIMER	TIMER1	Timer/Counter 1
10	0x4000A000	TIMER	TIMER2	Timer/Counter 2
11	0x4000B000	RTC	RTC0	Real Time Counter 0
12	0x4000C000	TEMP	TEMP	Temperature Sensor
13	0x4000D000	RNG	RNG	Random Number Generator
14	0x4000E000	ECB	ECB	Crypto AES ECB
15	0x4000F000	CCM	CCM	AES Crypto CCM
15	0x4000F000	AAR	AAR	Accelerated Address Resolver
16	0x40010000	WDT	WDT	Watchdog Timer
17	0x40011000	RTC	RTC1	Real Time Counter 1
18	0x40012000	QDEC	QDEC	Quadrature Decoder
19				Unused
20				Reserved as software input
21				Reserved as software input
22				Reserved as software input
23				Reserved as software input
24				Reserved as software input
25				Reserved as software input
26				Unused
27				Unused
28				Unused
29				Unused
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect
NA	0x50000000			General Purpose Input and Output
NA	0x10000000	FICR	FICR	Factory Information Configuration Registers
NA	0x10001000	UICR	UICR	User Information Configuration Registers

Table 12 Peripheral instance reference

注：烧写软件包后，某些外设不可用。参见适用软件包的资源使用

6 极限参数

Maximum ratings are the extreme limits to which nRF51822 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the nRF51822. *Table 13* specifies the absolute maximum ratings for nRF51822.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.6	V
DEC2 ¹			2	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental QFN48 package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		750	V
Environmental WLCSP package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		1	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		500	V
Flash memory				
Endurance		20 000		write/erase cycles
Retention		10 years at 40 °C		
Number of times an address can be written between erase cycles			2	times

- Forced in low voltage mode

Table 13 Absolute maximum ratings



7 工作条件

The operating conditions are the physical parameters that nRF51822 can operate within as defined in *Table 14*.

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage, normal mode		1.8	3.0	3.6	V
VDD	Supply voltage, normal mode, DC/DC converter output voltage 1.9 V		2.1	3.0	3.6	V
VDD	Supply voltage, low voltage mode	1	1.75	1.8	1.95	V
t _{R_VDD}	Supply rise time (0 V to 1.8 V)	2			60	ms
T _A	Operating temperature		-25	25	75	°C

1. DEC2 shall be connected to VDD in this mode.
2. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

Table 14 Operating conditions

Nominal operating conditions (NOC) - conditions under which nRF51822 is operated and tested are the typical (Typ.) values in *Table 14*.

Extreme operating conditions (EOC)

minimum (Min.) and maximum (Max.) values in *Table 14*.

7.1 nRF51822 WLCSP 光灵敏度

nRF51822 WLCSP 封装类型对可见光和近红外光很敏感，这意味着最终产品要对芯片进行合适的屏蔽。印记这面被光吸收膜覆盖，而芯片的侧边和球侧必须用涂料或其它的方式保护。

8 Electrical specifications

This chapter contains electrical specifications for device interfaces and peripherals including radio parameters and current consumption.

The test levels referenced are defined in *Table 15*.

Test level	Description
1	Simulated, calculated, by design (specification limit) or prototype samples tested at NOC
2	Parameters have been verified at Test level 1 and in addition: Prototype samples tested at EOC
3	Parameters have been verified at Test level 2 and in addition: Production samples tested at EOC in accordance with JEDEC47
4	Parameters have been verified at Test level 3 and in addition: Production devices are limit tested at NOC

Table 15 Test level definitions

8.1 Clock sources

8.1.1 16/32 MHz crystal startup

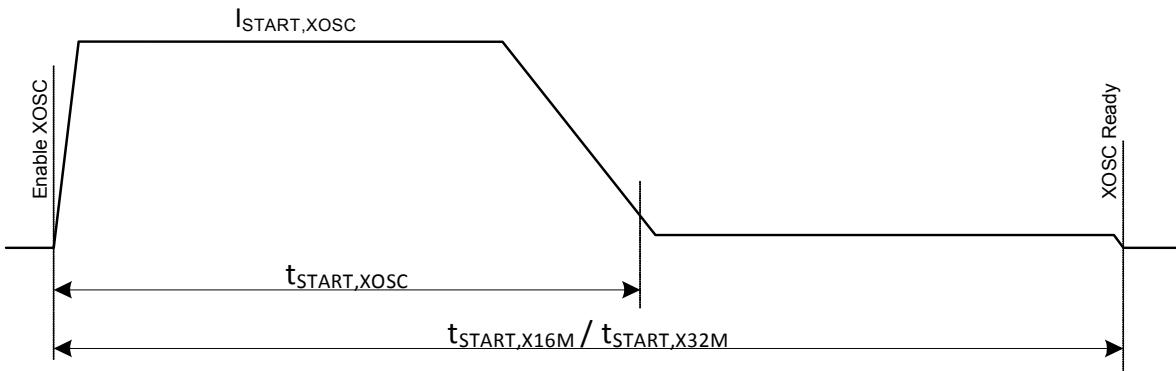


Figure 8 Current drawn at oscillator startup

This figure shows the current drawn by the crystal oscillator (XOSC) at startup. The $t_{START,XOSC}$ period is the time needed for the oscillator to start clocking. The length of $t_{START,XOSC}$ is depending on the crystal specifications.

The period following $t_{START,XOSC}$ to the end of $t_{START,X16M} / t_{START,X32M}$ is fixed. This is the debounce period where the clock stabilizes before it is made available to rest of the system.

8.1.2 16 MHz crystal oscillator (16M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM},X16M}$	Crystal frequency			16		MHz	N/A
$f_{\text{TOL},X16M}$	Frequency tolerance ¹			$\pm 60^2$		ppm	N/A
$f_{\text{TOL},X16M,\text{BLE}}$	Frequency tolerance, <i>Bluetooth</i> low energy applications			$\pm 40^2$		ppm	N/A
$R_{S,X16M}$	Equivalent series resistance	$C_0 \leq 7 \text{ pF}, C_{L,\text{MAX}} \leq 16 \text{ pF}$ $C_0 \leq 5 \text{ pF}, C_{L,\text{MAX}} \leq 12 \text{ pF}$ $C_0 \leq 3 \text{ pF}, C_{L,\text{MAX}} \leq 12 \text{ pF}$	50 75 100	100 150 200		Ω	N/A N/A N/A
$P_{D,X16M}$	Drive level			100		μW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads		4			pF	1
I_{X16M}	Run current for 16 MHz crystal oscillator	With SMD 2520 $C_L = 8 \text{ pF}$	400 ³			μA	1
$I_{\text{STBY},X16M}$	Standby current for 16 MHz crystal oscillator ⁴	With SMD 2520 $C_L = 8 \text{ pF}$	35			μA	1
$I_{\text{START},XOSC}$	Startup current for 16 MHz crystal oscillator		1.1			mA	3
$t_{\text{START},XOSC}$	Startup time for 16 MHz crystal oscillator	With SMD 2520 $C_L = 8 \text{ pF}$	400	500 ⁵		μs	2
$t_{\text{START},X16M}$	Total startup time ($t_{\text{START},XOSC}$ + debounce period) ⁶	With SMD 2520 $C_L = 8 \text{ pF}$	800			μs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See [Table 28 on page 39](#).
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 16M, meaning there is no clock management active (see [Table 24 on page 37](#)). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 16 16 MHz crystal oscillator

8.1.3 32 MHz crystal oscillator (32M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,X32M}$	Crystal frequency		32			MHz	N/A
$f_{TOL,X32M}$	Frequency tolerance ¹			$\pm 60^2$		ppm	N/A
$f_{TOL,X32M,BLE}$	Frequency tolerance, Bluetooth low energy applications			$\pm 40^2$		ppm	N/A
$R_{S,X32M}$	Equivalent series resistance	$C_0 \leq 7 \text{ pF}, C_{L,\text{MAX}} \leq 12 \text{ pF}$ $C_0 \leq 5 \text{ pF}, C_{L,\text{MAX}} \leq 12 \text{ pF}$ $C_0 \leq 3 \text{ pF}, C_{L,\text{MAX}} \leq 9 \text{ pF}$	30 40 50	60 80 100		Ω	N/A N/A N/A
$P_{D,X32M}$	Drive level			100		μW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads		4			pF	1
I_{X32M}	Run current for 32 MHz crystal oscillator	With SMD 2520 $C_L = 8 \text{ pF}$	440 ³			μA	1
$I_{STBY,X32M}$	Standby current for 32 MHz crystal oscillator ⁴	With SMD 2520 $C_L = 8 \text{ pF}$	43			μA	1
$I_{START,XOSC}$	Startup current for 32 MHz crystal oscillator		1.1			mA	3
$t_{START,XOSC}$	Startup time for 32 MHz crystal oscillator	With SMD 2520 $C_L = 8 \text{ pF}$	300	400 ⁵		μs	1
$t_{START,X32M}$	Total startup time ($t_{START,XOSC}$ + debounce period) ⁶	With SMD 2520 $C_L = 8 \text{ pF}$	750			μs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See [Table 28 on page 39](#).
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 32M, meaning there is no clock management active (see [Table 24 on page 37](#)). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 17 32 MHz crystal oscillator

8.1.4 16 MHz RC oscillator (16M RCOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM},\text{RC16M}}$	Nominal frequency		16		MHz	N/A
$f_{\text{TOL},\text{RC16M}}$	Frequency tolerance		± 1	± 5	%	3
I_{RC16M}	Run current for 16 MHz RC oscillator		750 ¹		μA	1
$t_{\text{START},\text{RC16M}}$	Startup time for 16 MHz RC oscillator		2.5	3.5	μs	1
$I_{\text{RC16M, START}}$	Startup current for 16 MHz RC oscillator		400		μA	1

1. This number includes the current used by the automated power and clock management system.

Table 18 16 MHz RC oscillator

8.1.5 32.768 kHz crystal oscillator (32k XOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM},\text{X32k}}$	Crystal frequency		32.768		kHz	N/A
$f_{\text{TOL},\text{X32k}}$	Frequency tolerance		± 250		ppm	N/A
$C_{\text{L},\text{X32k}}$	Load capacitance		12.5		pF	N/A
$C_{\text{0},\text{X32k}}$	Shunt capacitance		2		pF	N/A
$R_{\text{S},\text{X32k}}$	Equivalent series resistance	50	80		$\text{k}\Omega$	N/A
$P_{\text{D},\text{X32k}}$	Drive level		1		μW	N/A
C_{pin}	Input capacitance on XL1 and XL2 pads	4			pF	1
I_{X32k}	Run current for 32.768 kHz crystal oscillator	0.4	1		μA	1
$I_{\text{START},\text{X32k}}$	Startup current for 32.768 kHz crystal oscillator	1.3	1.8		μA	1
$t_{\text{START},\text{X32k}}$	Startup time for 32.768 kHz crystal oscillator	0.3	1		s	2

Table 19 32.768 kHz crystal oscillator

8.1.6 32.768 kHz RC oscillator (32k RCOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,RC32k}}$	Nominal frequency			32.768		kHz	N/A
$f_{\text{TOL,RC32k}}$	Frequency tolerance			± 2		%	3
$f_{\text{TOL,CAL,RC32k}}$	Frequency tolerance for 32.768 kHz RC oscillator after calibration	Calibration interval 4 s at constant temperature			± 250	ppm	1
I_{RC32k}	Run current for 32.768 kHz RC oscillator		0.5	0.8	1.1	μA	1
$t_{\text{START,RC32k}}$	Startup time for 32.768 kHz RC oscillator			100		μs	1

Table 20 32.768 kHz RC oscillator

8.1.7 32.768 kHz Synthesized oscillator (32k SYNT)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{\text{NOM,SYNT32k}}$	Nominal frequency			32.768		kHz	1
$f_{\text{TOL,SYNT}}$	Frequency tolerance			$f_{\text{TOL,XO16M}} \pm 8$		ppm	1
I_{SYNT32k}	Run and startup current for 32.768 kHz Synthesized clock			40		μA	1
$t_{\text{START,SYNT32k}}$	Startup time for 32.768 kHz Synthesized clock			100		μs	1

Table 21 32.768 kHz Synthesized oscillator

8.2 Power management

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
VPOF	Nominal power level warning thresholds (falling supply voltage)	Accuracy as defined by V_{TOL}	2.1 2.3 2.5 2.7			V	N/A
V_{TOL}	Threshold voltage tolerance			± 5	%	3	
V_{HYST}	Threshold voltage hysteresis		2.1 V 2.3 V 2.5 V 2.7 V	46 62 79 100		mV	3

Table 22 Power Fail Comparator

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{POR, 1\mu s}$	Time Reset is active from VDD reaches 1.7 V with 1 μs rise time		0.2	2.7		ms	1
$t_{POR, 50 ms}$	Time Reset is active from VDD reaches 1.7 V with 50 ms rise time		6.5	29		ms	1
I_{OFF}	Current in SYSTEM-OFF, no RAM retention			0.4		μA	1
$I_{OFF, 8 k}$	Current in SYSTEM-OFF mode 8 kB SRAM retention			0.6		μA	1
$I_{OFF, 16 k}$	Current in SYSTEM-OFF mode 16 kB SRAM retention			0.8		μA	1
I_{OFF2ON}	OFF to CPU execute transition current			400		μA	1
t_{OFF2ON}	OFF to CPU execute		9.6	10.6		μs	1
I_{ON}	SYSTEM-ON base current		2.3			μA	2
I_{1V2}	Current drawn by 1V2 regulator		290			μA	2
t_{1V2}	Startup time for 1V2 regulator		2.3			μs	1
I_{1V7}	Current drawn by 1V7 regulator		90			μA	2
t_{1V7}	Startup time for 1V7 regulator		2	3.6		μs	1
$I_{1V2RC16}$	Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time	See <i>Table 24</i>		830 ¹		μA	1

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{1V2X016}$	Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time	See <i>Table 24</i>	740 ¹			μA	1
I_{DCDC}	Current drawn by DC/DC converter		300			μA	1
F_{DCDC}	DC/DC converter current conversion factor		0.65 ²		1.2 ²		1
$t_{START,DCDC}$	DC/DC converter startup time		10 ²	425 ²		μs	1

1. This number includes the current used by the automated power and clock management system.
2. F_{DCDC} and $t_{START,DCDC}$ will vary depending on VDD and device internal current consumption (I_{DD}). The range of values stated in this specification is for VDD between 2.1 V and 3.6 V, and I_{DD} between 4 mA and 20 mA. Please refer to the *nRF51 Series Reference Manual*, v1.1 or later, for a method to calculate these numbers based on VDD and I_{DD} .

Table 23 Power management

8.3 Block resource requirements

Block	ID	Required resources			Comment
		1V2+16M	16M	32k	
Radio	1	x			Requires 16M XOSC
UART	2	x			
SPI	3, 4	x			
2W	3, 4	x			
GPIOTE	6		x		Only in input mode
ADC	7	x			Requires 16M XOSC
TIMER	8, 9, 10		x		
RTC	11, 17		x	x	16M will only be requested if the 32.768 kHz clock is synthesized from the 16 MHz clock
TEMP	12	x			Requires 16M XOSC
RNG	13	x			
ECB	14	x	x		
WDT	16			x	
QDEC	18	x			
CPU		x			

Table 24 Clock and power requirements for different blocks

8.4 CPU

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I _{CPU, Flash}	Run current at 16 MHz, Executing code from flash memory		4.4 ¹		mA	2
I _{CPU, RAM}	Run current at 16 MHz, Executing code from RAM		2.4 ²		mA	1
I _{START, CPU}	CPU startup current		600		µA	1
t _{START, CPU}	IDLE to CPU execute	0	3		µs	1

1. Includes CPU, flash, 1V2, 1V7, RC16M
2. Includes CPU, RAM, 1V2, RC16M
3. t_{1V2} if 1V2 regulator is not running already

Table 25 CPU specifications

8.5 Radio transceiver

8.5.1 General radio characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
f_{OP}	Operating frequencies	1 MHz channel spacing	2400		2483	MHz	N/A
PLL_{res}	PLL programming resolution			1		MHz	N/A
Δf_{250}	Frequency deviation @ 250 kbps			± 170		kHz	2
Δf_{1M}	Frequency deviation @ 1 Mbps			± 170		kHz	2
Δf_{2M}	Frequency deviation @ 2 Mbps			± 320		kHz	2
Δf_{BLE}	Frequency deviation @ BLE		± 225	± 250	± 275	kHz	4
bps_{FSK}	On-air data rate		250		2000	kbps	N/A

Table 26 General radio characteristics

8.5.2 Radio current consumption

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TX,+4\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = +4 \text{ dBm}$	1		16		mA	4
$I_{TX,0\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = 0 \text{ dBm}$	1		10.5		mA	4
$I_{TX,-4\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -4 \text{ dBm}$	1		8		mA	2
$I_{TX,-8\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -8 \text{ dBm}$	1		7		mA	2
$I_{TX,-12\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -12 \text{ dBm}$	1		6.5		mA	2
$I_{TX,-16\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -16 \text{ dBm}$	1		6		mA	2
$I_{TX,-20\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -20 \text{ dBm}$	1		5.5		mA	2
$I_{TX,-30\text{dBm}}$	TX only run current @ $P_{\text{OUT}} = -30 \text{ dBm}$	1		5.5		mA	2
$I_{\text{START,TX}}$	TX startup current	2		7		mA	1
$I_{\text{RX},250}$	RX only run current @ 250 kbps			12.6		mA	1
$I_{\text{RX},1M}$	RX only run current @ 1 Mbps			13		mA	4
$I_{\text{RX},2M}$	RX only run current @ 2 Mbps			13.4		mA	1
$I_{\text{START,RX}}$	RX startup current	3		8.7		mA	1

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps
2. Average current consumption (at 0 dBm TX output power) for TX startup (130 μs), and when changing mode from RX to TX (130 μs).
3. Average current consumption for RX startup (130 μs), and when changing mode from TX to RX (130 μs).

Table 27 Radio current consumption

8.5.3 Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units	Test level
P _{RF}	Maximum output power		4		dBm	4
P _{RFC}	RF power control range	20	24		dB	2
PRFCR	RF power accuracy			±4	dB	1
P _{WHISP}	RF power whisper mode		-30		dBm	2
P _{BW2}	20 dB bandwidth for modulated carrier (2 Mbps)	1800	2000		kHz	2
P _{BW1}	20 dB bandwidth for modulated carrier (1 Mbps)	950	1100		kHz	2
P _{BW250}	20 dB bandwidth for modulated carrier (250 kbps)	700	800		kHz	2
P _{RF1.2}	1 st Adjacent Channel Transmit Power 2 MHz (2 Mbps)			-20	dBc	2
P _{RF2.2}	2 nd Adjacent Channel Transmit Power 4 MHz (2 Mbps)			-45	dBc	2
P _{RF1.1}	1 st Adjacent Channel Transmit Power 1 MHz (1 Mbps)			-20	dBc	2
P _{RF2.1}	2 nd Adjacent Channel Transmit Power 2 MHz (1 Mbps)			-40	dBc	2
P _{RF1.250}	1 st Adjacent Channel Transmit Power 1 MHz (250 kbps)			-25	dBc	2
P _{RF2.250}	2 nd Adjacent Channel Transmit Power 2 MHz (250 kbps)			-40	dBc	2
t _{TX,30}	Maximum consecutive transmission time, f _{TOL} < ±30 ppm			16	ms	1
t _{TX,60}	Maximum consecutive transmission time, f _{TOL} < ±60 ppm			4	ms	1

Table 28 Transmitter specification

8.5.4 Receiver specification

Symbol	Description	Min.	Typ.	Max.	Units	Test level
Receiver operation						
PRX _{MAX}	Maximum received signal strength at < 0.1% PER	0			dBm	1
PRX _{SENS,2M}	Sensitivity (0.1% BER) @ 2 Mbps	-85			dBm	2
PRX _{SENS,1M}	Sensitivity (0.1% BER) @ 1 Mbps	-90			dBm	2
PRX _{SENS,250k}	Sensitivity (0.1% BER) @ 250 kbps	-96			dBm	2
P _{SENS} IT 1 Mbps BLE	Receiver sensitivity: Ideal transmitter	-93			dBm	2
P _{SENS} DT 1 Mbps BLE	Receiver sensitivity: Dirty transmitter	-91			dBm	2
RX selectivity - modulated interfering signal¹						
2 Mbps						
C/I _{CO}	C/I co-channel	12			dB	2
C/I _{1ST}	1 st ACS, C/I 2 MHz	-4			dB	2
C/I _{2ND}	2 nd ACS, C/I 4 MHz	-24			dB	2
C/I _{3RD}	3 rd ACS, C/I 6 MHz	-28			dB	2
C/I _{6th}	6 th ACS, C/I 12 MHz	-44			dB	2
C/I _{Nth}	N th ACS, C/I f _i > 25 MHz	-50			dB	2
1 Mbps						
C/I _{CO}	C/I co-channel (1 Mbps)	12			dB	2
C/I _{1ST}	1 st ACS, C/I 1 MHz	4			dB	2
C/I _{2ND}	2 nd ACS, C/I 2 MHz	-24			dB	2
C/I _{3RD}	3 rd ACS, C/I 3 MHz	-30			dB	2
C/I _{6th}	6 th ACS, C/I 6 MHz	-40			dB	2
C/I _{12th}	12 th ACS, C/I 12 MHz	-50			dB	2
C/I _{Nth}	N th ACS, C/I f _i > 25 MHz	-53			dB	2

Symbol	Description	Min.	Typ.	Max.	Units	Test level
250 kbps						
C/I _{CO}	C/I co-channel	4			dB	2
C/I _{1ST}	1 st ACS, C/I 1 MHz	-10			dB	2
C/I _{2ND}	2 nd ACS, C/I 2 MHz	-34			dB	2
C/I _{3RD}	3 rd ACS, C/I 3 MHz	-39			dB	2
C/I _{6th}	6 th ACS, C/I $f_i > 6$ MHz	-50			dB	2
C/I _{12th}	12 th ACS, C/I 12 MHz	-55			dB	2
C/I _{Nth}	N th ACS, C/I $f_i > 25$ MHz	-60			dB	2
Bluetooth Low Energy RX selectivity						
C/I _{CO}	C/I co-channel	10			dB	2
C/I _{1ST}	1 st ACS, C/I 1 MHz	1			dB	2
C/I _{2ND}	2 nd ACS, C/I 2 MHz	-25			dB	2
C/I _{3+N}	ACS, C/I (3+n) MHz offset [n = 0, 1, 2, ...]	-51			dB	2
C/I _{Image}	Image blocking level	-30			dB	2
C/I _{Image±1MHz}	Adjacent channel to image blocking level (± 1 MHz)	-31			dB	2
RX intermodulation²						
P_IMD _{2Mbps}	IMD performance, 2 Mbps, 3rd, 4th and 5th offset channel	-41			dBm	2
P_IMD _{1Mbps}	IMD performance, 1 Mbps, 3rd, 4th and 5th offset channel	-40			dBm	2
P_IMD _{250kbps}	IMD performance, 250 kbps, 3rd, 4th and 5th offset channel	-36			dBm	2
P_IMD _{BLE}	IMD performance, 1 Mbps BLE, 3rd, 4th and 5th offset channel	-39			dBm	2

1. Wanted signal level at $P_{IN} = -67$ dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals $BER = 0.1\%$ is presented.
2. Wanted signal level at $P_{IN} = -64$ dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals $BER = 0.1\%$ is presented.

Table 29 Receiver specification

8.5.5 Radio timing parameters

Symbol	Description	250 k	1 M	2 M	BLE	Jitter	Units
t_{TXEN}	Time between TXEN task and READY event	132	132	132	140	0	μs
$t_{TxDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX	10	4	3	4	1	μs
t_{RXEN}	Time between the RXEN task and READY event	130	130	130	138	0	μs
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX	0	0	0	0	1	μs
$t_{TXCHAIN}$	TX chain delay	5	1	0.5	1	0	μs
$t_{RXCHAIN}$	RX chain delay	12	2	2.5	3	0	μs

Table 30 Radio timing

8.6 RSSI specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
RSSI_{ACC}	RSSI accuracy	Valid between: -50 dBm and -80 dBm			± 6	dB	2
$\text{RSSI}_{\text{RESOLUTION}}$	RSSI resolution			1		dB	1
$\text{RSSI}_{\text{PERIOD}}$	Sample period		8.8			μs	1
$\text{RSSI}_{\text{CURRENT}}$	Current consumption in addition to I_{RX}			250		μA	1

Table 31 RSSI specifications

8.7 UART specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{UART1M}	Run current @ max baud rate		230			μA	1
I_{UART115k}	Run current @ 115200 bps		220			μA	1
I_{UART1k2}	Run current @ 1200 bps		210			μA	1
f_{UART}	Baud rate for UART		1.2		921.6	kbps	N/A

Table 32 UART specifications

8.8 SPI specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{SPI125K}$	Run current for SPI master @ 125 kbps		180		μA	1
I_{SPI8M}	Run current for SPI master @ 8 Mbps		200		μA	1
f_{SPI}	Bit rates for SPI	0.125	8	Mbps		N/A

Table 33 SPI specifications

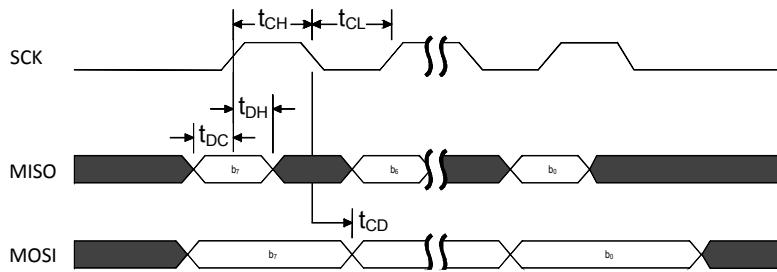


Figure 9 SPI timing diagram, one byte transmission, SPI mode 0

Symbol	Description	Note	Min.	Max.	Units	Test level
t_{DC}	Data to SCK setup		10		ns	1
t_{DH}	SCK to Data hold		10		ns	1
t_{CD}	SCK to Data valid	$C_{LOAD} = 0 \text{ pF}$ $C_{LOAD} = 5 \text{ pF}$ $C_{LOAD} = 10 \text{ pF}$ $C_{LOAD} = 35 \text{ pF}$		60 66 68 78	ns	1
t_{CL}	SCK Low time		40		ns	1
t_{CH}	SCK High time		40		ns	1
f_{SCK}	SCK Frequency		0.125	8	MHz	1
t_R, t_F	SCK Rise and Fall time			100	ns	1

Table 34 SPI timing parameters

8.9 TWI specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{2W100K}	Run current for TWI @ 100 kbps		380		μA	1
I_{2W400K}	Run current for TWI @ 400 kbps		400		μA	1
f_{2W}	Bit rates for TWI	100		400	kbps	N/A

Table 35 TWI specifications

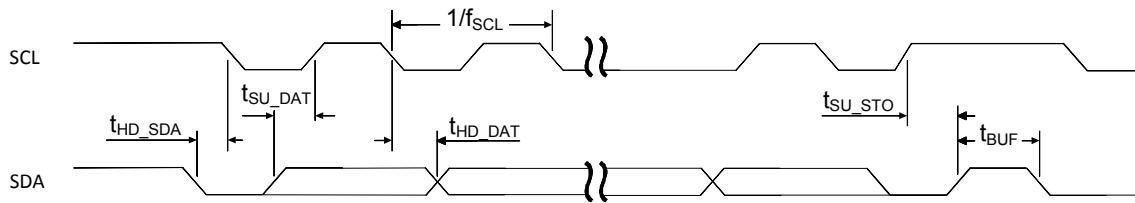


Figure 10 SCL/SDA timing

Symbol	Description	Standard		Fast		Units	Test level
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency	100		400		kHz	1
t_{HD_STA}	Hold time for START and repeated START condition	5200		1300		ns	1
t_{SU_DAT}	Data setup time before positive edge on SCL	300		300		ns	1
t_{HD_DAT}	Data hold time after negative edge on SCL	300		300		ns	1
t_{SU_STO}	Setup time from SCL goes high to STOP condition	5200		1300		ns	1
t_{BUF}	Bus free time between STOP and START conditions	4700		1300		ns	1

Table 36 TWI timing parameters

8.10 GPIOTE specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I _{GPIOTE,IN}	Run current with GPIOTE active in Input mode		100		µA	1
I _{GPIOTE,OUT}	Run current with GPIOTE active in Output mode		0.1		µA	1

Table 37 GPIOTE specifications

Note: Setting up one or more GPIO DETECT signals to generate PORT EVENT, that again could be used either as a wakeup source or to give an interrupt, will not lead to an increase of the current consumption.

8.11 Analog-to-Digital Converter (ADC) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
DNL _{10b}	Differential non-linearity (10 bit mode)			< 1		LSB	2
INL _{10b}	Integral non-linearity (10 bit mode)			2		LSB	2
V _{OS}	Offset error		-2		+2	%	2
e _G	Gain error		-2		+2	%	2
V _{REF_INT}	Internal reference voltage		-1.5	1.20 V	+1.5	%	2
T _{C_{REF_INT}}	Internal reference voltage drift		-200		+200	ppm/°C	2
V _{REF_EXT}	External reference voltage		0.83	1.2	1.3	V	1
t _{ADC10b}	Time required to convert a single sample in 10 bit mode			68		µs	1
t _{ADC9b}	Time required to convert a single sample in 9 bit mode			36		µs	1
t _{ADC8b}	Time required to convert a single sample in 8 bit mode			20		µs	1
I _{ADC}	Current drawn by ADC during conversion			290		µA	1
ADC_ERR_1V8				3		LSB	2
ADC_ERR_2V2	Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V and 3.4 V	Internal reference, input from VDD/3 10 bit setting	2			LSB	2
ADC_ERR_2V6			1			LSB	2
ADC_ERR_3V0			1			LSB	2
ADC_ERR_3V4			1			LSB	2

Table 38 Analog-to-Digital Converter (ADC) specifications

8.12 Timer specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{\text{TIMER}0/1/2,16M}$	Timer @16 MHz run current	24 bit		258		μA	1
		16 bit		178		μA	1
$t_{\text{TIMER,START}}$	Time from START task is given until timer start counting			0.25		μs	1

Table 39 Timer specifications

8.13 RTC

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{RTC}	Timer (LFCLK source)		0.2		μA	1

Table 40 RTC

8.14 Temperature sensor

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{TEMP}	Run current for Temperature sensor		185		μA	1
t_{TEMP}	Time required for temperature measurement		35		μs	1
T_{RANGE}	Temperature sensor range	-25		75	$^{\circ}\text{C}$	N/A
T_{ACC}	Temperature sensor accuracy	-4		+4	$^{\circ}\text{C}$	N/A
T_{RES}	Temperature sensor resolution		0.25		$^{\circ}\text{C}$	1

Table 41 Temperature sensor

8.15 Random Number Generator (RNG) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I _{RNG}	Run current @ 16 MHz			300		μA	1
t _{RNG,RAW}	Run time per byte in RAW mode	Uniform distribution of 0 and 1 is not guaranteed		167		μs	1
t _{RNG,UNI}	Run time per byte in Uniform mode	Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed		677		μs	1

Table 42 Random Number Generator (RNG) specifications

8.16 ECB/CCM/AAR specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I _{CRYPTO}	Run current for Crypto in all modes		400		μA	1
t _{CRYPTO}	Run time per 16 byte block in all modes		8.5		μs	1

Table 43 ECB/CCM/AAR specifications

8.17 Watch Dog Timer specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I _{WDT}	Run current for watch dog timer		1		μA	1
t _{WDT}	Time out interval, watch dog timer	30 μs		36 hrs		1

Table 44 Watch Dog Timer specifications

8.18 Quadrature Decoder specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{QDEC}				250		μA	1
t_{SAMPLE}	Time between sampling signals from quadrature decoder		128		16384	μs	N/A
t_{LED}	Time from LED is turned on to signals are sampled	Only valid for optical sensors	0		511	μs	N/A

Table 45 Quadrature Decoder specifications

8.19 NVMC specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{ERASEALL}$	Erase flash memory		21			ms	1
$t_{PAGEERASE}$	Erase page in flash memory		21			ms	1
t_{WRITE}^1	Write one word to flash memory		22	43		μs	1

1. Nominal value applies when writing 32 words or more. Maximum value applies when writing a single word.

Note: The CPU will be halted for the duration of NVMC operations.

Table 46 NVMC specifications

8.20 General purpose I/O (GPIO) specification

Symbol	Parameter (condition)	Note	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7 VDD		VDD	V
V_{IL}	Input low voltage		VSS		0.3 VDD	V
V_{OH}	Output high voltage (std. drive, 0.5 mA)		VDD-0.3		VDD	V
V_{OH}	Output high voltage (high-drive, 5 mA)	¹	VDD-0.3		VDD	V
V_{OL}	Output low voltage (std. drive, 0.5 mA)		VSS		0.3	V
V_{OL}	Output low voltage (high-drive, 5 mA)		VSS		0.3	V
R_{PU}	Pull-up resistance		11	13	16	k Ω
R_{PD}	Pull-down resistance		11	13	16	k Ω

1. Maximum number of pins with 5 mA high drive is 3.

Table 47 General purpose I/O (GPIO) specification

9 Mechanical specifications

9.1 QFN48 package

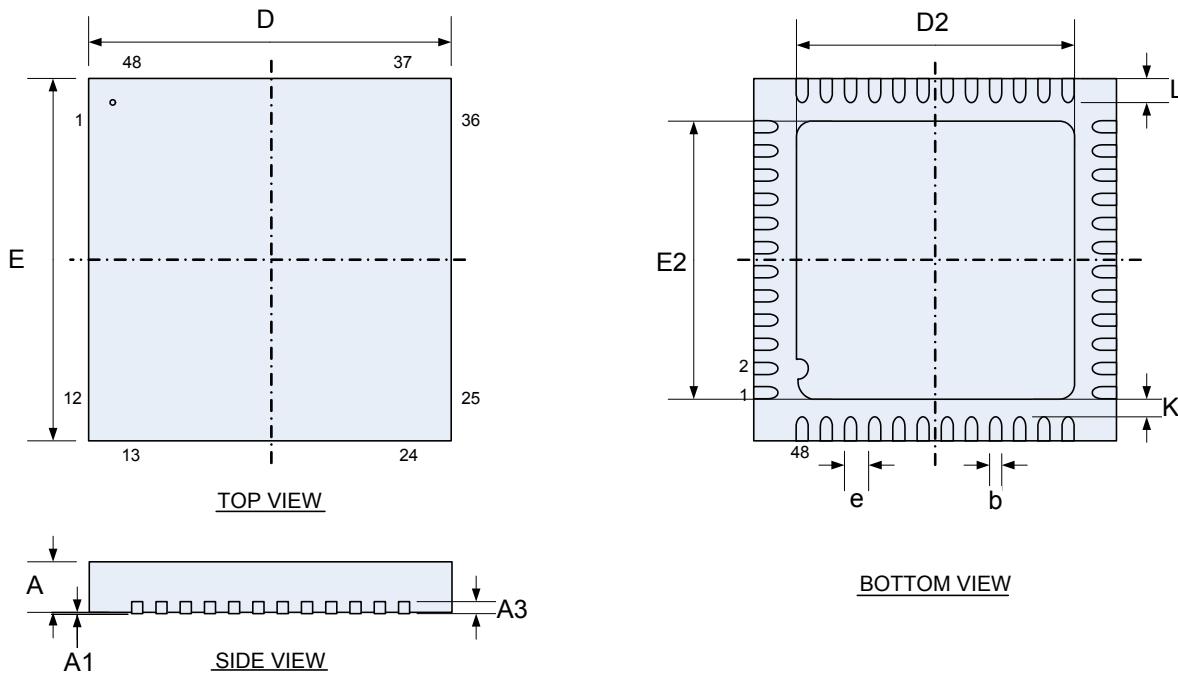


Figure 11 QFN48 6x6 mm package

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
QFN48 (6 x 6)	0.80	0.00		0.15		4.50		0.20	0.35	Min.
	0.85	0.02	0.2	0.20	6.0	4.60	0.4		0.40	Nom.
	0.90	0.05		0.25		4.70			0.45	Max.

Table 48 QFN48 dimensions in millimeters

9.2 WLCSP package

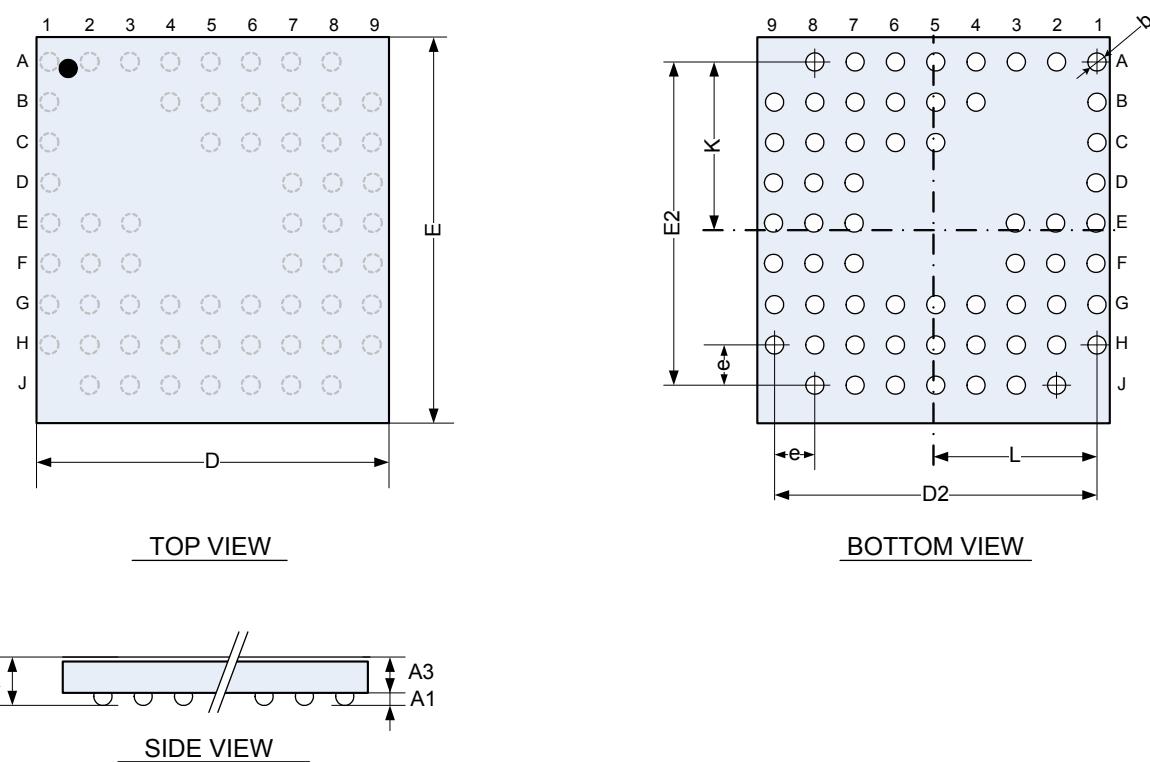


Figure 12 WLCSP package

Package	A	A1	A3	b	D	E	D2	E2	e	K	L	
WLCSP		0.12	0.31	0.16	3.45	3.78						Min.
	0.50	0.15	0.33	0.20	3.50	3.83	3.20	3.20	0.4	1.66	1.61	Nom.
	0.55	0.18	0.35	0.24	3.55	3.88						Max.

Table 49 WLCSP package dimensions in millimeters

10 Ordering information

10.1 Package marking

N	5	1	8	2	2
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Table 50 Package marking

10.2 Order code

n	R	F	5	1	8	2	2	-	<P	P>	<V	V>	-	<C	C>
---	---	---	---	---	---	---	---	---	----	----	----	----	---	----	----

Table 51 Order code

10.3 Abbreviations

Abbreviation	Definition and Implemented Codes
N51/nRF51	nRF51 series product
822	Part code
<PP>	Package code
<VV>	Variant code
<H><P>	Build code H - Hardware version code P - Production version code (production site, etc.)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 52 Abbreviations

10.4 Code ranges and values

<PP>	Packet	Size (mm)	Pin/Ball Count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CE	WLCSP	3.50 x 3.83	62	0.4

Table 53 Package codes

<VV>	Flash (kB)	RAM (kB)	DC/DC Bond-out
AA	256	16	YES
AB	128	16	YES

Table 54 Variant codes

<H>	Description
[A..Z]	Hardware version/revision identifier (incremental)

Table 55 Hardware version codes

<P>	Description
[0..9]	Production device identifier (incremental)
[A..T]	Engineering device identifier (incremental)

Table 56 Production version codes

<YY>	Description
[12..99]	Production year: 2012 to 2099

Table 57 Year codes

<WW>	Description
[1..52]	Week of production

Table 58 Week codes

<LL>	Description
[AA..ZZ]	Wafer production lot identifier

Table 59 Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel
T	Tray

Table 60 Container codes

10.5 Product options

10.5.1 nRF ICs

Order code	MOQ ¹
nRF51822-QFAA-R7	
nRF51822-QFAB-R7	1000
nRF51822-QFAA-R	
nRF51822-QFAB-R	
nRF51822-CEAA-R	3000
nRF51822-QFAA-T	
nRF51822-QFAB-T	490

1. Minimum Order Quantity

Table 61 Order code

10.5.2 Development tools

Order code	Description
nRF51822-DK ¹	nRF51822 Development Kit ²
nRF51822-EK ¹	nRF51822 Evaluation Kit
nRF6700	nRFgo Starter Kit

1. Uses the nRF51822-QFAA version of the chip
2. Requires nRF6700 nRFgo Starter Kit

Table 62 Development tools

11 参考电路

下面参考布局中， X1 和 XC1/XC2 间的电容 C_pcb 估算为每个 0.5pF 。

11.1 PCB指导

为获得良好的 RF 性能，一个优秀设计的PCB是必要的。差的布局可能会导致性能或功能丧失。
有关IC及其周围器件、网络匹配的合格布局资料可从网下载：www.nordicsemi.com 。

为获得最佳性能，推荐 PCB 至少为两层，其中一层为地层。

在超过两层的 PCB 中，在内层放置一个保留区来减少影响 RF 性能的寄生电容，保留区位于天线下面，与电路（ANT1、ANT2、VDD_PA间的器件和天线）匹配。

直流电源应该尽量靠近 VDD 引脚，连接一个高性能的 RF 电容。推荐的退耦电容值参考原理图。芯片的供电需要滤波，布线与数字电路的供电应相互隔离。

PCB上应避免长的电源线。所有的地线、VDD连线和VDD的旁路电容必须尽量靠近芯片。对于有顶层 RF 地平面的 PCB ， VSS 脚必须与地平面直接相连。对于底层为地平面的 PCB ，最好的设计是过孔尽量靠近 VSS 焊盘。每个 VSS 引脚应该有一个尽量小的过孔。

频繁切换的数字数据或控制信号不应该靠近晶体或电源线。数字信号输出线的负载电容应尽量小，避免无线电干扰。

11.2 QFN48 封装

QFN48 封装参考电路的文件，包括 Altium Designer 文件，PCB 布局文件和 PCB 产品文件可以从 nRF51822 产品页下载：www.nordicsemi.com .

11.2.1 nRF51822 QFN48 使用内部 LDO 稳压器的原理图

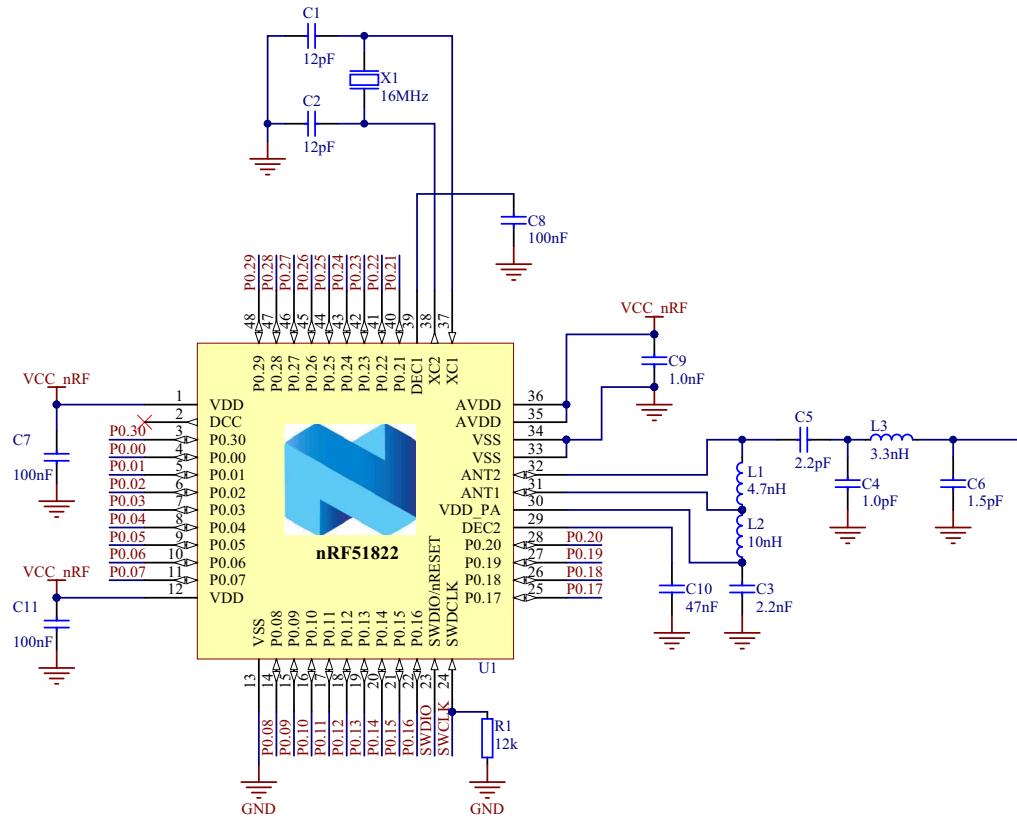


Figure 13 nRF51822 QFN48 with internal LDO regulator

11.2.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C4	1.0 pF	Capacitor, NP0, ± 0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ± 0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ± 0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
L1	4.7 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 nH	High frequency chip inductor $\pm 5\%$	0402
L3	3.3 nH	High frequency chip inductor $\pm 5\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 63 nRF51822 QFN48 with internal LDO regulator

11.2.2 nRF51822 QFN48 1.8V 低电压模式的原理图

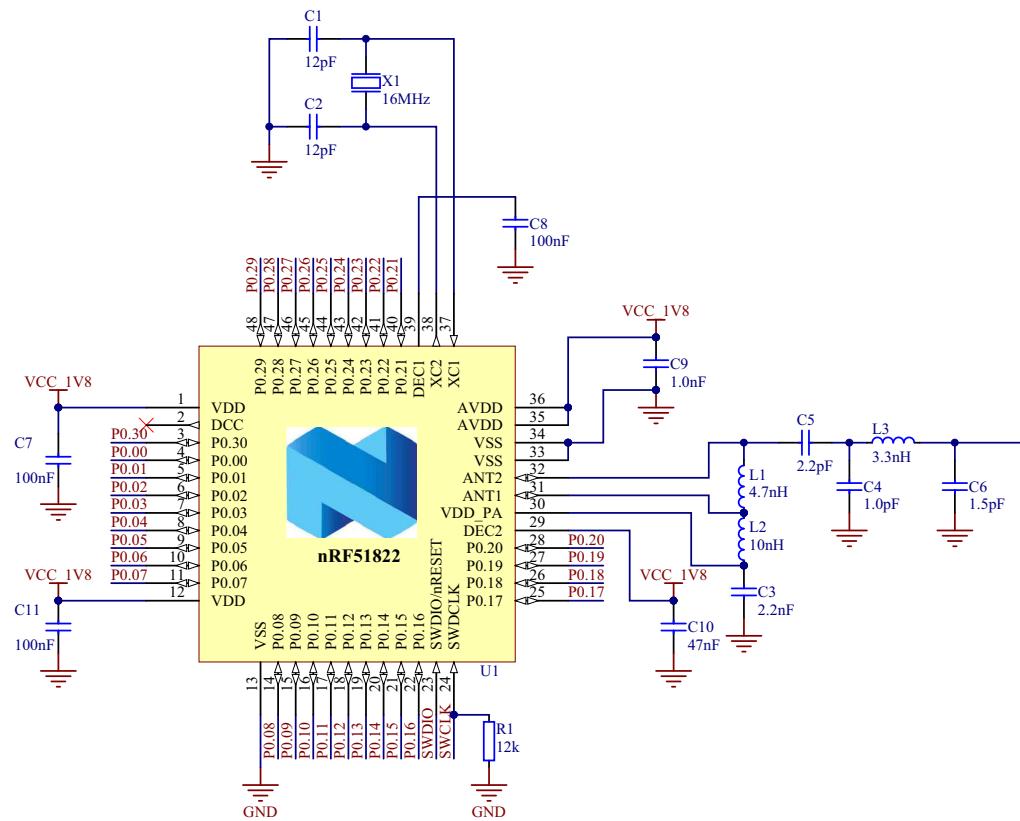


Figure 14 nRF51822 QFN48 with 1.8 V low voltage mode

11.2.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, $\pm 2\%$	0402
C3	2.2 nF	Capacitor, X7R, $\pm 10\%$	0402
C4	1.0 pF	Capacitor, NP0, ± 0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ± 0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ± 0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C9	1.0 nF	Capacitor, X7R, $\pm 10\%$	0402
C10	47 nF	Capacitor, X7R, $\pm 10\%$	0402
L1	4.7 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 nH	High frequency chip inductor $\pm 5\%$	0402
L3	3.3 nH	High frequency chip inductor $\pm 5\%$	0402
R1	12 k Ω	Resistor, $\pm 5\%$, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ± 40 ppm	2.5 x 2.0 mm

Table 64 nRF51822 QFN48 with 1.8 V low voltage mode

11.2.3 nRF51822 QFN48 使用内部 DC/DC 转换器的原理图

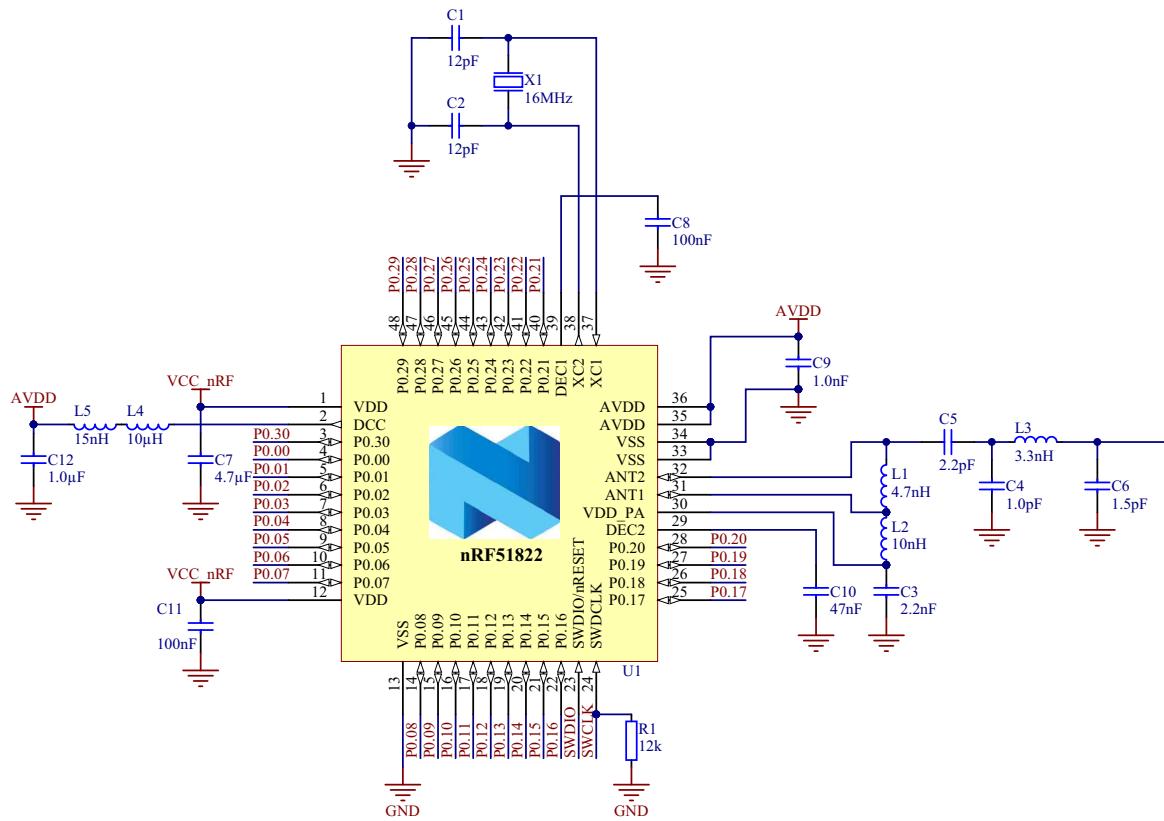


Figure 15 nRF51822 QFN48 with DC/DC converter

11.2.3.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
L4	10 µH	Chip inductor, $I_{DC,min} = 50 \text{ mA}$, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51822-QFAA nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 65 nRF51822 QFN48 with DC/DC converter

11.3 WLCSP 封装

WLCSP 封装参考电路的文件，包括 Altium Designer 文件，PCB 布局文件和 PCB 产品文件可以从 nRF51822 产品页下载：www.nordicsemi.com .

11.3.1 nRF51822 WLCSP 使用内部 LDO 稳压器的原理图

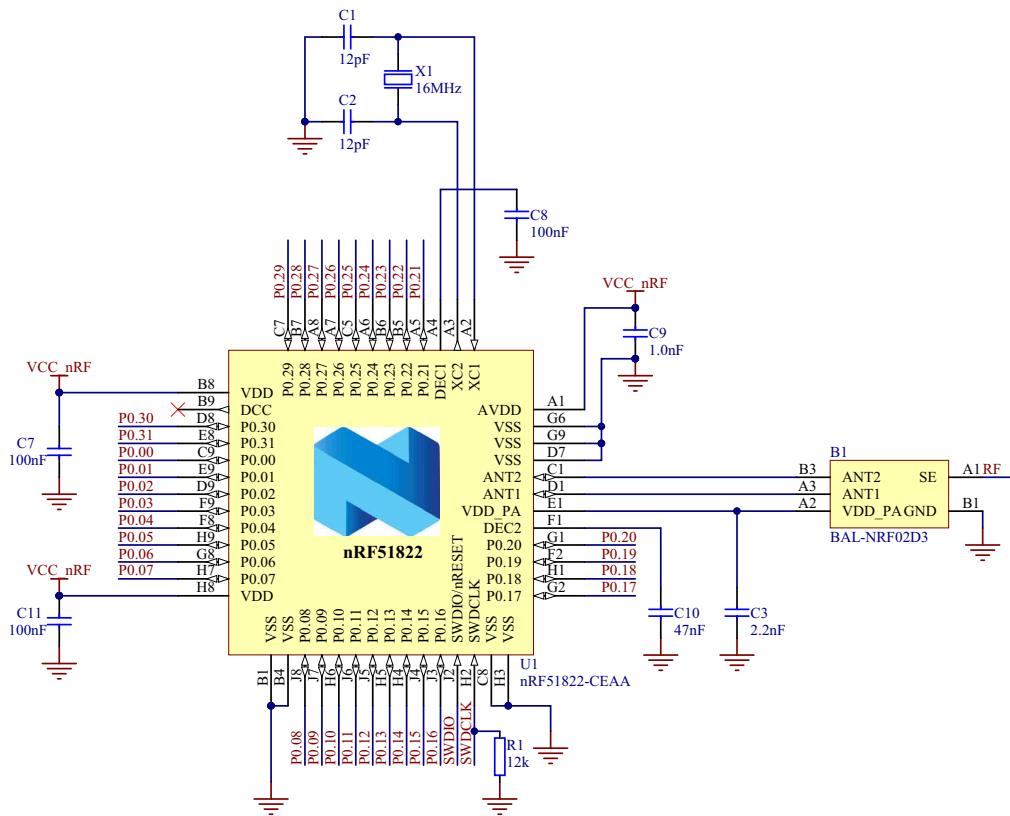


Figure 16 nRF51822 WLCSP with internal LDO regulator

11.3.1.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 66 nRF51822 WLCSP with internal LDO regulator

11.3.2 nRF51822 WLCSP 1.8V 低电压模式的原理图

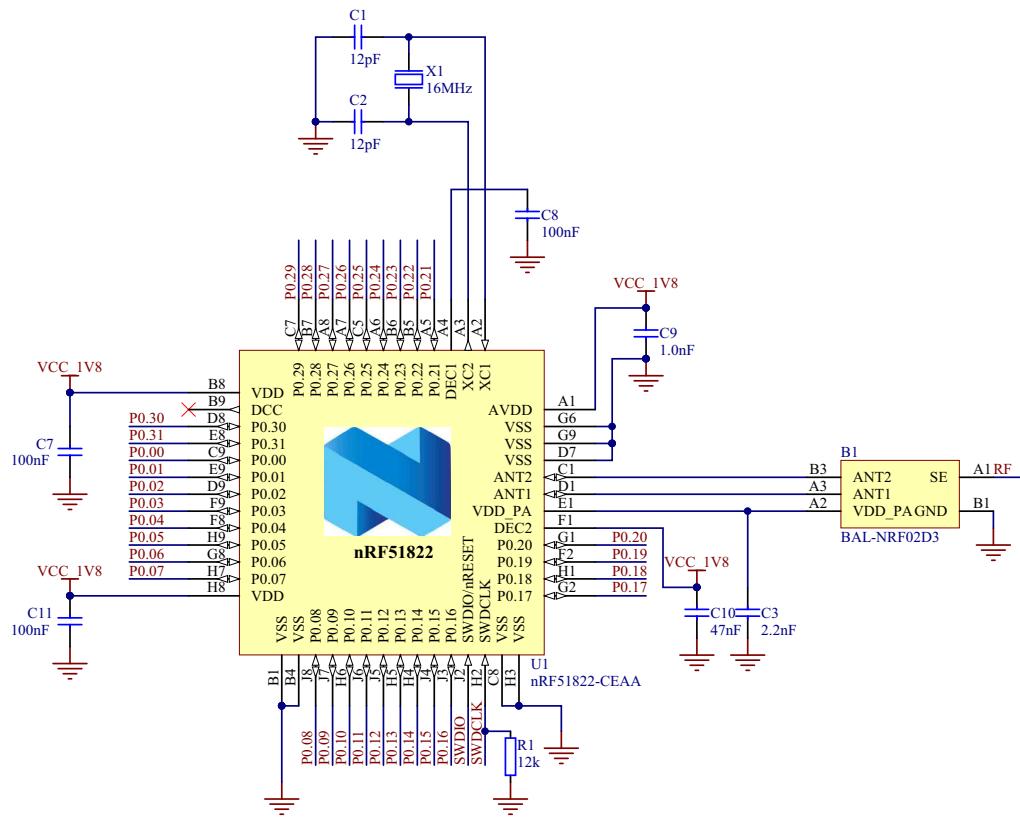


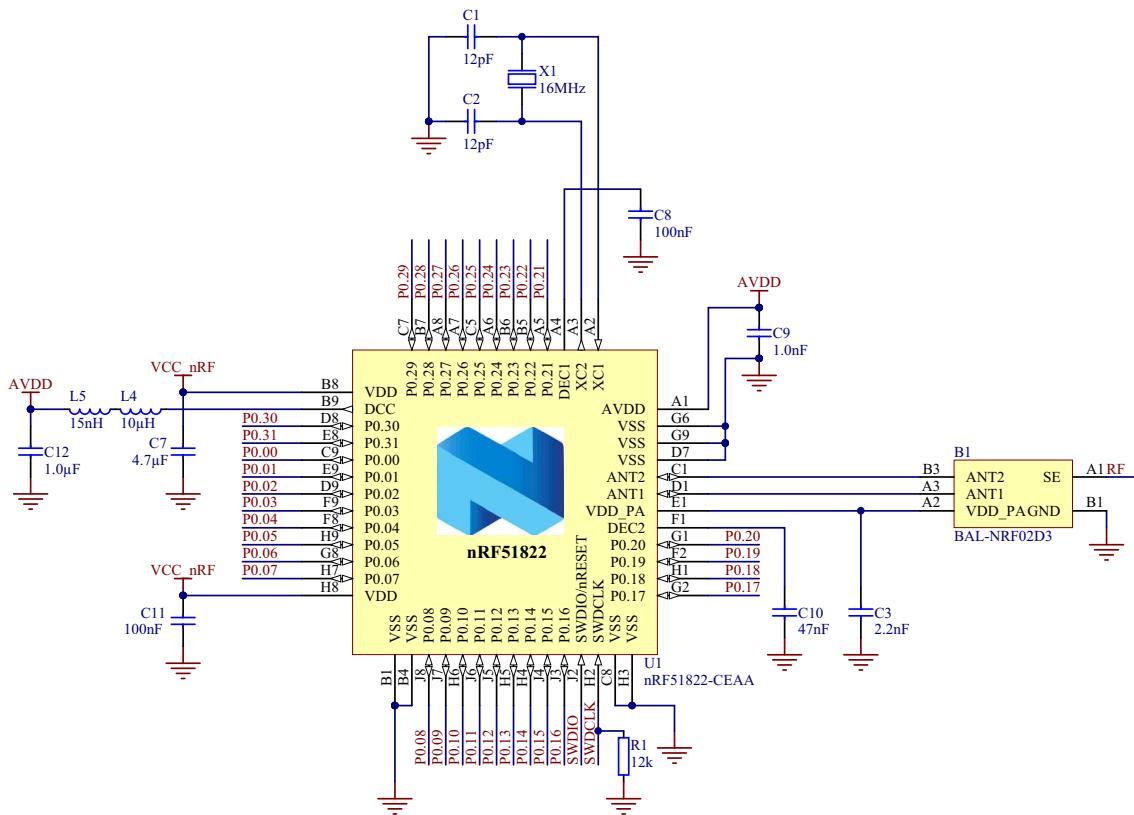
Figure 17 nRF51822 WLCSP with 1.8 V low voltage mode

11.3.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 67 nRF51822 WLCSP with 1.8 V low voltage mode

11.3.3 nRF51822 WLCSP 使用内部 DC/DC 转换器的原理图



11.3.3.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-NRF02D3
C1, C2	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L4	10 µH	Chip inductor, $I_{DC,min} = 50 \text{ mA}, \pm 20\%$	0603
L5	15 nH	High frequency chip inductor ±10%	0402
R1	12 kΩ	Resistor, ±5%, 0.063 W	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm

Table 68 nRF51822 WLCSP with DC/DC converter

12 Glossary

Term	Description
EOC	Extreme Operating Conditions
GFSK	Gaussian Frequency-Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial Scientific Medical
MOQ	Minimum Order Quantity
NOC	Nominal Operating Conditions
NVMC	Non-Volatile Memory Controller
QDEC	Quadrature Decoder
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Radio Signal Strength Indicator
SPI	Serial Peripheral Interface
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver Transmitter
WLCSP	Wafer Level Chip Scale Packet

Table 69 Glossary