Homework 2

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Chap 2

2.40 Write the decimal equivalents for these IEEE floating point numbers.

a. 0 10000000 00000000000000000000000
b. 1 10000011 00010000000000000000000
c. 0 11111111 00000000000000000000000
d. 1 10000000 10010000000000000000000

a.

$$
\begin{aligned}
Sign &= 0 \\
Exp &= (1000\ 0000)_B - 127_D = 128 - 127 = 1 \\
Frac &= 1.0 \\
\therefore N_a &= (-1)^0 * 1.0 * 2^1 = 2.0
\end{aligned}
$$

b.

$$
\begin{aligned}
Sign &= 1 \\
Exp &= (1000\ 0011)_B - 127_D = 4 \\
Frac &= 1.0001_B = 1\frac{1}{16} = 1.0625 \\
\therefore N_b &= (-1)^1 * 1.0625 * 2^4 = -17
\end{aligned}
$$

c.

$$
\begin{aligned}
&\because \begin{cases} Sign = 0 \\ Exp\ containing\ all\ 1's \\ Frac\ containing\ all\ 0's \end{cases} \\
&\therefore N_c = Positive\ Infinity
\end{aligned}
$$

d.

$$
\begin{aligned}
Sign &= 1 \\
Exp &= (1000\ 0000)_B - 127_D = 1 \\
Frac &= 1.1001_D = 1\frac{25}{16} = 1.5625 \\
\therefore N_d &= (-1)^1 * 1.5625 * 2^1 = -3.125
\end{aligned}
$$

2.48 Convert the following decimal numbers to hexadecimal representations of 2's complement numbers.

a. 256
b. 111
c. 123,456,789
d. −44

a.

$$\begin{aligned} 256 &= 0000\ 0001\ 0000\ 0000(2's\ complement) \\ &= 0100(hexadecimal) \end{aligned}$$

b.

$$\begin{aligned} 111 &= 0110\ 1111(2's\ complement) \\ &= 6F(hexadecimal) \end{aligned}$$

c.

$$\begin{aligned} 123456789 &= 0000\ 01111\ 0101\ 1100\ 1101\ 0001\ 0101(2's\ complement) \\ &= 075B\ CD15(hexadecimal) \end{aligned}$$

d.

$$\begin{cases} 44 = 0010\ 1100 \\ \overline{44} = 1101\ 0011 \\ \overline{44} + 1 = 1101\ 0100 \end{cases}$$

$$\therefore -44's\ 2's\ complement = 1101\ 0100$$

$$it's\ hexadecimal = D4$$

Chap 3

3.6 For the transistor-level circuit in Figure 3.38, fill in the truth table. What is Z in terms of A and B?

A	B	C	D	Z

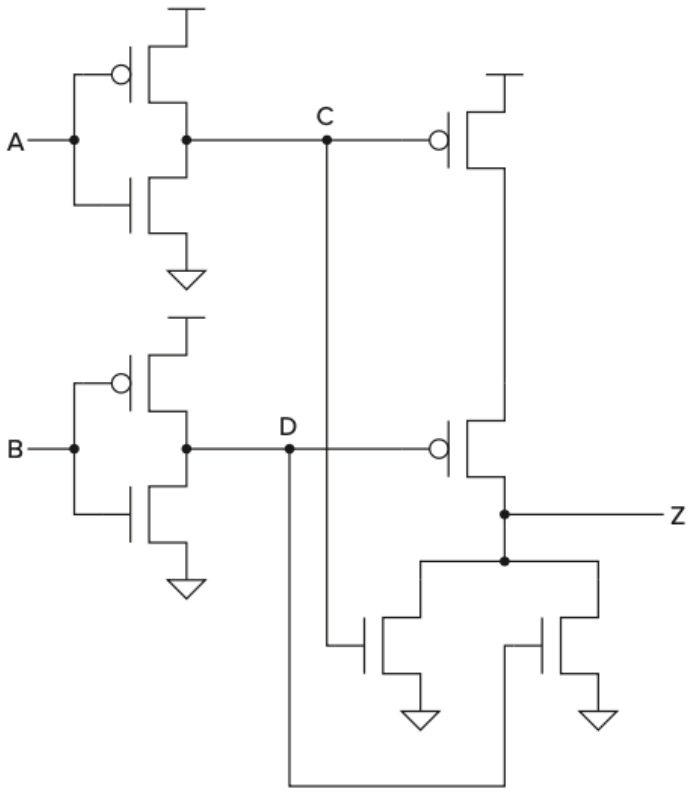


Figure 3.38 Diagram for Exercise 3.6.

- The truth table:

A	B	C	D	Z
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

$$Z = \overline{C} \cdot \overline{D} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B (A \; and \; B)$$

3.20 How many output lines will a 16-input multiplexer have? How many select lines will this multiplexer have?

Since the multiplexer has 16 input & $log_2(16) = 4$, it sould have:

- ONLY ONE output line.
- 4 select lines.

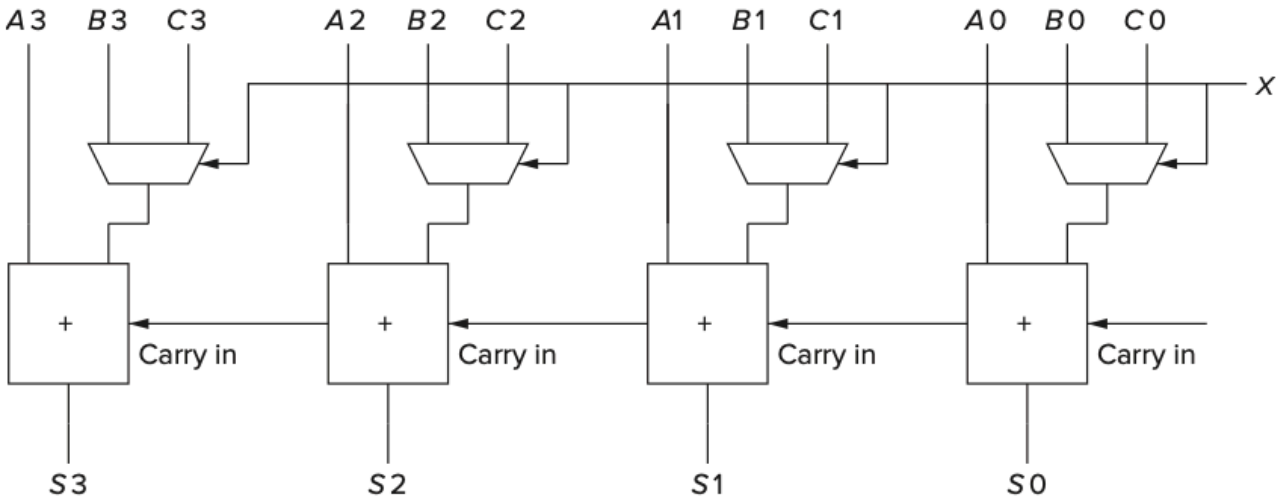


Figure 3.42 Diagram for Exercise 3.30.

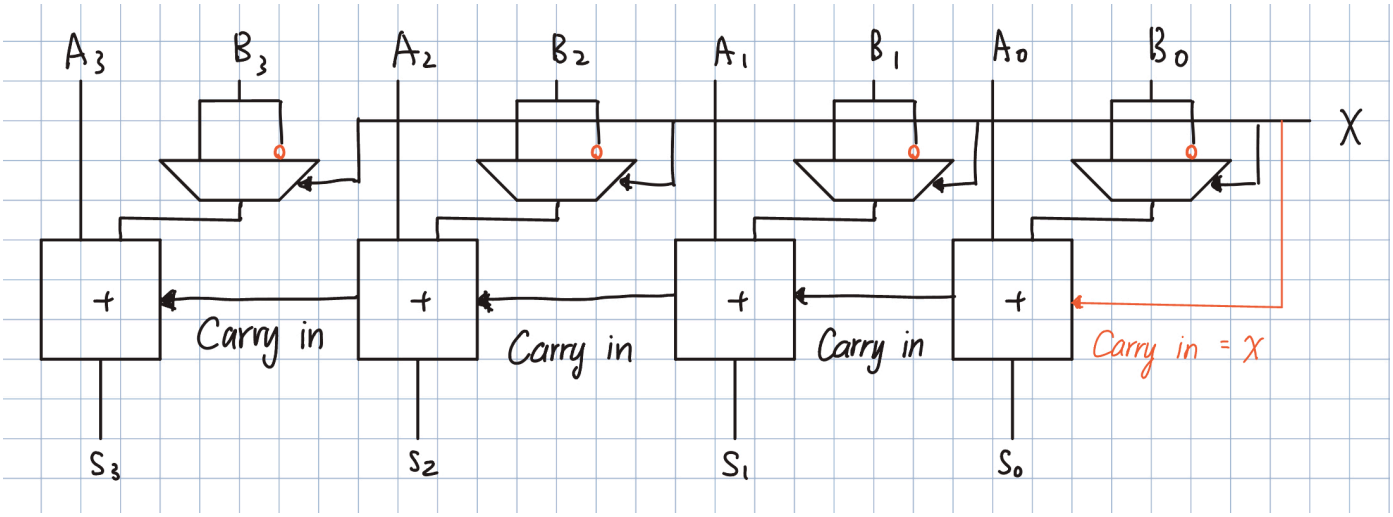
3.30 *a.* Figure 3.42 shows a logic circuit that appears in many of today's processors. Each of the boxes is a full-adder circuit. What does the value on the wire X do? That is, what is the difference in the output of this circuit if $X = 0$ vs. if $X = 1$?

b. Construct a logic diagram that implements an adder/subtractor. That is, the logic circuit will compute $A + B$ or $A - B$ depending on the value of X. *Hint*: Use the logic diagram of Figure 3.42 as a building block.

a.

$$\begin{cases} X = 0 \Rightarrow output = A + B \\ X = 1 \Rightarrow output = A + C \end{cases}$$

b.



$$\begin{cases} X = 0 \Rightarrow output = A + B \\ X = 1 \Rightarrow output = A + (\overline{B} + 1) = A + (-B) = A - B \end{cases}$$

3.36 A comparator circuit has two 1-bit inputs A and B and three 1-bit outputs G (greater), E (Equal), and L (less than). Refer to Figures 3.43 and 3.44 for this problem.

G is 1 if $A > B$	E is 1 if $A = B$	L is 1 if $A < B$
0 otherwise	0 otherwise	0 otherwise

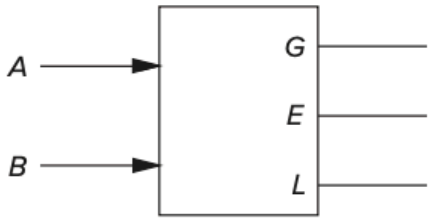


Figure 3.43 Diagram for Exercise 3.36.

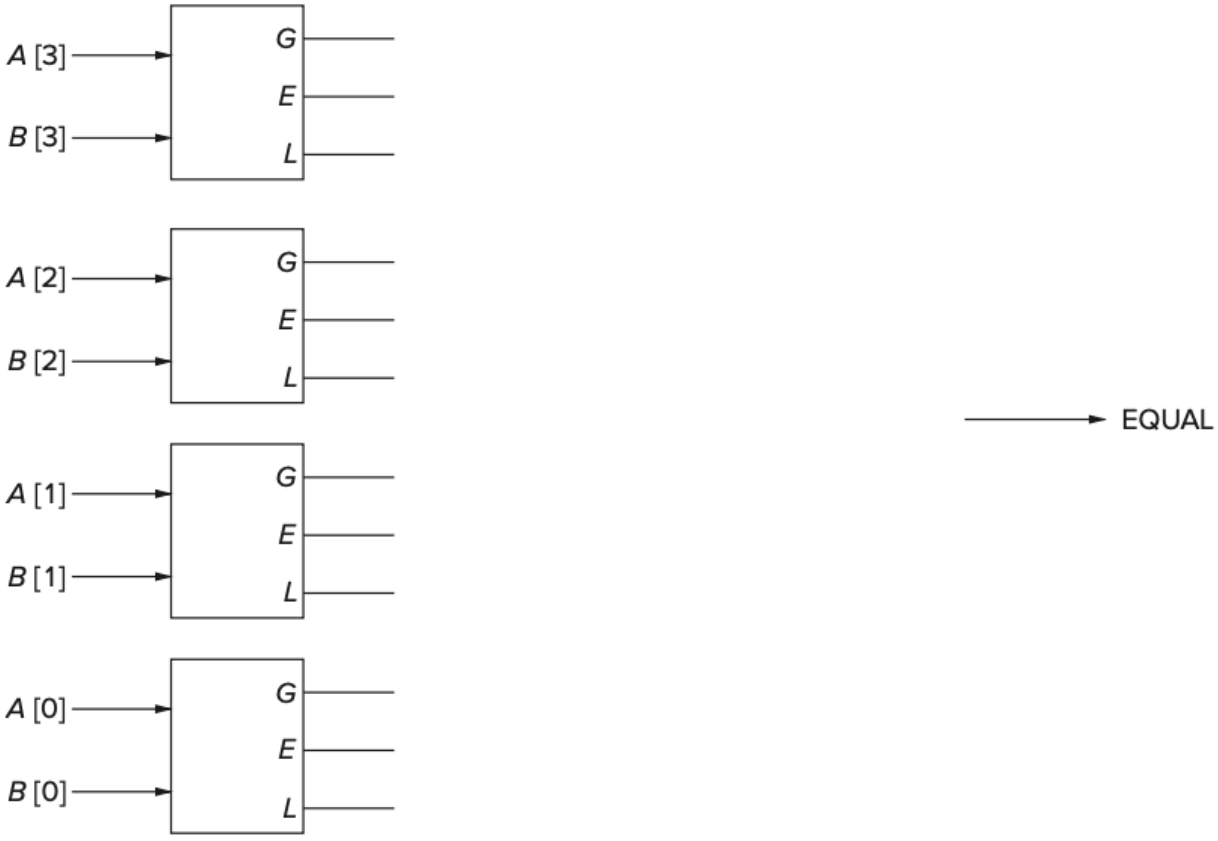


Figure 3.44 Diagram for Exercise 3.36.

a. Draw the truth table for a one-bit comparator.

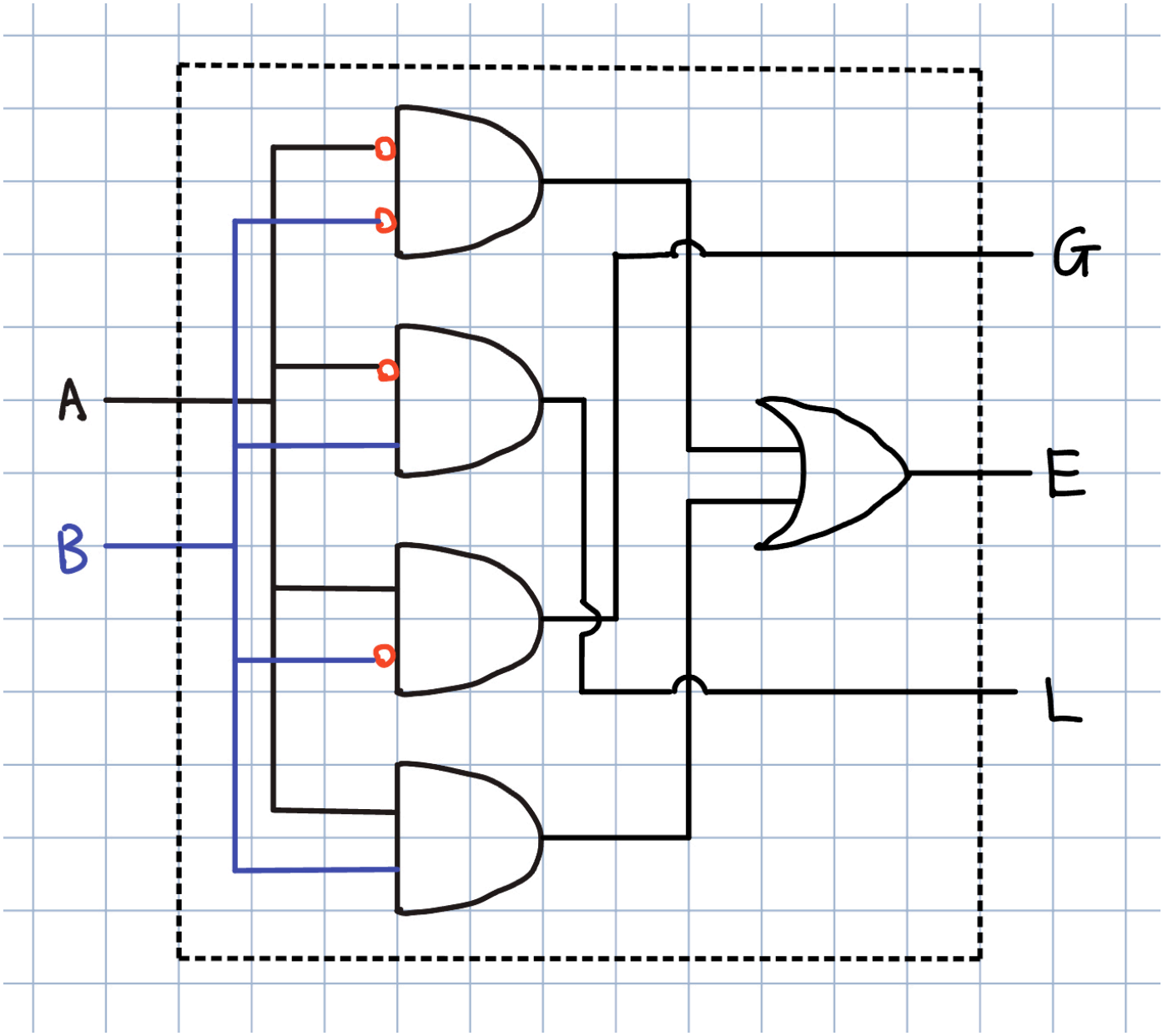
A	*B*	*G*	*E*	*L*
0	0			
0	1			
1	0			
1	1			

b. Implement *G*, *E*, and *L* using AND, OR, and NOT gates.
c. Using the one-bit comparator as a basic building block, construct a four-bit equality checker such that output EQUAL is 1 if A30 = B30, 0 otherwise.

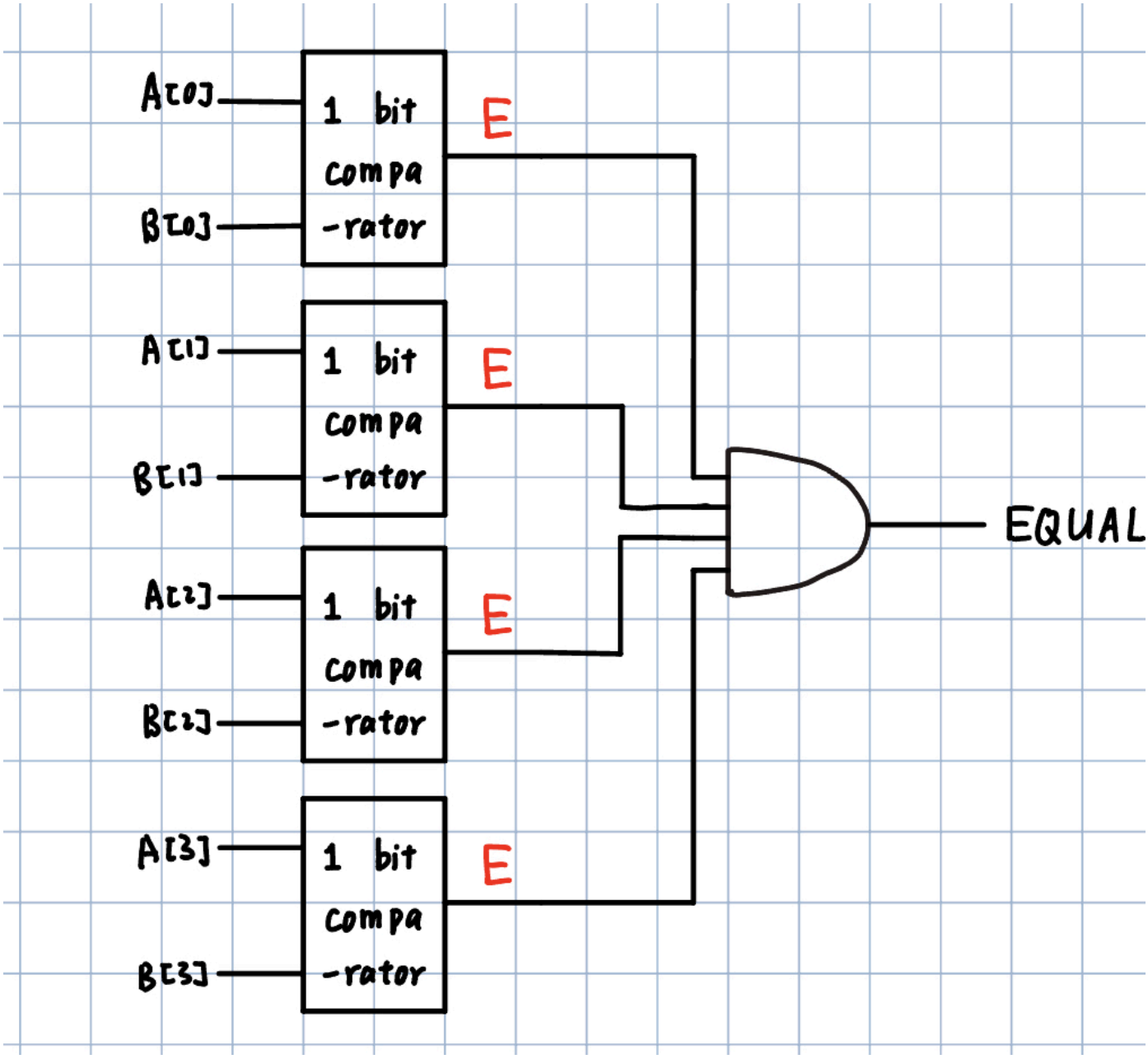
a. The truth table:

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	1

b.



c.



3.40 For the memory shown in Figure 3.45:

a. What is the address space?
b. What is the addressability?
c. What is the data at address 2?

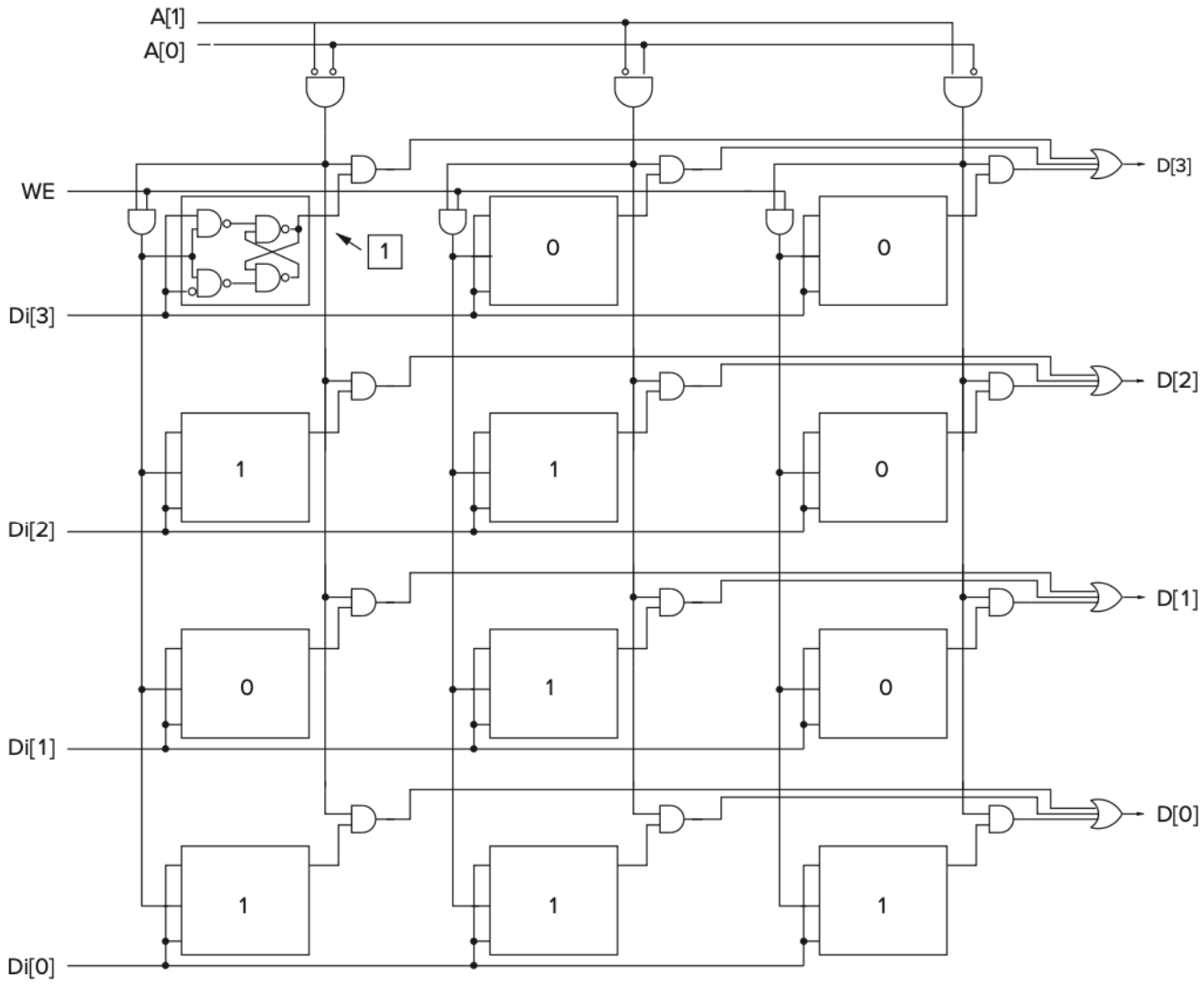


Figure 3.45 **Diagram for Exercise 3.40.**

a. According to Figure 3.45 the memory uses 2-bit (A[1] & A[0]) address, thus it's $address\_space = 2^2 = 4$

b. Since each memory location stores 4-bits(D[3:0]), it's $addressability = 4$

c. Since $address(2) = 10_B$, we could find that $data\ at\ address(2) = 0001$

3.50 Prove that the NAND gate, by itself, is logically complete (see Section 3.3.5) by constructing a logic circuit that performs the AND function, a logic circuit that performs the NOT function, and a logic circuit that performs the OR function. Use only NAND gates in these three logic circuits.

$$
\because \begin{cases}
NOT = \overline{X} = \overline{X} + \overline{X} = \overline{X \cdot X} & (1) \\
OR = X + Y = \overline{\overline{X} \cdot \overline{Y}} = \overline{\overline{X \cdot X} \cdot \overline{Y \cdot Y}} & (2) \\
AND = X \cdot Y = \overline{\overline{A \cdot B}} = \overline{\overline{A \cdot B} \cdot \overline{A \cdot B}} & (3)
\end{cases} \quad (4)
$$

$$
and\ Set\{AND, OR, NOT\}\ is\ logically\ complete
$$

$$
\therefore NAND\ is\ also\ logically\ complete
$$

The logical circuits are as follows: