Homework 7

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9.2   Why is a ready bit not needed if synchronous I/O is used?

When using *synchronous I/O* , the processor will know exactly when the data will arrive or be taken away, since it will do input & output *at regular intervals* . And it is guaranteed that input data will be taken by those consumers right during the intervals.

Thus, a ready bit is not needed in *synchronous I/O* .

9.6   What problem could occur if a program does not check the ready bit of the KBSR before reading the KBDR?

If the program doesn't check the ready bit of KBSR, it would *read the same input character more than once* if `KBSR[15] == 0` .

9.10   What problem could occur if the display hardware does not check the DSR before writing to the DDR?

If the program doesn't check the ready bit of DSR, *the former output character would never been displayed* if `DSR[15] == 0` .

9.14   An LC-3 Load instruction specifies the address xFE02. How do we know whether to load from the KBDR or from memory location xFE02?

Since address `xFE00~xFFFF` in LC-3 are reserved for input/output registers, the LC-3 Load instruction with address `xFE02` would load from **KBDR**, also it seems like a normal memory address to user.

During the EXECUTE phase, the *addr control logic* would select the corresponding device register to provide input according to the memory-mapped address.

9.26 The following program is supposed to print the number 5 on the screen. It does not work. Why? Answer in no more than ten words, please.

```
            .ORIG   x3000
            JSR     A
            OUT
            BRnzp   DONE
A           AND     R0,R0,#0
            ADD     R0,R0,#5
            JSR     B
            RET
DONE        HALT
ASCII       .FILL   x0030
B           LD      R1,ASCII
            ADD     R0,R0,R1
            RET
            .END
```

- No.

- R7 is overwritten by **B**, **A** can't return properly.