IT 451: Computer Organization and Architecture (Sessional)

Course Instructor: **Prof. Prasun Ghosal**

Assignment II

This assignment is to be completed individually. Use ISE Design Suite for the simulation and synthesis of your design. Use VHDL as the hardware description language.

1. Design and simulate the behavioral model of an UP/DOWN counter that is capable of counting up to 10. Use one input **count_mode** to control the mode of counting i.e. for **count_mode = '1'** the counter will operate as an UP counter and for **count_mode = '0'** the counter will behave as a DOWN counter. Use a **reset** input to reset the counter anytime to 0.

2. Design and simulate the behavioral model of a 4 bit shift register that can support the following modes of data transfer.

a. Serial in parallel out (SIPO)
b. Serial in serial out (SISO)
c. Parallel in serial out (PISO)
d. Parallel in parallel out (PIPO).

Use **case** statement for this design. Use one input **reg_mode [std_logic_vector (1 downto 0)]** to control the nature of behavior of the register. Use "00" for SIPO, "01" for SISO and so on.

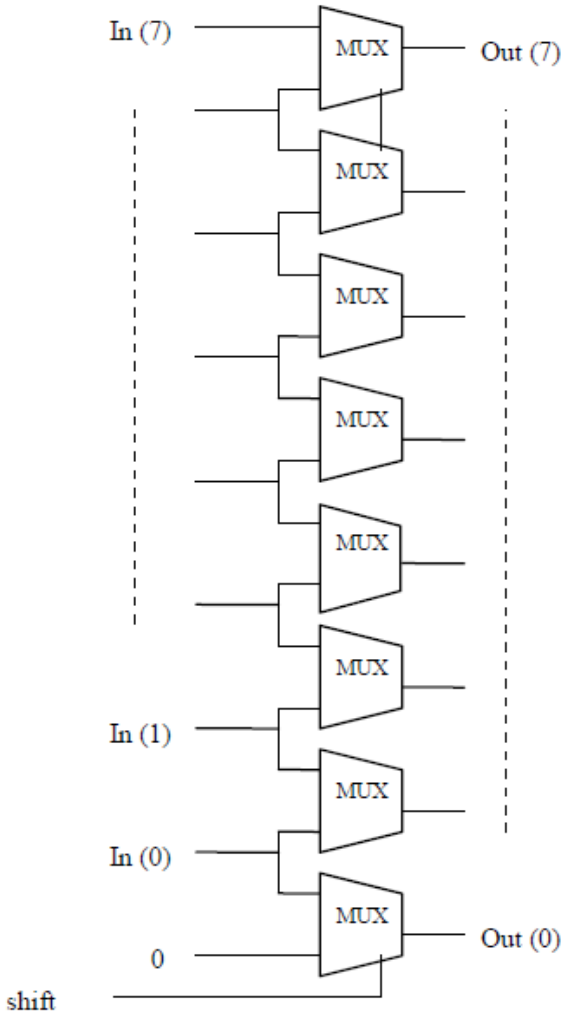
3. Design the followings:

a. Design and simulate the behavioral model of an 8 bit even parity generator.

b. Design and simulate the behavioral model an 8 bit even parity checker.

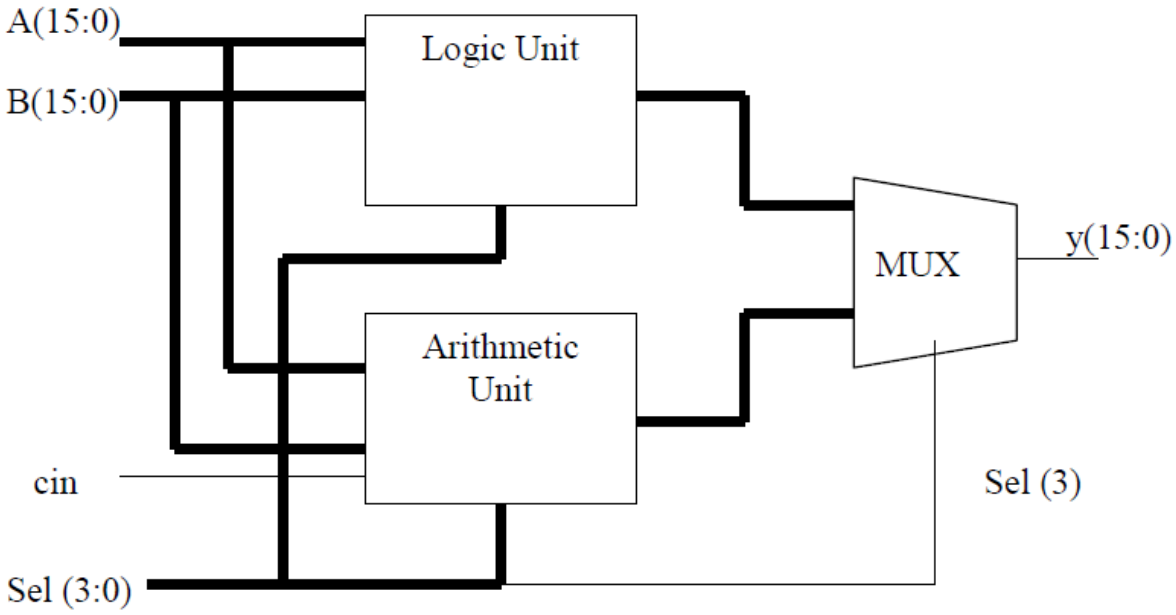
c. Design a top level module called **parity** and use the previously designed two modules as components to check whether the functionality of the two modules are in synchronization or not.

4. The diagram of a barrel shifter is shown below:



The circuit must shift the input vector of size 8 either 0 or 1 position to the left. When actually shifted (shift = 1), the LSB bit must be filled with '0'. If shift = 0, then out=in; else, if shift = 1, then out(0)='0' and out(i)=in(i-1), for $1 \leq i \leq 7$. Write a concurrent code for this circuit and verify its behavior.

5. Design an 16 bit ALU (Arithmetic Logic Unit) as shown in the following figure and verify it's behavior with simulation.



The arithmetic and logical operations that are supported are listed below:

Unit	Function	Sel
Arithmetic	Transfer a	0000
	Increment a	0001
	Decrement a	0010
	Transfer b	0011
	Increment b	0100
	Decrement b	0101
	Add a and b	0110
	Add a and b with carry	0111
Logical	Complement a	1000
	Complement b	1001
	AND	1010
	OR	1011
	NAND	1100
	NOR	1101
	XOR	1110
	XNOR	1111