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SCALA2-AMD

CPU :ZACATE

Chip Set :HUDSON-M1

GFX : SEYMOUR-S3

Remarks : AMD Brazos Platform

Model Name : SCALA2-AMD

PBA Name : MAIN

PCB Code : BA41-01533A (GCE)

BA41-01534A (NY)

BA41-01532A (HAN)

Dev. Step : MP

Revision : 1.0

T.R. Date : 2011.03.11

Design	CHECK	APPROVAL
Cun jia jun	Lei Guo	BC LEE

■ Owner: SEC IT Solution N/P LAB Signature: wanni

sheet01 : Cover sheet31 : MICOM

sheet02 : BLOCK DIAGRAM sheet32 : MICOM Glue Logic (KBD / TP) sheet03 : BOARD INFORMATION sheet33 : TOUCHPAD

sheet04: POWER DIAGRAM sheet34: TOUCHPAD sheet05: POWER RAILS sheet35: Audio - HP/MIC sheet06: POWER SEQUENCE sheet36: Audio - HP/MIC sheet37: LAN (Realtek 8111F)

sheet08: Thermal Sensor sheet38: WLAN

sheet09: CPU sheet39: SATA interface sheet10: CPU sheet40: SATA ODD SUB sheet11: CPU sheet41: 3-in-1 card

sheet12 : DDR3 SODIMM #0 sheet42 : USB/POWER SW SUB BD

sheet13: DDR3 SODIMM #1 sheet43: USB connector sheet14: FCH-HUDSON sheet44: Power - charger

sheet15: FCH-HUDSON sheet16: FCH-HUDSON sheet46: Power - P1.05V (Chipset Power)

sheet17 : FCH-HUDSON sheet47 : Power - DDR3

sheet18 : FCH-HUDSON sheet48 : Power - P1.1V_AUX(Chipset power)

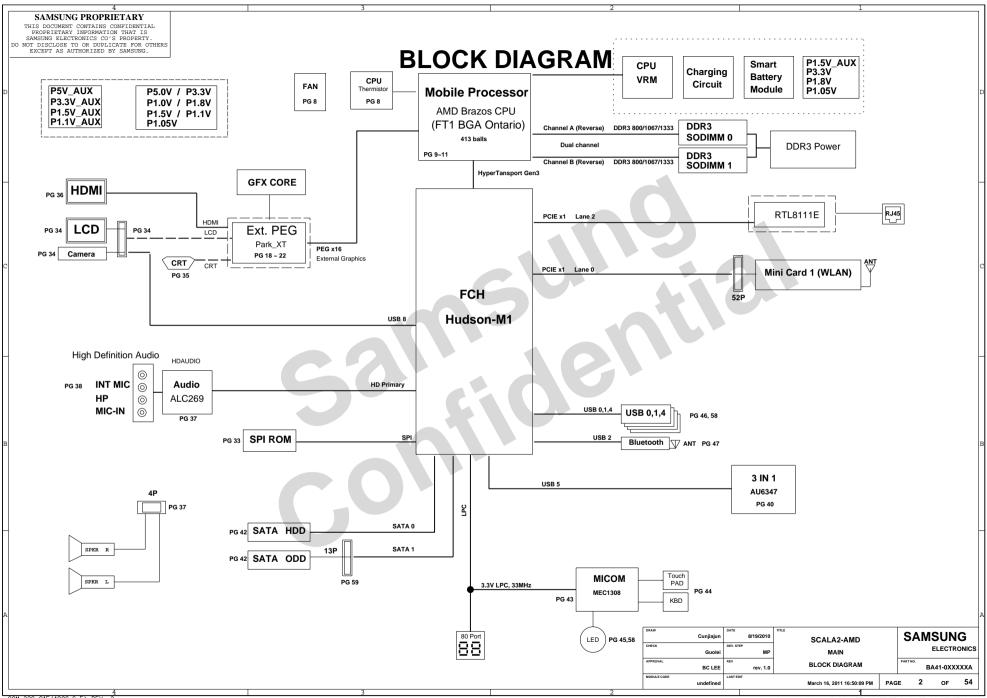
sheet54: MOUNT HOLE

sheet19: 80 port/BIOS sheet20: SEYMOUR S3_XT sheet21: SEYMOUR S3_XT sheet22: SEYMOUR S3_XT sheet23: SEYMOUR S3_XT sheet23: SEYMOUR S3_XT sheet53: Power - Puser Discharge

sheet24 : SEYMOUR S3_XT sheet25 : SEYMOUR S3_XT

sheet26 : GFX memory sheet27 : GFX memory sheet28 : LVDS / CAMERA

sheet29 : CRT sheet30 : HDMI



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage	Rails	Active in
VDC P12.0V_ALW P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 12.0V always power rail 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)	\$3
P5.0V P3.3V P1.8V P1.5V P1.05V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 1.05V power rail for chipset (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)	SO
VCC_CORE IGFX_CORE EGFX_CORE P1.05V (VCCP)	Core Voltage for CPU Core Voltage for IGFX Core Voltage for GPU VCC for Arrandale & IBEX Peak	S0

	USB PORT Assign	PCI	Express Assign
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0 1 2 3 4 5 6 7 8 9 10 11 12 13	SYSTEM PORT 0 SYSTEM PORT 1 Mini PCI Express Multi Memory Card Controller NC NC (NA WITH HM55) NC (NA WITH HM55) NC (NA WITH HM55) NC (NA WITH HM55) NC (NA WITH MM56) NC SYSTEM PORT 2 (SUB BOARD) Bluetooth Camera NC	1 2 3 4 5 6 7 8	Mini Card 1 (WLAN) NC NC NC LAN CONTROLLER NC

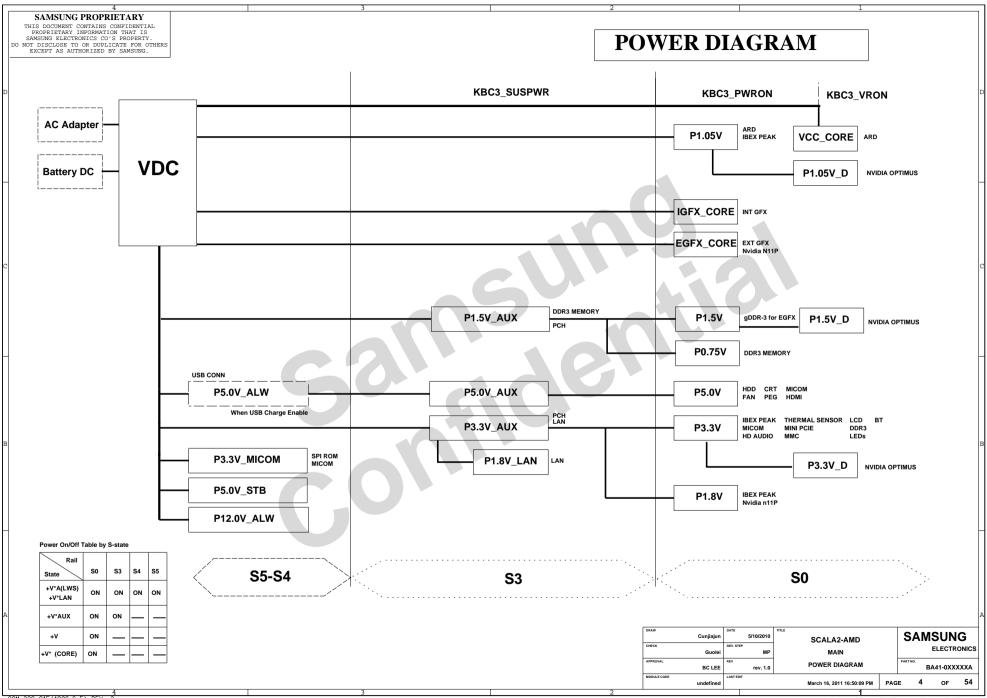
SATA PORT Assign					
PORT #	ASSIGNED TO				
0	HDD				
1	ODD				
2	(N/A WITH HM55)				
3	(N/A WITH HM55)				
4					
5					

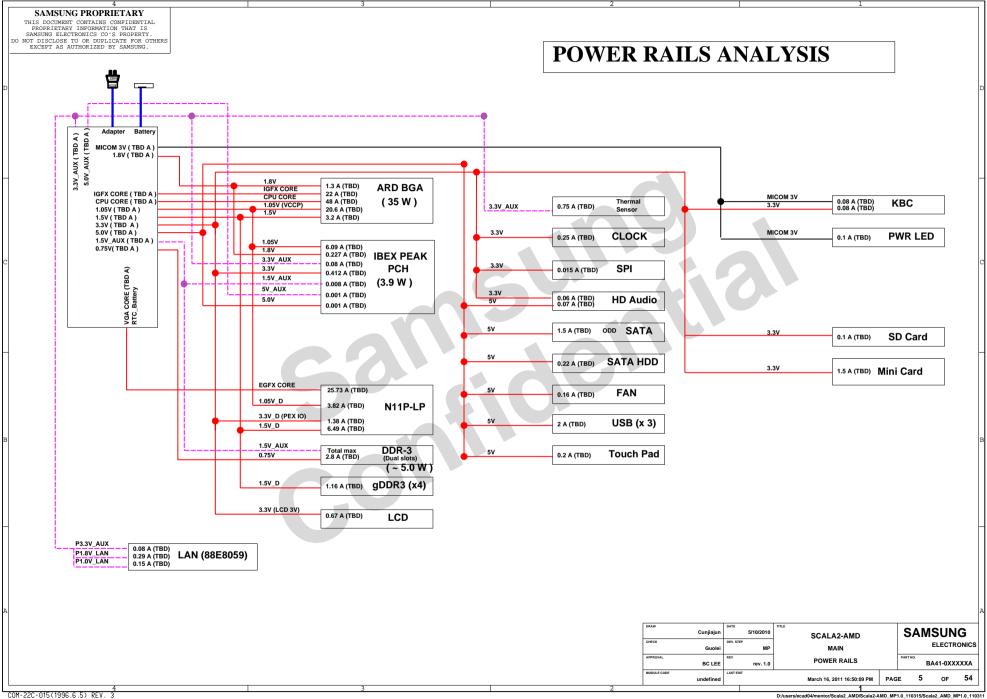
-	l / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE	
Crystal Crystal Crystal	32.768KHz 14.318MHz 25MHz	IBEX-PEAK CLOCK-Generator LAN	Real Time Clock CK-505 Intel LAN	

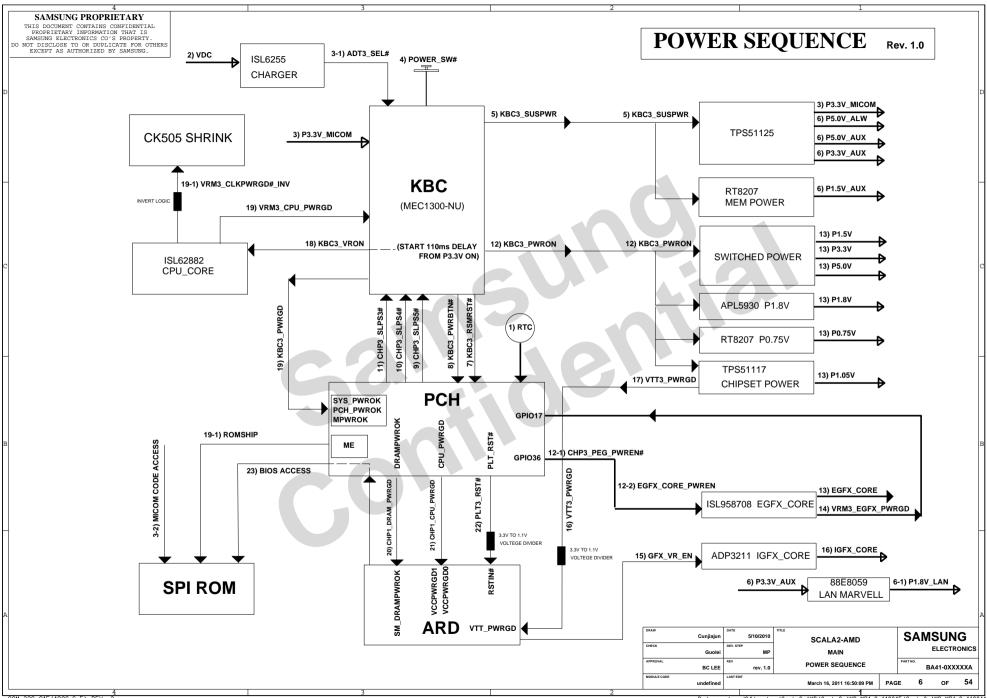
LCD Pannel D	Detect	
Devices	Resolution	PANNEL_DETECT_0
LTN140AT17	HD(1366x768)	SEC3250

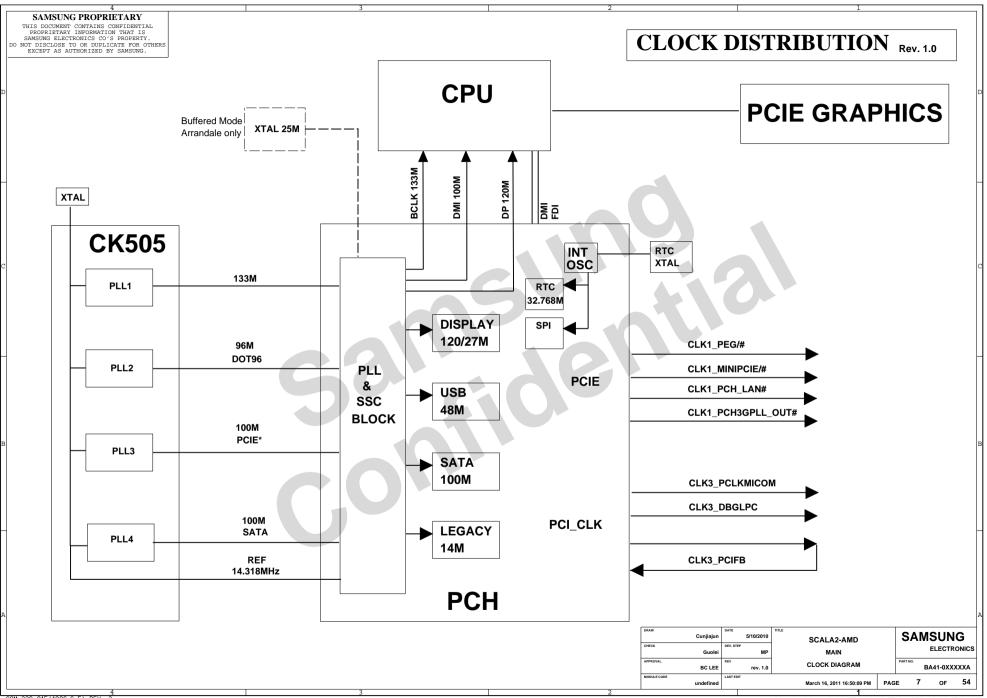
1 ² C / SMB Address							
Devices	Address	Hex	Bus				
IBEX PEAK	Master	-	SMBUS Master				
CPU Thermal Sensor SODIMMO SODIMMO SODIMM1 Thermal Sensor on SODIMMO Thermal Sensor on SODIMM1 CK-605M Shrink(Clock Generator) Thermal Sensor on board Power thermal management TS	0111 101x 1010 000x 1010 010x 0011 000x 0011 010x 1101 001x 1101 100x 1101 100x	7Ah A0h A4h 30h 34h D2h 98h 96h	Thermal Sensor Clock, Unused Clock Output Disable				

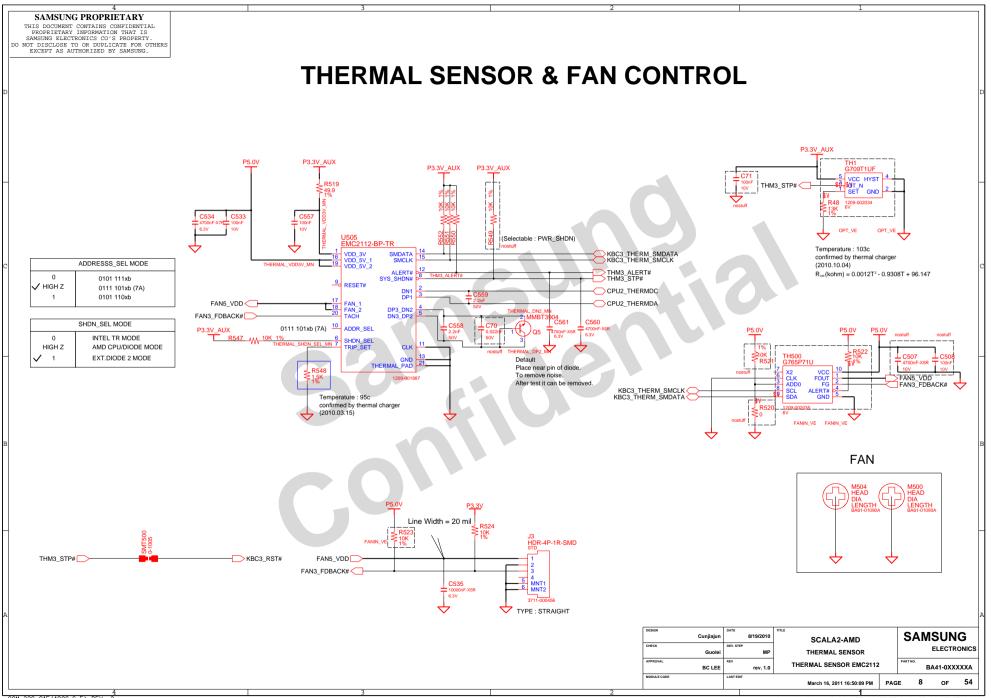
DRAW Cunjiajur	DATE 8	/19/2010	SCALA2-AMD								MSU	NG
CHECK Guole	DEV. STEP	МР	MAIN			ELEC	CTRONICS					
APPROVAL BC LEE	REV	rev. 1.0	BOARD INFO		PART NO.	BA41-0	XXXXXA					
MODULE CODE undefined	LAST EDIT		March 16, 2011 16:50:09 PM	PAG	E 3	01	54					

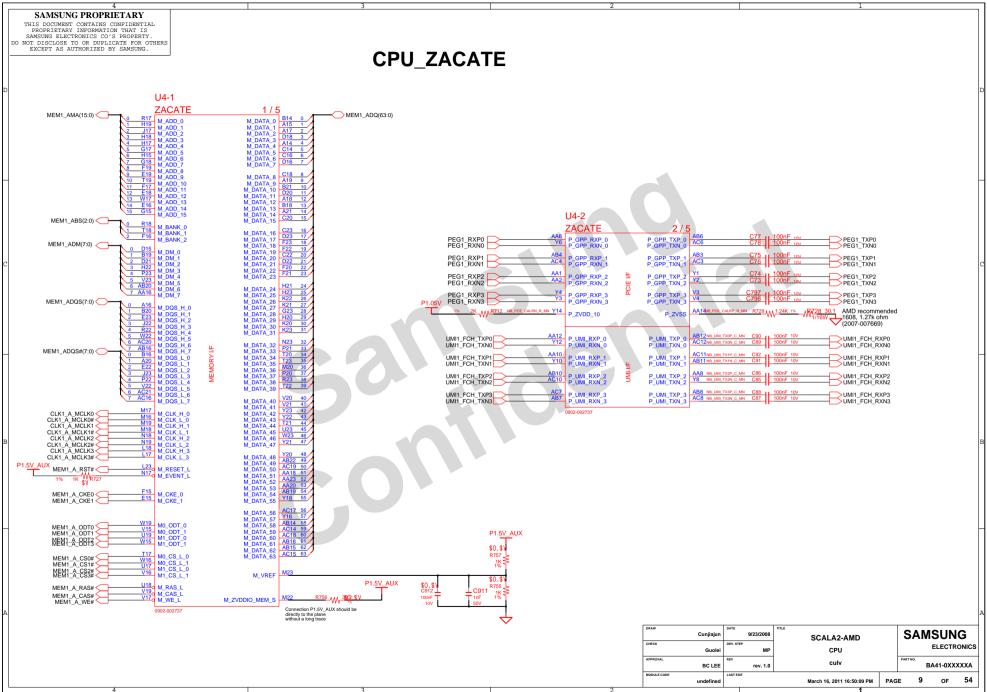


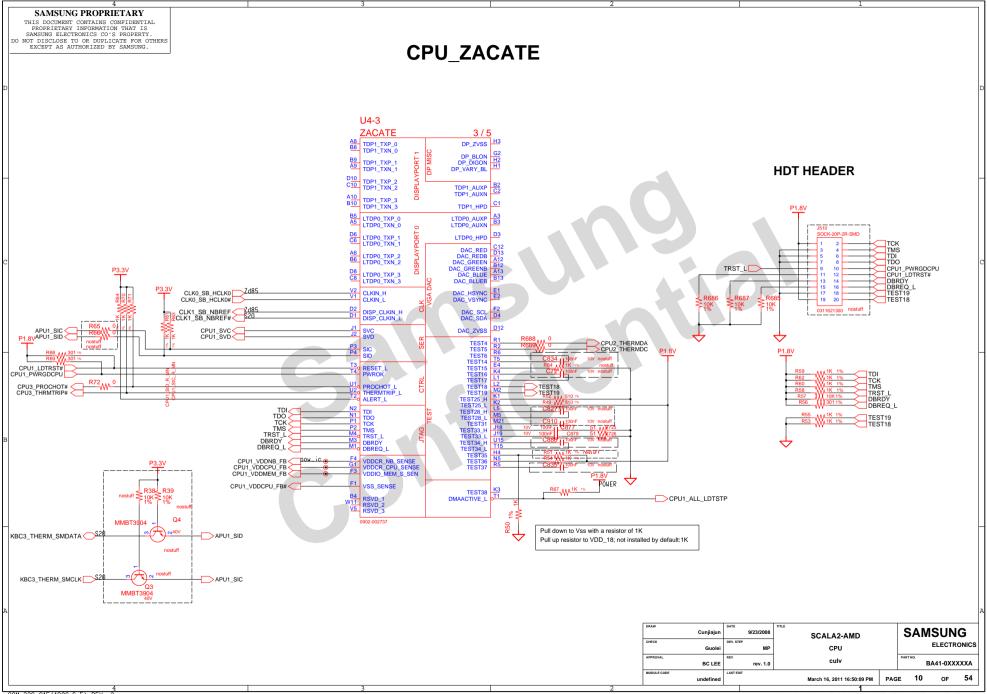


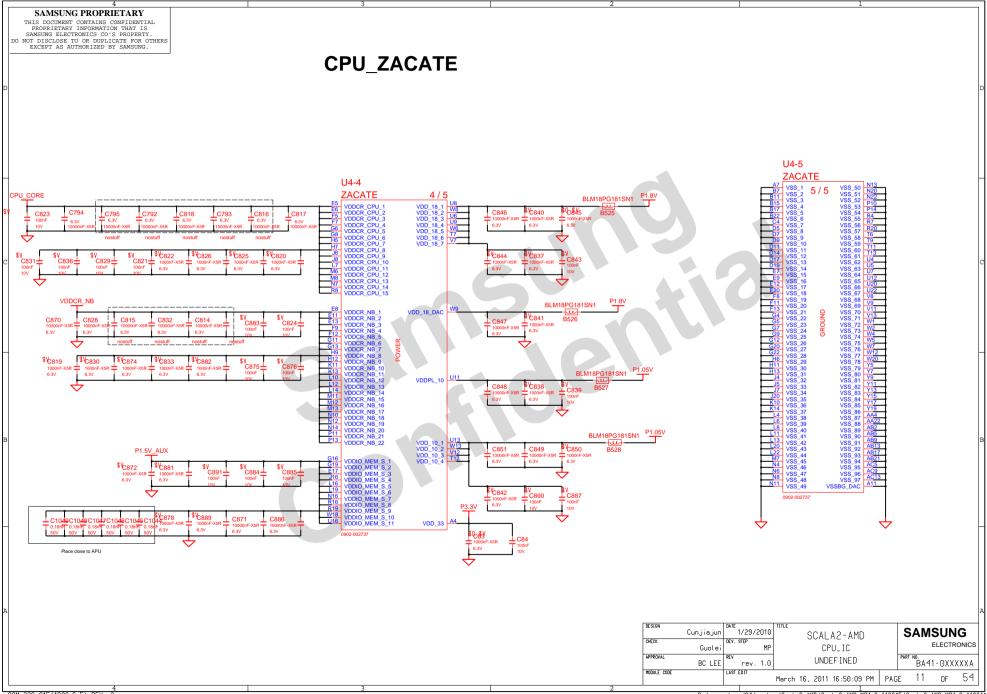


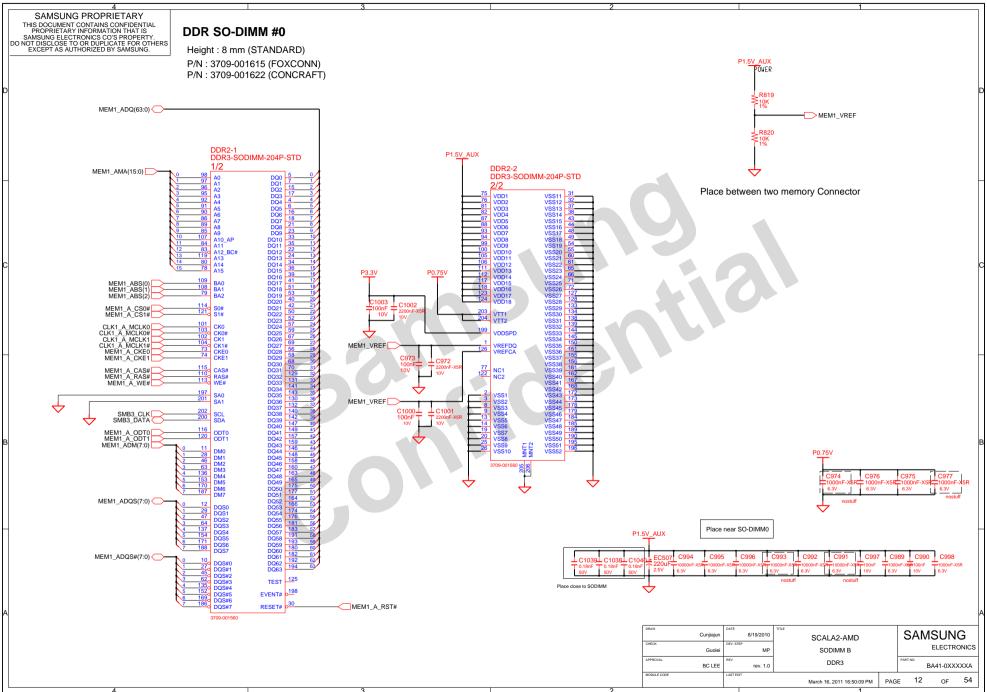


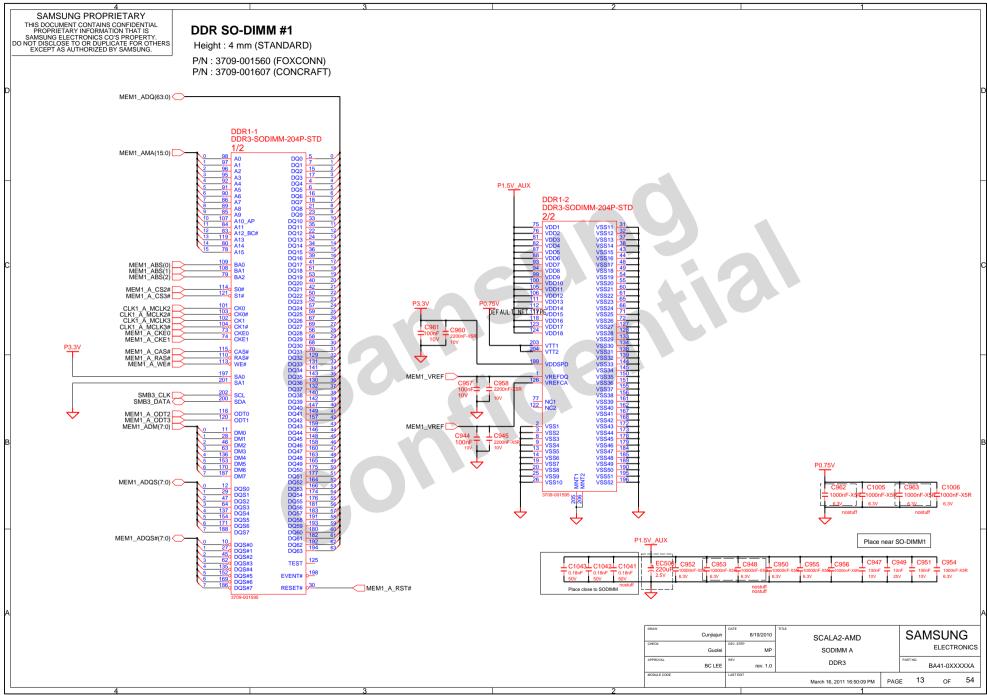


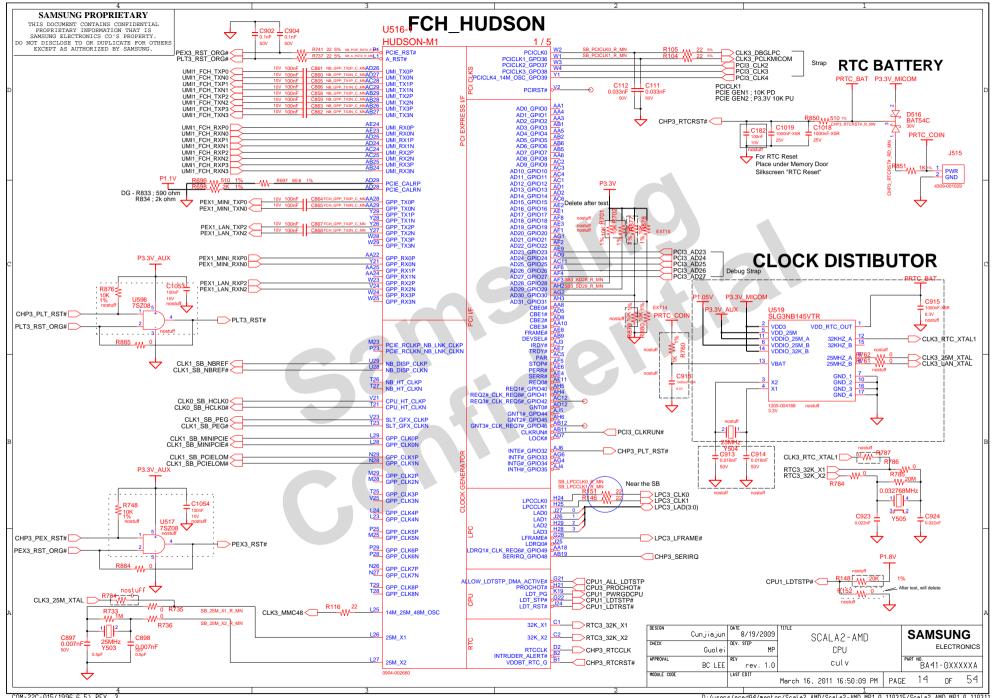


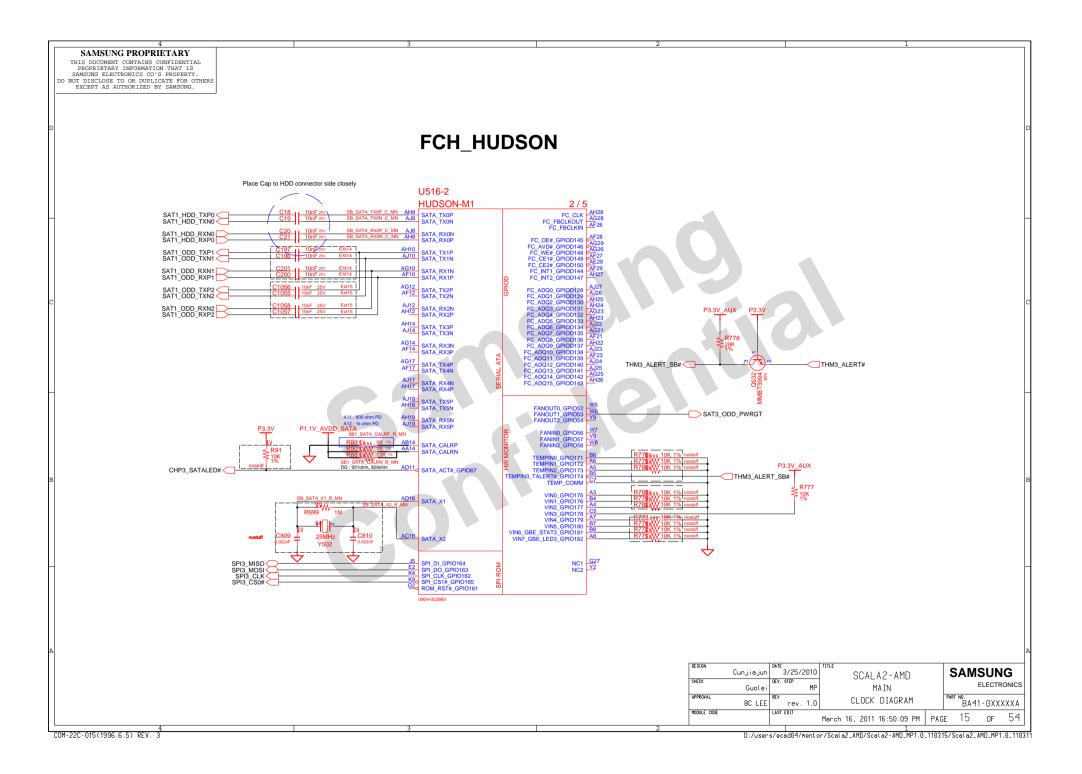


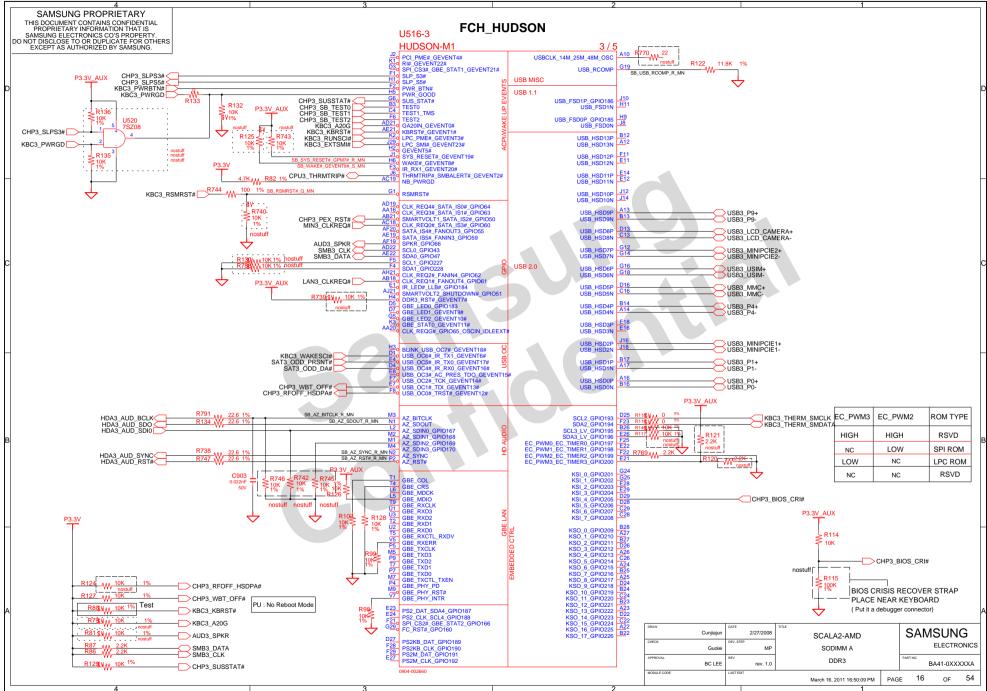


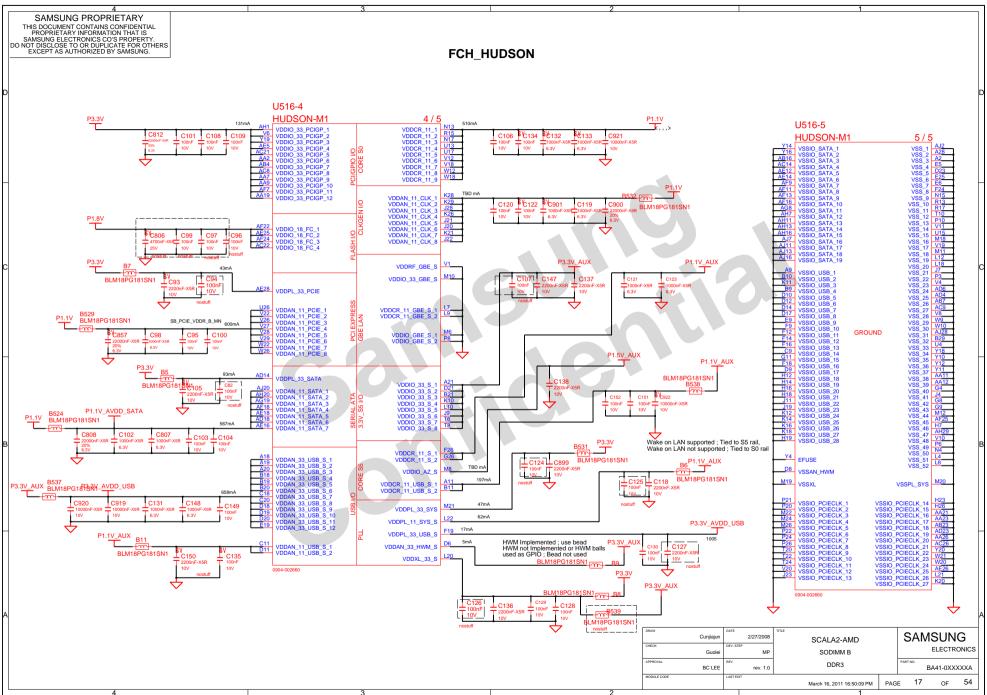








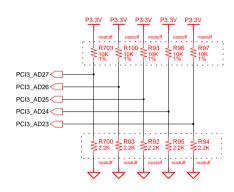


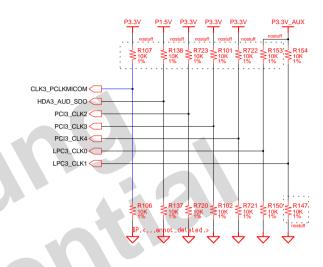


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Strap

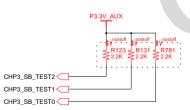




DEBUG STRAPS

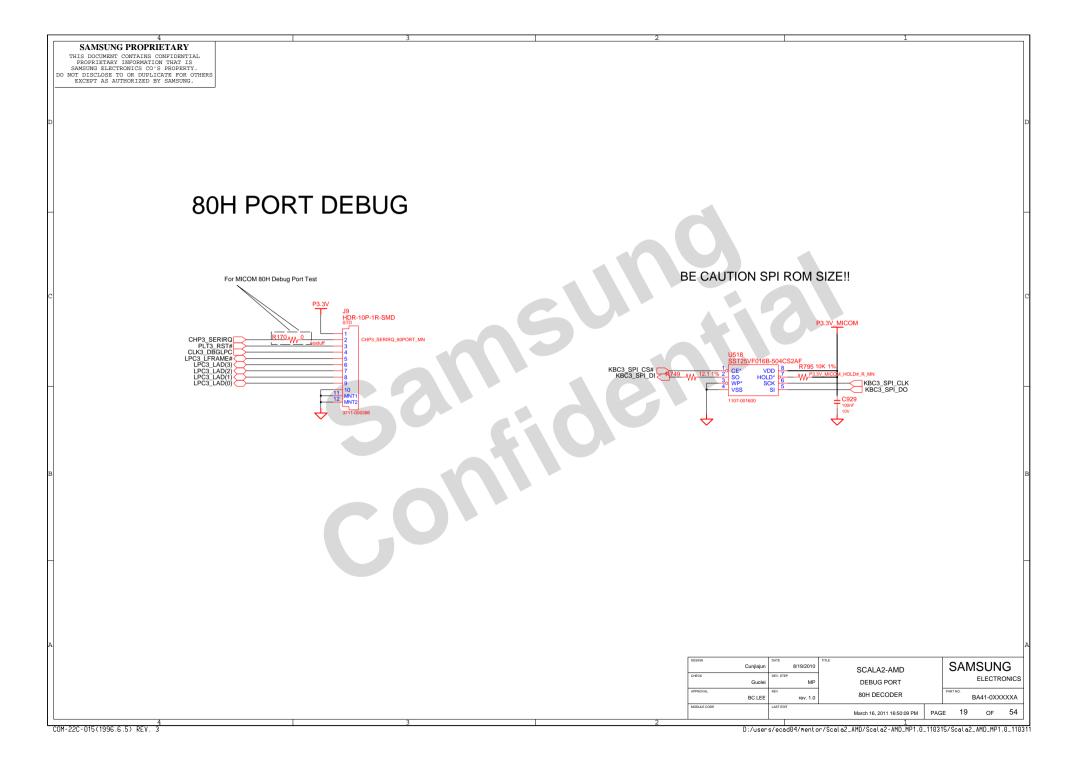
	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
	Bypass PCI PLL	ILA auto run Enable	Bypass FC CLK	I2C ROM Enable	Booting from PCI memory
STRAP HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
STRAP LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

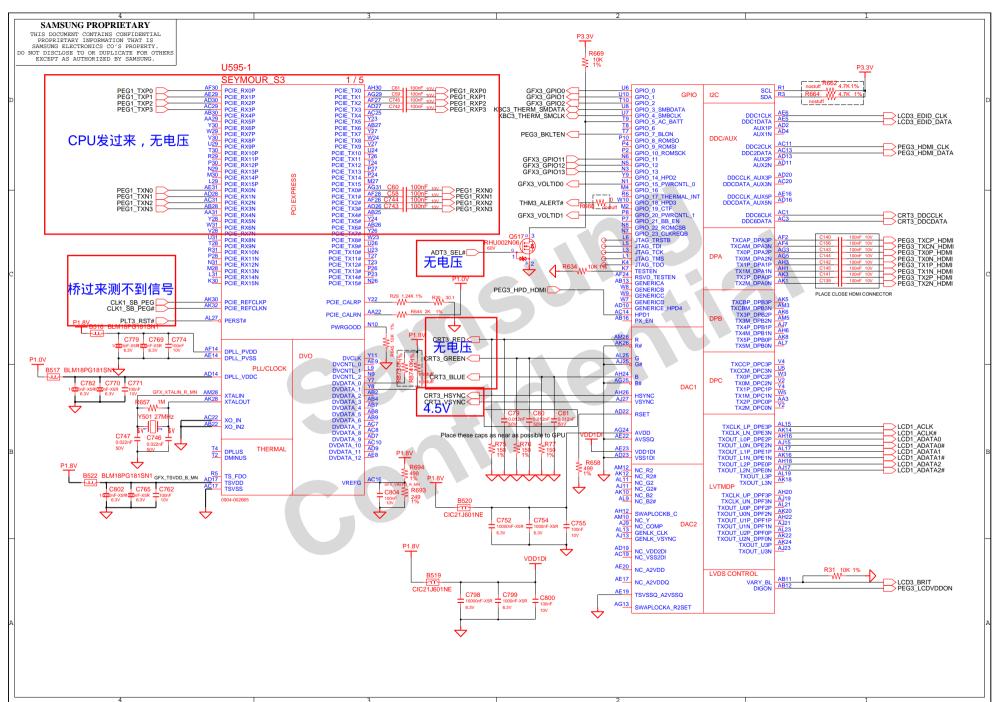
PULL HIGH	HDA3_AUD_SDO AZ_SDOUT	PCI3_CLK2	PCI3_CLK3	PCI_CLK4	LPC3_CLK0	LPC3_CLK1
	LOW POWER MODE	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLE	CLKGEN ENABLE DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED

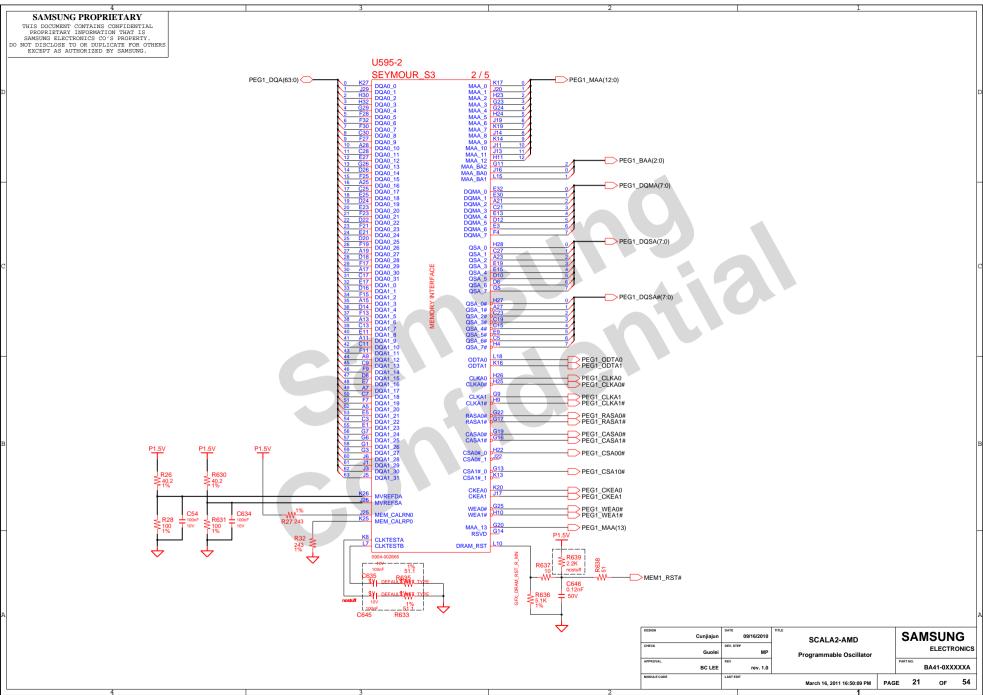


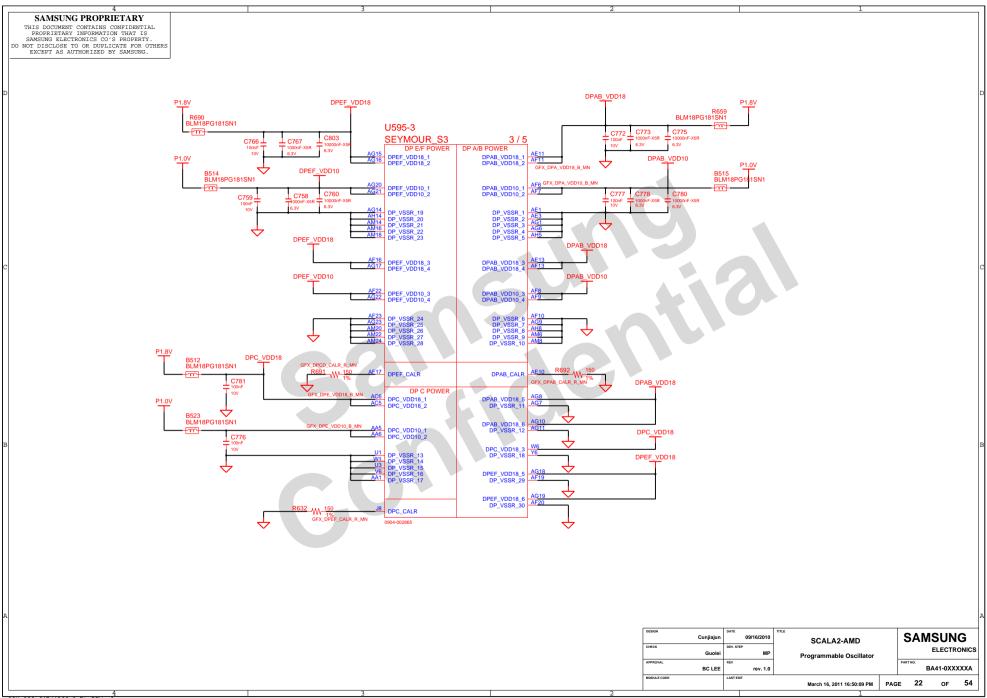
Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)

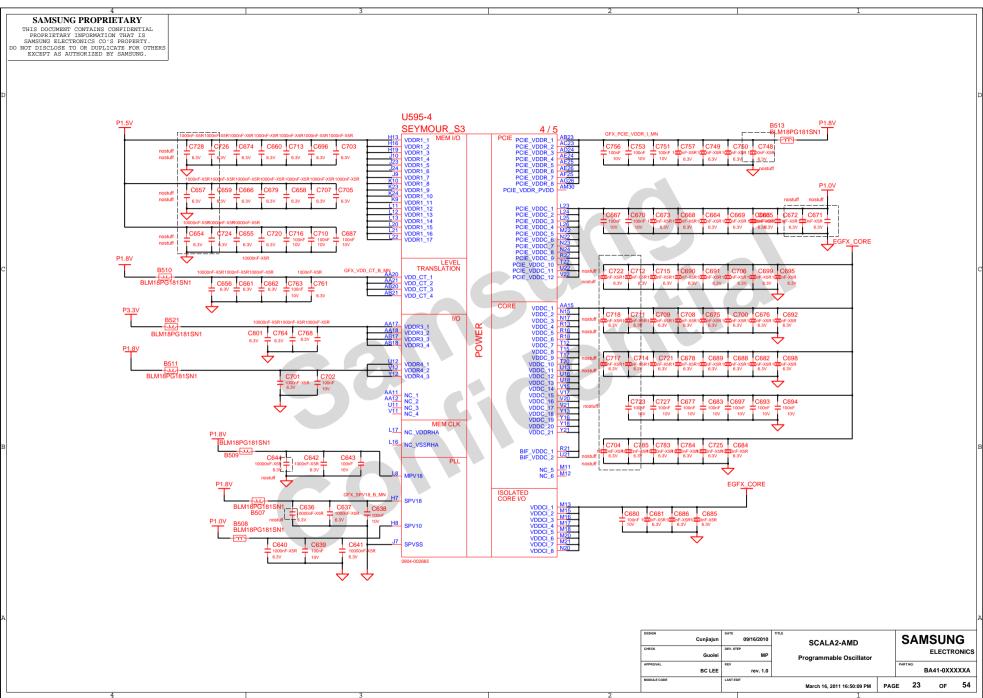
DESIGN Cunjiajun	B/19/2010	SCALA2-AMD		SAN	ISUN	IG
CHECK Guolei	DEV. STEP MP	CPU			ELECTF	RONICS
APPROVAL BC LEE	rev. 1.0	BGA CPU (4/5)		PART NO.	BA41-0XX	XXXA
MODULE CODE	LAST EDIT	March 16, 2011 16:50:09 PM	PAG	18	OF	54

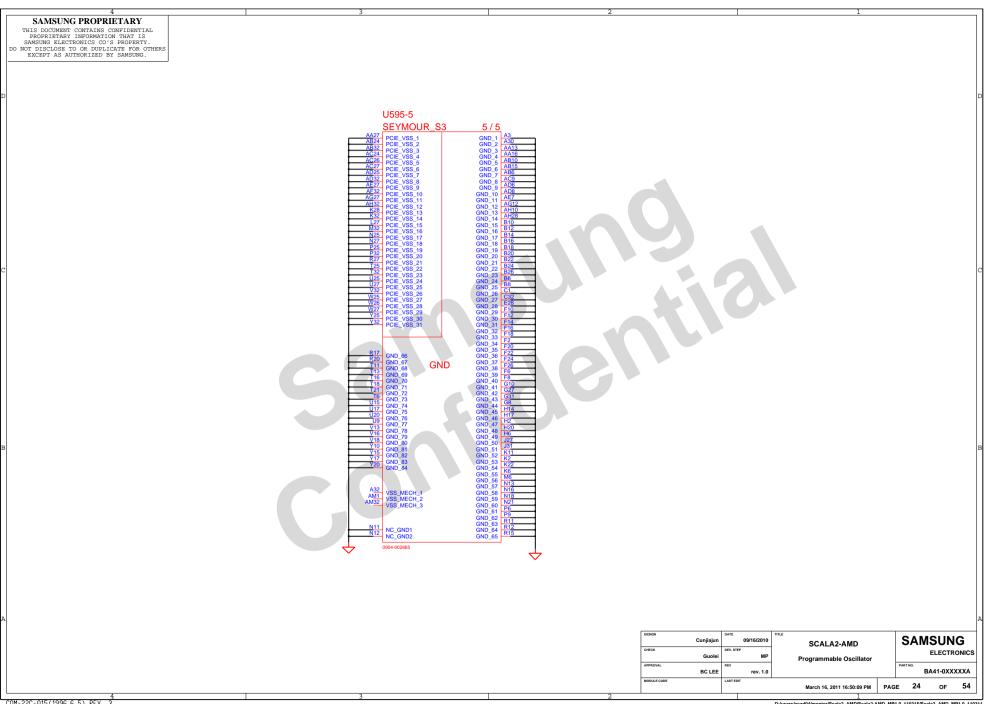


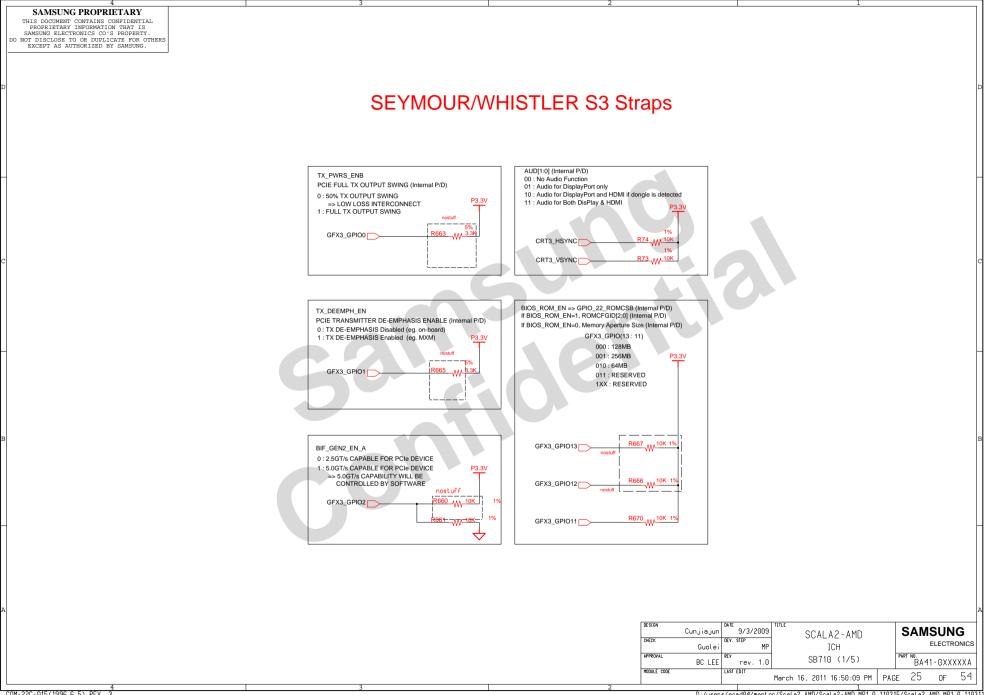


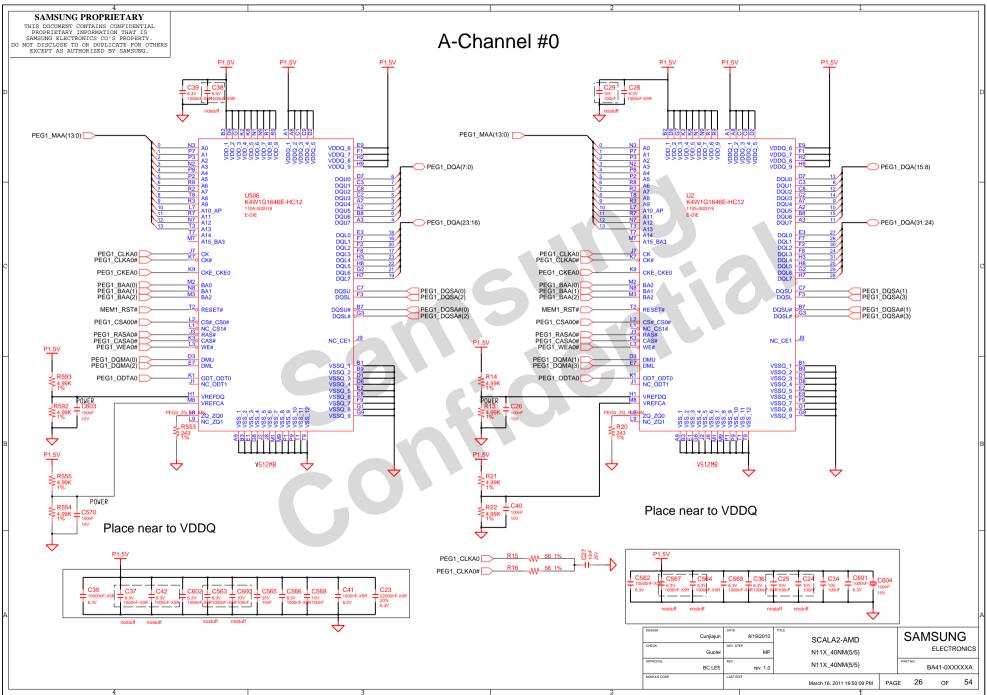


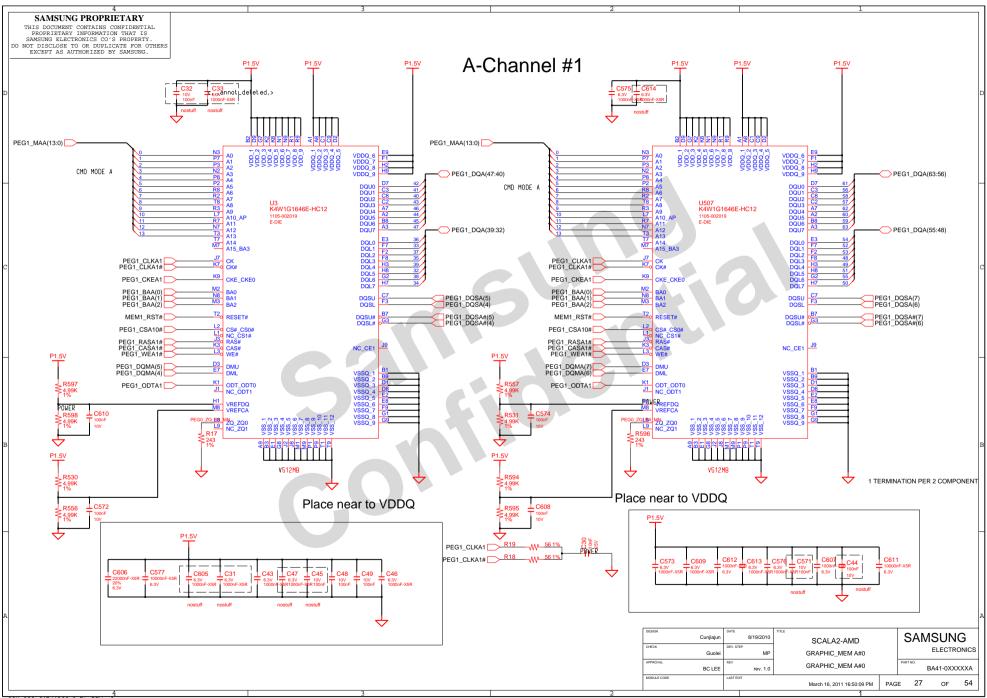




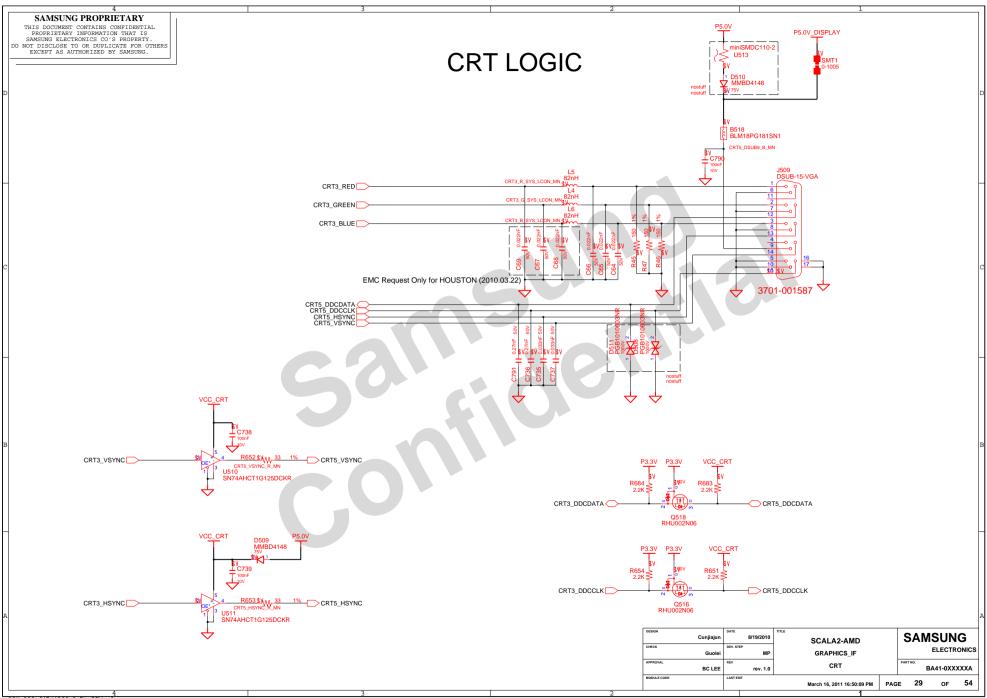


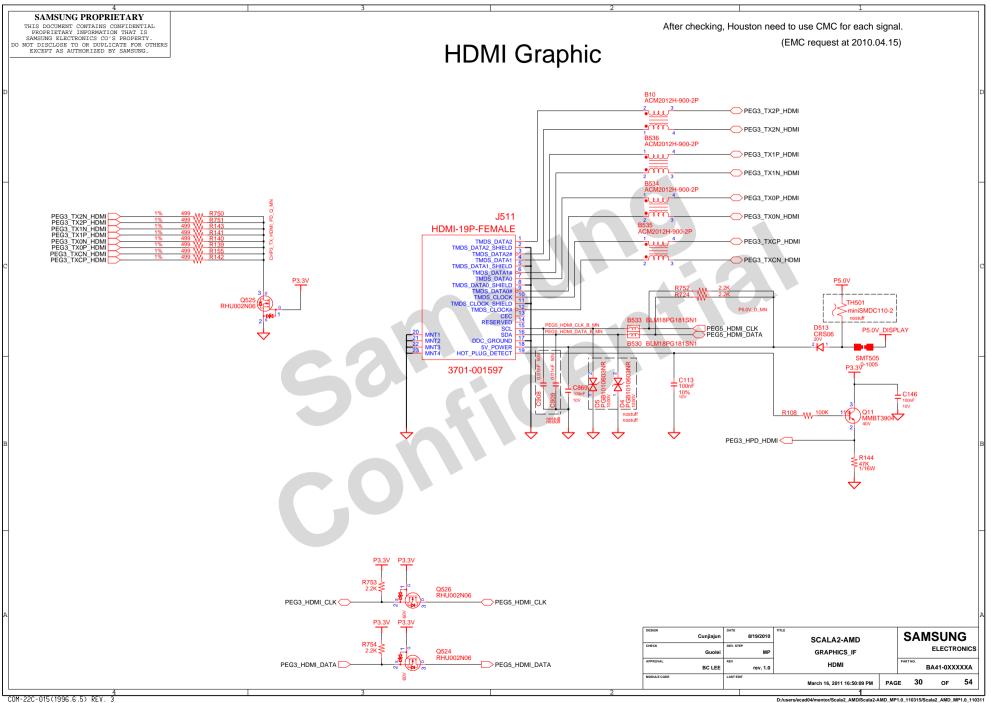


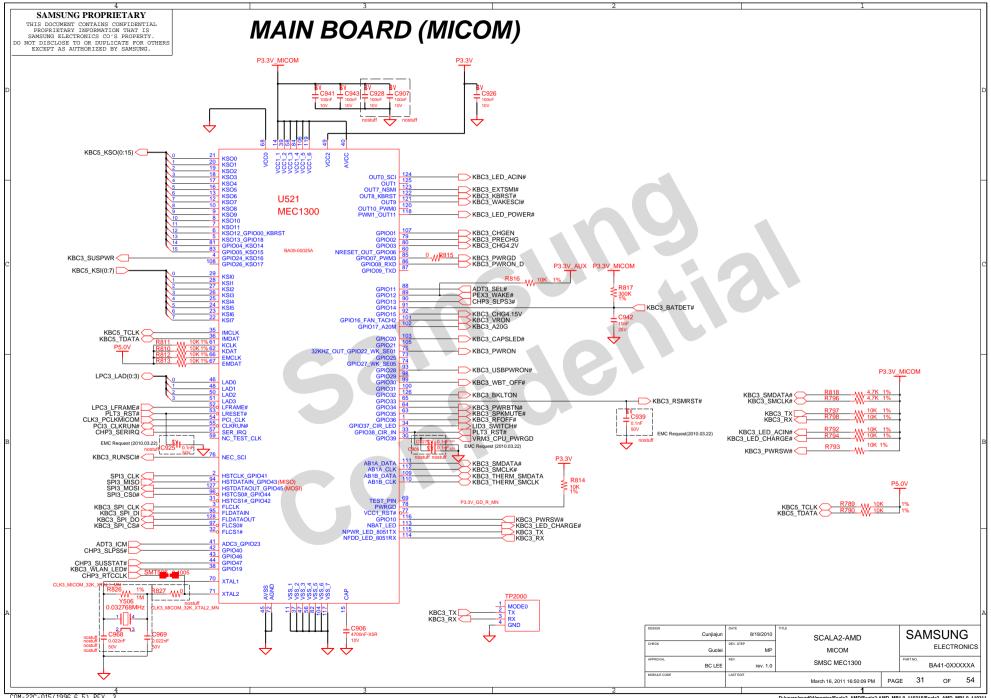


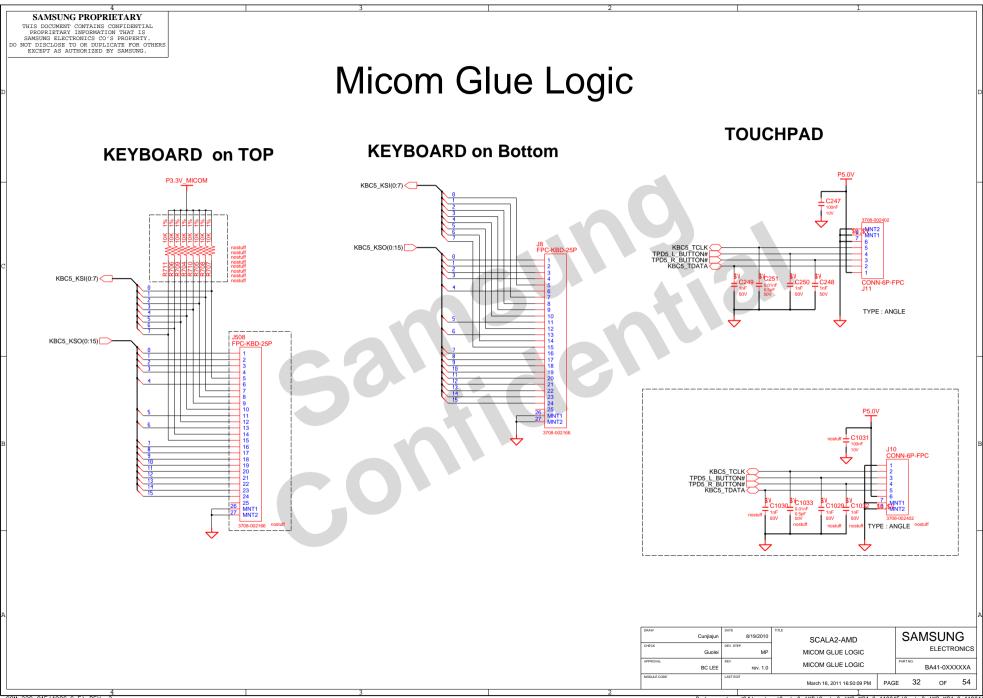


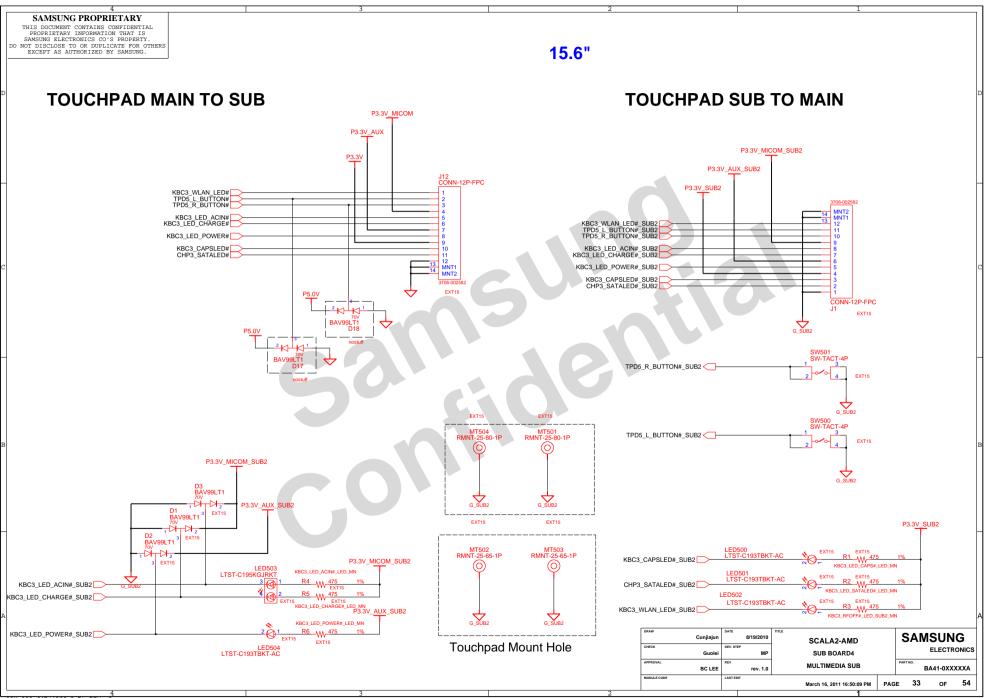
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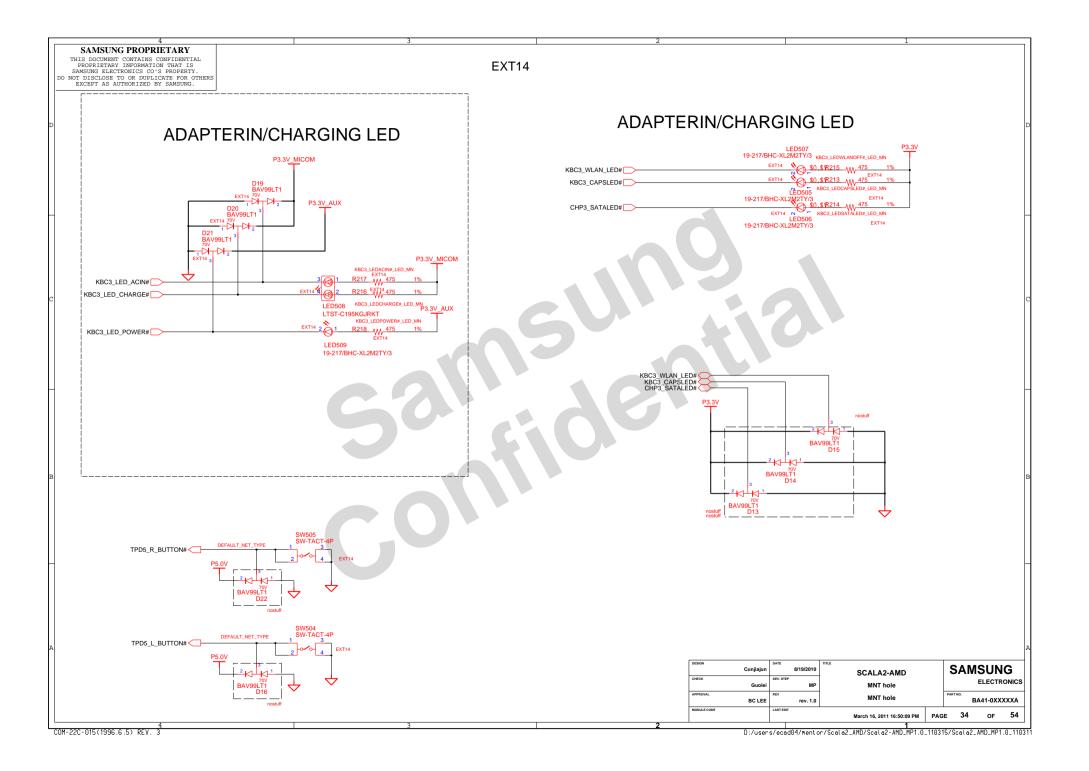


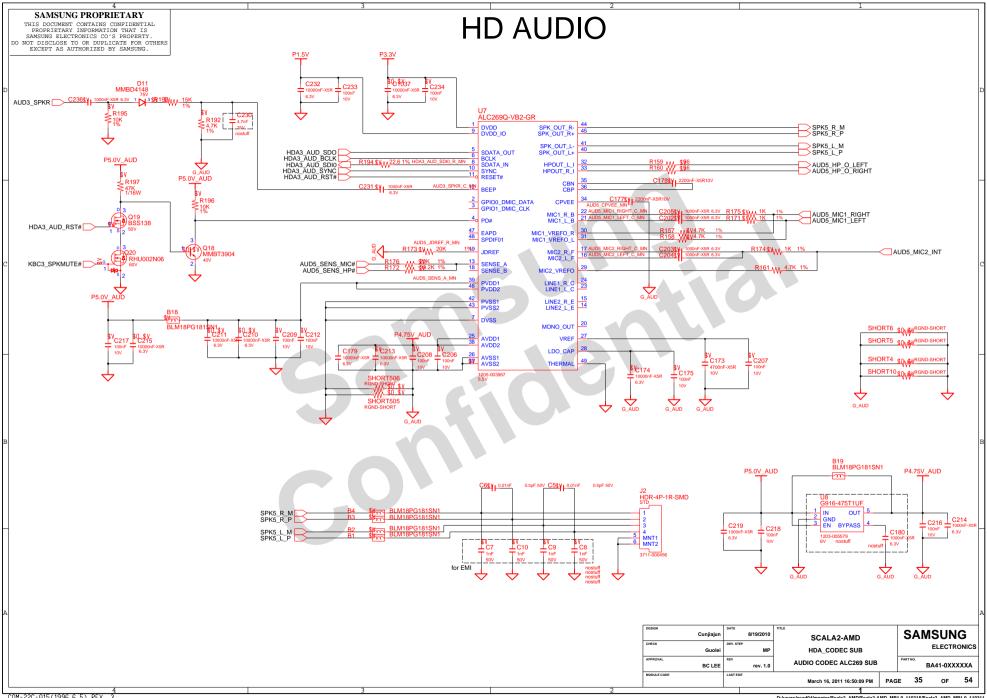


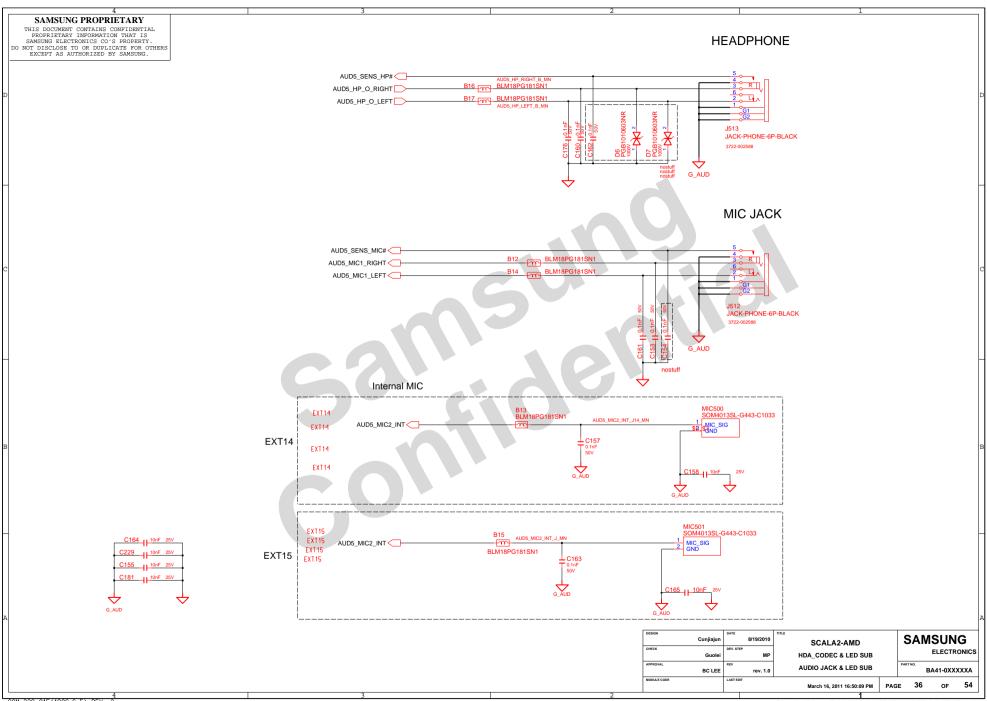


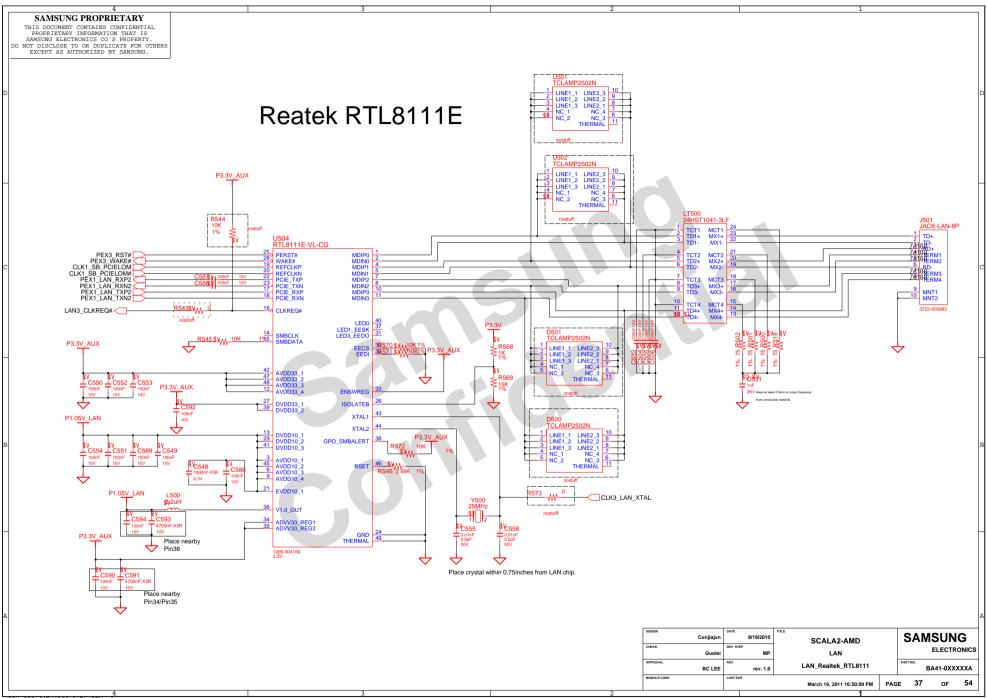


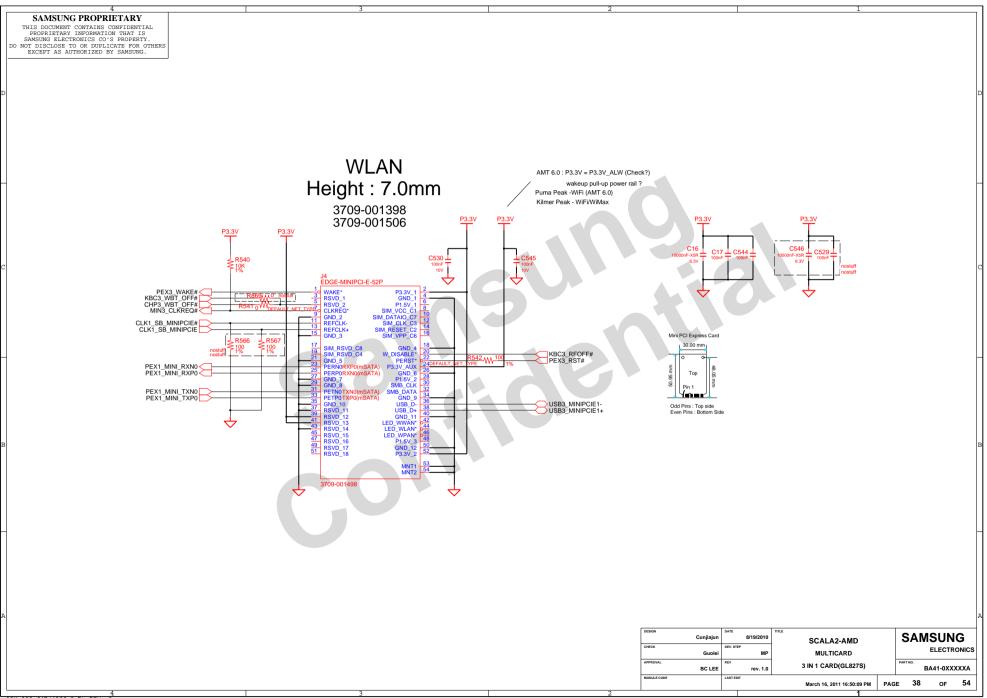


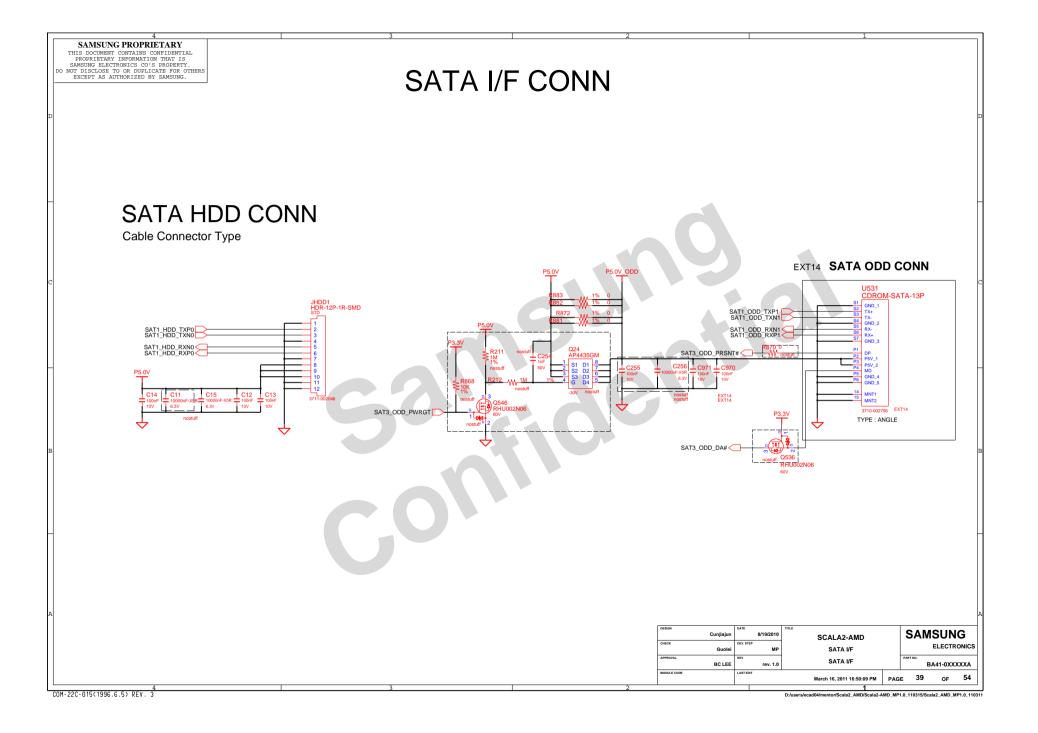


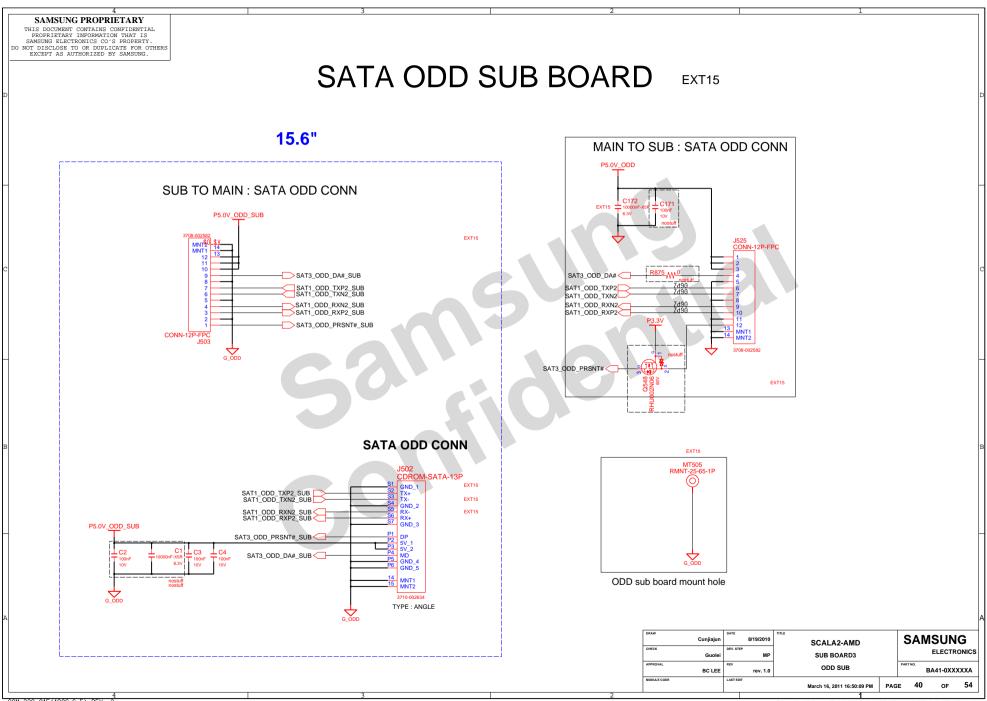


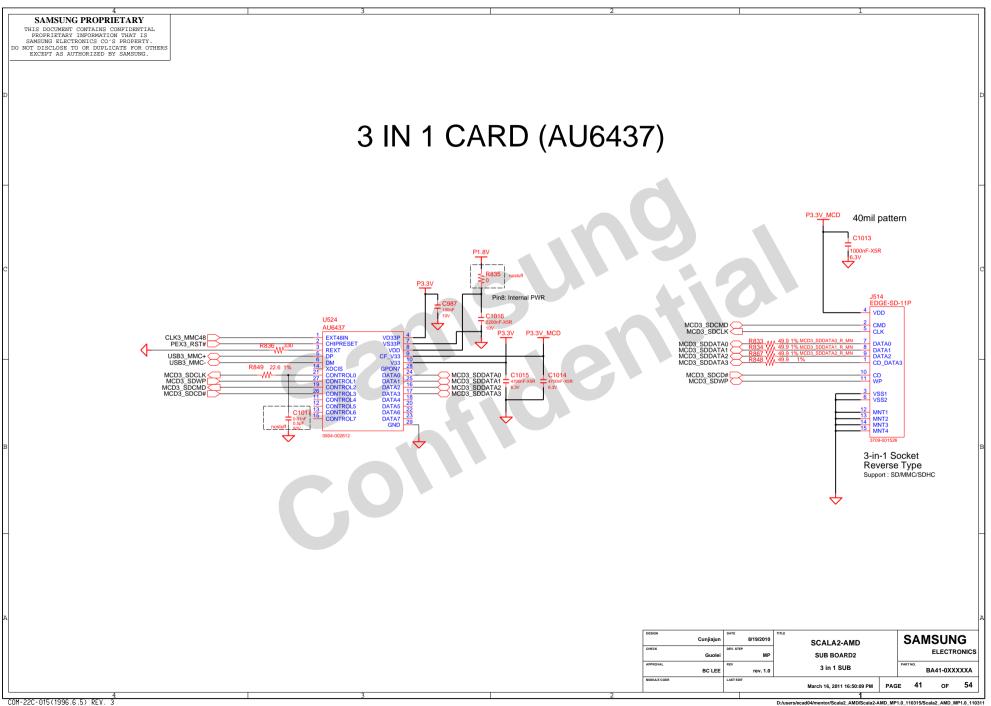


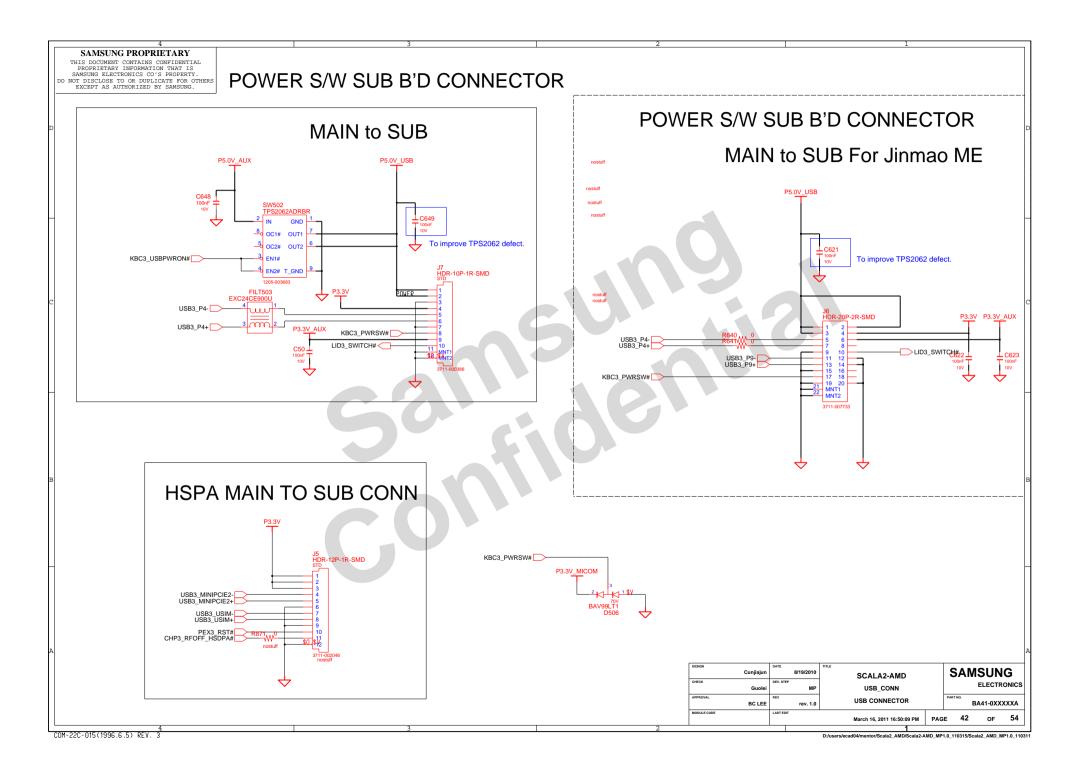


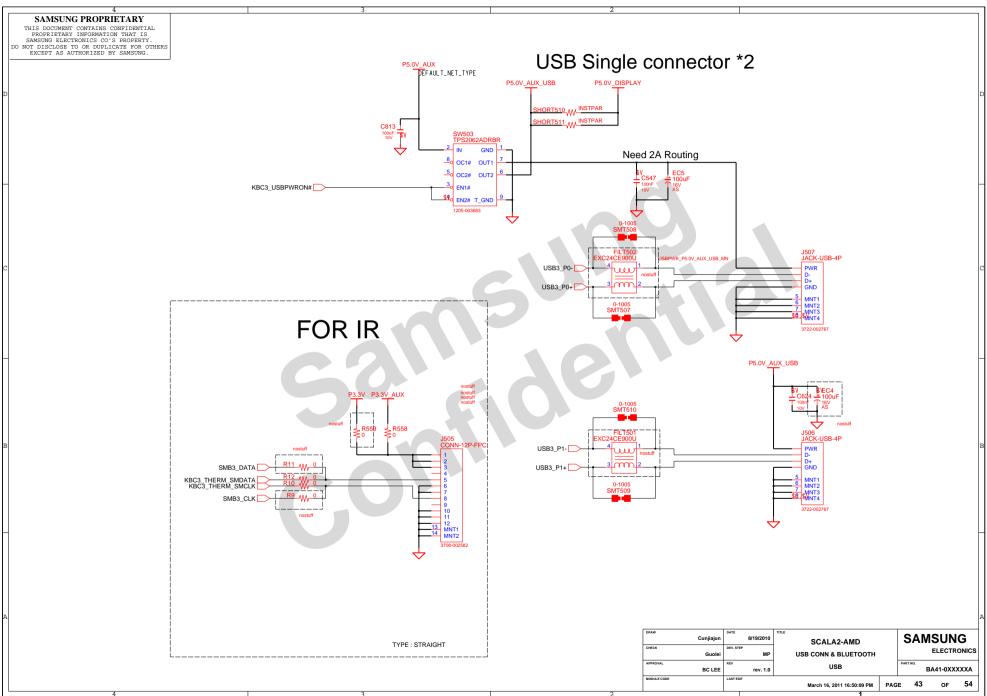


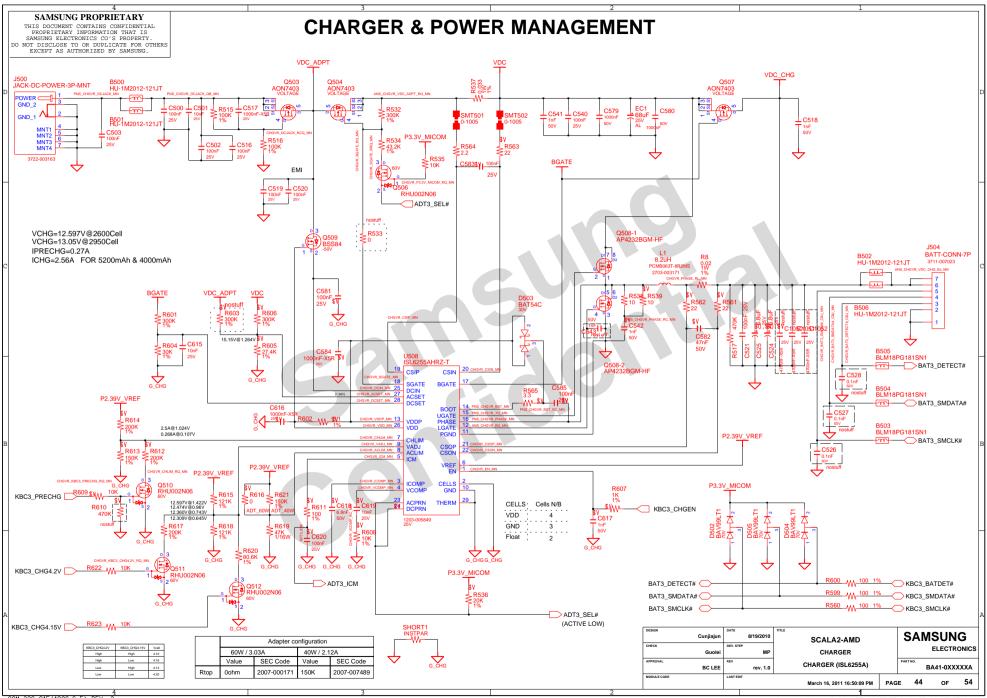


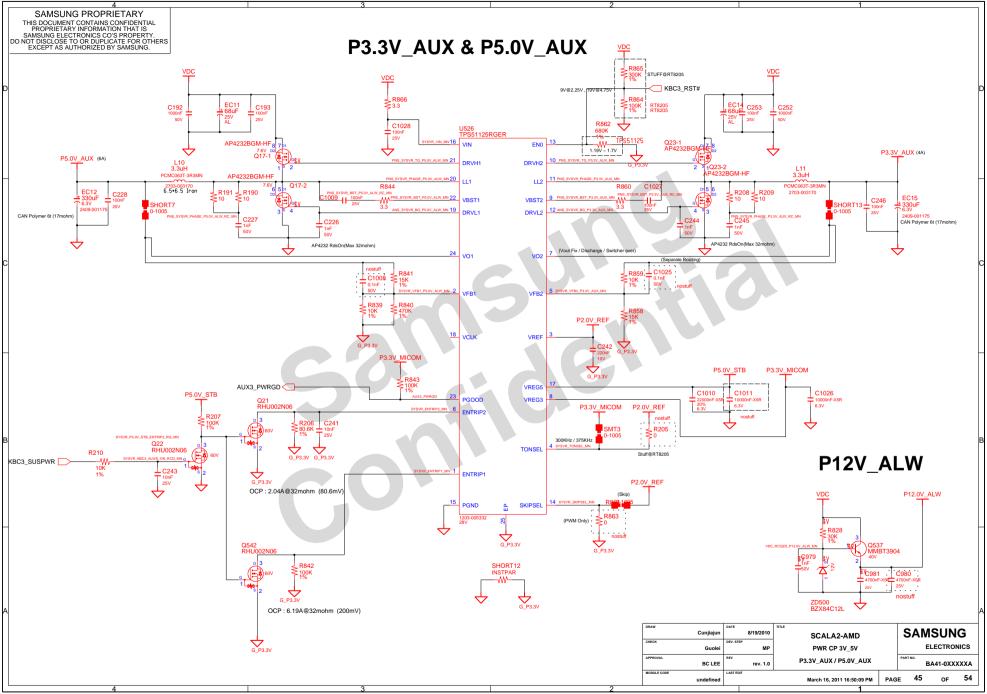


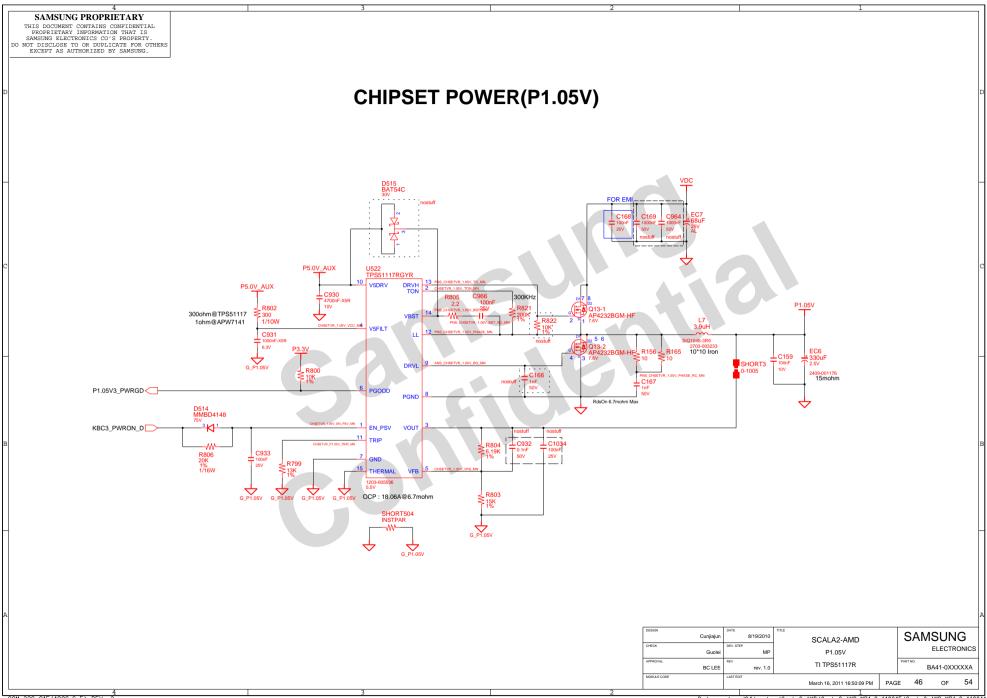


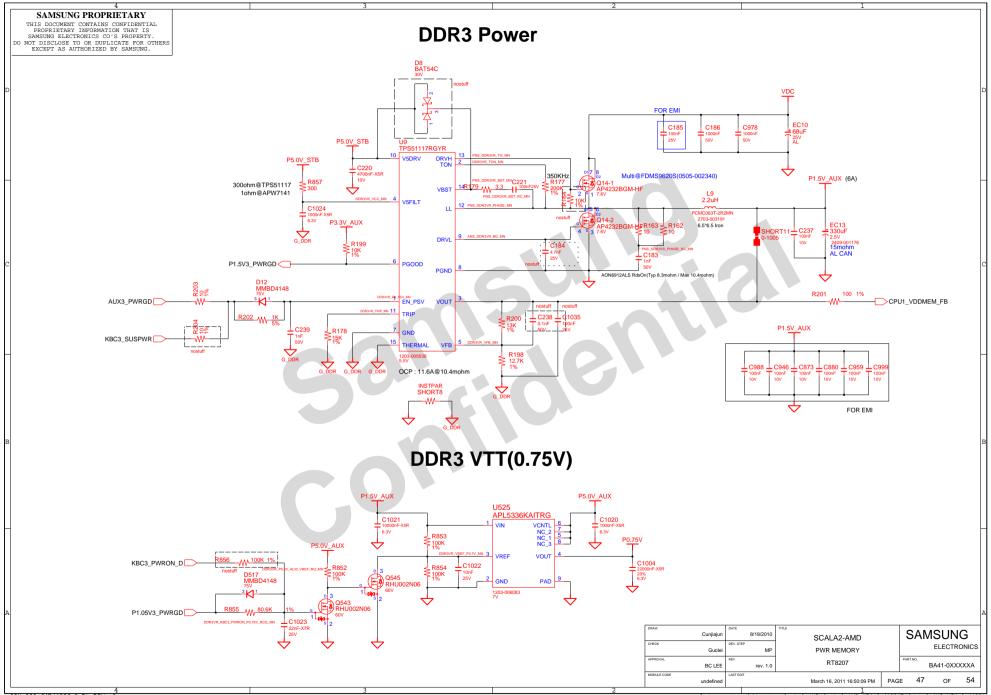


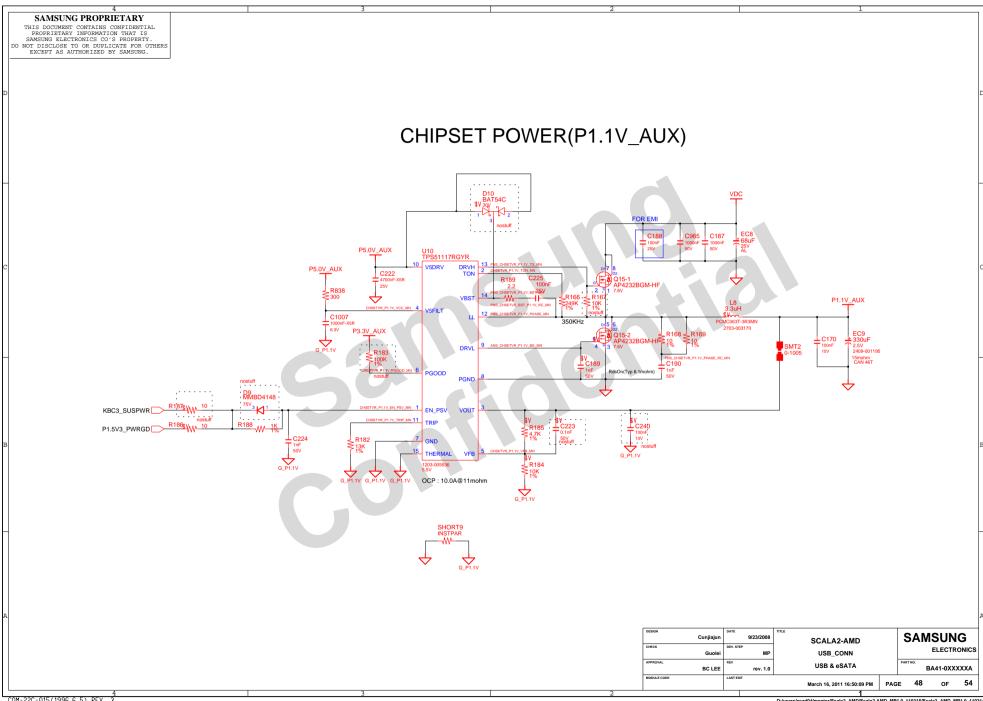


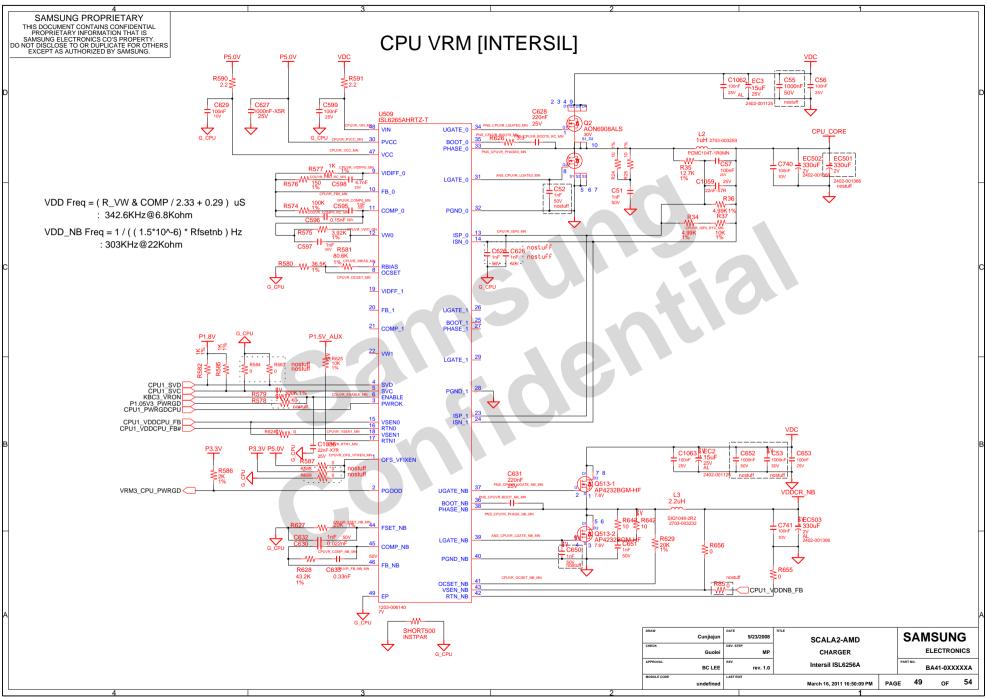


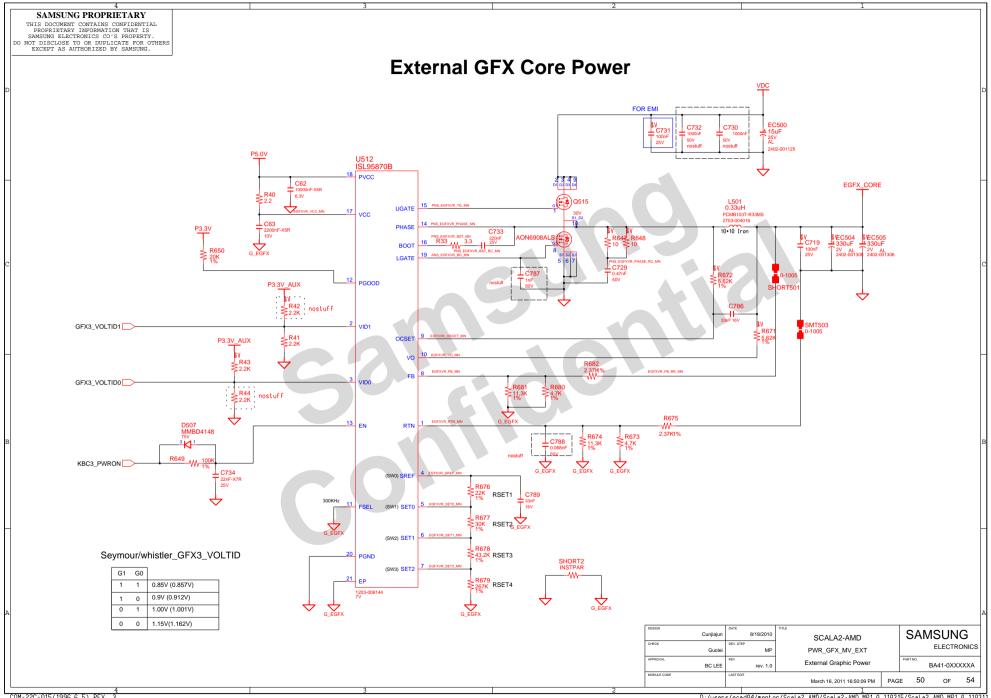


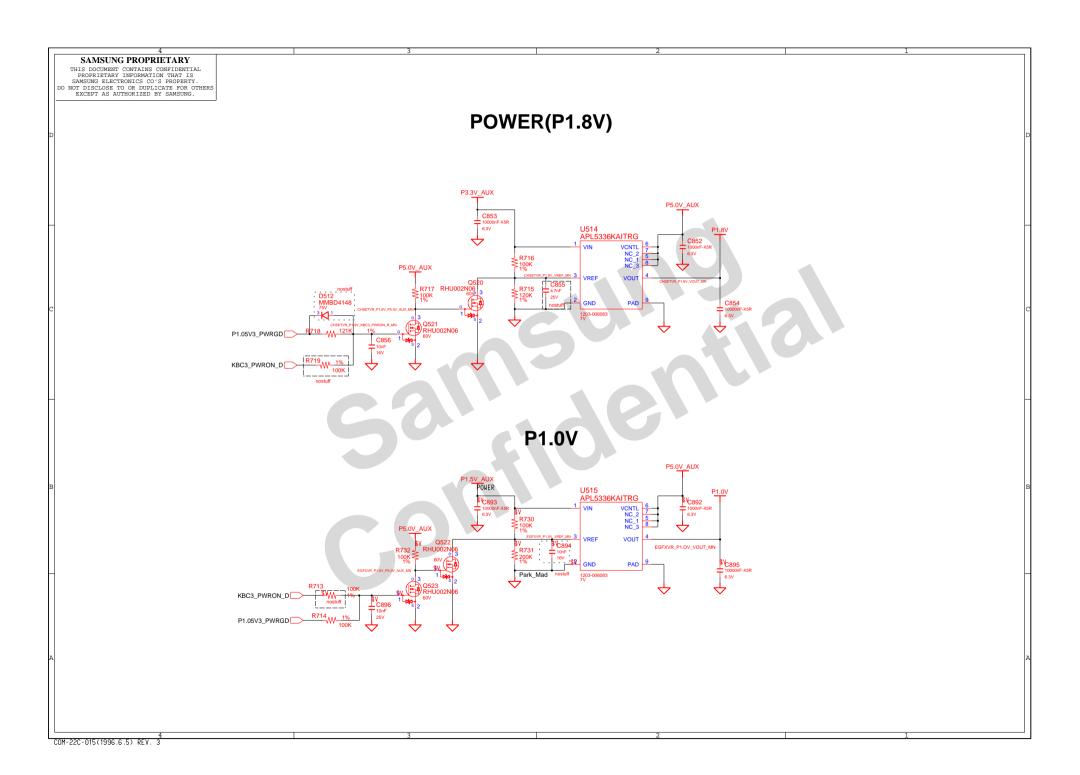


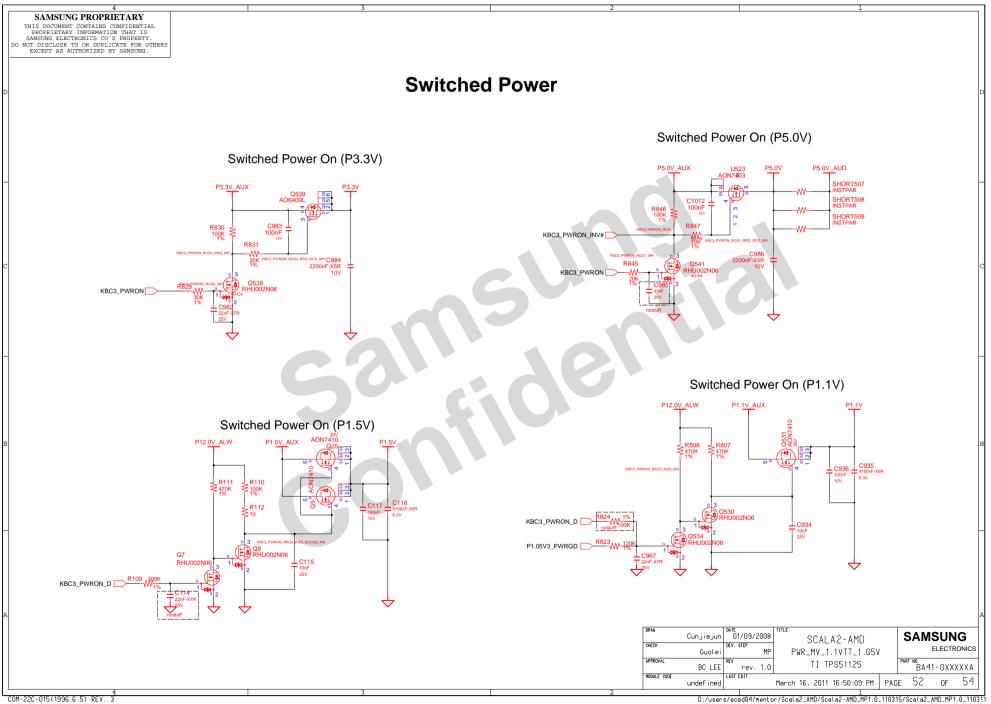


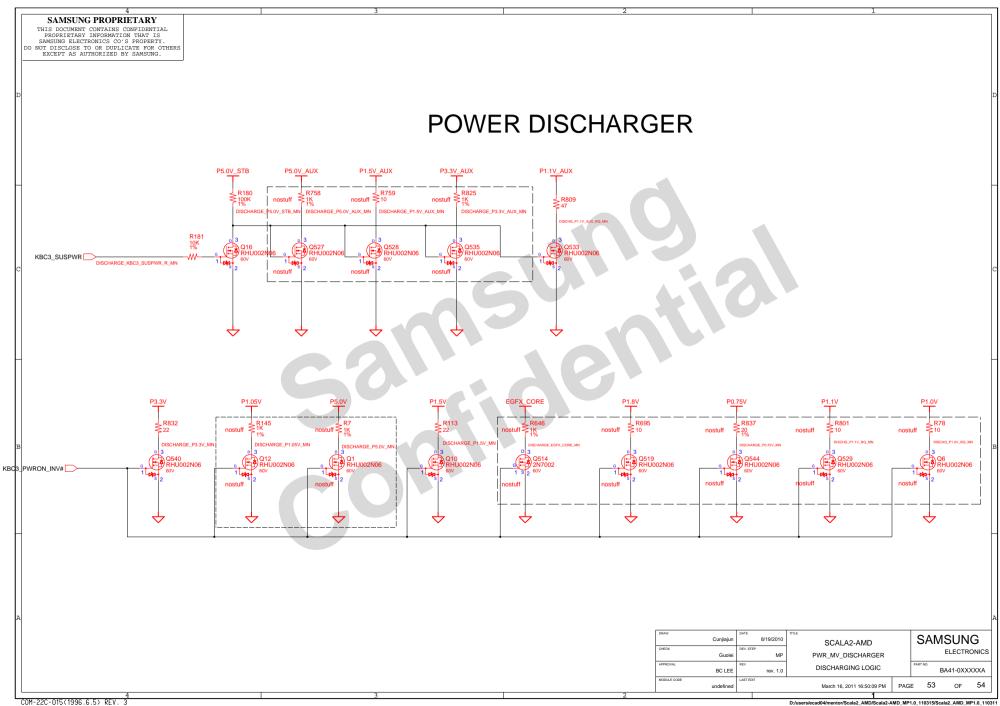


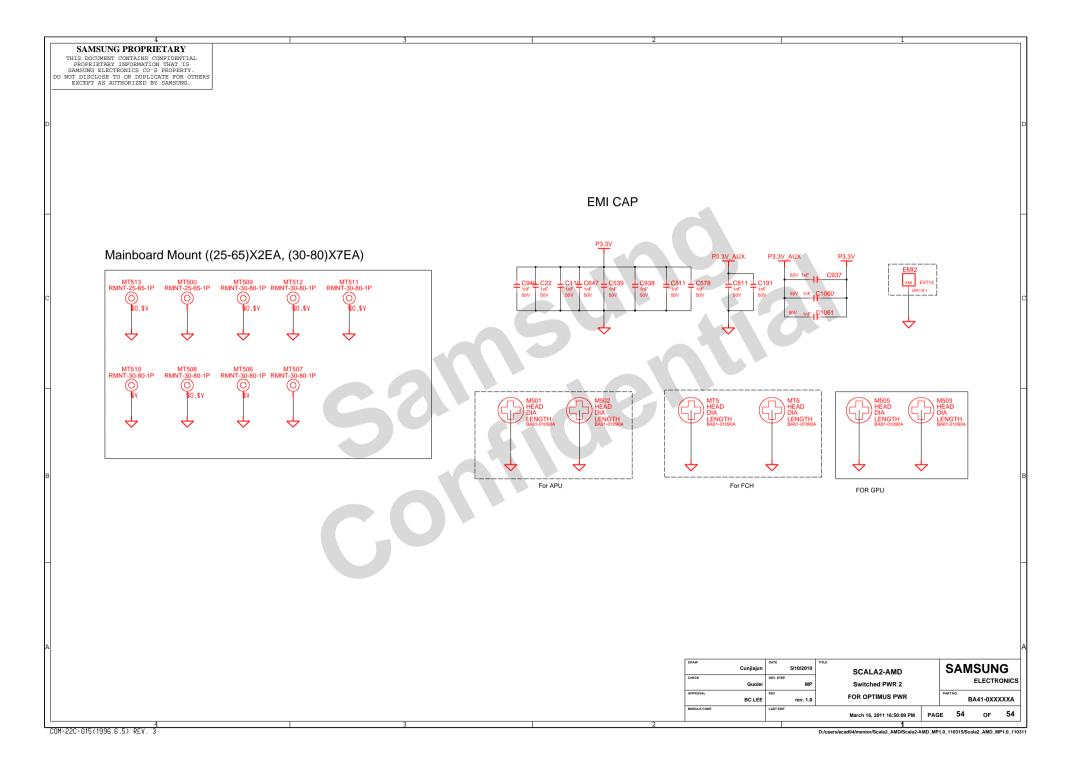












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