256M (16Mx16bit) Hynix SDRAM Memory

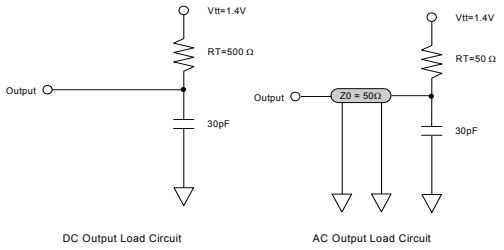
Memory Cell Array

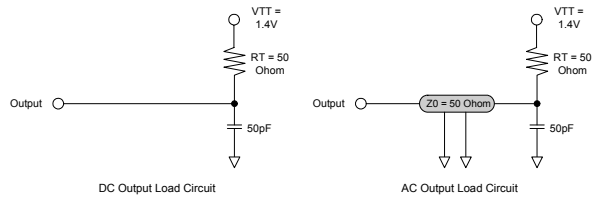
- Organized as 4banks of 4,194,304 x 16

Document Title

256Mbit (16M x16) Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	Dec. 2005	Preliminary
0.2	Define : Current value (Page 11 ~ 12)	Apr. 2006	Preliminary
0.3	1. Cerrect : 1-1. 4Banks x 2Mbits x32 --> 4Banks x 4Mbits x16(Ordering information; Page 06). 1-2. VDDQ / VSSQ : Power supply for output buffers (Page 08). 2. Remove : Special Power consumption function of Auto TCSR(Temperature Compensated Self Refresh) and PASR(Partial Array Self Refresh). 3. Define : AC Operating TEST condition and AC / DC Output Load circuit (page 10 & 11). Before :  	Jun. 2006	Preliminary

Revision No.	History	Draft Date	Remark
0.3	After :  4. Specification change : 4-1. IOH / IOL (Page 11) Before : -2 / 2mA --> After : -4 / 4mA. 4-2. tDH, tAH, tCKH, tCH (Page 13) Before : 1.0ns --> After : 0.8ns.	Jun. 2006	Preliminary
0.4	1. Delete 1-1. COMMAND TRUTH TABLE for Extended Mode Register (Page15) 2. Insert 2-1. DQM TRUTH TABLE (Page16) 3. Specitication change : 3-1. IDD6 Before : 3 / 1.5mA --> After : 2 / 1mA 3-2. IDD3N Before :25mA --> After : 30mA 3-3. tCHW / tCLW Change [HY57V561620F(L)T(P)-6x] Before :2.0ns --> After : 2.5ns	Jun. 2006	Preliminary
1.0	Final Ver.	Sep. 2006	Final
1.1	1. Update 1-1. Ordering Information table (Page 5) 200Mhz products added 1-2. DC Characteristics II (Page 11) 200Mhz spec. added 1-3. AC Characteristics I (Page 12) 200Mhz spec. added 1-4 AC Characteristics II (Page 13) 200Mhz spec. added 2. Cerrect HY57V561620FT-6 --> HY57V561620FLT-6 (Ordering Information. Page 5)	Apr. 2008	Final
1.2	Revise (Command Truth Table / P.15) Burst Read Single Write : /WE H --> L	Dec. 2009	Final
1.3	Revise (P.12) Symbol "-6" tCK2 (CL2) : 7.5 --> 10ns	Dec. 2009	Final

DESCRIPTION

The Hynix Synchronous DRAM is suited for advaced-consumer application which use the batteries such as Image display application (Digital still camera etc.) and portable applications (portable multimedia player and portable audio player). Also, Hynix SDRAMs is used high-speed consumer applications. Short for Hynix Synchronous DRAM, a type of DRAM that can run at much higher clock speeds memory.

The Hynix HY57V561620F(L)T(P) Synchronous DRAM is 268,435,456bit CMOS Synchronous DRAM, ideally suited for the consumer memory applications which requires large memory density and high bandwidth. It is organized as 4banks of 4,194,304 x 16 I/O.

Synchronous DRAM is a type of DRAM which operates in synchronization with input clock. The Hynix Synchronous DRAM latch each control signal at the rising edge of a basic input clock (CLK) and input/output data in synchronization with the input clock (CLK). The address lines are multiplexed with the Data Input/ Output signals on a multiplexed x16 Input/ Output bus. All the commands are latched in synchronization with the rising edge of CLK.

The Synchronous DRAM provides for programmable read or write Burst length of Programmable burst lengths: 1, 2, 4, 8 locations or full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. The Synchronous DRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compartible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, randon-access operation.

Read and write accesses to the Hynix Synchronous DRAM are burst oriented;
accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

All inputs are LVTTL compatible. Devices will have a V_{DD} and V_{DDQ} supply of 3.3V (nominal).

256Mb Synchronous DRAM(16M x 16) FEATURES

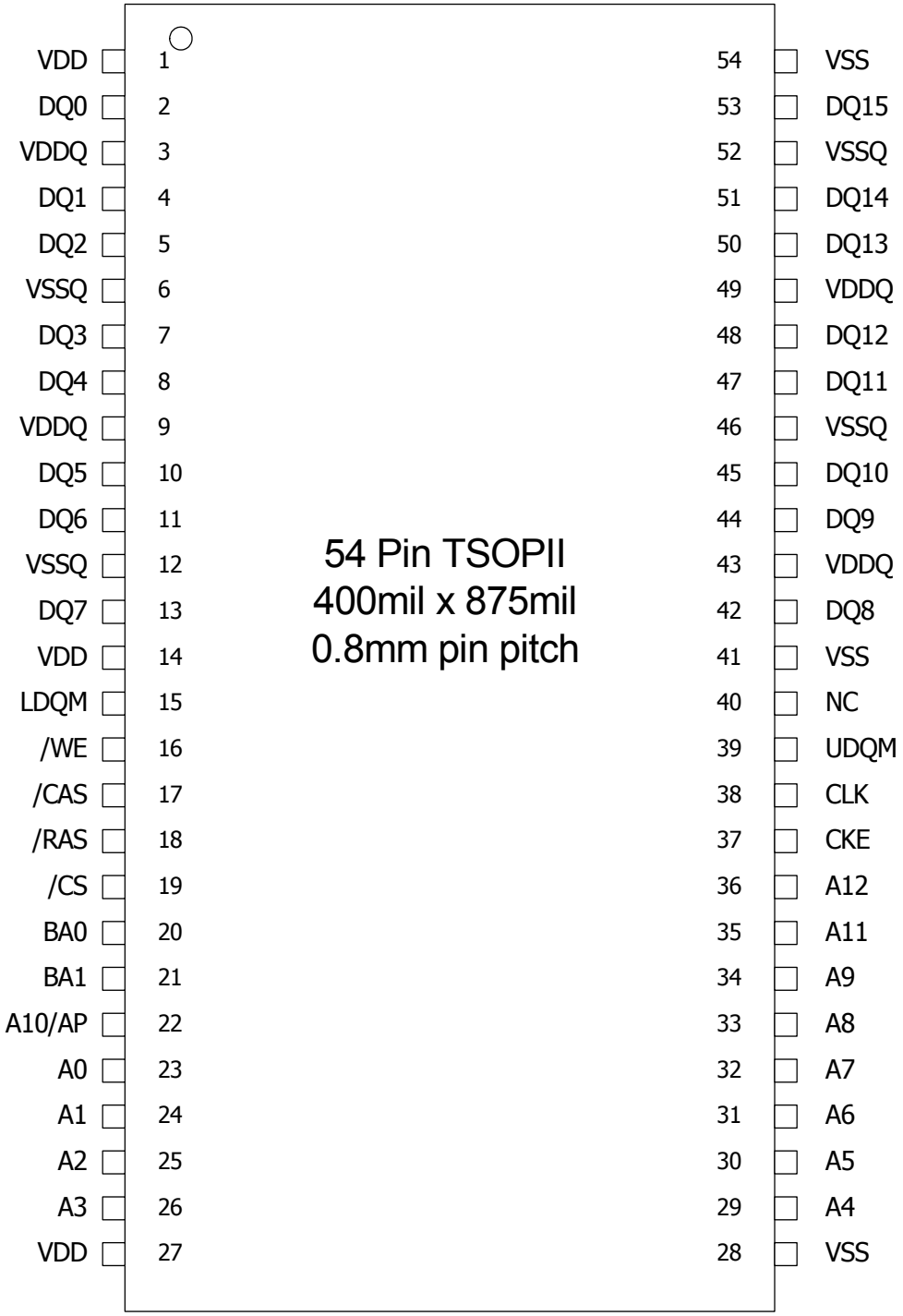
- Standard SDRAM Protocol
- Internal 4bank operation
- Power Supply Voltage : V_{DD} = 3.3V, V_{DDQ} = 3.3V
- All device pins are compatible with LVTTL interface
- Low Voltage interface to reduce I/O power
- 8,192 Refresh cycles / 64ms
- Programmable CAS latency of 2 or 3
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- $0^{o}C$ ~ $70^{o}C$ Operation
- Package Type : 54_Pin TSOPII (Lead Free, Lead)
  HY57V561620F(L)TP Series : Lead Free
  HY57V561620F(L)T Series : Leaded

ORDERING INFORMATION

Part Number	Clock Frequency	CAS Latency	Power	Voltage	Organization	Interface	54Pin TSOP
HY57V561620FT-6	166MHz	3	Normal	3.3V	4Banks x 4Mbits x16	LVTTL	Leaded
HY57V561620FT-H	133MHz	3					
HY57V561620FT-5	200MHz	3					
HY57V561620FLT-6	166MHz	3	Low Power				
HY57V561620FLT-H	133MHz	3					
HY57V561620FLT-5	200MHz	3					
HY57V561620FTP-6	166MHz	3	Normal				Lead Free
HY57V561620FTP-H	133MHz	3					
HY57V561620FTP-5	200MHz	3					
HY57V561620FLTP-6	166MHz	3	Low Power				
HY57V561620FLTP-H	133MHz	3					
HY57V561620FLTP-5	200MHz	3					

Note:
1. HY57V561620FT(P) Series: Normal power
2. HY57V561620FLT(P) Series: Low Power
3. HY57V561620F(L)T Series: Leaded 54Pin TSOPII
4. HY57V561620F(L)TP Series: Lead Free 54Pin

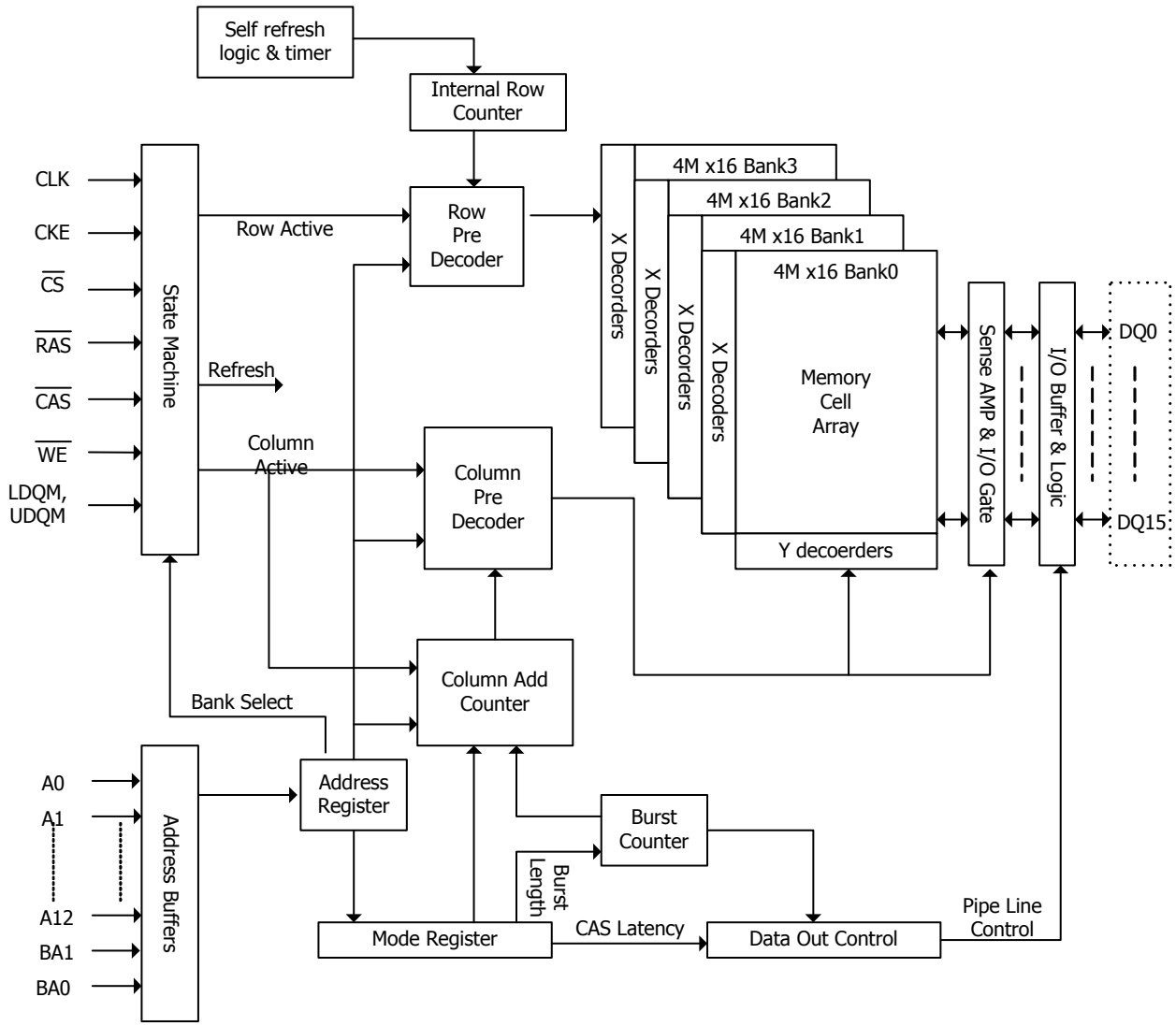
54 TSOP II Pin ASSIGNMENTS



54_TSOPII Pin DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CLK	INPUT	Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	INPUT	Clock Enable: Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	INPUT	Chip Select: Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	INPUT	Bank Address: Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A12	INPUT	Row Address: RA0 ~ RA12, Column Address: CA0 ~ CA8 Auto-precharge flag: A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	I/O	Data Mask: Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	I/O	Data Input / Output: Multiplexed data input / output pin
V_{DD} / V_{SS}	SUPPLY	Power supply for internal circuits and input buffers
V_{DDQ} / V_{SSQ}	SUPPLY	Power supply for output buffers
NC	-	No connection : These pads should be left unconnected

FUNCTIONAL BLOCK DIAGRAM
4Mbit x 4banks x 16 I/O Synchronous DRAM



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION

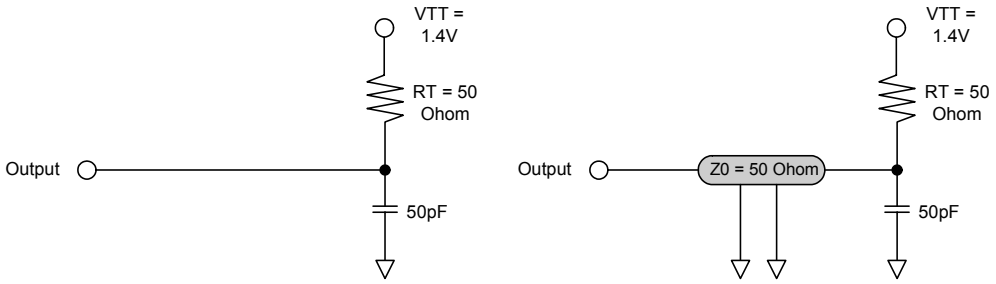
Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.6	V	1
Input High Voltage	V_{IH}	2.0	V_{DDQ} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	0.8	V	1, 3

Note: 1. All voltages are referenced to V_{SS} = 0V.
2. V_{IH}(Max) is acceptable VDDQ + 2V for a pulse width with <= 3ns of duration.
3. V_{IL}(min) is acceptable -2.0V for a pulse width with <= 3ns of duration.

AC OPERATING TEST CONDITION (T_A= 0 to 70°C, V_{DD}=3.3±0.3V / V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	V_{IH} / V_{IL}	2.4 / 0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note: 1. See Next Page



DC Output Load Circuit

AC Output Load Circuit

CAPACITANCE (f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.0	4.0	pF
	A0 ~ A12, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI2	2.0	4.0	pF
	LDQM, UDQM	CI3	2.0	4.0	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	3.5	6.5	pF

DC CHARACTERRISTICS I (T_A= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	I_{LI}	-1	1	uA	1
Output Leakage Current	I_{LO}	-1	1	uA	2
Output High Voltage	V_{OH}	2.4	-	V	IOH = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	IOL = +4mA

Note:
1. VIN = 0 to 3.6V, All other balls are not tested under VIN =0V
2. DOUT is disabled, VOUT=0 to 3.6

DC CHARACTERISTICS II (TA= 0 to 70°C)

Parameter	Symbol	Test Condition		Speed			Unit	Note
				5	6	H		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		110	100	90	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		1.0			mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		1.0			mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		15			mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		8				
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		3			mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		3				
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		30			mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		20				
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active		110	100	90	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active		190	180	170	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	Normal	2.0			mA	3
			Low Power	1.0				

Note: 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3. HY57V561620FT(P) Series: Normal, HY57V561620FLT(P) Series: Low Power

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	5		6		H		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CL = 3	tCK3	5.0	1000	6.0	1000	7.5	1000	ns	
	CL = 2	tCK2	10		10	1000	10	1000	ns	
Clock High Pulse Width		tCHW	2.0	-	2.5	-	2.5	-	ns	1
Clock Low Pulse Width		tCLW	2.0	-	2.5	-	2.5	-	ns	1
Access Time From Clock	CL = 3	tAC3	-	4.5	-	5.4	-	5.4	ns	2
	CL = 2	tAC2	-	6.0	-	6	-	6	ns	2
Data-out Hold Time		tOH	2.0	-	2.0	-	2.5	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.0	-	1.0	-	1.0	-	ns	
CLK to Data Output in High-Z Time	CL = 3	tOHZ3	-	4.5	2.7	5.4	2.7	5.4	ns	
	CL = 2	tOHZ2	-	6.0	2.7	5.4	3	6	ns	

Note:

1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & t_F > 1ns, then [(t_R+t_F)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If t_R > 1ns, then (t_R/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	5		6		H		Unit	Note
			Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	55	-	60	-	63	-	ns	
	Auto Refresh	tRRC	55	-	60	-	63	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	15	-	18	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	38.7	100K	42	100K	42	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	15	-	18	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	10	-	12	-	15	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	2	-	2	-	2	-	CLK	
Data-In to Active Command		tDAL	tDPL + tRP							
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output High-Z	CL = 3	tPROZ3	3	-	3	-	3	-	CLK	
	CL = 2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tDPE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note: 1. A new command can be given tRC after self refresh exit.

BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full page	Reserved

COMMAND TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10 /AP	BA	Note
Mode Register Set	H	X	L	L	L	L	X	Op Code			
No Operation	H	X	L	H	H	H	X	X			
Device Deselect	H	X	H	X	X	X	X	X			
Bank Active	H	X	L	L	H	H	X	Row Address		V	
Read	H	X	L	H	L	H		Col-umn	L	V	
Read with Autoprecharge	H	X	L	H	L	H	X	Col-umn	H	V	
Write	H	X	L	H	L	L	X	Col-umn	L	V	
Write with Autoprecharge	H	X	L	H	L	L	X	Col-umn	H	V	
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank	H	X	L	L	H	L	X	X	L	V	
Burst stop	H	X	L	H	H	L	X	X			
DQM	H	X	X				V	X			2
Auto Refresh	H	H	L	L	L	H	X	X			
Burst-Read Single-Write	H	X	L	L	L	L	X	A9 Pin High (Other Pins OP code)			
Self Refresh Entry	H	L	L	L	L	H	X	X			
Self Refresh Exit	L	H	H	X	X	X	X	X			1
			L	H	H	H					
Precharge Power Down Entry	H	L	H	X	X	X	X	X			
			L	H	H	H					
Precharge Power Down Exit	L	H	H	X	X	X	X	X			
			L	H	H	H					
Clock Suspend Entry	H	L	H	X	X	X	X	X			
			L	V	V	V					
Clock Suspend Exit	L	H	X				X	X			

Note : 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. see to Next page (DQM TRUTH TABLE)

DQM TRUTH TABLE

Function	CKEn-1	CKEn	LDQM	UDQM
Data Write/Output enable	H	X	L	L
Data Mask/Output disable	H	X	H	H
Lower byte write/Output enable, Upper byte mask/Output disable	H	X	L	H
Lower byte Mask/Output disable, Upper byte write/Output enable	H	X	H	L

Note 1. H: High Level, L: Low Level, X: Don't Care
2. Write DQM Latency is 0 CLK and Read DQM Latency is 2 CLK

CURRENT STATE TRUTH TABLE (Sheet 1 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A*max*-A0	Description		
idle	L	L	L	L	OP CODE		Mode Register Set	Set the Mode Register	
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	5
	L	L	H	L	BA	X	Precharge	No Operation	
	L	L	H	H	BA	Row Add.	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation	3
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	3
Row Active	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Precharge	7
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write : optional AP(A10=H)	6
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read : optional AP(A10=H)	6
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8,9
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8
	L	H	H	H	X	X	No Operation	Continue the Burst	

CURRENT STATE TRUTH TABLE (Sheet 2 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A*max*-A0	Description		
Read	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	10
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8,9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (Sheet 3 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A*max*-A0	Description		
Precharging	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	No Operation: Bank(s) idle after tRP	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Bank(s) idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation: Bank(s) idle after tRP	
Row Activating	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,11,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tRCD	
Write Recovering	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write: Optional AP(A10=H)	
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read: Optional AP(A10=H)	9
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tDPL	

CURRENT STATE TRUTH TABLE (Sheet 4 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A*max*-A0	Description		
Write Recovering	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tDPL	
Write Recovering with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,9,12
	L	H	H	H	X	X	No Operation	No Operation: Precharge after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation: Precharge after tDPL	
Refreshing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after tRC	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after tRC	
Mode Register Accessing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after 2 clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after 2 clock cycles	

Note :

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if t_{RCD} is not satisfied.
7. Illegal if t_{RAS} is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RRD} is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.

CKE Enable(CKE) Truth TABLE (Sheet 2 of 1)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0, BA1	ADDR		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
			L	H	H	H	X	X		
	L	H	L	L	X	X	X	X	ILLEGAL	2
				X	L	X	X	X		
				X	X	L	X	X		
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	Auto Refresh	
	H	H	L	L	L	L	OP CODE		Mode Register Set	4
	H	L	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP CODE		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4

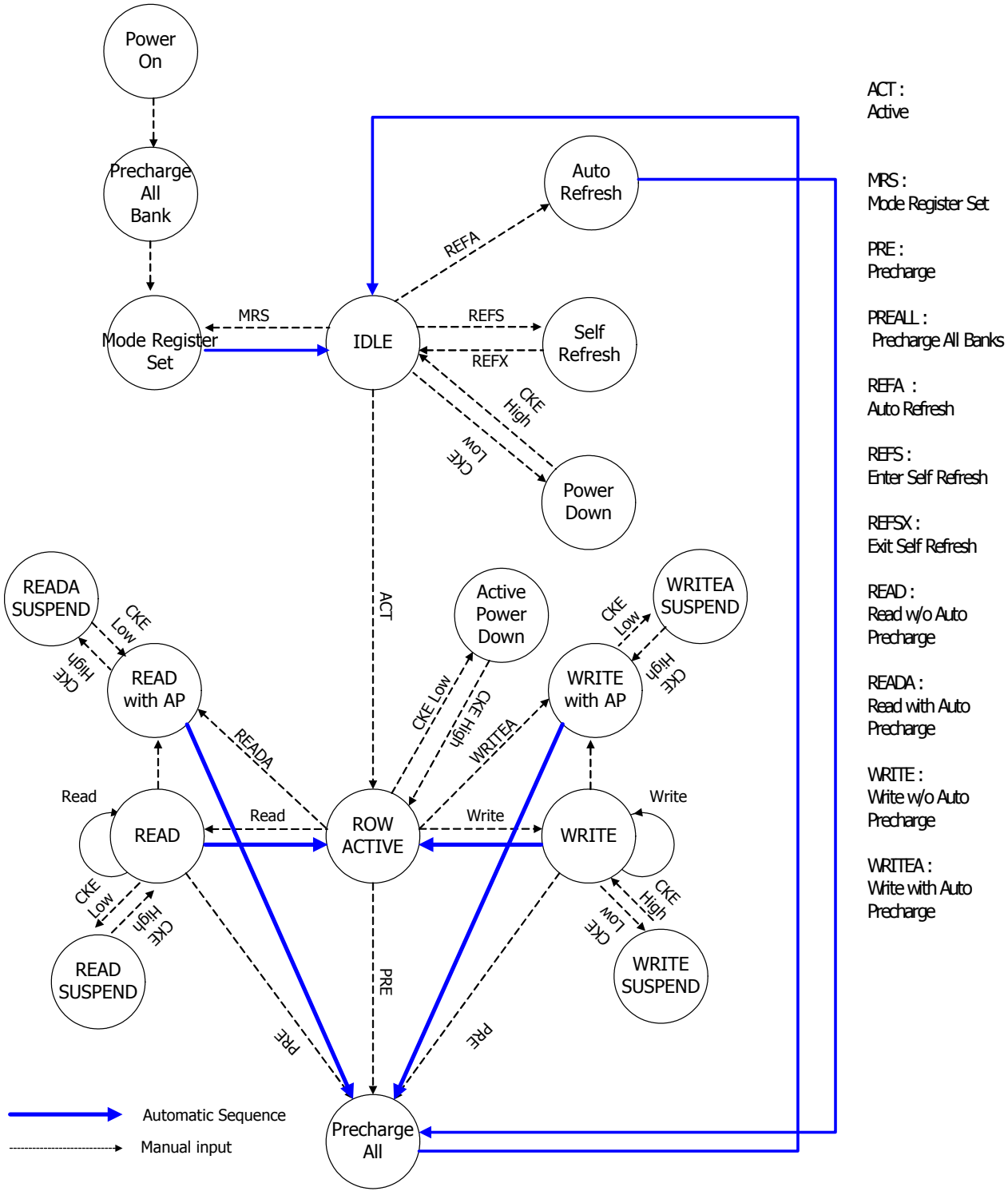
CKE Enable(CKE) Truth TABLE (Sheet 2 of 2)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0, BA1	ADDR		
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations of the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Note :
1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
3. The address inputs depend on the command that is issued.
4. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
5. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting deep power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high and is maintained for a minimum 200usec.

Mobile SDR SDRAM OPERATION

State Diagram



DESELECT

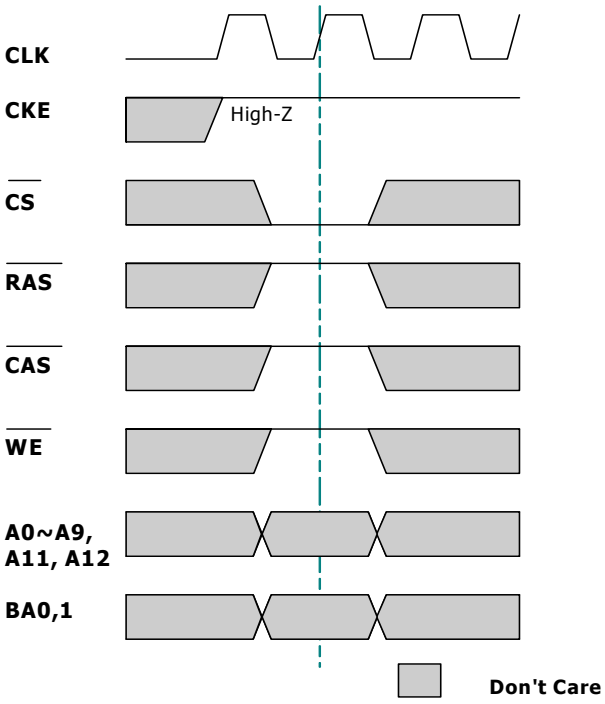
The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the SDRAM, the SDRAM ignore command input at the clock. However, the internal status is held. The Synchronous DRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION

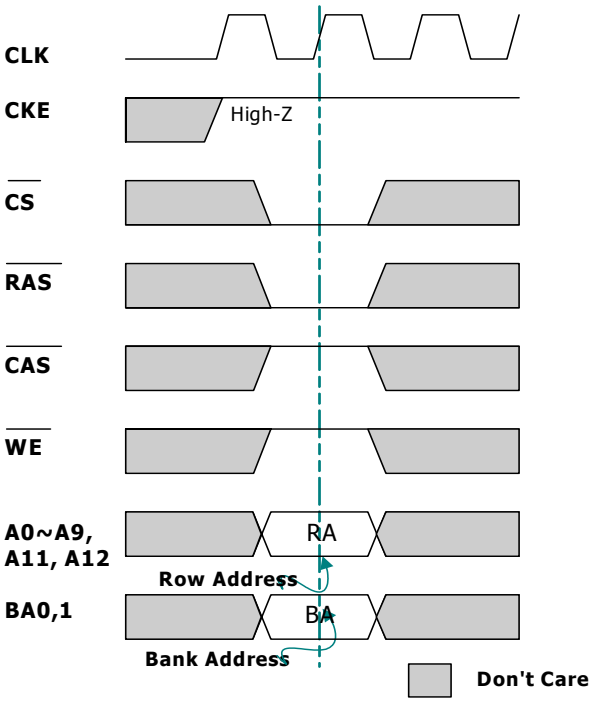
The NO OPERATION (NOP) command is used to perform a NOP to a SDRAM that is selected ($\overline{CS}$ = Low, $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = High). This command is not an execution command. However, the internal operations continue. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

ACTIVE

The Active command is used to activate a row in particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A12(or the highest address bit) selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. (see to next figure)



NOP command



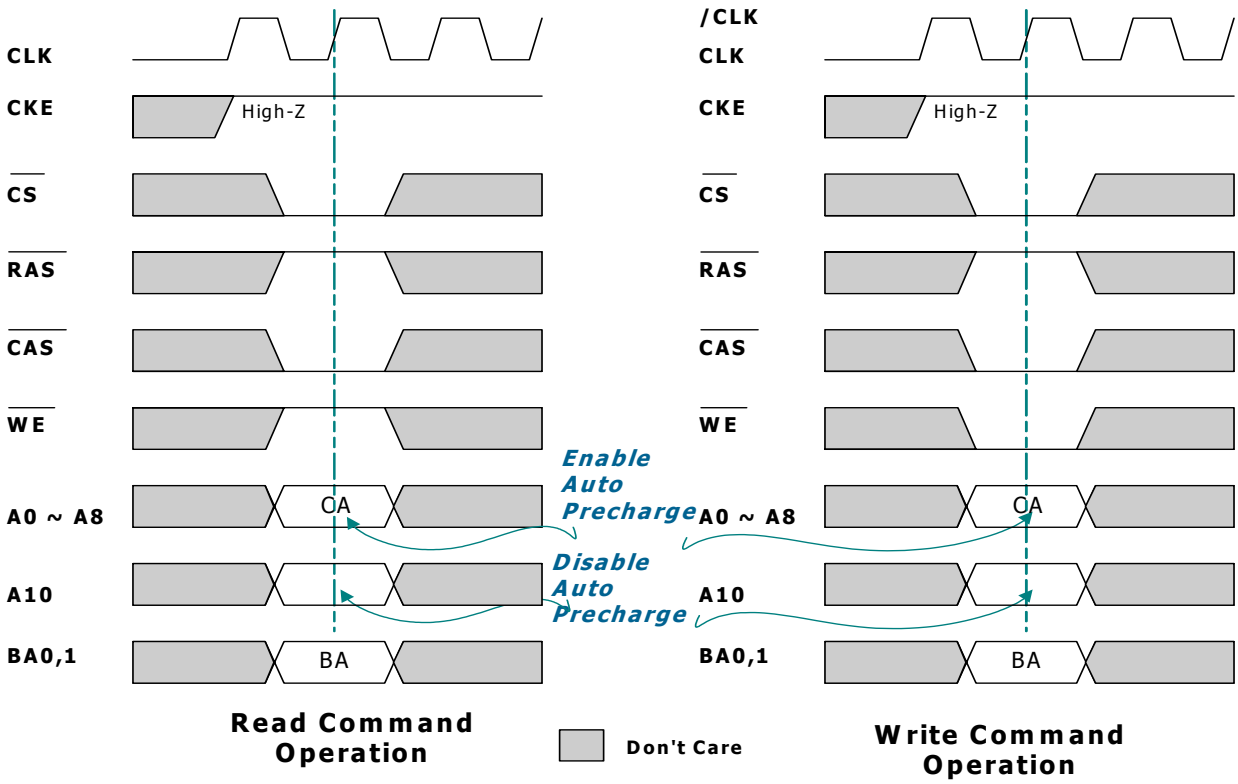
ACTIVATING A SPECIFIC
ROW IN A SPECIFIC BANK

READ / WRITE COMMAND

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto-precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued.

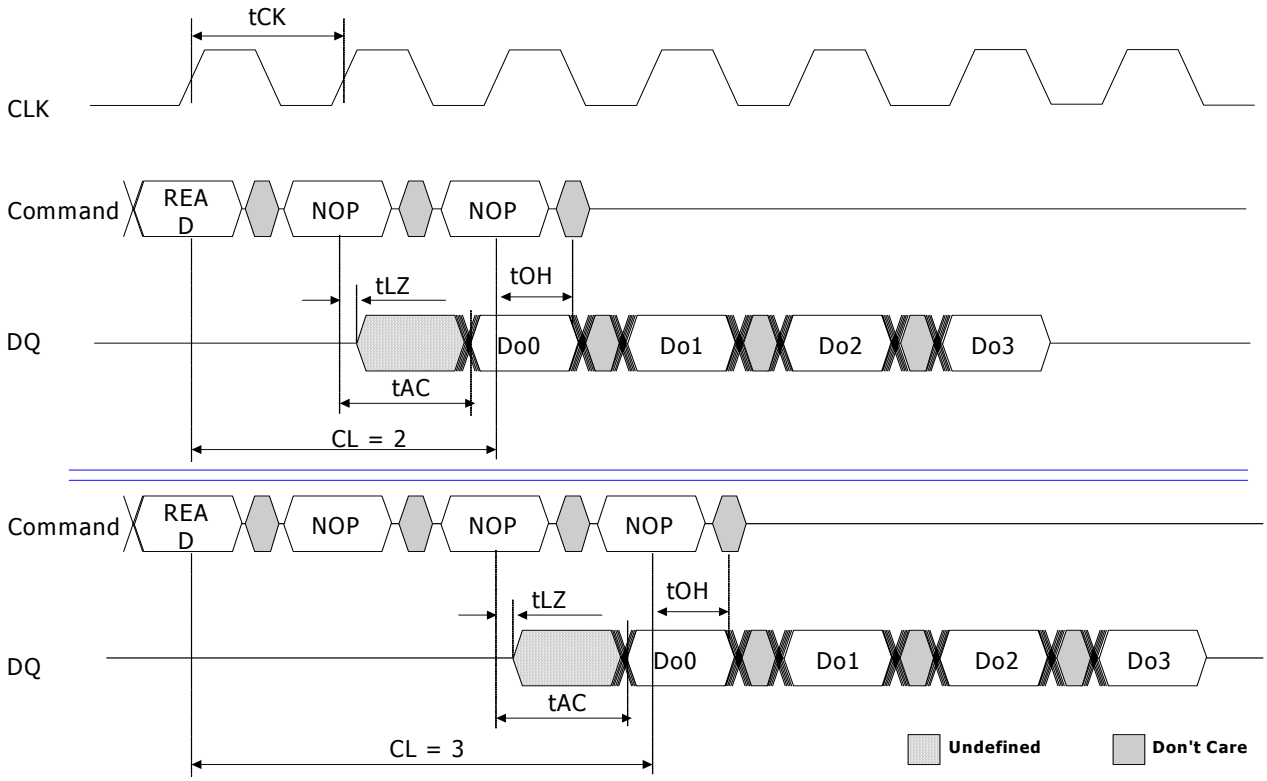
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto-precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access.



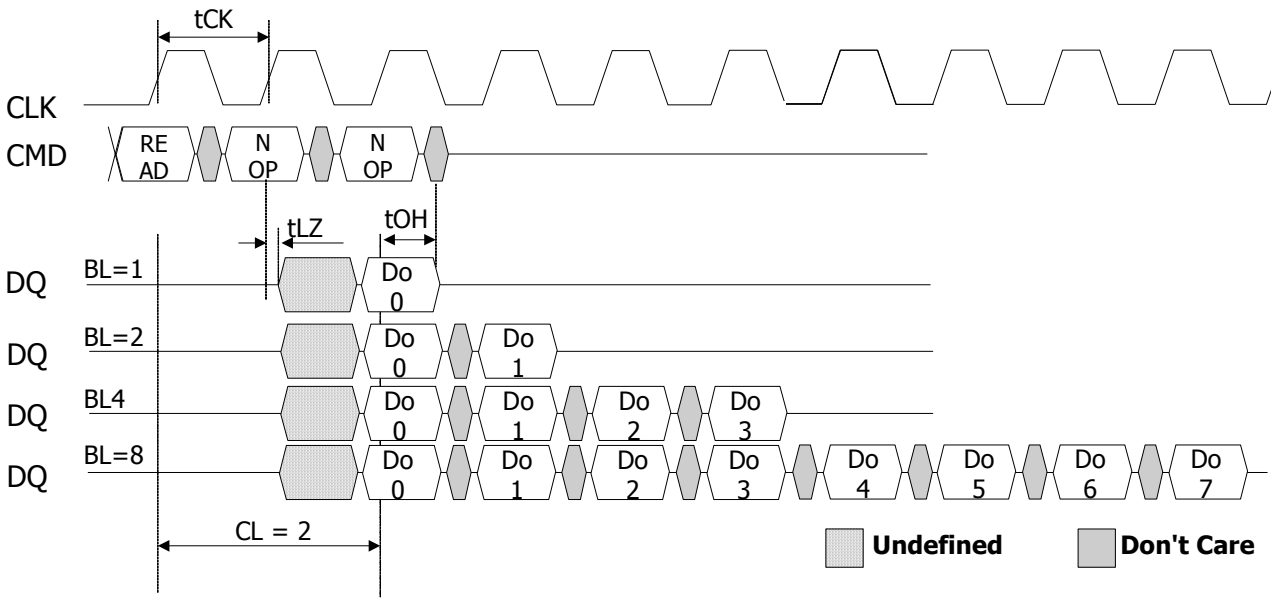
READ / WRITE COMMAND

READ

A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.
When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.
The /CAS latency and burst length must be specified at the mode register.



Read Burst Showing CAS Latency

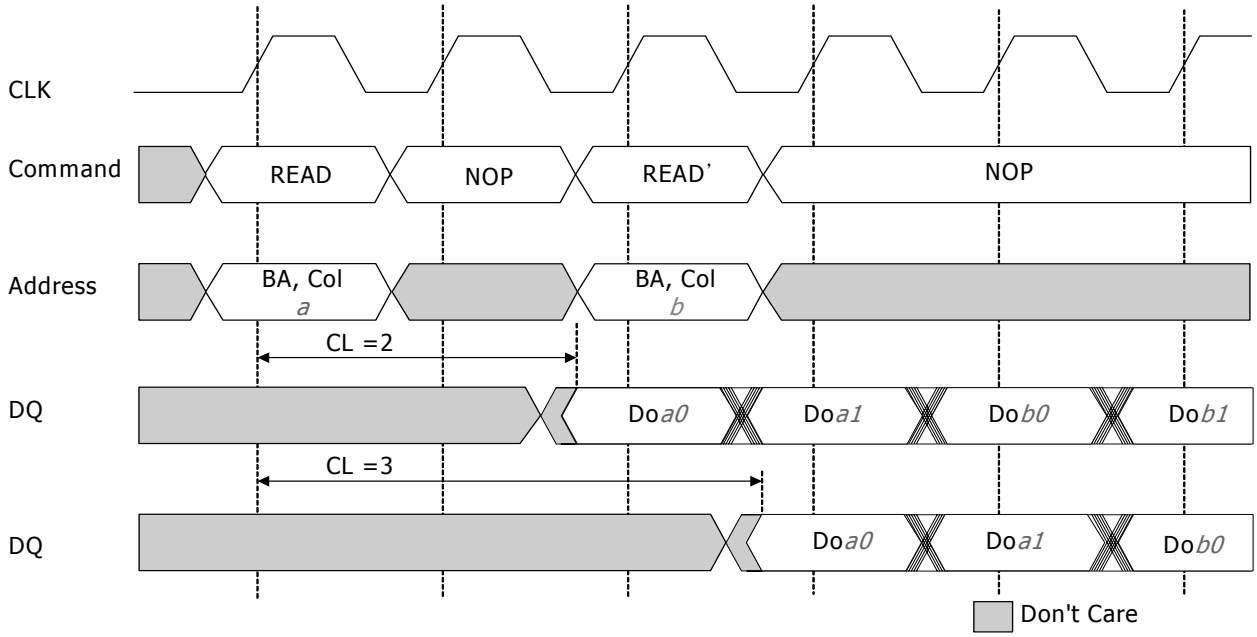


Read Burst Showing BL

READ to READ

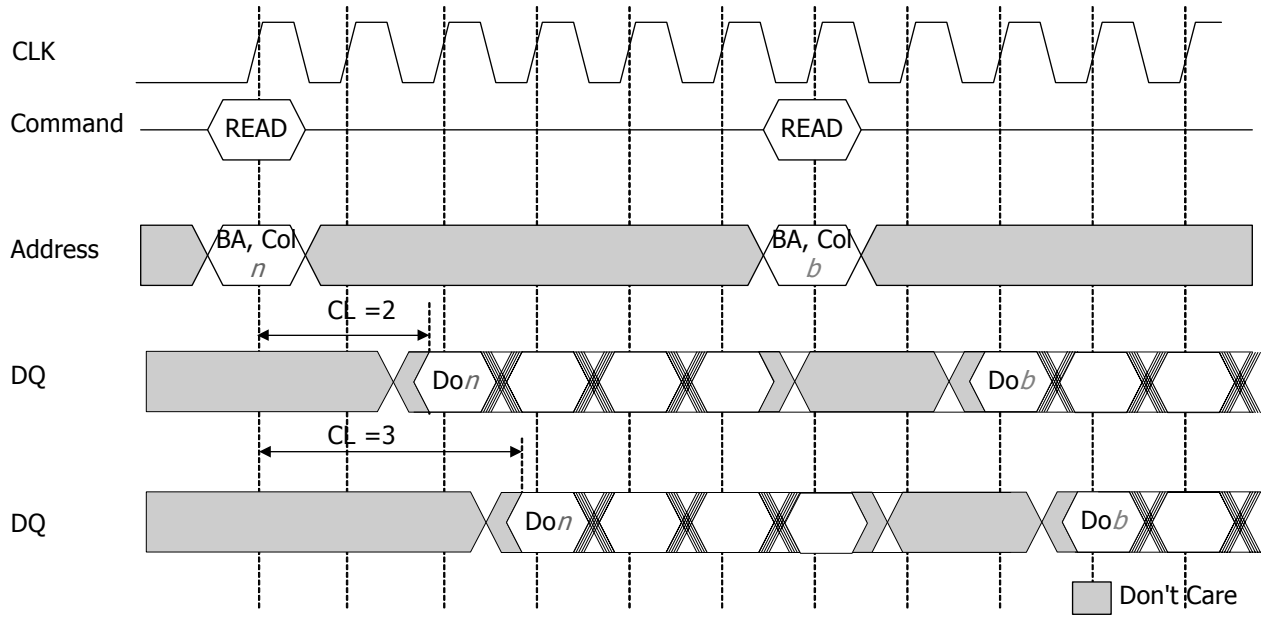
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated.

When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



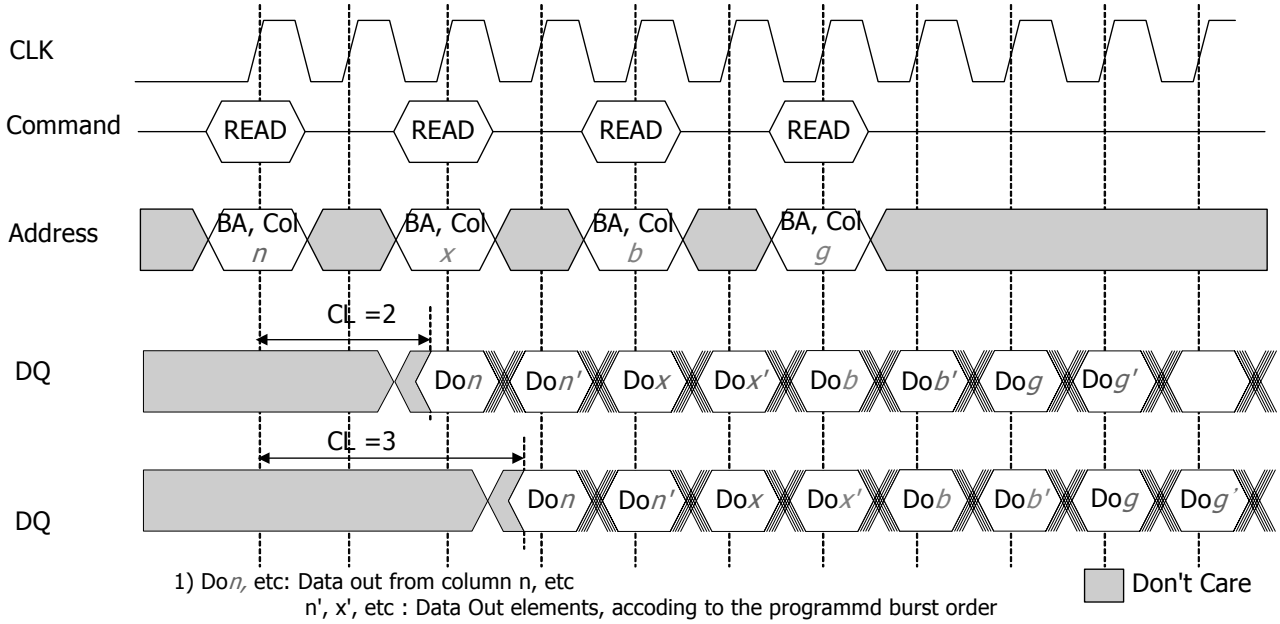
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in Figure. Full-speed random read accesses within a page or pages can be performed as shown in Fig.



1) Do*n* (or *b*): Data out from column n
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 : 3 subseqnent elements of Data Out appear in the programmed order following Do *n (b)*

Non-Consective Read Bursts

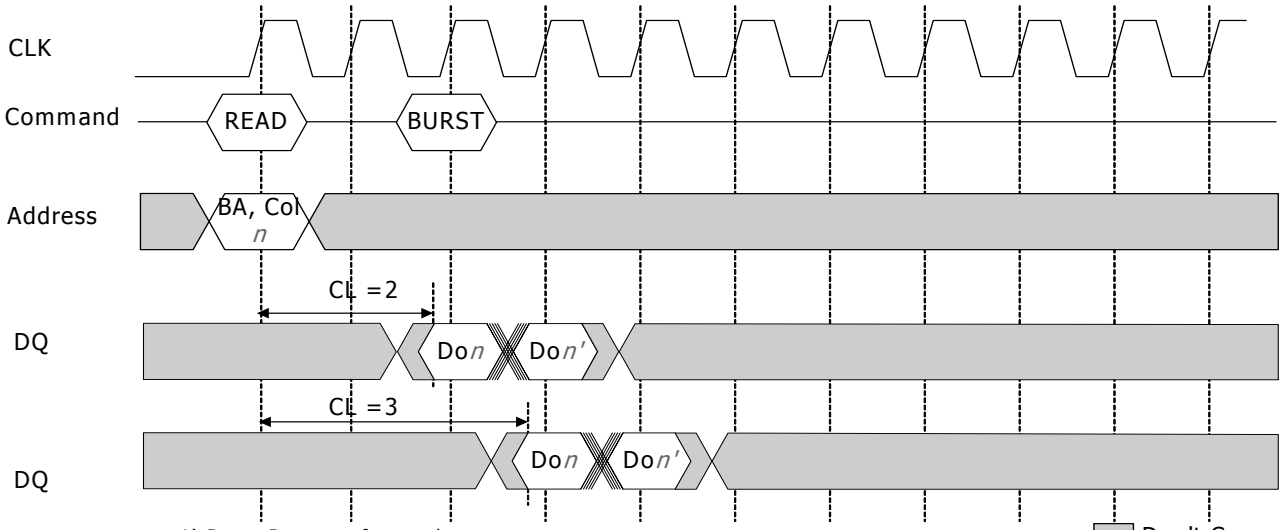


1) Do*n,* etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 1, 2, 4, 8 or full page in cases shown
4) Read are to active row in any banks

Randum Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element.

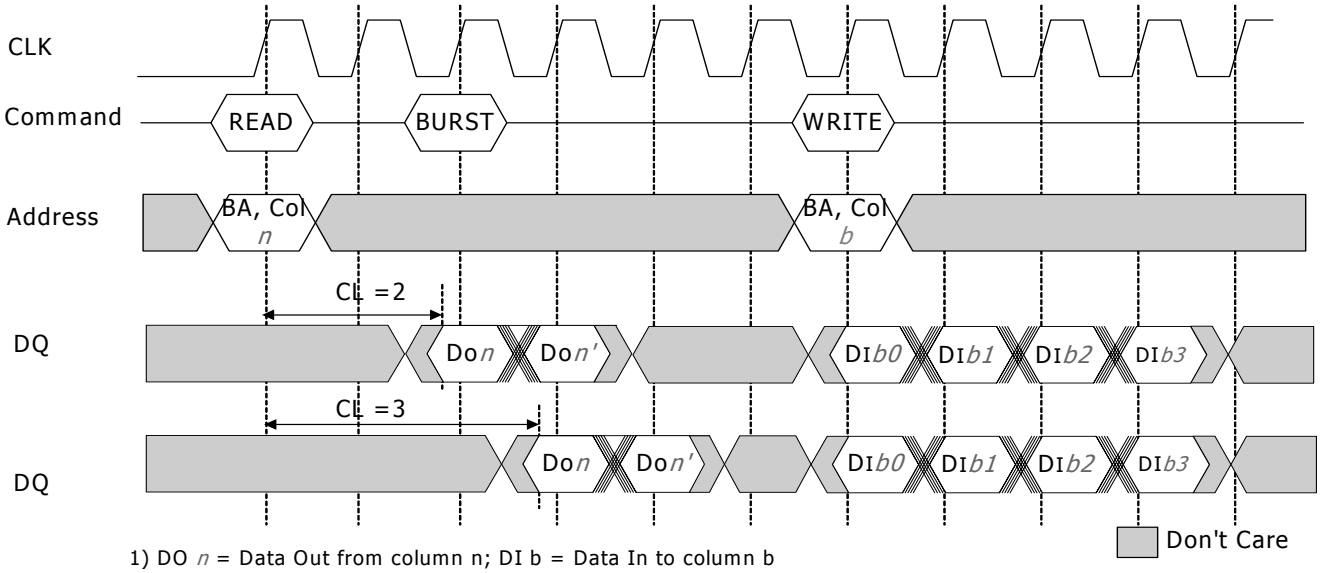


1) Don : Data out from column n
2) BA, Col n = Bank A, Column n
3) Cases shown are bursts of 4, 8, or full page terminated after 2 data elements

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig.



1) DO *n* = Data Out from column n; DI b = Data In to column b

Read to Write

Note :

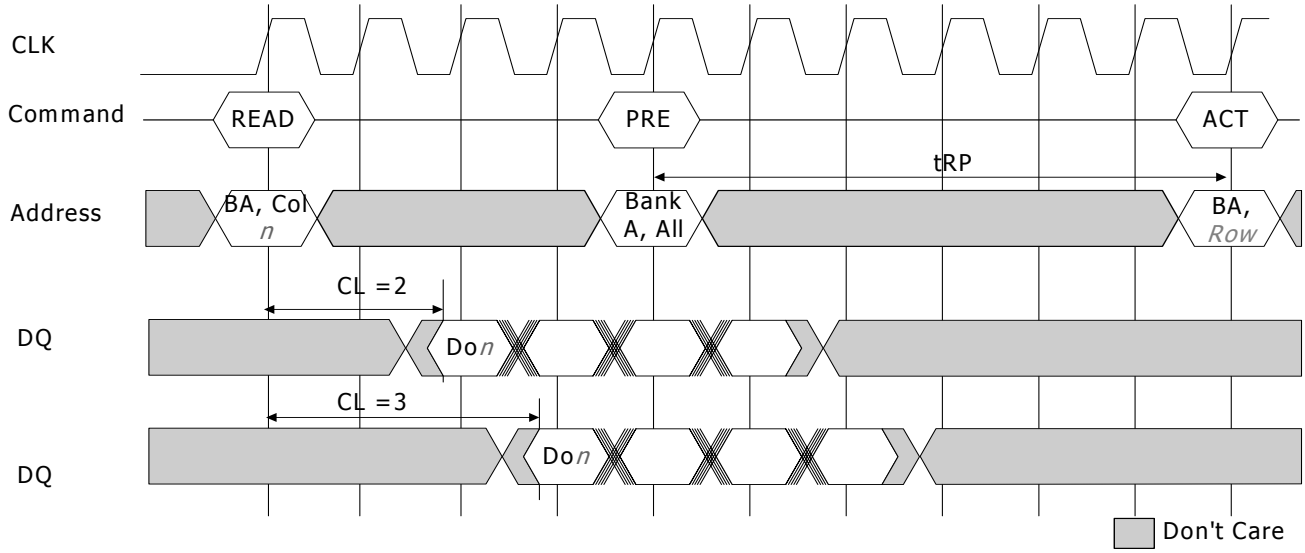
1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQM must be set High so that the output buffer becomes High-Z before data input.

2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.

3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

READ to PRECHARGE

Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto pre-charge.
The disadvantage of the PRECHARGEcommand is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to trun-cate fixed-length or full-page bursts.



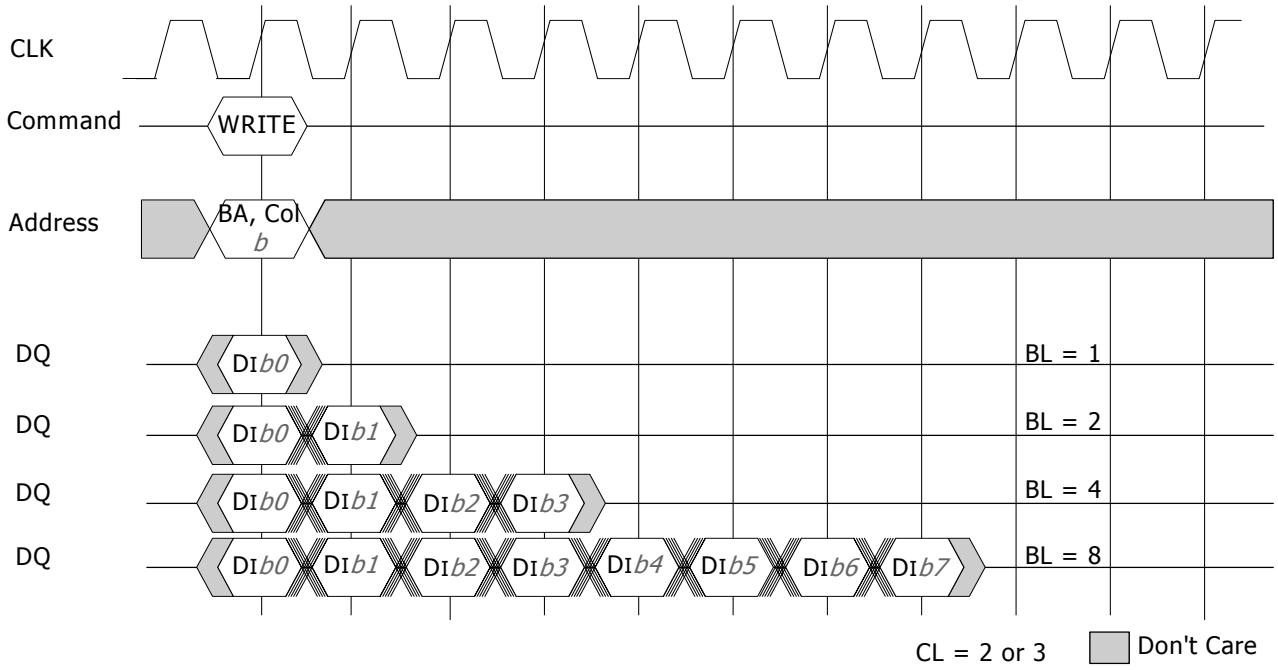
1) DO *n* = Data Out from column n
2) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
3) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.

During WRITE bursts, the first valild data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored. A full-page burst will continue until terminated.
Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command.

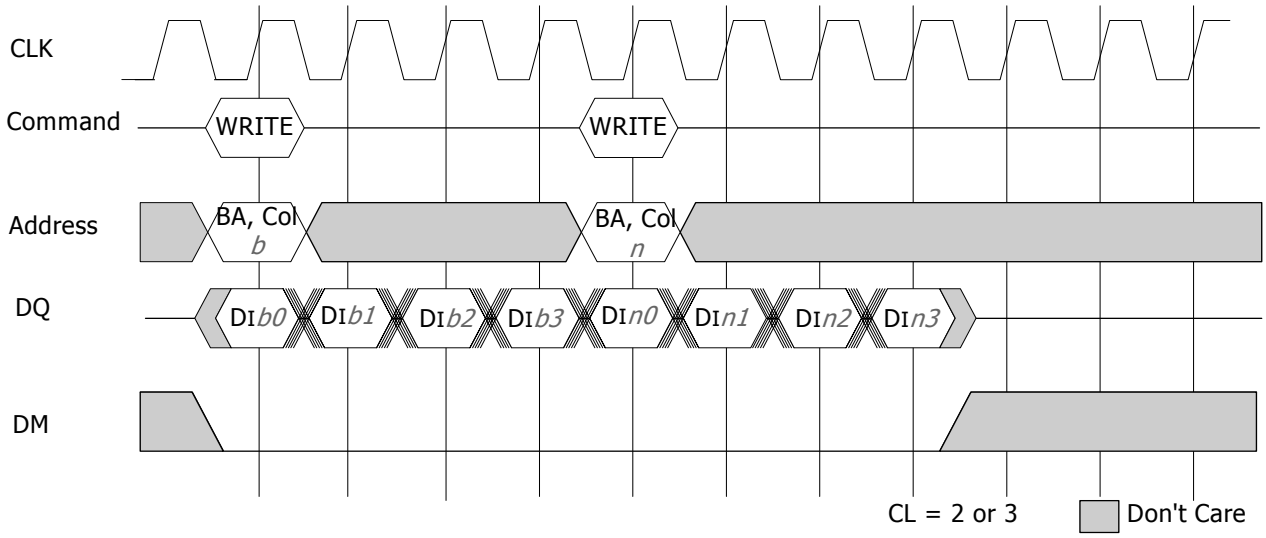


Basic Write timing parameters for Write Burst Operation

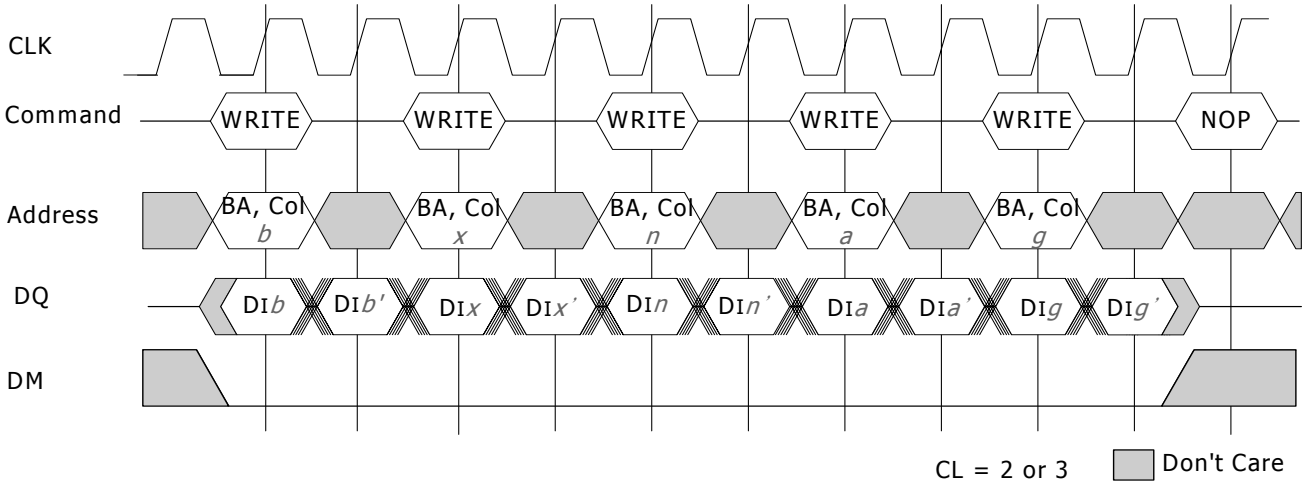
Note :
1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.

WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command. The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element.

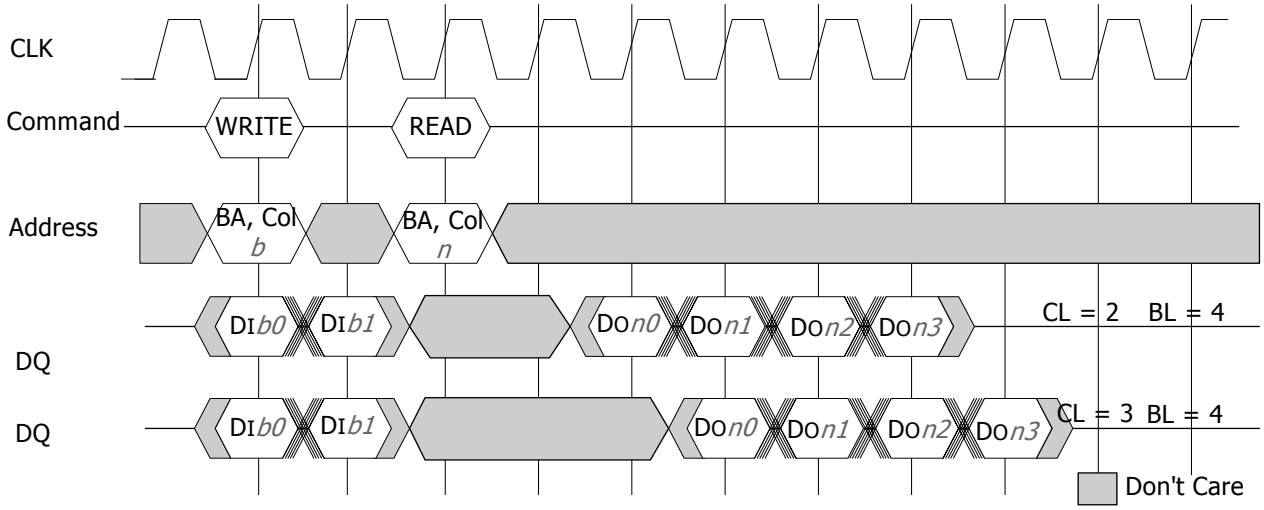


Concatenated Write Bursts



Random Write Cycles

WRITE to READ

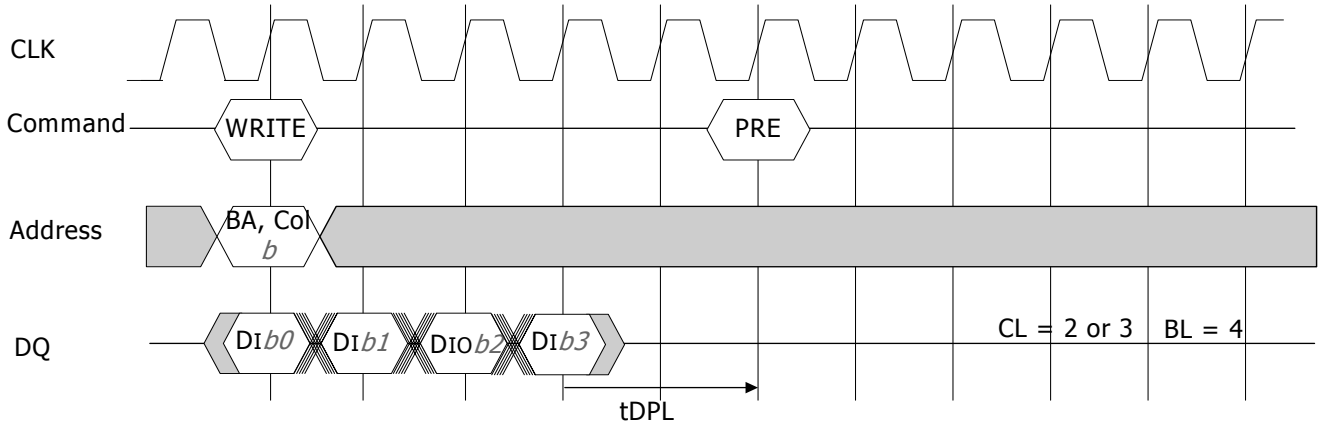


The preceding burst write operation can be aborted and a new burst read operation can be started by inputting a new read command in the write cycle. The data of the read command (READ) is output after the lapse of the /CAS latency.
The preceding write operation (WRIT) writes only the data input before the read command.
The data bus must go into a high-impedance state at least one cycle before output of the latest data.

Note:
1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.
2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

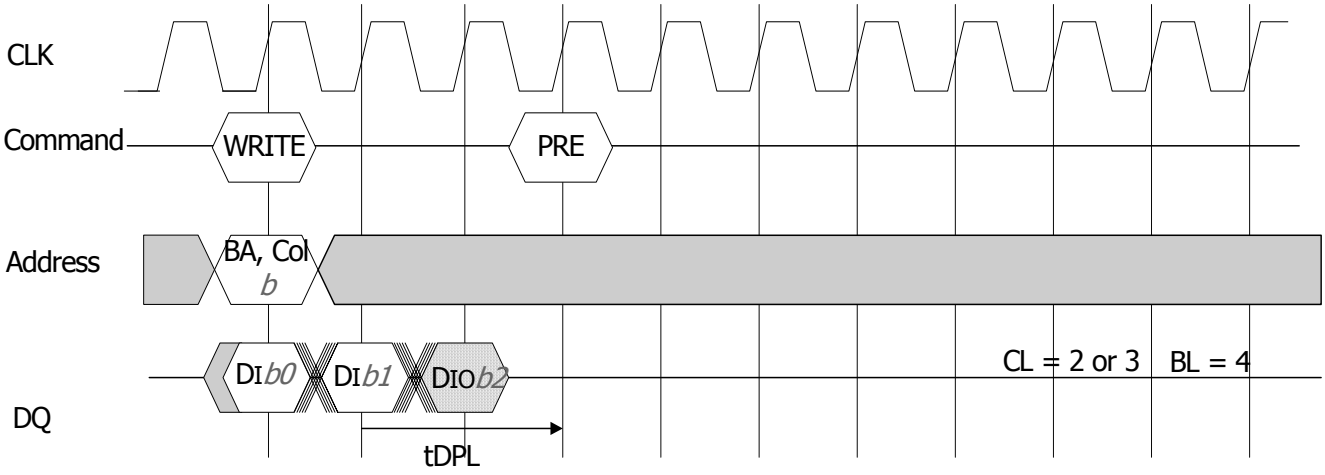
WRITE to PRECHARGE

Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the clock defined by tDPL. To follow a WRITE without truncating the WRITE burst, tDPL should be met as shown in Fig.



Non-Interrupting Write to Precharge

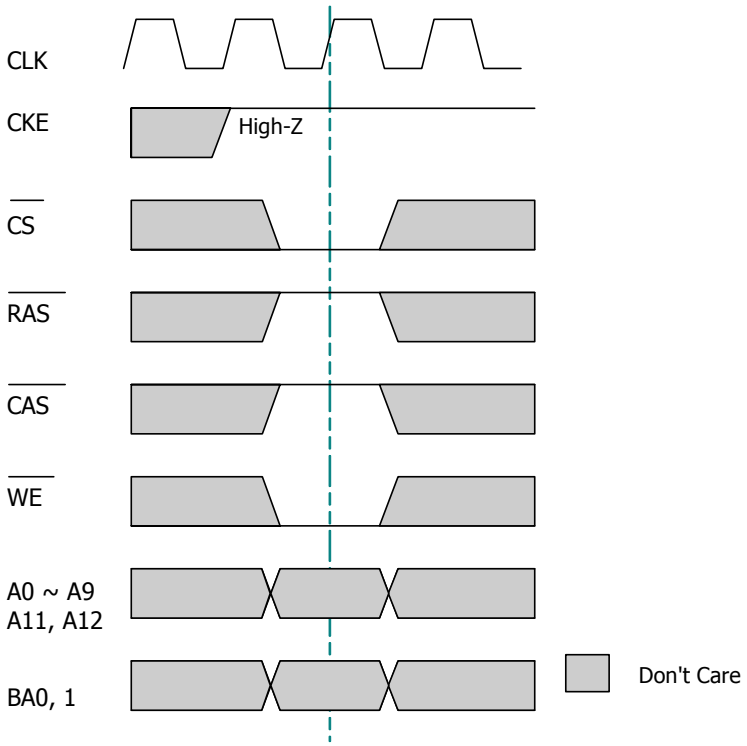
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-inthat are registered prior to the tDPL period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.



Interrupting Write to Precharge

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with autoprecharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

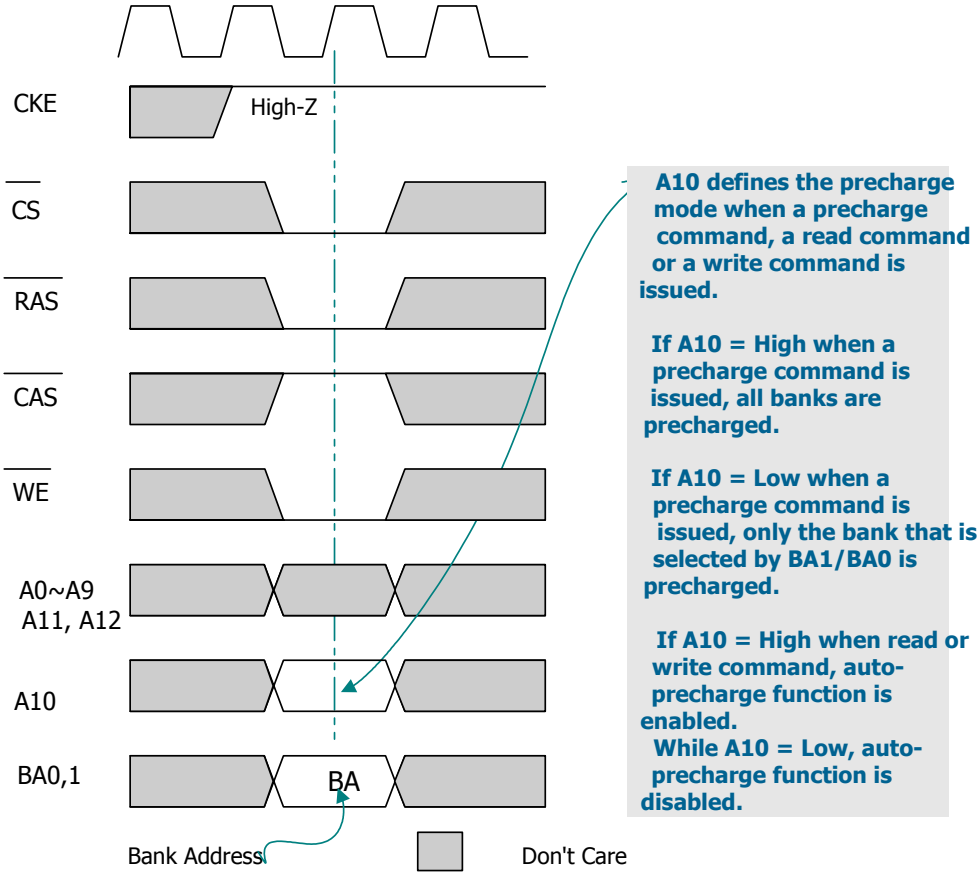


BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

Hynix SDR SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

– AUTO REFRESH.

This command is used during normal operation of the Hynix SDR SDRAM. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Hynix SDR SDRAM requires AUTO REFRESH commands at an average periodic interval of tREF.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given SDR SDRAM, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is *8*tREF*.

-SELF REFRESH.

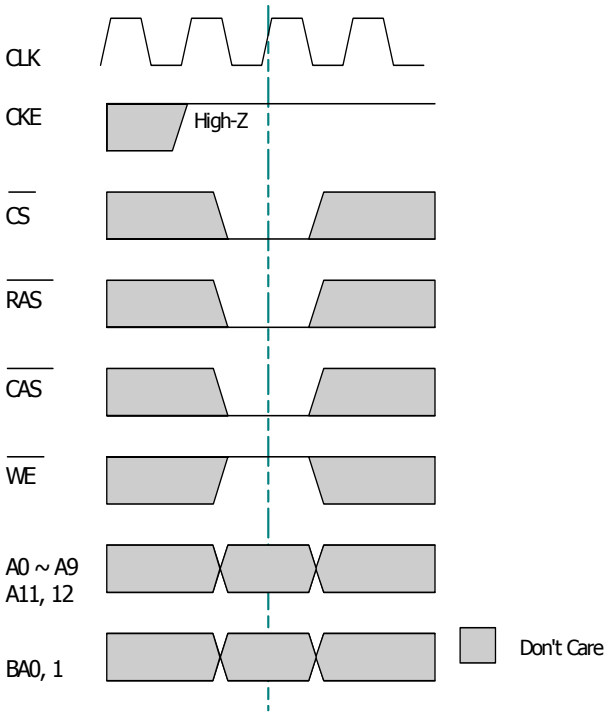
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low). This state retains data in the SDR SDRAM, even if the rest of the system is powered down. Note refresh interval timing while in Self Refresh mode is scheduled internally in the SDR SDRAM and may vary and may not meet tREF time.

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During selfrefresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.

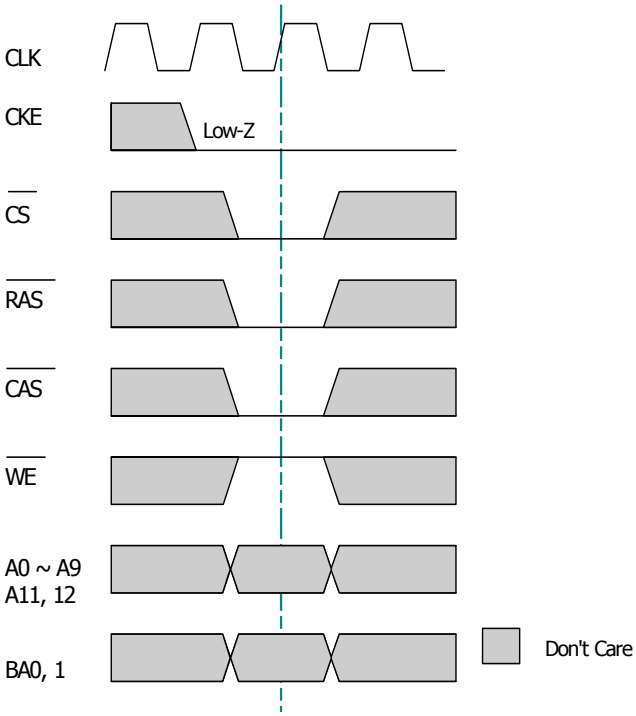
1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

Note: tREF (max.) / refresh cycles.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. The Self Refresh command is used to retain cell data in the SDR SDRAM. In the Self Refresh mode, the SDR SDRAM operates refresh cycle asynchronously.



AUTO REFRESH COMMAND



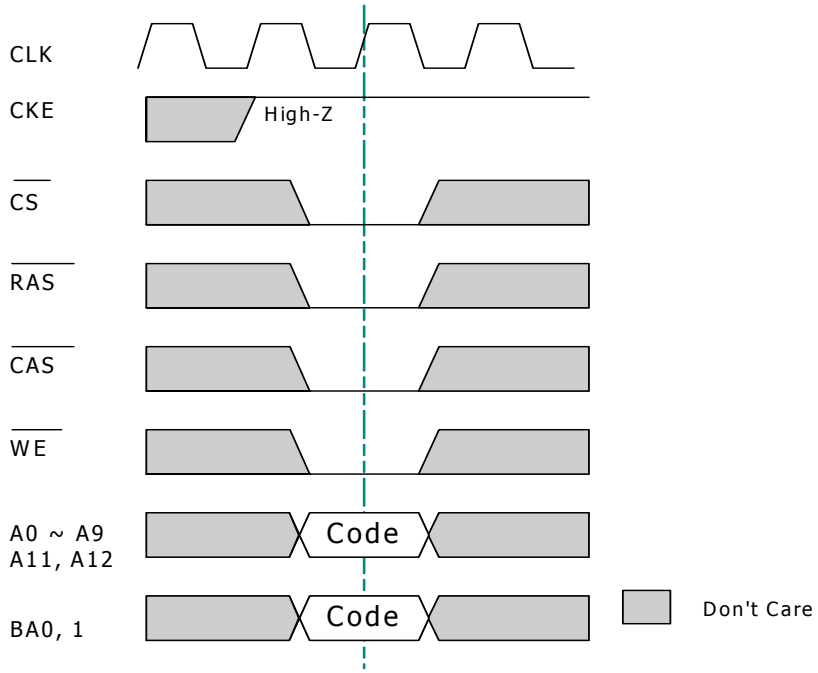
SELF REFRESH ENTRY COMMAND

Note 1: If all banks are in the idle status and CKE is inactive (low level), the self refresh mode is set.

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA
Auto Refresh	H	H	L	L	L	H	X	X		
Self Refresh Entry	H	L	L	L	L	H	X	X		

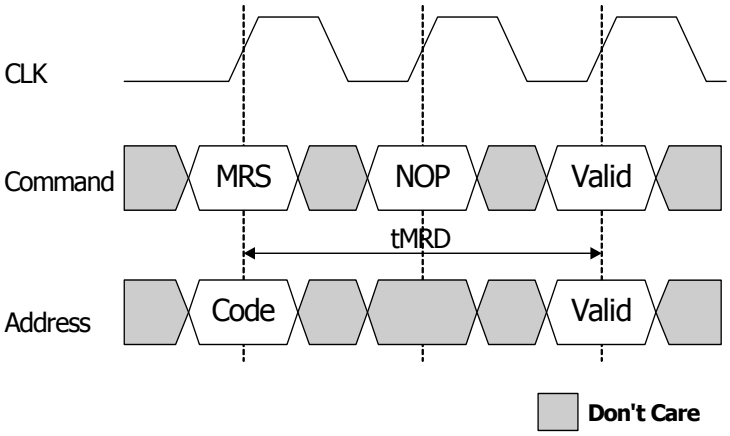
MODE REGISTER SET

The mode registers are loaded via the address bits.
BA0 and BA1 are used to select the Mode Register. See the Mode Register description in the register definition section.
The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.



MODE REGISTER SET COMMAND

Note:
BA0=BA1=Low loads the Mode Register.

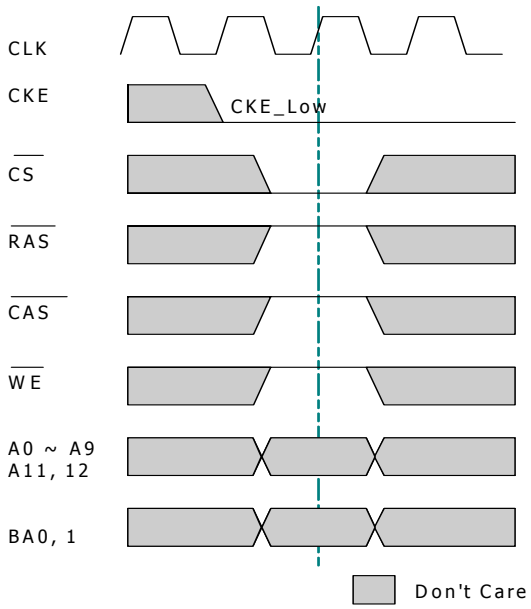


Code = Mode Register / Extended Mode Register selection
(BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

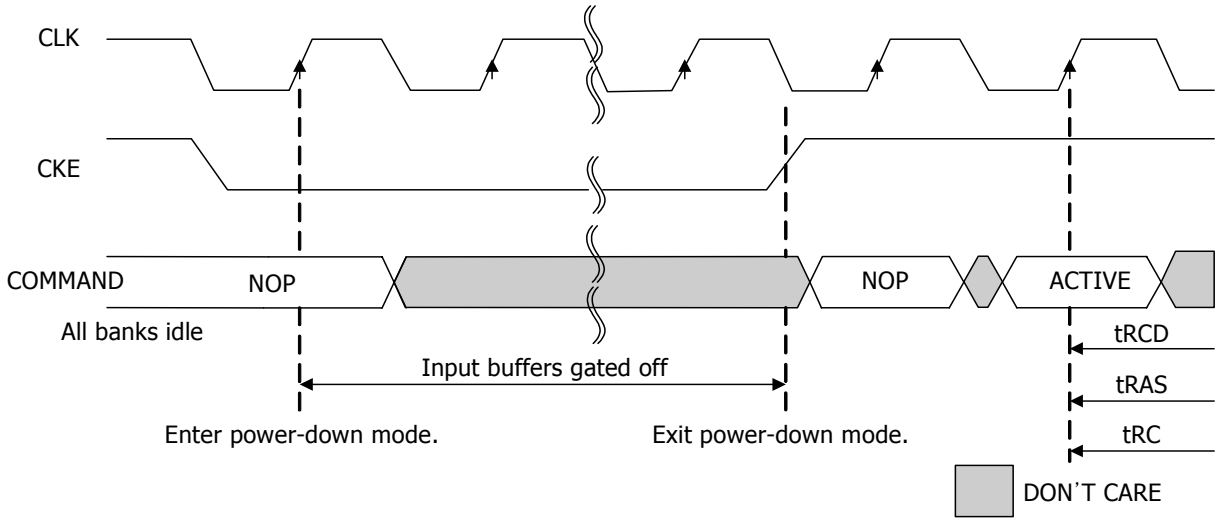
POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby.



POWER-DOWN COMMAND

NOTE:
This case shows CKE low coincident with NO OPERATION.
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.



Power Up and Initialization

Like a Synchronous DRAM, Low Power SDRAM(Mobile SDRAM) must be powered up and initialized in a predefined manner. Power must be applied to VDD and VDDQ(simultaneously). The clock signal must be started at the same time. After power up, an initial pause of 200 usec is required. And a precharge all command will be issued to the Mobile SDRAM. Then, 8 or more Auto refresh cycles will be provided. After the Auto refresh cycles are completed, a mode register set(MRS) command will be issued to program the specific mode of operation (Cas Latency, Burst length, etc.) And a extended mode register set command will be issued to program specific mode of self refresh operation(PASR). The following these cycles, the Mobile SDRAM is ready for normal opeartion.

Programming the registers

Mode Register

The mode register contains the specific mode of operation of the SDR SDRAM. This register includes the selection of a burst length(1, 2, 4, 8, Full Page), a cas latency(1, 2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.

Bank(Row) Active

The Bank Active command is used to activate a row in a specified bank of the device. This command is initiated by activating $\overline{CS}$, $\overline{RAS}$ and deasserting $\overline{CAS}$, $\overline{WE}$ at the positive edge of the clock. The value on the BA1 and BA0 selects the bank, and the value on the A0-A12 selects the row. This row remains active for column access until a precharge command is issued to that bank. Read and write opeartions can only be initiated on this activated bank after the minimum t_{RCD} time is passed from the activate command.

Read

The READ command is used to initiate the burst read of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$, $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the sarting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the READ burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.
The length of burst and the CAS latency will be determined by the values programmed during the MRS command.

Write

The WRITE command is used to initiate the burst write of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ and deasserting $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A8-A0 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used.
If Auto Precharge is selected the row being accessed will be precharged at the end of the WRITE burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.

Precharge

The Precharge command is used to close the open row in a particular bank or the open row in all banks. When the precharge command is issued with address A10, high, then all banks will be precharged, and If A10 is low, the open row in a particular bank will be precharged. The bank(s) will be available when the minimum t_{RP} time is met after the precharge command is issued.

Auto Precharge

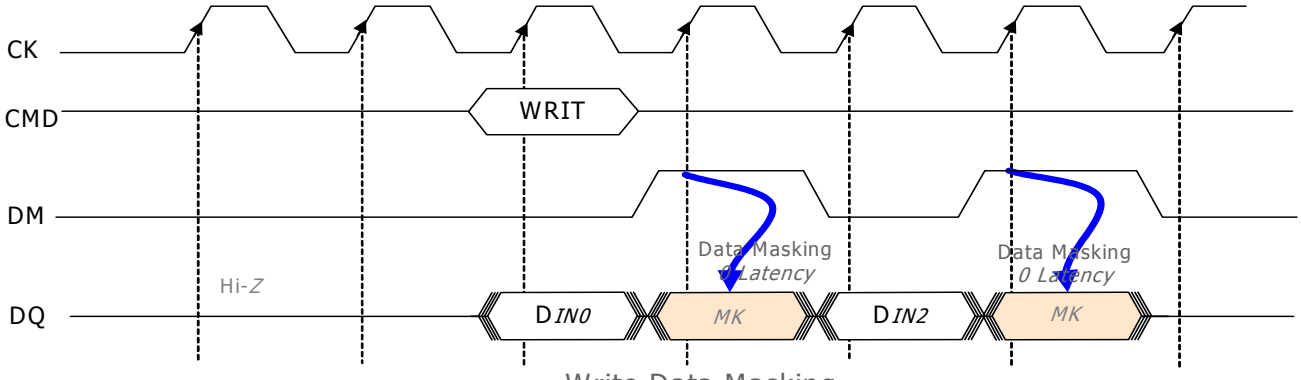
The Auto Precharge command is issued to close the open row in a particular bank after READ or WRITE operation. If A10 is high when a READ or WRITE command is issued, the READ or WRITE with Auto Precharge is initiated.

Burst Termination

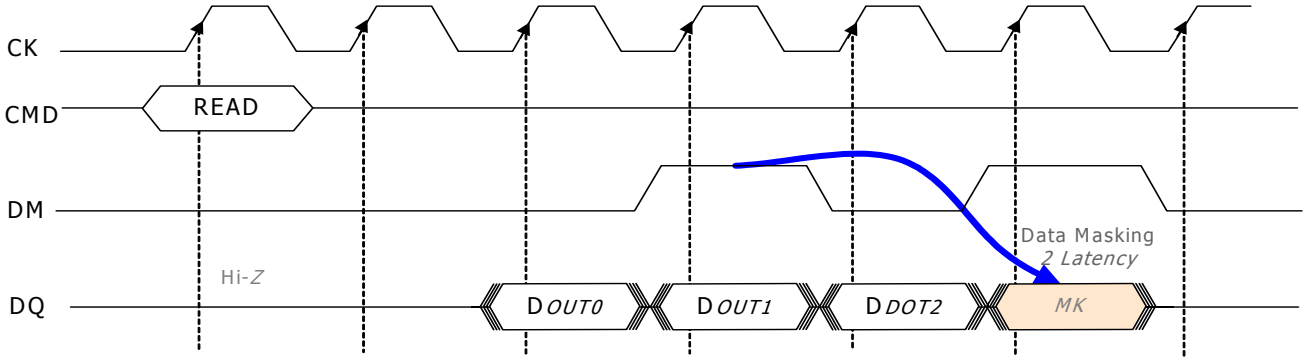
The Burst Termination is used to terminate the burst operation. This function can be accomplished by asserting a Burst Stop command or a Precharge command during a burst READ or WRITE operation. The Precharge command interrupts a burst cycle and close the active bank, and the Burst Stop command terminates the existing burst operation leave the bank open.

Data Mask

The Data Mask comamnd is used to mask READ or WRITE data. During a READ operation, When this command is issued, data outputs are disabled and become high impedance after two clock delay. During a WRITE operation, When this command is issued, data inputs can't be written with no clock delay.
If data mask is initiated by asserting low on DQM during the read cycle, the data outputs are enabled.
If DQM is asserted to High. the data outputs are masked (disabled) and become Hi-Z state after 2 cycle later. During the write cycle, DQM mask data input with zero latency



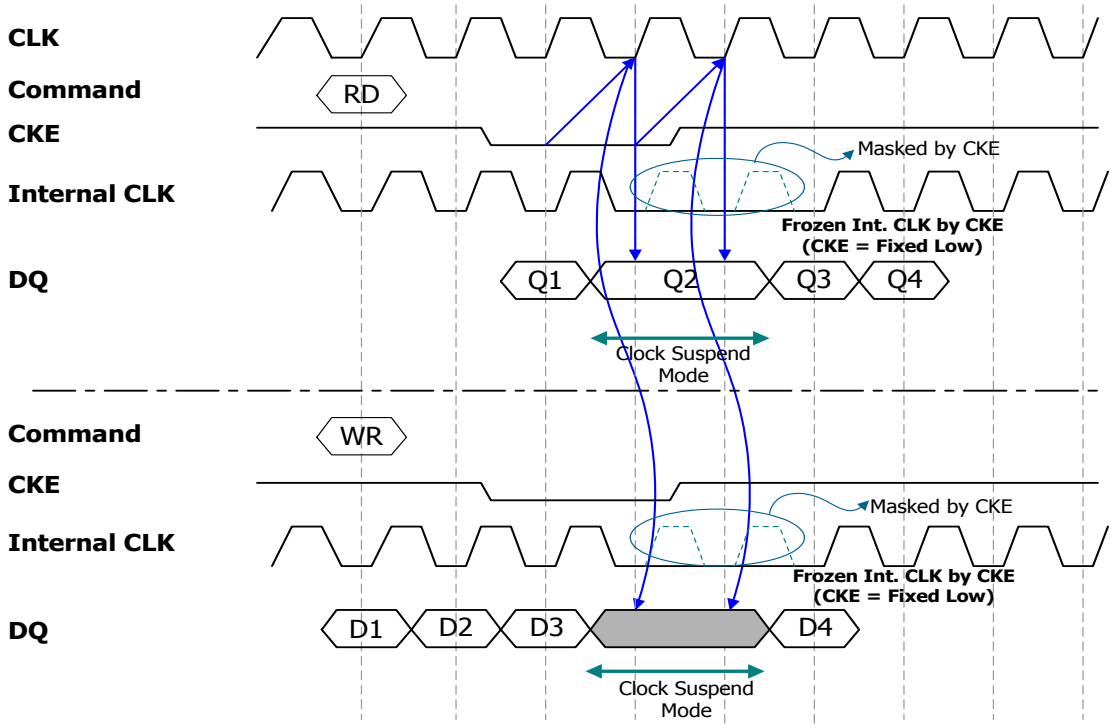
Write Data Masking



Read Data Masking

Clock Suspend

The Clock Suspend command is used to suspend the internal clock of SDR SDRAM. The clock suspend operation stops transmission of the clock to the internal circuits of the device during burst transfer of data to stop the operation of the device. During normal access mode, CKE is keeping High. When CKE is low, it freezes the internal clock and extends data Read and Write operations. (See examples in next Figures)



Power Down

The Power Down command is used to reduce standby current. Before this command is issued, all banks must be pre-charged and tRP must be passed after a precharge command. Once the Power Down command is initiated by keeping CKE low, all of the input buffer except CKE are gated off.

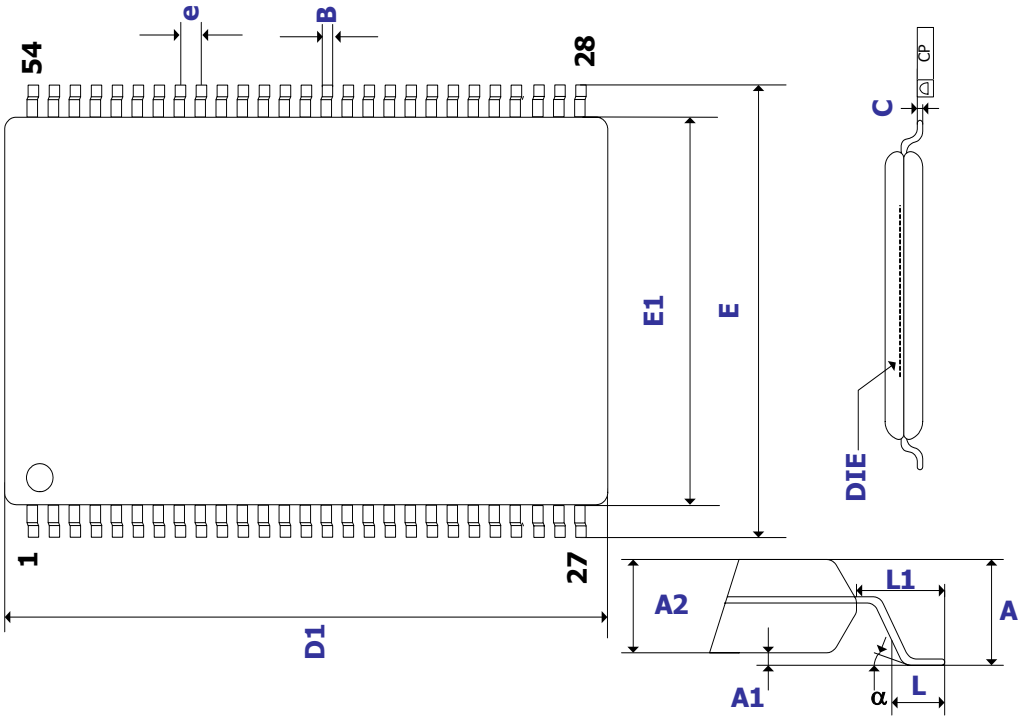
Auto Refresh

The Auto Refresh command is used during normal operation and is similar to CBR refresh in Coventional DRAMs. This command must be issued each time a refresh is required. When an Auto Refresh command is issued , the address bits is "Don't care", because the specific address bits is generated by internal refresh address counter.

Self Refresh

The Self Refresh command is used to retain cell data in SDRAM. In the Self Refresh mode, the SDRAM operates refresh cycle asynchronously. The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low).

PACKAGE INFORMATION



Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.991	-	1.194	0.0390		0.0470
A1	0.050	0.100	0.150	0.0020	0.0039	0.0059
A2	0.950	1.000	1.050	0.0374	0.0394	0.0413
B	0.300	-	0.400	0.012	-	0.016
C	0.120	-	0.210	0.0047	-	0.0083
CP		0.10			0.0039	
D1	22.149	22.22	22.327	0.8720	0.8748	0.8790
E	11.735	11.76	11.938	0.4620	0.4630	0.4700
E1	10.058	10.16	10.262	0.3950	0.4	0.4040
e	-	0.8	-	-	0.0315	-
L	0.406	-	0.597	0.0160	-	0.0235
L1	-	0.8	-	-	0.0315	-
alpha	0 / 5 (min / max)					