PrimeCell™ Color LCD Controller (PL110)

Revision: r1p2

Technical Reference Manual

ARM®

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PrimeCell Color LCD Controller (PL110)
Technical Reference Manual

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Release Information

The following changes have been made to this document.

Change history

Date	Issue	Change
August 1999	A	First release
26 August 1999	B	Minor corrections to Chapter 4. Changes to Appendix A, Tables A-5 and A-6 added.
8 September 1999	C	Figs 2-3 to Fig 2-8 inserted. Changes to Tables A-5 and A-6.
1 December 2000	D	Errata changes to Fig 2-6, Table 3-2, 3-9, 3-14, and A-5. Section 1.1.6 and Fig 1-1 added.
9 May 2003	E	Update to r1p2. Conversion to SGML.

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Product Status

The information in this document is final, that is for a developed product.

Web Address

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Preface

This preface introduces the *PrimeCell Color LCD Controller (PL110) r1p2 Technical Reference Manual*. It contains the following sections:

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About this document

This document is the *Technical Reference Manual* (TRM) for the ARM PrimeCell *Color LCD Controller* (CLCDC).

Intended audience

This document has been written for hardware and software engineers implementing *System-on-Chip* (SoC) designs. It provides information to enable designers to integrate the peripheral into a target system as quickly as possible.

Organization

This document is organized as follows:

Chapter 1 ***Introduction***

Read this chapter for an introduction to the CLCDC and its features. The product history of the CLCDC is also provided in thsi chapter.

Chapter 2 ***Functional Overview***

Read this chapter for a description of the major functional blocks of the CLCDC.

Chapter 3 ***Programmer's Model***

Read this chapter for a description of the CLCDC registers and programming details.

Chapter 4 ***Programmer's Model for Test***

Read this chapter for a description of the logic in the CLCDC for functional verification and production testing.

Appendix A ***Signal Descriptions***

Read this appendix for a description of the CLCDC signals.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this document, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

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Typographical conventions

The following typographical conventions are used in this book:

italic	Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes ARM processor signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.
`monospace italic`	Denotes arguments to commands and functions where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.

Other conventions

This document uses other conventions. They are described in the following sections:

- *Signals*
- *Bits, bytes, and word lengths* on page xii
- *Numbers* on page xii
- *Register fields* on page xii.

Signals

When a signal is described as being asserted, the level depends on whether the signal is active HIGH or active LOW. Asserted means HIGH for active high signals and LOW for active low signals:

Prefix n	Active LOW signals are prefixed by a lowercase n except in the case of AHB or APB reset signals. These are named **HRESETn** and **PRESETn** respectively.
Prefix H	AHB signals are prefixed by an upper case H.
Prefix P	APB signals are prefixed by an upper case P.

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Bits, bytes, and word lengths

Suffix b Indicates bits.

Suffix B Indicates bytes.

Byte Eight bits.

Halfword Two bytes (16 bits).

Word Four bytes (32 bits).

Quadword 16 contiguous bytes (128 bits).

Numbers

Suffix k Indicates 1000.

Suffix K Indicates an amount of memory. It means 1024.

Suffix M When used to indicate an amount of memory means $1\,024^2 = 1048576$. When used to indicate a frequency means 1000000.

Prefix 0x Indicates hexadecimal.

Prefix b Indicates binary.

Register fields

All reserved or unused address locations must not be accessed as this can result in unpredictable behavior of the device.

All reserved or unused bits of registers must be written as zero, and ignored on read unless otherwise stated in the relevant text.

All registers bits are reset to logic 0 by a system reset unless otherwise stated in the relevant text.

Unless otherwise stated in the relevant text, all registers support read and write accesses. A write updates the contents of the register and a read returns the contents of the register.

All registers defined in this document can only be accessed using word reads and word writes, unless otherwise stated in the relevant text.

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Further reading

This section lists publications by ARM Limited.

ARM periodically provides updates and corrections to its documentation. See `http://www.arm.com` for current errata sheets, addenda, and the ARM Frequently Asked Questions list.

ARM publications

This document contains information that is specific to the ARM PrimeCell Color LCD Controller (PL110). Refer to the following documents for other relevant information:

- *AMBA Specification (Rev 2.0)* (ARM IHI 0011)
- *ARM PrimeCell CLCDC PL110 Design Manual* (PL110 DDES 0000)
- *ARM PrimeCell CLCDC PL110 Integration Manual* (PL110 INTM 0000).

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Feedback

ARM Limited welcomes feedback on both the ARM PrimeCell Color LCD Controller (PL110), and the documentation.

Feedback on this document

If you have any comments on this document, send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the ARM PrimeCell CLCDC (PL110)

If you have any comments or suggestions about this product, contact your supplier giving:

- the product name
- a concise explanation of your comments.

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Chapter 1
Introduction

This chapter introduces the ARM PrimeCell Color LCD Controller (PL110) and contains the following section:

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1.1 About the ARM PrimeCell Color LCD Controller (PL110)

The ARM PrimeCell *Color Liquid Crystal Display Controller* (CLCDC) is an *Advanced Microcontroller Bus Architecture* (AMBA) master-slave module that connects to the *Advanced High-performance Bus* (AHB). The PrimeCell CLCDC is an AMBA-compliant *System-on-a-Chip* (SoC) peripheral that is developed, tested, and licensed by ARM.

The PrimeCell CLCDC is a reusable soft-IP block that has been developed with the prime aim of reducing time-to-market for ASIC development.

The PrimeCell CLCDC provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

1.1.1 Features of the PrimeCell Color LCD Controller

The principal features of the PrimeCell CLCDC are:

- compliance to the *AMBA Specification (Rev 2.0)* onwards for easy integration into SoC implementation
- dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display data
- supports single and dual panel mono *Super Twisted Nematic* (STN) displays with 4 or 8-bit interfaces
- supports single and dual-panel color and monochrome STN displays
- supports *Thin Film Transistor (*TFT) color displays
- resolution programmable up to 1024 x 768
- 15 gray-level mono, 3375 color STN, and 32K color TFT support
- 1, 2, or 4 *bits-per-pixel* (bpp) palettized displays for mono STN
- 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
- 16 *bits-per-pixel* (bpp) true-color non-palettized, for color STN and TFT
- 24 bpp true-color non-palettized, for color TFT
- programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically
- frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels
- patented gray scale algorithm
- supports little and big-endian, as well as WinCE data formats.

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1.1.2 Programmable parameters

You can program the following key parameters:

- horizontal front and back porch
- horizontal synchronization pulse width
- number of pixels per line
- vertical front and back porch
- vertical synchronization pulse width
- number of lines per panel
- number of panel clocks per line
- signal polarity, active HIGH or LOW
- AC panel bias
- panel clock frequency
- bpp
- display type, STN mono/color or TFT
- STN 4 or 8-bit interface mode
- STN dual or single panel mode
- little-endian, big-endian, or WinCE mode
- interrupt generation event.

1.1.3 Target markets

The markets to which the PrimeCell CLCDC is addressed are primarily in the portable segment. Typical applications for the PrimeCell CLCDC include:

- *Personal Digital Assistant* (PDA)
- ultra-sub notebook computer
- smart-phone
- hand-held, portable color games terminal.

1.1.4 LCD panel resolution

You can program the PrimeCell CLCDC to support a wide range of panel resolutions such as:

- 320x200, 320x240
- 640x200, 640x240, 640x480
- 800x600
- 1024x768.

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1.1.5 Types of LCD panel supported

The PrimeCell CLCDC supports the following types of LCD panel:

- active matrix TFT panels with up to 24-bit bus interface
- single-panel monochrome STN panels (4-bit and 8-bit bus interface)
- dual-panel monochrome STN panels (4-bit and 8-bit bus interface per panel)
- single-panel color STN panels, 8-bit bus interface
- dual-panel color STN panels, 8-bit bus interface per panel.

1.1.6 Number of colors supported

The number of colors supported by the different types of panels are described in:

- *TFT panels*
- *Color STN panels*
- *Mono STN panels* on page 1-5.

TFT panels

TFT panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from available colors.
- 2 bpp, palettized, 4 colors selected from available colors.
- 4 bpp, palettized, 16 colors selected from available colors.
- 8 bpp, palettized, 256 colors selected from available colors.
- 16 bpp, direct 5:5:5 RGB, with one bpp not normally being used. This pixel is still output, and can be used as a bright bit to connect to the *Least Significant Bit* (LSB) of R, G and B components of a 6:6:6 TFT panel.
- 24 bpp, direct 8:8:8 RGB, providing over 16 million colors.

Each 16-bit palette entry is composed of five bpp (RGB) plus a common intensity bit. This gives better memory utilization and performance compared with a full six bpp structure. The total amount of colors supported can be doubled from 32K to 64K if the intensity bit is used and applied to all three color components simultaneously. Refer to Appendix A *Signal Descriptions* for more information.

Color STN panels

Color STN panels support one or more of the following color modes:

- 1 bpp, palettized, 2 colors selected from 3375

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- 2 bpp, palettized, 4 colors selected from 3375
- 4 bpp, palettized, 16 colors selected from 3375
- 8 bpp, palettized, 256 colors selected from 3375
- 16 bpp, direct 4:4:4 RGB, with 4 bpp not being used.

Mono STN panels

Mono STN panels support one or more of the following modes:

- 1 bpp, palettized, 2 gray scales selected from 15
- 2 bpp, palettized, 4 gray scales selected from 15
- 4 bpp, palettized, 16 gray scales selected from 15.

You can program greater than four bpp for mono panels but using these modes does not make sense because the maximum number of gray scales supported on the display is 15.

1.1.7 LCD powering up and powering down sequence support

The PrimeCell CLCDC (PL110) enables the following power up sequence:

1. V_{dd} is simultaneously applied to the SoC that contains the CLCDC and panel display driver logic. The signals **CLLP**, **CLCP**, **CLFP**, **CLAC**, **CLD[23:0]**, and **CLLE** are held LOW.

2. When V_{dd} is stabilized, a 1 is written to the LcdEn bit in the LCDControl Register. This puts the signals **CLLP**, **CLCP**, **CLFP**, **CLAC**, and **CLLE** into their active states but the **CLD[23:0]** signals remain LOW.

3. When the signals in Step 2 have stabilized, where appropriate, the contrast voltage V_{ee} (this is not controlled or supplied by the CLCDC) is then applied.

4. You can use a software timer routine, if required, to provide the minimum display specific delay time between application of the control signals and power to the panel display. On completion of the software timer routine, power is applied to the panel by writing a 1 to the LcdPwr bit within the LcdControl Register which, in turn, sets the **CLPOWER** signal HIGH and puts the **CLD[23:0]** signals into their active state. The **CLPOWER** signal is expected to be used to gate the power to the LCD panel.

The power down sequence is the reverse of the above four stages and must be strictly followed, this time write the relevant register bits with 0.

The power up and power down sequences are shown in Figure 1-1 on page 1-6.

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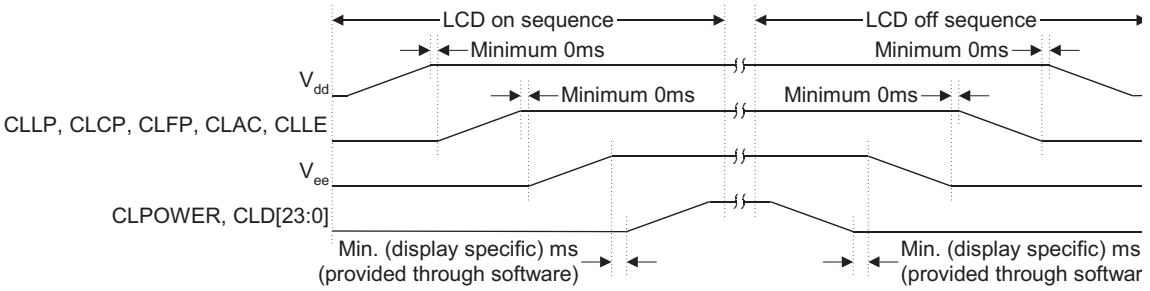

Figure 1-1 Power up and power down sequences

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1.2 Product history

lists the product history of the PrimeCell CLCDC (PL110)

Table 1-1 Product history

Release	Change
REL1v1	Maintence release, no change to functionality
r1p2	Maintence release, no change to functionality

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Chapter 2
Functional Overview

This chapter describes the major functional blocks of the ARM PrimeCell CLCDC (PL110) and contains the following sections:

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2.1 ARM PrimeCell Color LCD Controller (PL110) overview

The PrimeCell CLCDC performs translation of pixel-coded data into the required formats and timings to drive a variety of single/dual mono and color LCDs.

Support is provided for passive *Super Twisted Nematic* (STN) and active *Thin Film Transisto*r (TFT) LCD display types:

STN displays STN display panels require algorithmic pixel pattern generation to provide pseudo gray scaling on mono, or color creation on color displays.

TFT displays TFT display panels require the digital color value of each pixel to be applied to the display data inputs.

Packets of pixel coded data are fed, through the AMBA AHB interface, to two independent, programmable, 32-bit wide, DMA FIFOs that act as input data flow buffers.

The buffered pixel coded data is then unpacked using a pixel serializer.

Depending on the LCD type and mode, the unpacked data can represent:

- an actual true display gray or color value
- an address to a 256 x 16 bit wide palette RAM gray or color value.

In the case of STN displays, either a value obtained from the addressed palette location or the true value is passed to the gray scaling generators. The hardware coded gray scale algorithm logic sequences the addressed pixels activity over a programmed number of frames to provide the effective display appearance.

For TFT displays, either an addressed palette value or true color value is passed directly to the output display drivers, bypassing the gray scaling algorithmic logic.

Besides data formatting, the PrimeCell CLCDC provides a set of programmable display control signals, which include:

- LCD panel power enable
- pixel clock
- horizontal and vertical synchronization pulses
- display bias.

The PrimeCell CLCDC generates individual interrupts for:

- upper or lower panel DMA FIFO underflow
- base address update signification
- vertical compare
- bus error.

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There is also a single combined interrupt that is raised when any of the individual interrupts become active.

A simplified block diagram of the PrimeCell CLCDC is shown in Figure 2-1.

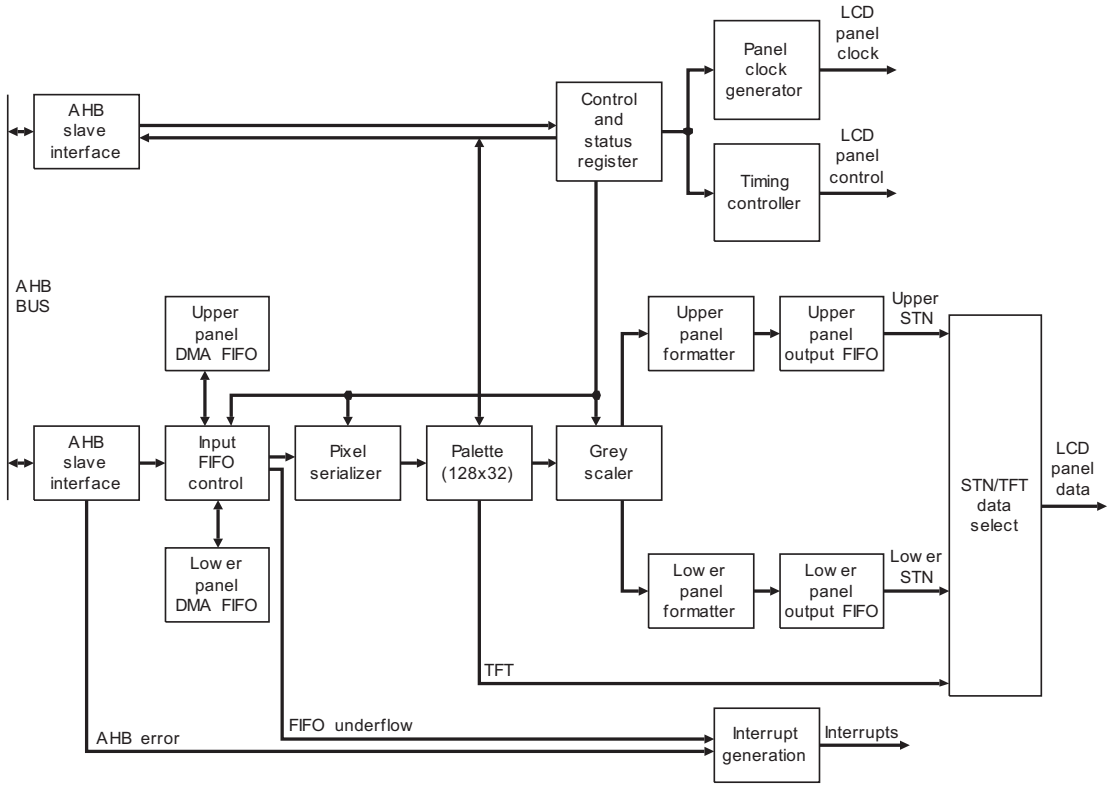

Figure 2-1 Block diagram of the PrimeCell CLCDC

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2.2 AMBA AHB interface

The AMBA AHB interface comprises the following blocks:

- *AMBA AHB slave interface*
- *AMBA AHB master interface*.

2.2.1 AMBA AHB slave interface

The AMBA AHB slave interface connects the PrimeCell CLCDC to the AMBA AHB bus and provides CPU accesses to the registers and palette RAM. For more information on AMBA AHB slave interfaces, refer to the *AMBA Specification (Rev 2.0)*.

The following features are supported by the PrimeCell CLCDC AMBA AHB slave interface:

- standard write and read AMBA AHB accesses
- INCR4, INCR8, and undefined length WORD bursts only
- OKAY response only.

2.2.2 AMBA AHB master interface

The AMBA AHB master interface transfers display data from a selected slave (memory) to the PrimeCell CLCDC DMA FIFOs. It can be connected directly to the AMBA AHB system bus or to the AMBA AHB port of a memory controller, such as an SDRAM controller.

The inherent AMBA AHB master interface state machine performs the following functions:

- Loads the upper panel base address into the AMBA AHB address incrementor on recognition of a new frame.
- Monitors both the upper and lower DMA FIFO levels and asserts **HBUSREQM** to request display data from memory, filling them to above the programmed water mark. **HBUSREQM** is re-asserted when there are at least four locations available within either FIFO (dual panel mode).
- Checks for 1KB boundaries during fixed-length bursts, appropriately adjusting the address in such occurrences.
- Generates the address sequences for fixed-length and undefined bursts.
- Controls the handshaking between the memory and DMA FIFOs. It inserts busy cycles if the FIFOs have not completed their synchronization and updating sequence.

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- Fills up the DMA FIFOs, in dual panel mode, in an alternating fashion from a single **HBUSREQM** request and subsequent **HGRANTM**.
- Asserts the **CLCDMBEINTR** interrupt if an error occurs during an active burst.
- Responds to retry commands by restarting the failed access.

2.2.3 Dual DMA FIFOs and associated control logic

The pixel data accessed from memory is buffered by two DMA FIFOs that can be independently controlled to cover single and dual-panel LCD types. Each FIFO is 16 words deep by 32 bits wide and can be cascaded to form an effective 32-word deep FIFO in single-panel mode. The input ports of the FIFOs are connected to the AMBA AHB interface and the output port feeds the pixel serializer.

Synchronization logic is used to transfer the pixel data from the AMBA AHB **HCLK** domain to the **CLCDCLK** clock domain, the DMA FIFOs being clocked by the former.

The water level marks within each FIFO are set so that each FIFO requests data when at least four locations become available.

An interrupt signal is asserted if an attempt is made to read either of the two DMA FIFOs when they are empty, in other words an underflow condition has occurred.

2.2.4 Pixel serializer

This block reads the 32-bit wide LCD data from output port of the DMA FIFO and extracts 24, 16, 8, 4, 2, or 1 BPP data, depending on the current mode of operation. The PrimeCell CLCDC supports big-endian, little-endian, and WinCE data formats. In dual panel mode, data is alternately read from the upper and lower DMA FIFOs. Depending upon the mode of operation, you can use the extracted data to point to a color/gray scale value in the palette ram or it can be a true color value that you can apply directly to an LCD panel input.

Figure 2-2 on page 2-6 to Figure 2-7 on page 2-8 show the structure of the data in each DMA FIFO word corresponding to the endianness and bpp combinations. For each of the three supported data formats, the required data for each panel display pixel must be extracted from the data word.

The nomenclature used in the figures is:

- *Little Endian Byte, Little Endian Pixel* (LBLP) order
- *Big Endian Byte, Big Endian Pixel* (BBBP) order
- *Little Endian Byte, Big Endian Pixel* (LBBP) order (this is the WinCE format).

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bpp	DMA FIFO output bits															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p31	p30	p29	p28	p27	p26	p25	p24	p23	p22	p21	p20	p19	p18	p17	p16
2	p15		p14		p13		p12		p11		p10		p9		p8	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p7				p6				p5				p4			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p3								p2							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-2 LBLP, DMA FIFO output bits 31 to 16

bpp	DMA FIFO output bits															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p15	p14	p13	p12	p11	p10	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
2	p7		p6		p5		p4		p3		p2		p1		p0	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p3				p2				p1				p0			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p1								p0							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 2-3 LBLP, DMA FIFO output bits 15 to 0

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bpp	DMA FIFO output bits															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p0	p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15
2	p0		p1		p2		p3		p4		p5		p6		p7	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p0				p1				p2				p3			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p0								p1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-4 BBBP, DMA FIFO output bits 31 to 16

bpp	DMA FIFO output bits															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p16	p17	p18	p19	p20	p21	p22	p23	p24	p25	p26	p27	p28	p29	p30	p31
2	p8		p9		p10		p11		p12		p13		p14		p15	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p4				p5				p6				p7			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p2								p3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-5 BBBP, DMA FIFO output bits 15 to 0

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bpp	DMA FIFO output bits															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	p24	p25	p26	p27	p28	p29	p30	p31	p16	p17	p18	p19	p20	p21	p22	p23
2	p12		p13		p14		p15		p8		p9		p10		p11	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p6				p7				p4				p5			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p3								p2							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-6 LBBP, DMA FIFO output bits 31 to 16

bpp	DMA FIFO output bits															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	p8	p9	p10	p11	p12	p13	p14	p15	p0	p1	p2	p3	p4	p5	p6	p7
2	p8		p9		p10		p11		p12		p13		p14		p15	
	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4	p2				p3				p0				p1			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8	p1								p0							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16	p0															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24	p0															
									23	22	21	20	19	18	17	16

Figure 2-7 LBBP, DMA FIFO output bits 15 to 0

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2.2.5 RAM palette

The RAM-based palette is a 256 x 16 bit dual-port RAM physically structured as 128 x 32 bit. This allows two entries to be written into the palette from a single word write access. The least significant bit of the serialized pixel data is used to select between upper and lower halves of the palette RAM. Which half is selected depends on the byte ordering mode. In little-endian mode, the LSB being set selects the upper half, but in big-endian, the lower half of the palette is selected. WinCE byte ordering is little-endian, so the former case applies.

Pixel data values can be written and verified through the AMBA AHB slave interface. For information on the numbers of colors supported, refer to *Number of colors supported* on page 1-4.

The palette RAM is a dual port RAM with independent controls and addresses for each port. Port1 is used as a read/write port and is connected to the AMBA AHB slave interface. The palette entries can be written and verified through this port. Port2 is used as a read-only port and is connected to the unpacker and gray scaler. Table 2-1 shows the bit representation of each word in the palette.

Table 2-1 Palette data storage

Bit	Name	Description
[31]	I	Intensity/unused
[30:26]	B[4:0]	Blue palette data
[25:20]	G[4:0]	Green palette data
[19:16]	R[4:0]	Red palette data
[15]	I	Intensity/unused
[14:10]	B[4:0]	Blue palette data
[9:5]	G[4:0]	Green palette data
[4:0]	R[4:0]	Red palette data

For mono STN mode only the red palette field bits [4:1] are used. However, in STN color mode the green and blue [4:1] are also used.

The red and blue pixel data can be swapped to support BGR data format using a Control Register bit.

In 16 and 24 bpp TFT mode, the palette is bypassed and the output of the pixel serializer is used as the TFT panel data.

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2.2.6 Gray scaler

A patented gray scale algorithm drives mono and color STN panels. This provides 15 gray scales for mono displays. In the case of STN color displays, the three color components (red, green, and blue) are gray scaled simultaneously which results in 3 375 (15x15x15) colors being available. The gray scaler transforms each 4-bit gray value into a sequence of activity-per-pixel over several frames, relying to some degree on the display characteristics, to give the representation of gray scales and color.

2.2.7 Upper and lower panel formatters

Each formatter consists of three 3-bit (red, green, and blue) shift left registers. Red, green and blue pixel data bit values from the gray scaler are concurrently shifted into the respective registers. When enough data is available, a byte is constructed by multiplexing the registered data to the correct bit position to satisfy the RGB data pattern of LCD panel. The byte is transferred to the three-byte FIFO which has enough space to store eight color pixels.

2.2.8 Panel clock generator

The output of the panel clock generator block is the panel clock. This is a divided down version of **CLCDCLK**. It can be programmed in the range **CLCDCLK/**2 to **CLCDCLK/**33 to match the bpp data rate of the LCD panel.

2.2.9 Timing controller

The primary function of the timing controller block is to generate the horizontal and vertical timing panel signals. It also provides panel bias/enable signal. These timings are all register programmable through the AMBA AHB slave interface.

2.2.10 Interrupt generation

The PrimeCell CLCDC provides four individually maskable interrupts and a single combined interrupt. The single combined interrupt is asserted if any of the combined interrupts are asserted and unmasked.

2.2.11 Bus architecture

The PrimeCell CLCDC incorporates a master interface and can be connected directly onto the main system AHB bus, or alternatively to an AMBA AHB port of a memory controller, such as an SDRAM controller.

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In addition to the AMBA AHB master interface, there is also an AMBA AHB slave interface for programming registers within the device. The slave interface and the master interface are separate AMBA AHB slaves and masters. This means that the PrimeCell CLCDC can be connected up in one of two ways:

- It can be built so that the master interface and the slave interface connect to a single multi-master AMBA AHB bus interface.
- The master interface can connect directly to a memory controller (for example an SDRAM controller) with an AMBA AHB slave interface, while the slave interface connects to the AMBA AHB bus.

These two arrangements are shown in Figure 2-8 and Figure 2-9.

AMBA AHB supports a wide range of on-chip bus sizes, from eight bits up to 1 024 bits. The PrimeCell CLCDC master and slave interfaces are implemented as 32-bit data bus devices only.

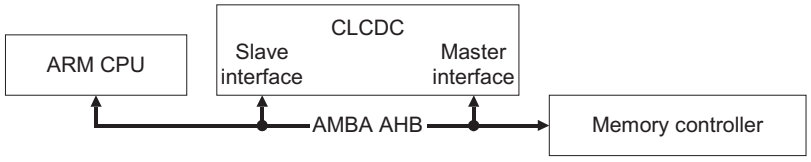

Figure 2-8 Single AHB architecture

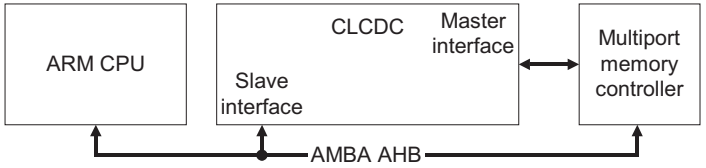

Figure 2-9 Dual-bus AMBA AHB architecture

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Chapter 3
Programmer's Model

This chapter describes the ARM PrimeCell Color LCD Controller (PL110) registers and provides details required when programming the microcontroller. It contains the following sections:

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3.1 Summary of registers

The base address of the ARM PrimeCell CLCDC is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed.

The following locations are reserved, and must not be used during normal operation:

- locations at offsets `0x030-0x1FC` are reserved for possible future extensions
- locations at offsets `0x400-0x7FF` are reserved for test purposes.

The PrimeCell CLCDC registers are shown in Table 3-1.

Table 3-1 PrimeCell CLCDC register summary

Address offset	Type	Width	Reset value	Name	Description
`0x00`	Read/write	32	`0x00000000`	LCDTiming0	See *Horizontal Axis Panel Control Register, LCDTiming0* on page 3-4
`0x004`	Read/write	32	`0x00000000`	LCDTiming1	See *Vertical Axis Panel Control Register, LCDTiming1* on page 3-5
`0x08`	Read/write	32	`0x00000000`	LCDTiming2	See *Clock and Signal Polarity Control Register, LCDTiming2* on page 3-7
`0x0C`	Read/write	17	`0x00000`	LCDTiming3	See *Line End Control Register, LCDTiming3* on page 3-9
`0x010`	Read/write	32	`0x0000000`	LCDUPBASE	See *Upper and Lower Panel Frame Base Address Registers, LCDUPBASE and LCDLPBASE* on page 3-9
`0x14`	Read/write	32	`0x00000000`	LCDLPBASE	See *Upper and Lower Panel Frame Base Address Registers, LCDUPBASE and LCDLPBASE* on page 3-9
`0x18`	Read/write	5	`0x00`	LCDIMSC	See *Interrupt Mask Set/Clear Register, LCDIMSC* on page 3-10
`0x1C`	Read/write	16	`0x0000`	LCDControl	See *Control Register, LCDControl* on page 3-11
`0x20`	Read	5	`0x00`	LCDRIS	See *Raw Interrupt Status Register, LCDRIS* on page 3-13
`0x024`	Read	5	`0x00`	LCDMIS	See *Masked Interrupt Status Register, LCDMIS* on page 3-13

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Table 3-1 PrimeCell CLCDC register summary (continued)

Address offset	Type	Width	Reset value	Name	Description
0x28	Write	5	0x00	LCDICR	See *Interrupt Clear Register, LCDICR* on page 3-14
0x2C	Read	32	X	LCDUPCURR	See *Upper and Lower Panel Current Address Value Registers LCDUPCURR and LCDLPCURR* on page 3-14
0x30	Read	32	X	LCDLPCURR	See *Upper and Lower Panel Current Address Value Registers LCDUPCURR and LCDLPCURR* on page 3-14
0x034-0x1FC	-	-	-	-	Reserved
0x200-0x3FC	Read/write	32	-	LCDPalette	See *Color Palette Register, LCDPalette* on page 3-15
0xFE0	Read	8	0x10	CLCDPERIPHID0	See *Peripheral Identification Register 0, CLCDPERIPHID0* on page 3-16
0xFE4	Read	8	0x11	CLCDPERIPHID1	See *Peripheral Identification Register 1, CLCDPERIPHID1* on page 3-17
0xFE8	Read	4	0x04	CLCDPERIPHID2	See *Peripheral Identification Register 2, CLCDPERIPHID2* on page 3-17
0xFEC	Read	8	0x00	CLCDPERIPHID3	See *Peripheral Identification Register 3, CLCDPERIPHID3* on page 3-17
0xFF0	Read	8	0x0D	CLCDPCELLID0	See *PrimeCell Identification Register 0, CLCDPCELLID0* on page 3-18
0xFF4	Read	8	0xF0	CLCDPCELLID1	See *PrimeCell Identification Register 1, CLCDPCELLID1* on page 3-19
0xFF8	Read	8	0x05	CLCDPCELLID2	See *PrimeCell Identification Register 2, CLCDPCELLID2* on page 3-19
0xFFC	Read	8	0xB1	CLCDPCELLID3	See *PrimeCell Identification Register 3, CLCDPCELLID3* on page 3-19

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3.2 Register descriptions

The register descriptions are provided in this section.

3.2.1 Horizontal Axis Panel Control Register, LCDTiming0

LCDTiming0 is a read/write register that controls the:

- *Horizontal Synchronization pulse Width* (HSW)
- *Horizontal Front Porch* (HFP) period
- *Horizontal Back Porch* (HBP) period
- *Pixels-Per-Line* (PPL).

Table 3-2 shows the bit assignments for the LCDTiming0.

Table 3-2 LCDTiming0 Register bit assignments

Bit	Name	Type	Description
[31:24]	HBP	Read/write	Horizontal back porch, is the number of **CLCP** periods between the falling edge of **CLLP** and the start of active data. Program with value minus 1. The 8-bit HBP field specifies the number of pixel clock periods inserted at the beginning of each line or row of pixels. After the line clock for the previous line has been deasserted, the value in HBP counts the number of pixel clocks to wait before starting the next display line. HBP can generate a delay of 1-256 pixel clock cycles.
[23:16]	HFP	Read/write	Horizontal front porch, is the number of **CLCP** periods between the end of active data and the rising edge of **CLLP**. Program with value minus 1. The 8-bit HFP field sets the number of pixel clock intervals at the end of each line or row of pixels, before the LCD line clock is pulsed. When a complete line of pixels is transmitted to the LCD driver, the value in HFP counts the number of pixel clocks to wait before asserting the line clock. HFP can generate a period of 1-256 pixel clock cycles.
[15:8]	HSW	Read/write	Horizontal synchronization pulse width, is the width of the **CLLP** signal in **CLCP** periods. Program with value minus 1. The 8-bit HSW field specifies the pulse width of the line clock in passive mode, or the horizontal synchronization pulse in active mode.
[7:2]	PPL	Read/write	Pixels-per-line. Actual pixels-per-line = 16 * (PPL + 1). The PPL bit field specifies the number of pixels in each line or row of the screen. PPL is a 6-bit value that represents between 16 and 1 024 PPL. PPL controls how much data is read from the DMA input buffers through to the gray scaler.
[1:0]	-	-	Reserved, do not modify, read as zero, write as zero.

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Horizontal timing restrictions

DMA requests new data at the start of a horizontal display line. Some time must be allowed for the DMA transfer and for the data to propagate down the FIFO path in the LCD interface. The data path latency forces some restrictions on the usable minimum values for horizontal porch width in STN mode. The minimum values are HSW = 2 and HBP = 2.

Single panel mode:

- HSW = 3
- HBP = 5
- HFP = 5
- *Panel Clock Divisor* (PCD) = 1 (**CLCDCLK**/3).

Dual panel mode:

- HSW = 3
- HBP = 5
- HFP = 5
- PCD = 5 (**CLCDCLK**/7).

If sufficient time is given at the start of the line (for example, setting HSW = 6, HBP = 10), data is not corrupted for PCD = 4 (minimum value).

3.2.2 Vertical Axis Panel Control Register, LCDTiming1

LCDTiming1 is a read/write register that controls the:

- number of *Lines-Per-Panel* (LPP)
- *Vertical Synchronization pulse Width (VSW)*
- *Vertical Front Porch* (VFP) period
- *Vertical Back Porch* (VBP) period.

Table 3-3 on page 3-6 shows the bit assignments for the LCDTiming1 Register.

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Table 3-3 LCDTiming1 Register bit assignments

Bit	Name	Type	Description
[31:24]	VBP	Read/write	Vertical back porch is the number of inactive lines at the start of a frame, after vertical synchronization period. Program to 0 on passive displays or reduced contrast results. The 8-bit VBP field specifies the number of line clocks inserted at the beginning of each frame. The VBP count starts just after the vertical synchronization signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit field in passive mode. After this has occurred, the count value in VBP sets the number of line clock periods inserted before the next frame. VBP generates from 0–255 extra line clock cycles.
[23:16]	VFP	Read/write	Vertical front porch is the number of inactive lines at the end of frame, before vertical synchronization period. Program to 0 on passive displays or reduced contrast results. The 8-bit VFP field specifies the number of line clocks to insert at the end of each frame. When a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed the vertical synchronization signal, **CLFP**, is asserted in active mode, or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates from 0–255 line clock cycles.
[15:10]	VSW	Read/write	Vertical synchronization pulse width is the number of horizontal synchronization lines. Must be small (for example, program to zero) for passive STN LCDs. Program to the number of lines required minus one. The higher the value the worse the contrast on STN LCDs. The 6-bit VSW field specifies the pulse width of the vertical synchronization pulse. The register is programmed with the number of line clocks in VSync minus one. Number of horizontal synchronization lines. Must be small (for example, program to 0) for passive STN LCDs. Program to the number of lines required minus 1. The higher the value the worse the contrast on STN LCDs.
[9:0]	LPP	Read/write	Lines per panel is the number of active lines per screen. Program to number of lines required minus 1. The LPP field specifies the total number of lines or rows on the LCD panel being controlled. LPP is a 10-bit value that allows 1-1 024 lines. The register is programmed with the number of lines per LCD panel minus 1. For dual panel displays this register is programmed with the number of lines on each of the upper and lower panels.

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3.2.3 Clock and Signal Polarity Control Register, LCDTiming2

LCDTiming2 is a read/write register that controls the CLCDC timing. Table 3-3 on page 3-6 shows the bit assignments for the LCDTiming1 Register.

Table 3-4 LCDTiming2 Register bit assignments

Bit	Name	Type	Description
[31:27]	PCD_HI	Read/write	Upper five bits of Panel Clock Divisor.[a] The ten-bit PCD field, comprising PCD_HI and PCD_LO (bits [4:0]), is used to derive the LCD panel clock frequency **CLCP** from the **CLCDCLK** frequency: **CLCP** = **CLCDCLK**/(PCD+2). For mono STN displays with a four or eight-bit interface, the panel clock is a factor of four and eight down on the actual individual pixel clock rate. For color STN displays, $2^2/_3$ pixels are output per **CLCP** cycle, therefore the panel clock is 0.375 times.For TFT displays the pixel clock divider can be bypassed by setting the LCDTiming2[26] BCD bit.
[26]	BCD	Read/write	Bypass pixel clock divider. Setting this to 1 bypasses the pixel clock divider logic. This is mainly used for TFT displays.
[25:16]	CPL	Read/write	Clocks per line. This field specifies the number of actual **CLCP** clocks to the LCD panel on each line. This is the number of PPL divided by 1 for TFT, 4 or 8 for mono passive, or $2^2/_3$ for color passive, minus one. This must be correctly programmed in addition to PPL for the LCD controller to work correctly.
[15]	-	-	Reserved, do not modify, read as zero, write as zero.
[14]	IEO	Read/write	Invert output enable: 0 = **CLAC** output pin is active HIGH in TFT mode 1 = **CLAC** output pin is active LOW in TFT mode. The *Invert Output Enable* (IOE) bit is used to select the active polarity of the output enable signal in TFT mode. In this mode, the CLAC pin is used as an enable that indicates to the LCD panel when valid display data is available. In active display mode, data is driven onto the LCD data lines at the programmed edge of CLCP when CLAC is in its active state.
[13]	IPC	Read/write	Invert panel clock: 0 = Data is driven on the LCDs data lines on the rising-edge of **CLCP** 1 = Data is driven on the LCDs data lines on the falling-edge of **CLCP**. The IPC bit is used to select the edge of the panel clock on which pixel data is driven out onto the LCD data lines.

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Table 3-4 LCDTiming2 Register bit assignments (continued)

Bit	Name	Type	Description
[12]	IHS	Read/write	Invert horizontal synchronization: 0 = **CLLP** pin is active HIGH and inactive LOW 1 = **CLLP** pin is active LOW and inactive HIGH. The *Invert HSync* (IHS) bit is used to invert the polarity of the CLLP signal.
[11]	IVS	Read/write	Invert vertical synchronization: 0 = **CLFP** pin is active HIGH and inactive LOW 1 = **CLFP** pin is active LOW and inactive HIGH. The *Invert VSync* (IVS) bit is used to invert the polarity of the CLFP signal.
[10:6]	ACB	Read/write	AC bias pin frequency. The AC bias pin frequency is only applicable to STN displays, which require the pixel voltage polarity to be periodically reversed to prevent damage due to DC charge accumulation. Program this field with the required value minus 1 to apply the number of line clocks between each toggle of the AC bias pin, **CLAC**. This field has no effect if the CLCDC is operating in TFT mode when the **CLAC** pin is used as a data enable signal.
[5]	CLKSEL	Read/write	This bit drives the **CLCDCLKSEL** signal which is used as the select signal for the external LCD clock multiplexor.
[4:0]	PCD_LO	Read/write	Lower five bits of Panel Clock Divisor.[a] The ten-bit PCD field, comprising PCD_HI (bits [31:27]) and PCD_LO, is used to derive the LCD panel clock frequency **CLCP** from the CLCDCLK frequency, **CLCP** = **CLCDCLK**/(PCD+2). For mono STN displays with a four or eight-bit interface, the panel clock is a factor of four and eight down on the actual individual pixel clock rate. For color STN displays, $2\ ^2/_3$ pixels are output per **CLCP** cycle, so the panel clock is 0.375 times. You can bypass the pixel clock divider for TFT displays by setting the LCDTiming2[26] BCD bit.

a. The data path latency forces some restrictions on the usable minimum values for the panel clock divider in STN modes.:
Single-panel color mode: PCD = 1 (**CLCP** = **CLCDCLK**/3)
Dual-panel color mode: PCD = 4 (**CLCP** = **CLCDCLK**/6)
Single-panel mono 4-bit interface mode: PCD = 2(**CLCP** = **CLCDCLK**/4)
Dual-panel mono 4-bit interface mode: PCD = 6(**CLCP** = **CLCDCLK**/8)
Single-panel mono 8-bit interface mode: PCD = 6(**CLCP** = **CLCDCLK**/8)
Dual-panel mono 8-bit interface mode: PCD = 14(**CLCP** = **CLCDCLK**/16).

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3.2.4 Line End Control Register, LCDTiming3

LCDTiming3 is a read/write register that controls the enabling of line-end signal **CLLE**. When enabled, a positive pulse, four **CLCDCLK** periods wide, is output on **CLLE** after a programmed delay set by the LED bits. If the line-end signal is disabled then it is held permanently LOW. Table 3-5 shows the bit assignments for the LCDTiming3 Register.

Table 3-5 LCDTiming3 Register bit assignments

Bit	Name	Type	Description
[31:17]	-	-	Reserved, do not modify, read as zero, write as zero.
[16]	LEE	Read/write	LCD Line end enable: 0 = **CLLE** disabled (held LOW) 1 = **CLLE** signal active.
[15:7]	-	-	Reserved, do not modify, read as zero, write as zero.
[6:0]	LED	Read/write	Line-end signal delay from the rising-edge of the last panel clock, **CLCP**. Program with number of **CLCDCLK** clock periods minus 1.

3.2.5 Upper and Lower Panel Frame Base Address Registers, LCDUPBASE and LCDLPBASE

LCDUPBASE and LCDLPBASE are the color LCD DMA Frame Address Registers. They are read/write registers used to program the base address of the frame buffer. LCDUPBASE is used for:

- TFT displays
- single panel STN displays
- the upper panel of dual panel STN displays.

LCDLPBASE is used for the lower panel of dual panel STN displays.

You must initialize LCDUPBASE (and LCDLPBASE for dual panels) before enabling the CLCDC.

You can change the value mid-frame to enable double-buffered video displays to be created. These registers are copied to the corresponding current registers at each LCD vertical synchronization. This event causes the LNBU bit and an optional interrupt to be generated. You can use the interrupt to reprogram the base address when generating double-buffered video.

Bits [1:0] are 0 value when read.

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Table 3-6 shows the bit assignment for the LCDUPBASE Register.

Table 3-6 LCDUPBASE Register bit assignments

Bit	Name	Type	Description
[31:2]	LCDUPBASE	Read/write	LCD upper panel base address. This is the start address of the upper panel frame data in memory and is word aligned.
[1:0]	-	-	Reserved, do not modify, read as zero, write as zero.

Table 3-7 shows the bit assignment for the LCDLPBASE Register.

Table 3-7 LCDLPBASE Register bit assignments

Bit	Name	Type	Description
[31:2]	LCDLPBASE	Read/write	LCD lower panel base address. This is the start address of the lower panel frame data in memory and is word aligned.
[1:0]	-	-	Reserved, do not modify, read as zero, write as zero.

3.2.6 Interrupt Mask Set/Clear Register, LCDIMSC

LCDIMSC is the Interrupt Mask Set/Clear Register. Setting bits in this register enables the corresponding raw interrupt LCDRIS bit values to be passed to the LCDMIS Register. Table 3-8 shows the bit assignment for the LCDIMSC Register.

Table 3-8 LCDIMSC Register bit assignments

Bit	Name	Type	Description
[4]	MBERRINTRENB	Read/write	AHB master error interrupt enable
[3]	VCOMPINTRENB	Read/write	Vertical compare interrupt enable
[2]	LNBUINTRENB	Read/write	Next base update interrupt enable
[1]	FUFINTRENB	Read/write	FIFO underflow interrupt enable
[0]	-	-	Reserved, do not modify, read as zero, write as zero

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3.2.7 Control Register, LCDControl

LCDControl is the Control Register. It is a read/write register that controls the mode in which the CLCDC operates. Table 3-9 shows the bit assignments for the LCDControl Register.

Table 3-9 LCDControl Register bit assignments

Bit	Name	Type	Description
[31:17]	-	-	Reserved, do not modify, read as zero, write as zero.
[16]	WATERMARK	Read/write	LCD DMA FIFO Watermark level: 0 = **HBUSREQM** is raised when either of the two DMA FIFOs have four or more empty locations 1 = **HBUSREQM** is raised when either of the DMA FIFOs have eight or more empty locations.
[15:14]	-	-	Reserved, do not modify, read as zero, write as zero.
[13:12]	LcdVComp	Read/write	Generate interrupt at: 00 = start of vertical synchronization 01 = start of back porch 10 = start of active video 11 = start of front porch.
[11]	LcdPwr	Read/write	LCD power enable: 0 = power not gated through to LCD panel and **CLD[23:0]** signals disabled, (held LOW) 1 = power gated through to LCD panel and **CLD[23:0]** signals enabled, (active). See *LCD powering up and powering down sequence support* on page 1-5 for details on LCD power sequencing.
[10]	BEPO	Read/write	Big-endian pixel ordering within a byte: 0 = little-endian pixel ordering within a byte 1= big-endian pixel ordering within a byte. The BEPO bit selects between little and big-endian pixel packing for 1, 2, and 4 bpp display modes. It has no effect on 8 or 16 bpp pixel formats. See *Pixel serializer* on page 2-5 for more information on the data format.
[9]	BEBO	Read/write	Big-endian byte order: 0 = little-endian byte order 1 = big-endian byte order.

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Table 3-9 LCDControl Register bit assignments (continued)

Bit	Name	Type	Description
[8]	BGR	Read/write	RGB of BGR format selection: 0 = RGB normal output 1 = BGR red and blue swapped.
[7]	LcdDual	Read/write	LCD interface is dual panel STN: 0 = single panel LCD is in use 1 = dual panel LCD is in use.
[6]	LcdMono8	Read/write	Monochrome LCD has an 8-bit interface. This bit controls whether monochrome STN LCD uses a 4 or 8-bit parallel interface: 0 = mono LCD uses 4-bit interface 1 = mono LCD uses 8-bit interface. LcdMono8 has no meaning in other modes and must be programmed to 0.
[5]	LcdTFT	Read/write	LCD is TFT: 0 = LCD is an STN display, use gray scaler 1 = LCD is TFT, do not use gray scaler.
[4]	LcdBW	Read/write	STN LCD is monochrome (black and white): 0 = STN LCD is color 1 = STN LCD is monochrome. This bit has no meaning in TFT mode.
[3:1]	LcdBpp	Read/write	LCD bits per pixel: 000 = 1 bpp 001 = 2 bpp 010 = 4 bpp 011 = 8 bpp 100 = 16 bpp 101 = 24 bpp (TFT panel only) 110 = reserved 111 = reserved.
[0]	LcdEn	Read/write	LCD controller enable: 0 = **CLLP**, **CLCP**, **CLFP**, **CLAC**, and **CLLE** disabled (held LOW) 1 = **CLLP**, **CLCP**, **CLFP**, **CLAC**, and **CLLE** enabled (active). Refer to *LCD powering up and powering down sequence support* on page 1-5 for details on LCD power sequencing.

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3.2.8 Raw Interrupt Status Register, LCDRIS

LCDRIS is a read-only register. On a read it returns five bits that can generate interrupts when set. Table 3-10 shows the bit assignments for the LCDRIS Register.

Table 3-10 LCDRIS Register bit assignments

Bit	Name	Type	Description
[4]	MBERROR	Read	AHB Master bus error status, set when the AHB Master encounters a bus error response from a slave.
[3]	Vcomp	Read	Vertical compare, set when one of the four vertical regions, selected through the LCDControl Register, is reached.
[2]	LNBU	Read	LCD next address base update, mode dependent, set when the Current Base Address Registers have been successfully updated by the next Address Registers. Signifies that a new next address can be loaded if double buffering is in use.
[1]	FUF	Read	FIFO underflow, set when either the upper or lower DMA FIFOs have been read accessed when empty causing an underflow condition to occur.
[0]	-	-	Reserved, read as zero.

3.2.9 Masked Interrupt Status Register, LCDMIS

LCDMIS is a read-only register. It is a bit-by-bit logical AND of the LCDRIS Register and the LCDIMSC Register. Interrupt lines correspond to each interrupt. A logical OR of all interrupts is provided to the system interrupt controller. Table 3-11 shows the bit assignment for the LCDMIS Register.

Table 3-11 LCDMIS Register bit assignments

Bit	Name	Type	Description
[31:5]	-	-	Reserved, read as zero
[4]	MBERRORINTR	Read	AHB master error interrupt status bit
[3]	VCOMPINTR	Read	Vertical compare interrupt status bit
[2]	LNBUINTR	Read	LCD next base address update interrupt status bit
[1]	FUFINTR	Read	FIFO underflow interrupt status bit
[0]	-	-	Reserved, read as zero

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3.2.10 Interrupt Clear Register, LCDICR

The LCDICR is a write-only register. Writing a logic 1 to the relevant bit clears the corresponding interrupt. Table 3-12 shows the bit assignments for the LCDICR Register.

Table 3-12 LCDICR Register bit assignments

Bit	Name	Type	Description
[31:5]	-	-	Reserved, do not modify, write as zero
[4]	Clear MBERROR	Write	Clear AHB Master error interrupt
[3]	Clear Vcomp	Write	Clear vertical compare interrupt
[2]	Clear LNBU	Write	Clear LCD next base address update interrupt
[1]	Clear FUF	Write	Clear FIFO underflow interrupt
[0]	-	-	Reserved, do not modify, write as zero

3.2.11 Upper and Lower Panel Current Address Value Registers LCDUPCURR and LCDLPCURR

LCDUPCURR and LCDLPCURR are read-only registers that contain an approximate value of the upper and lower panel data DMA addresses when read. The registers can change at any time and therefore can only be used as a mechanism for coarse delay.

Table 3-13 shows the bit assignments for the LCDUPCURR Register.

Table 3-13 LCDUPCURR Register bit assignments

Bit	Name	Type	Description
[31:0]	LCDUPCURR	Read	Contains the approximate current upper panel data DMA address

Table 3-14 shows the bit assignments for the LCDLPCURR Register.

Table 3-14 LCDLPCURR Register bit assignments

Bit	Name	Type	Description
[31:0]	LCDLPCURR	Read	Contains the approximate current lower panel data DMA address

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3.2.12 Color Palette Register, LCDPalette

The LCDPalette Register contains 256 palette entries organized as 128 locations of two entries per word. Only TFT displays use all of the palette entry bits.

Each word location contains two palette entries. This means that 128 word locations are used for the palette. When configured for little-endian byte ordering, bits [15:0] are the lower numbered palette entry and bits [31:16] are the higher numbered palette entry. When configured for big-endian byte ordering this is reversed because bits [31:16] are the low numbered palette entry and bits [15:0] are the high numbered entry.

Table 3-15 shows the bit assignment for the LCDPalette Register.

Table 3-15 LCDPalette Register bit assignments

Bit	Name	Type	Description
[31]	I	Read/write	Intensity/unused.
[30:26]	B[4:0]	Read/write	Blue palette data.
[25:21]	G[4:0]	Read/write	Green palette data.
[20:16]	R[4:0]	Read/write	Red palette data.
[15]	I	Read/write	Intensity bit. Can be used as the LSB of the R, G, and B inputs to a 6:6:6 TFT display, doubling the number of colors to 64K, where each color has two different intensities.
[14:10]	B[4:0]	Read/write	Blue palette data.
[9:5]	G[4:0]	Read/write	Green palette data.
[4:0]	R[4:0]	Read/write	Red palette data. For STN displays, only the four MSBs (bits [4:1]) are used. For monochrome displays only the red palette data is used. All of the Palette Registers have the same bit fields.

3.2.13 Peripheral Identification Registers, CLCDPERIPHID0-3

The CLCDPERIPHID0-3 Registers are four 8-bit registers, that span address locations `0xFE0-0xFEC`. The registers can conceptually be treated as a single 32-bit register. The read-only registers provide the following options of the peripheral:

PartNumber[11:0] This is used to identify the peripheral. The product code `0x10` is used for the PrimeCell CLCDC.

DesignerID[19:12] This is the identification of the designer. ARM Limited is `0x41` (ASCII A).

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Revision[23:20] This is the revision number of the peripheral. The revision number starts from 0 and is revision dependent.

Configuration[31:24]

This is the configuration option of the peripheral. The configuration value is 0.

Figure 3-1 shows the bit assignment for the CLCDPERIPHID0-3 Registers.

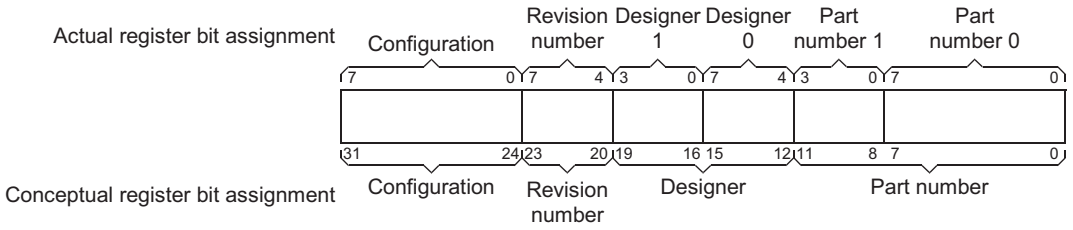

Figure 3-1 Peripheral Identification Register bit assignments

The four Peripheral Identification Registers are described in the following sections:

- *Peripheral Identification Register 0, CLCDPERIPHID0*
- *Peripheral Identification Register 1, CLCDPERIPHID1* on page 3-17
- *Peripheral Identification Register 2, CLCDPERIPHID2* on page 3-17
- *Peripheral Identification Register 3, CLCDPERIPHID3* on page 3-17.

Peripheral Identification Register 0, CLCDPERIPHID0

The CLCDPERIPHID0 Register is hard-coded and the fields in the register determine the reset value. Table 3-16 shows the bit assignments of the CLCDPERIPHID0 Register.

Table 3-16 CLCDPERIPHID0 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	PartNumber0	These bits read back as `0x10`

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Peripheral Identification Register 1, CLCDPERIPHID1

The CLCDPERIPHID1 Register is hard-coded and the fields in the register determine the reset value. Table 3-17 shows the bit assignments of the CLCDPERIPHID1 Register.

Table 3-17 CLCDPERIPHID1 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:4]	Designer0	These bits read back as `0x1`
[3:0]	PartNumber1	These bits read back as `0x1`

Peripheral Identification Register 2, CLCDPERIPHID2

The CLCDPERIPHID2 Register is hard-coded and the fields in the register determine the reset value. Table 3-18 shows the bit assignments of the CLCDPERIPHID2 Register.

Table 3-18 CLCDPERIPHID2 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:4]	Revision	These bits read back as `0x0`
[3:0]	Designer1	These bits read back as `0x4`

Peripheral Identification Register 3, CLCDPERIPHID3

The CLCDPERIPHID3 Register is hard-coded and the fields in the register determine the reset value. Table 3-19 shows the bit assignments of the CLCDPERIPHID3 Register.

Table 3-19 CLCDPERIPHID3 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	Configuration	These bits read back as `0x00`

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3.2.14 PrimeCell Identification Registers, CLCDPCELLIDID0-3

The CLCDPCELLIDID0-3 Registers are four 8-bit registers, that span address locations `0xFF0-0xFFC`. The registers can conceptually be treated as a 32-bit register. The register is used as a standard cross-peripheral identification system. Figure 3-2 shows the bit assignments for the CLCDPCELLIDID0-3 Registers.

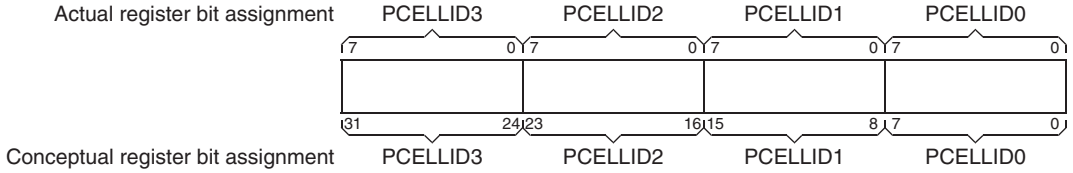

Figure 3-2 PrimeCell Identification Register bit assignments

The four PrimeCell Identification Registers are described in the following subsections:

- *PrimeCell Identification Register 0, CLCDPCELLID0*
- *PrimeCell Identification Register 1, CLCDPCELLID1* on page 3-19
- *PrimeCell Identification Register 2, CLCDPCELLID2* on page 3-19
- *PrimeCell Identification Register 3, CLCDPCELLID3* on page 3-19.

PrimeCell Identification Register 0, CLCDPCELLID0

The CLCDPCELLIDID0 Register is hard-coded and the fields in the register determine the reset value. Table 3-20 shows the bit assignments of the CLCDPCELLIDID0 Register.

Table 3-20 CLCDPCELLIDID0 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	PCELLIDID0	These bits read back as `0x0D`

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PrimeCell Identification Register 1, CLCDPCELLID1

The CLCDPCELLIDID1 Register is hard-coded and the fields in the register determine the reset value. Table 3-21 shows the bit assignments of the CLCDPCELLIDID1 Register.

Table 3-21 CLCDPCELLIDID1 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	PCELLIDID1	These bits read back as `0xF0`

PrimeCell Identification Register 2, CLCDPCELLID2

The CLCDPCELLIDID2 Register is hard-coded and the fields in the registers determine the reset value. Table 3-22 shows the bit assignments of the CLCDPCELLIDID2 Register.

Table 3-22 CLCDPCELLIDID2 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	PCELLIDID2	These bits read back as `0x05`

PrimeCell Identification Register 3, CLCDPCELLID3

The CLCDPCELLIDID3 Register is hard-coded and the fields in the registers determine the reset value. Table 3-23 shows the bit assignment of the CLCDPCELLIDID3 Register.

Table 3-23 CLCDPCELLIDID3 Register bit assignments

Bits	Name	Description
[31:8]	-	Reserved, read as zero
[7:0]	PCELLIDID3	These bits read back as `0xB1`

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3.3 Interrupts

There are five interrupts generated by the CLCDC. The following are individual maskable active HIGH interrupts:

- *CLCDMBEINTR*
- *CLCDVCOMPINTR*
- *CLCDLNBUINTR* on page 3-21
- *CLCDFUFINTR* on page 3-21.

The outputs are also output as a combined single interrupt CLCDINTR.

Each of the four individual maskable interrupts is enabled or disabled by changing the mask bits in the LCDIMSC Register.

Provision of individual outputs as well as a combined interrupt output enables you to use either:

- a global interrupt service routine
- modular device drivers to handle interrupts.

The status of the individual interrupt sources can be read from the LCDRIS Register.

3.3.1 CLCDMBEINTR

The master bus error interrupt is asserted when an ERROR response is received by the master interface during a transaction with a slave. When such an error is encountered, the master interface enters an error state and remains in this state until clearance of the error has been signalled to it. On completion of the respective interrupt service routine, the master bus error interrupt can be cleared by writing a 1 to the MBERROR bit within the LCDICR Register. This action releases the master interface from its ERROR state to the start of FRAME state, enabling a fresh frame of data display to be initiated.

3.3.2 CLCDVCOMPINTR

The vertical compare interrupt is asserted when one of four vertical display regions, selected using the Control Register, is reached. The interrupt can be made to occur at the start of:

- vertical synchronization
- back porch
- active video
- front porch.

You can clear the interrupt by writing a 1 to the VComp bit in the LCDICR Register.

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3.3.3 CLCDLNBUINTR

The LCD next base address update interrupt is asserted when either the LCDUPBASE or the LCDLPBASE values are transferred to the LCDUPCURR or LCDLPCURR incrementors respectively. This signals to the system that it is safe to update the LCDUPBASE or the LCDLPBASE Registers with new frame base addresses if required.

You can clear the interrupt by writing a 1 to the LNBU bit in the LCDICR Register.

3.3.4 CLCDFUFINTR

The FIFO underflow interrupt is asserted when internal data is requested from an empty DMA FIFO. Internally, individual upper and lower panel DMA FIFO underflow interrupt signals are generated and CLCDFUFINTR is the single combined version of these.

You can clear the interrupt by writing a 1 to the FUF bit in the LCDICR Register.

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Chapter 4
Programmer's Model for Test

This chapter describes the additional logic for functional verification and production testing. It contains the following sections:

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4.1 Scan testing

The PrimeCell CLCDC has been designed to enable:

- the automatic insertion of scan test cells
- the use of *Automatic Test Pattern Generation* (ATPG).

This is the recommended method of manufacturing test.

During scan testing, the **SCANENABLE** must be driven HIGH to enable bypassing of the DMS FIFOs. For normal use **SCANENABLE** must be negated LOW.

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4.2 Summary of test registers

The PrimeCell CLCDC test registers are memory-mapped as shown in Table 4-1.

Table 4-1 CLCDC test register summary

Address offset	Type	Width	Name	Description
0xF00	Read/write	1	CLCDTCR	See *Test Control Register, CLCDTCR* on page 4-4
0xF04	Read/write	6	CLCDITOP1	See *Integration Test Output Register 1, CLCDITOP1* on page 4-4
0xF08	Read/write	30	CLCDITOP1	See *Integration Test Output Register 2, CLCDITOP2* on page 4-5

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4.3 Test register descriptions

This section describes the CLCDC test registers

4.3.1 Test Control Register, CLCDTCR

The CLCDTCR Register is a single-bit control register. This register must only be used in test mode. The register bit assignments are listed in Table 4-2.

Table 4-2 CLCDTCR bit assignments

Bit	Name	Type	Description
[31:1]	-	-	Reserved, do not modify, write as zero
[1]	ITEN	Read/write	Integration test enable bit. When set to 1, the CLCDITOP1 and CLCDITOP2 Registers are used to read and write values to the intra-chip and primary outputs respectively.

4.3.2 Integration Test Output Register 1, CLCDITOP1

CLCDITOP1 is one of two Integration Test Output Registers. If the CLCDTCR[0] ITEN bit is high then the CLCDITOP1 register value is used, otherwise the functional mode value is driven onto the intra-chip output port. The register bit assignments are listed in Table 4-3.

Table 4-3 CLCDITOP1 bit assignments

Bit	Name	Type	Description
[31:6]	-	-	Reserved, do not modify, write as zero
[5]	CLCDCLKSEL	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDCLKSEL** line when in integration test mode. A read returns the value of the **CLCDCLKSEL** signal at the output of the test multiplexor.
[4]	CLCDMBEINTR	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDMBEINTR** line when in integration test mode. A read returns the value of the **CLCDMBEINTR** signal at the output of the test multiplexor.
[3]	CLCDFUFINTR	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDFUFINTR** line when in integration test mode. A read returns the value of the **CLCDFUFINTR** signal at the output of the test multiplexor.

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Table 4-3 CLCDITOP1 bit assignments (continued)

Bit	Name	Type	Description
[2]	CLCDLNBUINTR	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDLNBUINTR** line when in integration test mode. A read returns the value of the **CLCDLNBUINTR** signal at the output of the test multiplexor.
[1]	CLCDVCOMPINTR	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDVCOMPINTR** line when in integration test mode. A read returns the value of the **CLCDVCOMPINTR** signal at the output of the test multiplexor.
[0]	CLCDINTR	Read/write	Intra-chip output. Writes specify the value to be driven on the **CLCDINTR** line when in integration test mode. A read returns the value of the **CLCDINTR** signal at the output of the test multiplexor.

4.3.3 Integration Test Output Register 2, CLCDITOP2

CLCDITOP2 is one of two Integration Test Output Registers. If the CLCDTCR[0] ITEN bit is high, the CLCDITOP2 register value is used, otherwise the functional mode value is driven onto the primary output port. The register bit assignments are listed in Table 4-4.

Table 4-4 CLCDITOP2 bit assignments

Bit	Name	Type	Description
[31:30]	-	-	Reserved, do not modify, write as zero
[29]	CLPOWER	Read/write	Primary output. Writes specify the value to be driven on the **CLPOWER** line when in integration test mode.
[28]	CLLP	Read/write	Primary output. Writes specify the value to be driven on the **CLLP** line when in integration test mode.
[27]	CLCP	Read/write	Primary output. Writes specify the value to be driven on the **CLCP** line when in integration test mode.
[26]	CLFP	Read/write	Primary output. Writes specify the value to be driven on the **CLFP** line when in integration test mode.

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Table 4-4 CLCDITOP2 bit assignments (continued)

Bit	Name	Type	Description
[25]	CLAC	Read/write	Primary output. Writes specify the value to be driven on the **CLAC** line when in integration test mode.
[24]	CLLE	Read/write	Primary output. Writes specify the value to be driven on the **CLLE** line when in integration test mode.
[23:0]	CLD	Read/write	Primary output. Writes specify the value to be driven on the **CLD** line when in integration test mode.

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Appendix A
Signal Descriptions

This appendix describes the signals that interface with the ARM PrimeCell Color LCD Controller (PL110) and contains the following sections:

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A.1 AMBA AHB Slave interface signals

Table A-1 lists the AMBA AHB Slave interface signals.

Table A-1 AMBA AHB Slave interface signals

Signal name	Type	Source/ destination	Description
HADDRS[11:2]	Input	AMBA AHB bus	Address bus.
HCLK	Input	AMBA AHB bus	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of **HCLK**.
HRDATAS[31:0]	Output	AMBA AHB bus	Read data bus.
HREADYSin	Input	AMBA AHB bus	When HIGH this signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend the transfer.
HREADYSout	Output	AMBA AHB bus	When HIGH this signal indicates that the slave is ready for the next transfer. This signal can be driven LOW to extend the transfer.
HRESETn	Input	AMBA AHB bus	Bus reset signal. The bus reset signal is used to reset the system and the bus. This is an active LOW signal.
HRESPS[1:0]	Output	AMBA AHB bus	The transfer response provides additional information on the status of a transfer. Only the OKAY response is supported.
HSELCLCD	Input	Decoder	Device select signal.
HTRANSS[1:0]	Input	AMBA AHB bus	Indicates the type of the current transfer, which can be nonsequential, sequential, idle or busy.
HWDATAS[31:0]	Input	AMBA AHB bus	Write data bus.
HWRITES	Input	AMBA AHB bus	When HIGH this signal indicates a write transfer and when LOW a read transfer.

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A.2 AMBA AHB Master interface signals

Table A-2 lists the AMBA AHB Master interface signals.

Table A-2 AMBA AHB Master interface signals

Signal name	Type	Source/ destination	Description
HADDRM[31:0]	Output	AMBA AHB bus	Address bus.
HBURSTM[2:0]	Output	AMBA AHB bus	Indicates if the transfer forms a part of the burst. 4, 8, and 16 incrementing bursts are supported.
HBUSREQM	Output	Arbiter	Bus request. When HIGH this indicates that the bus master requires the bus.
HGRANTM	Input	Arbiter	Bus grant. This signal indicates that the bus master is currently the highest priority master. Ownership of the address/control signals changes at the end of a transfer when **HREADYMin** is HIGH, and this master gets access to the bus when both **HREADYMin** and **HGRANTM** are HIGH.
HLOCK	Output	Arbiter	When HIGH this signal indicates that the master requires locked access.
HPROT[3:0]	Output	AMBA AHB bus	The protection signals provide additional information about a bus access. They are primarily intended for use by any module that wishes to implement some level of protection.
HRDATAM[31:0]	Input	AMBA AHB bus	Read data bus.
HREADYMin	Input	AMBA AHB bus	When HIGH this signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend the transfer.
HRESPM[1:0]	Input	AMBA AHB bus	The transfer response provides additional information on the status of a transfer. Only OKAY, ERROR, and RETRY responses are fully supported.
HSIZEM[2:0]	Output	AMBA AHB bus	Indicates the size of the transfer. Only word size accesses are supported.
HTRANSM[1:0]	Output	AMBA AHB bus	Indicates the type of the current transfer, which can be nonsequential, sequential, idle or busy.
HWRITEM	Output	AMBA AHB bus	When HIGH this signal indicates a write transfer and when LOW a read transfer.

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A.3 External pad interface signals

Table A-3 lists the output PAD interface signals.

Table A-3 External pad interface signals

Signal name	Type	Source/ destination	Description
CLAC	Output	PAD	STN AC bias drive or TFT data enable output
CLCP	Output	PAD	LCD panel clock
CLD[23:0]	Output	PAD	LCD panel data
CLFP	Output	PAD	Frame pulse (STN)/vertical synchronization pulse (TFT)
CLLE	Output	PAD	Line end signal
CLLP	Output	PAD	Line synchronization pulse (STN)/horizontal synchronization pulse (TFT)
CLPOWER	Output	PAD	LCD panel power enable

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A.4 On-chip signals

A free-running reference clock, **CLCDCLK**, must be provided. By default it is assumed to be asynchronous to **HCLK**.

The reset inputs are asynchronously asserted but synchronously removed for each of the clock domains within the CLCDC. This ensures that logic is reset even if clocks are not present, to avoid any static power consumption problems at power up. Each clock domain has an individual reset to simplify the process of inserting scan test cells.

The on-chip signals required in addition to the AMBA AHB signals are shown in Table A-4.

Table A-4 On-chip signals

Signal name	Type	Source/ destination	Description
CLCDCLK	Input	Clock multiplexor	CLCDC reference clock.
CLCDCLKSEL	Output	Clock multiplexor	CLCDC reference clocks select signal. It is driven by bit 5 of LCDTiming2 Register and selects between **HCLK** or **CLCDCLK** as the source for the reference clocks.
CLCDFUFINTR	Output	Interrupt controller	CLCDC FIFO underflow interrupt, active HIGH. A combined interrupt generated when either of the upper or lower panel DMA FIFOs underflow.
CLCDINTR	Output	Interrupt controller	CLCDC interrupt, active HIGH. A single combined interrupt generated as an OR function of the four individually maskable interrupts above.
CLCDLNBUINTR	Output	Interrupt controller	CLCDC next base address update interrupt, active HIGH.
CLCDMBEINTR	Output	Interrupt controller	CLCDC master bus error interrupt, active HIGH.
CLCDVCOMPINTR	Output	Interrupt controller	CLCDC vertical region compare interrupt, active HIGH.
CLCLKRESETn	Input	Reset multiplexor	CLCDC reset signal to the **CLCDCLK** domain, active LOW. The reset controller must use **HRESETn** to assert **CLCLKRESETn** asynchronously but negate it synchronously with **CLCDCLK**.
nCLCDCLK	Input	Clock multiplexor	Inverse of CLCDC reference clock.

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A.5 Scan test signals

Table A-5 shows the CLCDC scan test signals.

Table A-5 Scan test signals

Signal name	Type	Source/ Destination	Description
SCANENABLE	Input	Test Controller	Scan enable
SCANINCLCDCLK	Input	Test Controller	Scan input for **CLCDCLK** domain
SCANINHCLK	Input	Test Controller	Scan input for **HCLK** domain
SCANINnCLCDCLK	Input	Test Controller	Scan input for **nCLCDCLK** domain
SCANOUTCLCDCLK	Output	Test Controller	Scan output for **CLCDCLK** domain
SCANOUTHCLK	Output	Test Controller	Scan output for **HCLK** domain
SCANOUTnCLCDCLK	Output	Test Controller	Scan output for **nCLCDCLK** domain

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A.6 LCD panel signal multiplexing details

The **CLLP**, **CLAC**, **CLFP**, **CLCP** and **CLLE** signals are common but the CLD[23:0] bus has eight modes of operation corresponding to:

- TFT 24-bit interface
- TFT 18-bit interface
- color STN single panel
- color STN Dual panel
- 4-bit mono STN single panel
- 4-bit mono STN dual panel
- 8-bit mono STN single panel
- 8-bit mono STN dual panel.

Note

- CUSTN = Color upper panel STN, dual and/or single panel
- CLSTN = Color lower panel STN, single
- MUSTN = Mono upper panel STN, dual and/or single panel
- MLSTN = Mono lower panel STN, single.

Table A-6 shows which **CLD[23:0]** pins are used to supply the pixel data to the STN panel for each of the above modes of operation.

Table A-6 LCD STN panel signal multiplexing

External pin	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[23]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[22]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[21]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[20]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[19]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[18}	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[17]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
CLD[16]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Table A-6 LCD STN panel signal multiplexing (continued)

External pin	Color STN single panel	Color STN dual panel	4-bit mono STN single panel	4-bit mono STN dual panel	8-bit mono STN single panel	8-bit mono STN dual panel
CLD[15]	Reserved	**CLSTN[0]**	Reserved	Reserved	Reserved	**MLSTN[0]**
CLD[14]	Reserved	**CLSTN[1]**	Reserved	Reserved	Reserved	**MLSTN[1]**
CLD[13]	Reserved	**CLSTN[2]**	Reserved	Reserved	Reserved	**MLSTN[2]**
CLD[12]	Reserved	**CLSTN[3]**	Reserved	Reserved	Reserved	**MLSTN[3]**
CLD[11]	Reserved	**CLSTN[4]**	Reserved	**MLSTN[0]**	Reserved	**MLSTN[4]**
CLD[10]	Reserved	**CLSTN[5]**	Reserved	**MLSTN[1]**	Reserved	**MLSTN[5]**
CLD[9]	Reserved	**CLSTN[6]**	Reserved	**MLSTN[2]**	Reserved	**MLSTN[6]**
CLD[8]	Reserved	**CLSTN[7]**	Reserved	**MLSTN[3]**	Reserved	**MLSTN[7]**
CLD[7]	**CUSTN[0]**	**CUSTN[0]**	Reserved	Reserved	**MUSTN[0]**	**MUSTN[0]**
CLD[6]	**CUSTN[1]**	**CUSTN[1]**	Reserved	Reserved	**MUSTN[1]**	**MUSTN[1]**
CLD[5]	**CUSTN[2]**	**CUSTN[2]**	Reserved	Reserved	**MUSTN[2]**	**MUSTN[2]**
CLD[4]	**CUSTN[3]**	**CUSTN[3]**	Reserved	Reserved	**MUSTN[3]**	**MUSTN[3]**
CLD[3]	**CUSTN[4]**	**CUSTN[4]**	**MUSTN[0]**	**MUSTN[0]**	**MUSTN[4]**	**MUSTN[4]**
CLD[2]	**CUSTN[5]**	**CUSTN[5]**	**MUSTN[1]**	**MUSTN[1]**	**MUSTN[5]**	**MUSTN[5]**
CLD[1]	**CUSTN[6]**	**CUSTN[6]**	**MUSTN[2]**	**MUSTN[2]**	**MUSTN[6]**	**MUSTN[6]**
CLD[0]	**CUSTN[7]**	**CUSTN[7]**	**MUSTN[3]**	**MUSTN[3]**	**MUSTN[7]**	**MUSTN[7]**

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Table A-7 shows which **CLD[23:0]** pins are used to supply the pixel data to the TFT panel for each of the above modes of operation.

Table A-7 LCD TFT panel signal multiplexing

External pin	TFT 24 bit	TFT 18 bit
CLD[23]	**BLUE[7]**	Reserved
CLD[22]	**BLUE[6]**	Reserved
CLD[21]	**BLUE[5]**	Reserved
CLD[20]	**BLUE[4]**	Reserved
CLD[19]	**BLUE[3]**	Reserved
CLD[18}	**BLUE[2]**	Reserved
CLD[17]	**BLUE[1]**	**BLUE[4]**
CLD[16]	**BLUE[0]**	**BLUE[3]**
CLD[15]	**GREEN[7]**	**BLUE[2]**
CLD[14]	**GREEN[6]**	**BLUE[1]**
CLD[13]	**GREEN[5]**	**BLUE[0]**
CLD[12]	**GREEN[4]**	Intensity bit
CLD[11]	**GREEN[3]**	**GREEN[4]**
CLD[10]	**GREEN[2]**	**GREEN[3]**
CLD[9]	**GREEN[1]**	**GREEN[2]**
CLD[8]	**GREEN[0]**	**GREEN[1]**
CLD[7]	**RED[7]**	**GREEN[0]**
CLD[6]	**RED[6]**	Intensity bit
CLD[5]	**RED[5]**	**RED[4]**
CLD[4]	**RED[4]**	**RED[3]**
CLD[3]	**RED[3]**	**RED[2]**

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Table A-7 LCD TFT panel signal multiplexing (continued)

External pin	TFT 24 bit	TFT 18 bit
CLD[2]	**RED[2]**	**RED[1]**
CLD[1]	**RED[1]**	**RED[0]**
CLD[0]	**RED[0]**	Intensity bit

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