EMV®*
Integrated Circuit Card Specifications for Payment Systems

EMVCo Terminal Type Approval: Level 1 Mechanical and Electrical Test Cases

Version 4.3a
November 2015

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1 Scope

EMVCo, LLC ("EMVCo") is the owner of the EMV Integrated Circuit Card Specification for Payment Systems (version 4.3), hereinafter called EMV Specification.

This specification is divided in 4 books:

- Book 1: Application Independent ICC to Terminal Interface Requirements
- Book 2: Security and Key Management
- Book 3: Application Specification
- Book 4: Cardholder, Attendant, and Acquirer Interface Requirements

The Book 1 (Part II) and Book 2 define the complete flow of a transaction between an Integrated Circuit Card (ICC) and a terminal, from the selection of an application in the ICC to the completion of the transaction.

The Book 3 defines the format of ICC commands used during the transaction flow between the ICC and terminal. Also defined is the transaction flow and associated data for an application compliant with the EMV specifications.

Finally, the Book 4 defines the characteristics of a Terminal that supports an ICC conforming to the two previous specifications mentioned.

EMVCo's objective is that terminals used for any transaction within the payment systems of EMVCo's members (i.e. American Express, China UnionPay, Discover Financial Services, JCB, MasterCard International and VISA International) are conform to the EMV Specification.

Within Book 1, Part I of the Integrated Circuit Card Specification for Payment Systems defines electromechanical characteristics, logical interface, and transmission protocols as they apply to the exchange of information between an Integrated Circuit Card (ICC) and a terminal. The purpose of the specification mentioned above is to maximize confidence that ICCs and terminals do not damage each other, and that ICCs and terminals function together correctly up to the point of exchanging information.

The present document, 'EMVCo Terminal Type Approval: Level 1 Mechanical and Electrical Test Cases', describes the test cases that, when applied to the IFM part of terminals, are designed to determine whether the IFM meets the mechanical and electrical requirements listed in the Book 1, Part I.

The test cases described cover only the IFM interface as defined in the 'EMVCo Type Approval – Terminal Level 1 – Administrative Process' (See [D05]), and test mechanical, electrical and answer to reset requirements. Testing of character transmission, T=0 protocol, and T=1 protocol requirements is described in a separate document. The test cases presented below do not cover the terminal/host interface (if present), general terminal functionality, or other regulatory requirements such as electrical safety or electromagnetic compatibility.

The environment and conditions to be maintained during testing are defined in section 4.3 below. If any special conditions are required for a specific test case, these conditions are described in the test case itself.

The intended audience for this document is testers (EMVCo accredited test laboratories), terminal equipment vendors and qualified auditors.

A testing laboratory that wants to implement and run test cases described in the present document shall follow the rules defined in EMVCo 'Terminal Level 1 Type Approval – Administrative Process' document (See [D05]).

2 Reference Documents

The following are the standards and card approval documentation referenced within the Level 1 Terminal Type Approval process.

2.1 EMVCo Documents

EMV documents are available on the EMVCo website : http://www.emvco.com
The following publications relate to this manual:

[D01] "*EMV Integrated Circuit Card Specifications for Payment Systems — Book 1 — Application Independent ICC to Terminal Interface Requirements*", version 4.3, November 2011.

[D02] "*EMV Integrated Circuit Card Specifications for Payment Systems — Book 2 — Security and Key Management*", version 4.3, November 2011.

[D03] "*EMV Integrated Circuit Card Specifications for Payment Systems — Book 3 — Application Specification*", version 4.3, November 2011.

[D04] "*EMV Integrated Circuit Card Specifications for Payment Systems — Book 4 — Cardholder, Attendant, and Acquirer Interface Requirements*", version 4.3, November 2011.

[D05] "*EMVCo Terminal Type Approval — IFM Level 1 Administrative Process*", version 4.3a, November 2015.

[D06] "*EMVCo Type Approval — Contact Terminal Level 1 — Protocol Test Cases*", version 4.3a, November 2015.

[D07] "*EMVCo Terminal Type Approval — Level 1 Loopback Upper Tester Specification*", version 4.3a, November 2015.

2.2 ISO Standards

The following ISO Standards apply to this document:

ISO/IEC 7816 (15 parts)	*Identification cards – Integrated circuit cards*
ISO/IEC 17025:2005	*General Requirements for the Competence of Calibration and Testing Laboratories.*
ISO/IEC Guide 98-3:2008	*Uncertainty of measurement — Part 3 — Guide to the Expression of Uncertainty in Measurements.*
ISO 5725 (5 parts)	*Accuracy (trueness and precision) of measurements methods and results.*

3 Glossary of Terms

3.1 Abbreviations and Notations

The following abbreviations and notations are used in this document:

εΩ	Resistance Measurement Uncertainty of the Test Tool equipment
ε%	Duty Cycle Measurement Uncertainty of the Test Tool equipment
εA	Current Measurement Uncertainty of the Test Tool equipment
εHz	Frequency Measurement Uncertainty of the Test Tool equipment
εN	Force Measurement Uncertainty of the Test Tool equipment
εs	Time Measurement Uncertainty of the Test Tool equipment
εV	Absolute Voltage Measurement Uncertainty of the Test Tool equipment
εVV	Voltage Measurement Uncertainty of the Test Tool Equipment for Voltages that are a Function of V_{CC}
µA	Microampere or 10^{-6} A
µs	Microsecond or 10^{-6} s
Ω	Ohm
AC	Alternating Current
ADC	Analogue-Digital Conversion
APDU	Application Protocol Data Unit
ATR	Answer To Reset
BGT	Block Guard Time
BWI	Block Waiting Time Integer
BWT	Block Waiting Time
C-APDU	Command APDU
C_{IN}	Input Capacitance
CLA	Class Byte of the Command Message
CLK	Clock
C-TPDU	Command TPDU
CWI	Character Waiting Time Integer

CWT	Character Waiting Time
DAD	Destination Node Address
DC	Direct Current
DUT	Device Under Test
EDC	Error Detection Code
Etu	Elementary Time Unit
f	Frequency
f_i	Average Frequency for the i^{th} Monitoring Interval
GND	Ground
ICC	Integrated Circuit card
I_{CC}	Current on the VCC contact
I_{CLK}	Current on the CLK contact
ICS	Implementation Conformance Statement
I_{IO}	Current on the I/O contact
I_{RST}	Current on the RST contact
ID-1	Identification Card Format
IFD	Interface Device
IFM	Interface Module
IFS	Information Field Size
IFSC	Information Field Size for the ICC
IFSD	Information Field Size for the Terminal
IFSI	Information Field Size Integer
I_{IH}	High Level Input Current
I_{IL}	Low Level Input Current
INF	Information Field
INS	Instruction Byte of Command Message
IUT	Implementation Under Test
I/O	Input/Output
I_{OH}	High Level Output Current
I_{OL}	Low Level Output Current
ISO	International Organization for Standardization

Lc	Exact Length of Data Sent by the TAL in a Case 3 or 4 Command
Le	Maximum Length of Data Expected by the TAL in Response to a Case 2 or 4 Command
Licc	Exact Length of Data Available in the ICC to be Returned in Response to the Case 2 or 4 Command Received by the ICC
LEN	Length
Lr	Length of Response Data Field
MΩ	Megohm or 10^6 Ω
mA	Milliampere or 10^{-3} A
max.	Maximum
MHz	Megahertz or 10^6 Hz
min.	Minimum
mm	Millimeter or 10^{-3} m
LT	Lower tester
N	Newton
NAD	Node Address
NAK	Negative Acknowledgment
ns	Nanosecond or 10^{-9} s
P1	Parameter 1
P2	Parameter 2
P3	Parameter 3
PCB	Protocol Control Byte
PCO	Point of Control and Observation
pF	Picofarad or 10^{-12} F
R-APDU	Response APDU
R-block	Receive Ready Block
RH	Relative Humidity
RST	Reset
R-TPDU	Response TPDU
S-block	Supervisory Block
SI	International System of Units Standard
SUT	System Under Test

SW1	Status Word 1
SW2	Status Word 2
TCK	Check Character
t_F	Fall Time Between 90% and 10% of Signal Amplitude
TPDU	Transport Protocol Data Unit
t_R	Rise Time Between 10% and 90% of Signal Amplitude
TTL	Terminal Transport Layer
UT	Upper Tester
V	Volt
V_{CC}	Voltage Measured between VCC and GND Contacts
VCC	Supply Voltage
V_{IH}	High Level Input Voltage
V_{IL}	Low Level Input Voltage
V_{OH}	High Level Output Voltage
V_{OL}	Low Level Output Voltage
Vpp	Volts Peak to Peak
VPP	Programming Voltage
WI	Waiting Time Integer
WTX	Waiting Time Extension

All units in this document follow the International System of Units (SI) standard.

3.2 Definitions

In addition of terms already defined in the reference documentation, the following terms are used in this document:

Acceptance Testing	Set of procedures and tests to perform for the qualification of a Test Tool or Test Bench.
Protocol Tests	A defined set of test that checks the software responsible for the data exchange between ICC and IFM.
Sample	A physical implementation of an ICC or an IFM (design), delivered to the Testing Laboratory for the test.
Test Bench	A system designed to perform the Test Cases described in this document.
Test Case	A test to verify a defined subset of the requirements under specific test conditions.
Test Code	The code identifying a Test Case.
Testing Laboratory	A facility accredited by EMVCo for performing EMV Type Approval testing of IFMs.
Transaction	A sequence of logic interactions that the ICC and the Terminal shall execute as foreseen by the EMV application.
Trigger delay	Property of a digitizing circuit to not follow immediately the input signal changes that are shorter than the Trigger Delay, so that less switching is generated.

4 General requirements

4.1 Testing Strategy

4.1.1 Compliance Demonstration Objective

Within EMVCo Level 1 type approval process, EMVCo compliance demonstration objectives are:

1. To ensure implementation of the EMVCo Book 1 requirements (see [D01]);
2. To ensure that ICC and Terminal do not damage one another;
3. To ensure ICC / Terminal interoperability whatever the terminal customization performed by the vendor.

4.1.2 Device Under Test for Level 1 Approval.

The DUT is the Interface Module (IFM) as defined in the "Terminal Level 1 Type Approval - Administrative Process" document (See [D05]).

4.2 Test Tool Implementation Requirements

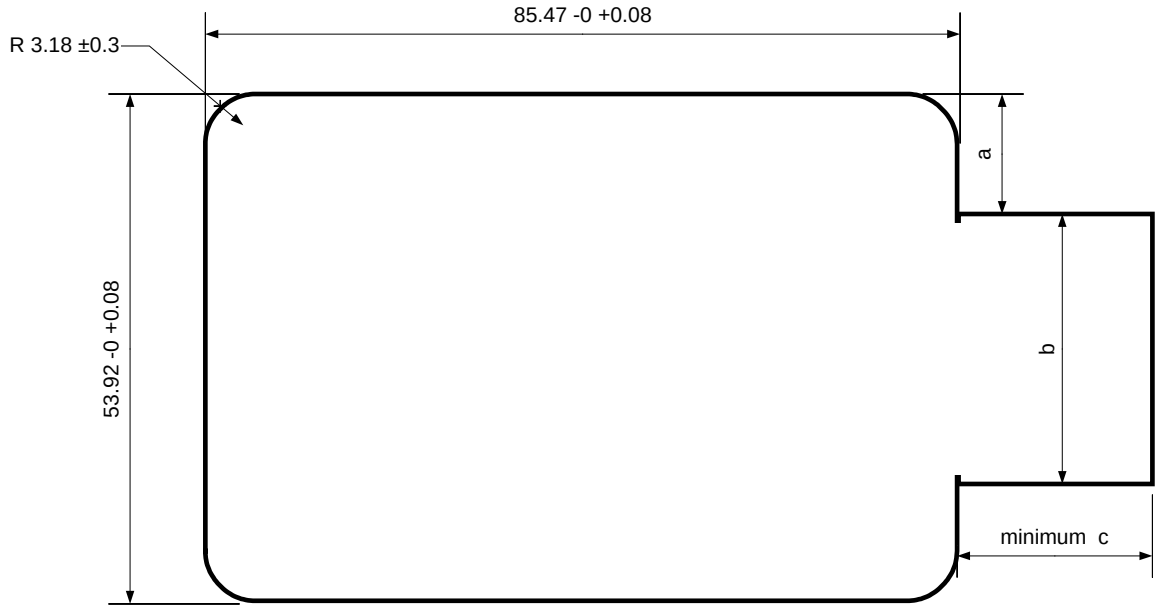
4.2.1 Physical compatibility requirements

The physical compatibility shall be verified by using probes that are dimensionally calibrated. The first probe has minimum dimensions and the second has maximum dimensions.

The «Minimum dimensions probe» shall have the following size :

- Length = 85.47 mm -0 +80 µm
- Width = 53.92 mm -0 +80 µm
- Thickness = 680 µm -0 +40 µm for the card surface
  680 µm -0 µm +60 µm for the contacting areas
  680 µm ± 100 µm for the probe connectors zone located outside of the ISO card surface
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm
- Specific dimensions (to be described in the Tool documentation) : a, b and c.

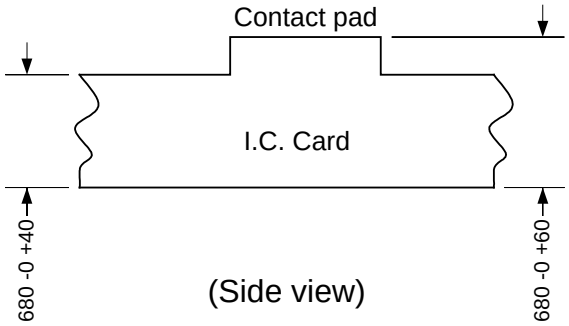
The layout (top view) of the minimum dimensions probe shall be as follows :



(Top view)
Dimensions in mm

Figure 1 – Top view of the minimum dimensions probe

The cross-section (side view) of the minimum dimensions probe shall be as follows :



(Side view)
Dimensions in µm

Figure 2 – Side view of the minimum dimensions probe

The «Maximum dimensions probe» shall have the following size :

- Length = 85.90 mm +0 -80 µm
- Width = 54.18 mm +0 -80 µm
- Thickness = 840 µm -40 +0 µm for the card surface
  840 µm -60 + 0 µm for the contacting areas
  1350 µm -80 +0 µm for the embossing areas (Card number area, name and address area)
  840 µm ± 100 µm for the probe connectors zone located outside of the ISO card surface
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm
- Specific dimensions (to be described in the Tool documentation) : a, b and c.

The layout (top view) of the maximum dimensions probe shall be as follows :

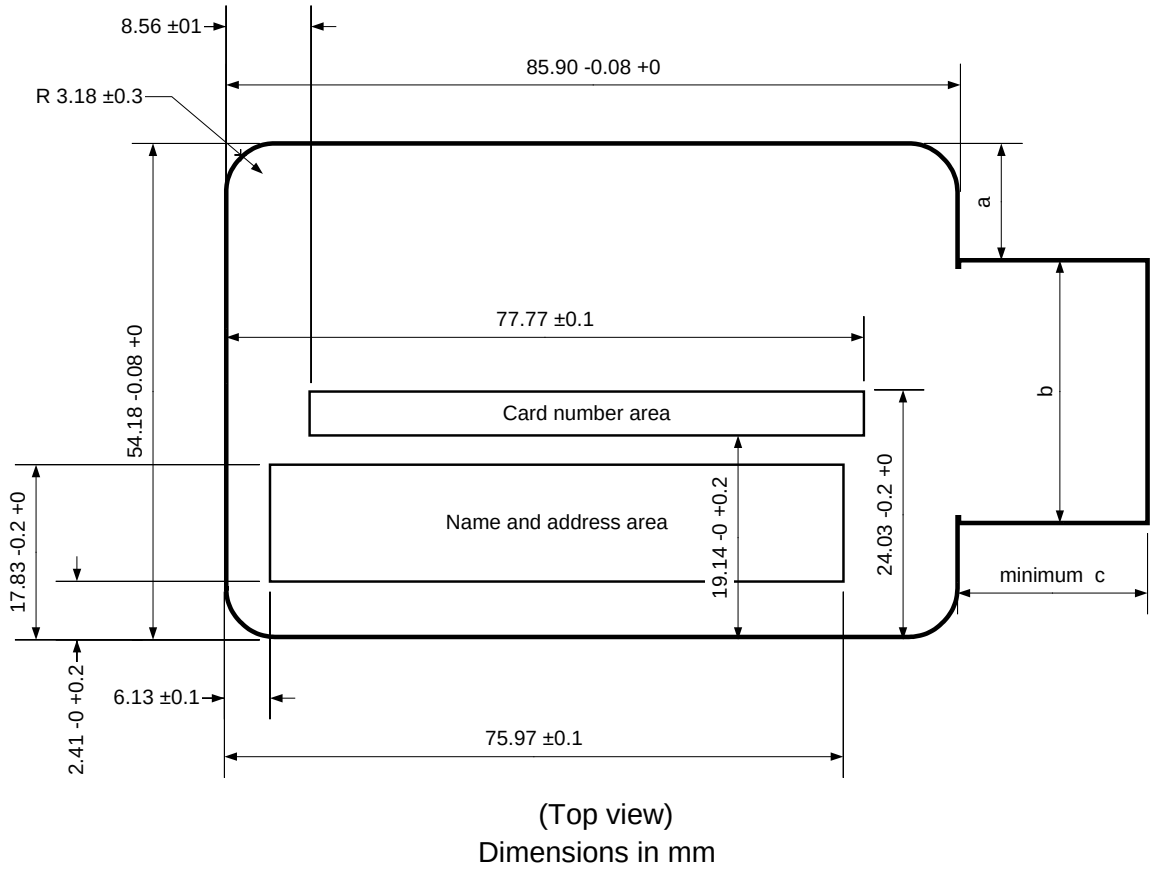


Figure 3 – Top view of the maximum dimensions probe

The cross-section (side view) of the maximum dimensions probe shall be as follows :

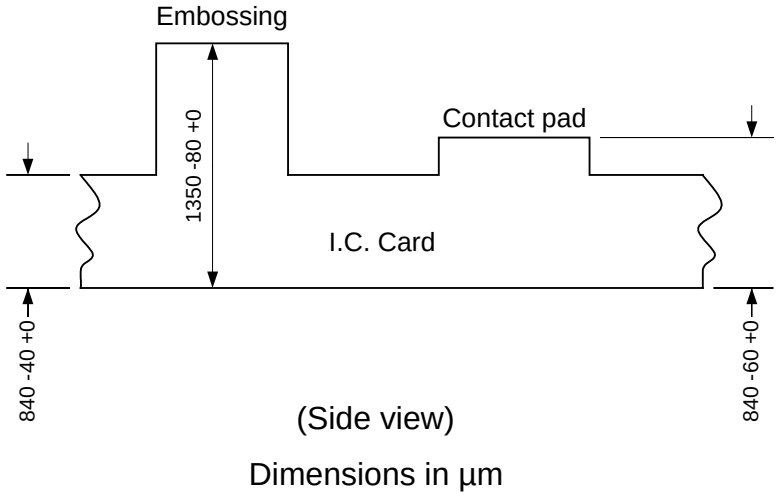


Figure 4 – Side view of the maximum dimensions probe

The contacts locations and dimensions for both probes shall be the minimum contact size that is allowed by ISO 7816-2. The test probes contact pads dimensional tolerance allowed is -0 +40 µm in length or width, measured from the center of the pad and based on the 'ISO minimal contacts' definition, as shown below :

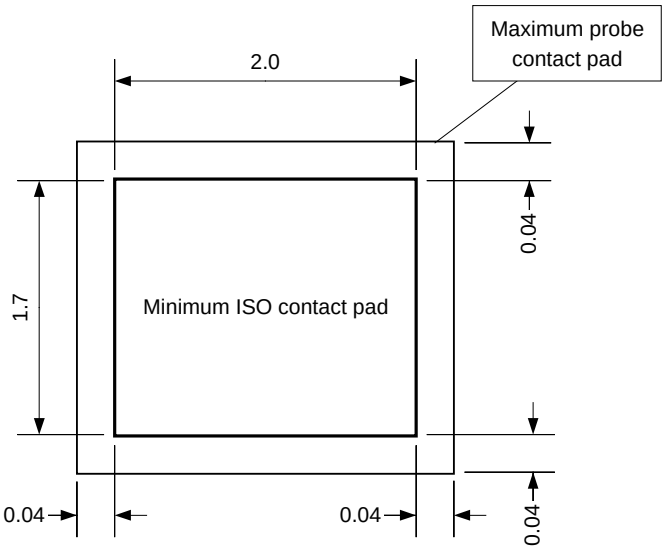


Figure 5 – Top view of a contact pad for both probes

4.2.2 Contact forces requirements

The contact forces shall be verified by using a probe that is calibrated for its dimensions as well as its capabilities to measure the forces that the DUT exerts on each individual contact.

The «Contact forces measurement probe» shall have the following size :

- Length = 85.72 mm ±40 µm
- Width = 54.03 mm ±40 µm
- Thickness = 760 µm -0 +40 µm
- Radius (card corners) = 3.18 mm ± 0.3 mm
- Radius (card thickness) ≤ 0.15 mm

The ISO minimum window must be located completely inside the measurement window.

The contact forces measurement probe shall be able to measure contact forces from 0.0 N to 1.0 N with a measurement uncertainty of ± 0.15 N for each contact. The influence of neighboring contact forces on any measurement shall be as minimized as possible.

During contact force measurements, the contact force measuring device surface shall not move along the force axis by more than +20 -80 µm from its nominal surface position when sustaining IFM contact forces ranging from 0.0 N to 0.8 N.

The probe used for the contact force measurement shall not apply more torque than a normal card.

4.2.3 Electrical signal generation requirements

The Test Bench shall be capable of generating the signals needed to conduct appropriately the Test Cases listed below. This means that the Test Bench shall be capable of driving the contacts listed below for the ranges specified, with the corresponding uncertainties (or better), as follows :

Contact	Parameter	Range or value	Uncertainty
CLK			
	I_{CLK}	-49 µA	± 1 µA
		-10 µA	± 1 µA
		+10 µA	± 1 µA
		+49 µA	± 1 µA
I/O			
	I_{IO}	-495 µA	± 2.5 µA
		-5 µA	± 1 µA
		+5 µA	± 1 µA
	Rise and fall times	≤ 100 ns	N/A
		1075 ns	± 125 ns
	V_{OL}	0.0 V DC	± 30 mV
		0.5 V DC	± 30 mV
	V_{OH}	$0.6 \times V_{CC}$	± 30 mV (1)
		V_{CC}	± 30 mV (2)
RST			
	I_{RST}	-49 µA	± 1 µA
		-10 µA	± 1 µA
		+10 µA	± 1 µA
		+49 µA	± 1 µA

(1) This uncertainty includes the related V_{CC} measurement uncertainty.

(2) This uncertainty includes the related V_{CC} measurement uncertainty.

Contact	Parameter	Range or value	Uncertainty
VCC			
	I_{CC}	≤ 0.2 mA	N/A
		1 mA	± 2% ± 0.1 mA
		2 mA	± 2% ± 0.1 mA
		25 mA	± 2% ± 0.1 mA
		54 mA	± 2% ± 0.1 mA
	I_{CC} spikes	See test case 1CB.018.0x, Table 22 and Table 23 for details	

Table 1 – Electrical signal generation requirements

All contacts except VCC shall present a capacitance less than or equal to 30 pF.

4.2.4 Electrical measurement requirements

The Test Bench shall be capable of measuring the signals needed to perform appropriately the Test Cases listed below. This means that the Test Bench shall be capable of measuring the parameters of the contacts listed below for the ranges specified, with the corresponding uncertainties (or better), as follows :

Contact	Parameter	Range	Uncertainty
CLK			
	Duty cycle	30% to 70%	± 1%
	Frequency	0.1 MHz to 6.0 MHz	± 1%
	Rise and fall times	0 ns to 1000 ns	± 5% ± 2ns
		1000 ns to 2000 ns	± 125 ns
	Voltage to GND	-1 V DC to 6 V DC	± 15 mV
	Voltage compared to V_{CC}	-1 V DC to 6 V DC	± 25 mV

Contact	Parameter	Range	Uncertainty
I/O			
	I_{IO}	-20 mA to + 20 mA	± 0.1 mA
	Rise and fall times	0 ns to 1000 ns	± 50 ns
		1000 ns to 2000 ns	± 125 ns
	Voltage to GND	-1 V DC to 6 V DC	± 15 mV
	Voltage compared to V_{CC}	-1 V DC to 6 V DC	± 25 mV
RST			
	Rise and fall times	0 ns to 1000 ns	± 50 ns
		1000 ns to 2000 ns	± 125 ns
	Voltage to GND	-1 V DC to 6 V DC	± 15 mV
	Voltage compared to V_{CC}	-1 V DC to 6 V DC	± 25 mV
VCC			
	Voltage to GND	-1 V DC to 6 V DC	± 15 mV
VPP			
	Resistance to GND	0.1 MΩ to 20 MΩ	± 5%
	Voltage to GND	-1 V DC to 6 V DC	± 15 mV

Table 2 – Electrical signal measurement requirements

All contacts shall be protected such as to withstand contact voltages ranging from -10 V DC to +25 V DC with a maximum input current of ± 20 mA without any damage for the Test Bench.

4.2.5 Environmental monitoring requirements

The Laboratory shall be capable of measuring the environmental conditions enforced around the IFM during the Test Cases, as listed below. This means that the Test Bench shall be capable of measuring the parameters listed below in the Laboratory room and / or the climatic chamber for the ranges specified, with the corresponding uncertainties (or better), as follows :

Parameter	Range	Uncertainty
Temperature	0°C to 50°C	± 1°C
Relative Humidity	5% RH to 95% RH	± 3% RH

Table 3 – Environmental monitoring requirements

4.3 Test Conditions

4.3.1 Default environmental conditions

Each Electrical and Card Session Type Approval test shall be performed under the following environmental conditions :

Condition	Temperature	Relative humidity
Low temperature	6°C ± 1°C	50% RH ± 10% RH
Normal temperature	23°C ± 3°C	50% RH ± 10% RH
High temperature	39°C ± 1°C	50% RH ± 10% RH

Table 4 – Type Approval Tests environmental conditions

4.3.2 ATR

Unless specified otherwise in the Test Cases below, the default T=0 ATR shall be used. For details on the ATR used, please refer to document [D06].

4.3.3 Loopback

The transactions needed to perform the Test Cases described below rely on a specific application called “Loopback”. For a description of this application, please refer to the document [D07].

4.3.4 Test Case Naming Convention

The Test Cases References are established as follows :

1Ct.nnn.cc

where

1C stands contact terminal level 1 test case
t is a letter indicating the category of test case
nnn is a the number of the test case
cc is the number of the test sub-case, or 00 if there is no sub-case

5 Mechanical Test Cases

5.1 1CA.001.0x - Physical compatibility and contact location

This test verifies that the physical characteristics of the DUT allow the acceptance of ICCs having a size between the standard minimum and the maximum dimensions, and that galvanic contact is established between the DUT and ICCs having minimal area contacts.

Test Code

1CA.001.0x

Reference

This test refers to requirements in [D01], section 5.4.1.

Test Conditions

Use Table 5 for the test conditions during verifications of the physical compatibility and contact location.

Value of x	Reference probe to be used
1	Minimum dimensions
2	Maximum dimensions

Table 5 – Test conditions for 1CA.001.0x

Procedure

Follow this procedure to verify the physical compatibility and contact location :

1. Stabilize the DUT at normal temperature.
2. Insert the reference probe listed in the first line of Table 5 into the DUT.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
5. Withdraw the reference probe from the DUT.
6. Using the reference probe listed in the second line of Table 5, repeat steps 3 to 5.

Acceptance criteria

The following acceptance criteria shall be met under all test conditions :

1. The reference probes may be inserted without mechanical interference into the DUT.
2. The contact activation sequence and the processing of the command sequence between the Test Bench and IUT are correctly performed.

3. The reference probes may be withdrawn from the DUT without mechanical interference.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

5.2 1CA.002.00 – IFM Contact Forces

This test verifies that the force exerted by any one DUT contact over its corresponding ICC contact is within specifications.

Test Code

1CA.002.00

Reference

This test refers to requirements in [D01], section 5.4.2.

Test Conditions

The DUT is not supplied any power.

Procedure

Follow this procedure to verify the IFM contact forces :

1. Stabilize the DUT at normal temperature.
2. Insert the contact force measuring probe into the DUT, up to its nominal seated position. Position the probe so as to avoid any perturbations during the measurement.
3. Measure the force on each existing contact pad at least three times with at least one second between measurements.
4. Withdraw the contact forces measuring probe from the DUT.

Acceptance criteria

The following acceptance criteria shall be met for each contact :

1. $(0.2\ N - \varepsilon N) \leq \text{contact force} \leq (0.6\ N + \varepsilon N)$

The “contact force” mentioned in the Acceptance Criteria 1 above is the average of the three measurements performed on the concerned contact.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6 Electrical Test Cases

6.1 Foreword

This section describes the general conditions for all electrical and card session test cases. The indications below are applicable to all the test cases, unless otherwise is stated in the description of a specific test case.

The monitoring of the signals shall start the first time that V_{CC} reaches its lowest stable limit, i.e. (4.6 V DC - εV) for Class A or (2.76 V - εV) for Class B, and end when VCC is deactivated.

Regarding signal voltages, a differentiated approach has been selected :

- The "Signal voltage" series of test cases focus on the general DC shape of the signals. Shortest spikes, i.e. those lasting less than the "Trigger delay" value, are ignored. For these test cases :
  - All acceptance limits are set according to the requirements applicable to the IFM.
  - Appropriate trigger delays are applied. Spikes shorter than the concerned trigger delay are ignored.
  - To accommodate for the unavoidable internal resistance of the transmission lines, the outer voltage limits, i.e. the lower V_{IL} limit and the upper V_{IH} limit, are shifted by 50mV from their nominal specified value.
- The "Signal perturbations" series of test cases focus on the high-frequency components of the signal, and on ensuring that the signals are appropriate for interpretation by the ICC. For these test cases :
  - No trigger delay is applied. A spike that is outside limits results in a failed test case, whatever its duration.
  - The outer limits, i.e. the lower V_{IL} limit and the upper V_{IH} limit, are verified against the "Signal perturbations" IFM specifications.
  - The inner limits, i.e. the lower V_{IH} limit and the upper V_{IL} limit, are verified against the ICC receiver specifications.
  - The correct signals transitions, i.e. from low to high state and vice-versa, are verified.

The I_{CC} current specified in each test condition shall be driven by the Test Tool from the moment when VCC is powered up and stable until its deactivation.

6.2 1CB.001.0x - Short circuit resilience

This test verifies that the DUT is not damaged by a short circuit between any pair or group of contacts.

Test Code

1CB.001.0x

Reference

This test refers to requirements in [D01], section 5.5.8.

Test Conditions

Use Table 6 for the test conditions during verifications of the short circuit resilience.

Value of x	Probe description	I_{CC} (3)
1	Shorts I/O, CLK and RST to GND with ≤ 2Ω each	2 mA ± 2% ± 0.1 mA
2	Shorts I/O, CLK and RST to VCC with ≤ 2Ω each	2 mA ± 2% ± 0.1 mA
3	Shorts VCC to GND with ≤ 2Ω	54 mA ± 2% ± 0.1 mA
4	Fully metallic probe with ≤ 2Ω between any pair of contacts, or between any contact and any point of the surface of the probe.	54 mA ± 2% ± 0.1 mA

Table 6 – Test conditions for 1CB.001.0x

Procedure

Follow this procedure to verify the short circuit resilience :

1. Stabilize the DUT at normal temperature.
2. Insert the reference probe listed in the first line of Table 6 into the DUT.
3. Keep the probe inserted for at least 10 seconds.
4. Withdraw the reference probe.
5. If required by the DUT operating instructions, perform a reset of the DUT.
6. Insert the normal measurement probe and initiate cold reset.
7. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
8. During step 7, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND) when the DUT is transmitting, the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
9. Use the reference probe listed in the next line of Table 6 and repeat steps 2 to 8. Repeat this step until the end of the table.

(3) This current applies to the transaction performed after each short (steps 6, 7 and 8), not during the shorts (steps 2 and 3).

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all test conditions :

1. Each sequence of commands and answers in step 7 of the procedure above is performed correctly.
2. (-0.25 V - εV) ≤ Low state I/O voltage ≤ ((0.15 × V_{CC}) + εVV)
3. ((0.8 × V_{CC}) - εVV) ≤ High state I/O voltage ≤ (V_{CC} + 0.25 V + εVV)
4. (-0.25 V - εV) ≤ Low state CLK voltage ≤ ((0.15 × V_{CC}) + εVV)
5. ((0.8 × V_{CC}) - εVV) ≤ High state CLK voltage ≤ (V_{CC} + 0.25 V + εVV)
6. (-0.25 V - εV) ≤ Low state RST voltage ≤ ((0.15 × V_{CC}) + εVV)
7. ((0.8 × V_{CC}) - εVV) ≤ High state RST voltage ≤ (V_{CC} + 0.25 V + εVV)
8. (-0.25 V - εV) ≤ Vcc voltage (at any time)
9. For Class A :
    a. (-0.25 V - εV) ≤ Vcc voltage ≤ (5.40 V + εV)
    b. When CLK is active : (4.60 V - εV) ≤ Vcc voltage
10. For Class B :
    a. (-0.25 V - εV) ≤ Vcc voltage ≤ (3.24 V + εV)
    b. When CLK is active : (2.76 V - εV) ≤ Vcc voltage

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.3 1CB.002.00 - VPP isolation

This test verifies the isolation of the VPP contact for new IFM designs.

This test case is applicable to all Class B DUTs and to Class A DUTs when their ICS mentions that the VPP contact (C6) is not connected. For other Class A DUTs, please perform the test case 1CB.003.0x instead.

Test Code

1CB.002.0x

Reference

This test refers to requirements in [D01], section 5.5.3.

Test Conditions

No specific test conditions are applicable to this test case.

Procedure

Follow this procedure to verify the isolation of the VPP contact for new IFM designs :

1. Stabilize the DUT at normal temperature.
2. Initiate cold reset.
3. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
4. During step 3, measure the DC resistance between contacts C6 (VPP) and C5 (GND). The test voltage used shall not exceed 5 V DC between these contacts.

Acceptance criteria

The following acceptance criteria shall be met :

1. VPP isolation $\geq$ (10 MΩ - εΩ)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.4 1CB.003.0x - VPP voltage

This test verifies the voltage on the VPP contact for existing Class A IFM designs.

This test case is applicable only to existing Class A DUTs, when their ICS mentions that the VPP contact (C6) is connected. For all other DUTs, please perform the test case 1CB.002.00 instead.

Test Code

1CB.003.0x

Reference

This test refers to requirements in [D01], section 5.5.3.

Test Conditions

Use Table 7 for the test conditions during verifications of the voltage on the VPP contact for existing Class A IFM designs.

Value of x	I_{CC}
1	≤ 0.2 mA
2	2 mA ± 2% ± 0.1 mA
3	54 mA ± 2% ± 0.1 mA

Table 7 – Test conditions for 1CB.003.0x

Procedure

Follow this procedure to verify the voltage on the VPP contact for existing Class A IFM designs :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 7.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During steps 3 and 4, monitor the VPP voltage between contacts C6 (VPP) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 7 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-0.25\ V - \varepsilon V) \leq$ VPP voltage $\leq ((1.05 \times V_{CC}) + 0.25\ V\ DC + \varepsilon VV)$

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.5 1CB.004.0x - I/O current

This test verifies the current limitation on the I/O contact.

Test Code

1CB.004.0x

Reference

This test refers to requirements in [D01], section 5.5.2.

Test Conditions

Use Table 8 for the test conditions during verifications of the current limitation on the I/O contact.

Value of x	I_{CC}	Shorting
1	2 mA ± 2% ± 0.1 mA	≤ 75Ω from I/O to VCC
2	54 mA ± 2% ± 0.1 mA	≤ 75Ω from I/O to VCC
3	2 mA ± 2% ± 0.1 mA	≤ 75Ω from I/O to GND
4	54 mA ± 2% ± 0.1 mA	≤ 75Ω from I/O to GND

Table 8 – Test conditions for 1CB.004.0x

Procedure

Follow this procedure to verify the current limitation on the I/O contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the "I_{CC}" column of the first line of Table 8.
3. Initiate cold reset.
4. Send the default T=0 ATR without any short circuit.
5. When the DUT sends data to the LT, apply the short circuit specified in the "Shorting" column of the concerned line of Table 8 until the short collapses I/O and cause contact deactivation, or after one second.
6. During step 5, monitor the I/O current on contact C7 (I/O) starting 100 ns after the application of the short circuit.
7. Set the test conditions as listed in the next line of Table 8 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. (-15 mA - εA) ≤ I/O current ≤ (15 mA + εA)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.6 1CB.005.0x - I/O transmission voltage

This test verifies the voltage trends on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

Test Code

1CB.005.0x

Reference

This test refers to requirements in [D01], section 5.5.2.1, Table 10.

Test Conditions

Use Table 9 for the test conditions during verifications of the voltage trends on the I/O contact during transmission.

Value of x	I_{CC}	I_{IO}	Trigger delay
1	2 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA	320 ns
2	54 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA	320 ns

Table 9 – Test conditions for 1CB.005.0x

Procedure

Follow this procedure to verify the voltage trends on the I/O contact during transmission :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 9.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O voltage between contacts C7 (I/O) and C5 (GND) when the DUT is transmitting.
6. Set the test conditions as listed in the next line of Table 9 and repeat steps 3 to 5.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-\ 50\ mV - \varepsilon V) \leq$ Low state I/O voltage $\leq ((0.15 \times V_{CC}) + \varepsilon VV)$
2. $((0.8 \times V_{CC}) - \varepsilon VV) \leq$ High state I/O voltage $\leq (V_{CC} + 50\ mV + \varepsilon VV)$

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.7 1CB.006.0x - I/O transmission rise and fall time

This test verifies the rise and fall times on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

Test Code

1CB.006.0x

Reference

This test refers to requirements in [D01], section 5.5.2.1, Table 10.

Test Conditions

Use Table 10 for the test conditions during verifications of the rise and fall times on the I/O contact.

Value of x	I_{CC}	I_{IO}
1	2 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -5 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -5 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA
4	54 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA

Table 10 – Test conditions for 1CB.006.0x

Procedure

Follow this procedure to verify the rise and fall times on the I/O contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 10.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O rise time (10% to 90% of ($0.2 \times V_{CC}$) to ($0.7 \times V_{CC}$)) and the I/O fall time (90% to 10% of ($0.7 \times V_{CC}$) to ($0.2 \times V_{CC}$)) between contacts C7 (I/O) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 10 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. I/O rise time ≤ (800 ns + εs)
2. I/O fall time ≤ (800 ns + εs)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.8 1CB.007.0x - I/O transmission signal perturbations

This test verifies the voltage perturbations on the I/O contact when the DUT is transmitting, i.e. when the DUT is controlling the level on the I/O contact.

Test Code

1CB.007.0x

Reference

This test refers to requirements in [D01], section 5.5.2.1, Table 10.

Test Conditions

Use Table 11 for the test conditions during verifications of the voltage perturbations on the I/O contact during transmission.

Value of x	I_{CC}	I_{IO}
1	2 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -5 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -5 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA
4	54 mA ± 2% ± 0.1 mA	+5 µA ± 1 µA -495 µA ± 2.5 µA

Table 11 – Test conditions for 1CB.007.0x

Procedure

Follow this procedure to verify the voltage perturbations on the I/O contact during transmission :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 11.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the I/O voltage between contacts C7 (I/O) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 11 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-0.25\ V - \varepsilon V) \leq$ I/O voltage $\leq (V_{CC} + 0.25\ V + \varepsilon VV)$
2. Each time that the I/O voltage increases over $((0.2 \times V_{CC}) + \varepsilon VV)$, it reaches next $((0.7 \times V_{CC}) - \varepsilon VV)$ or above before decreasing again under $((0.2 \times V_{CC}) + \varepsilon VV)$. To avoid inappropriate detection of failures in open-drain IFM implementations, the two first clock cycles after each state transition shall be ignored.
3. Each time that the I/O voltage decreases under $((0.7 \times V_{CC}) - \varepsilon VV)$, it reaches next $((0.2 \times V_{CC}) + \varepsilon VV)$ or below before increasing again over $((0.7 \times V_{CC}) - \varepsilon VV)$.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.9 1CB.008.0x - I/O reception voltage

This test verifies that the DUT is able to correctly interpret the signal from an ICC that generates I/O voltages which are on the boundaries of the acceptable voltage specifications.

Test Code

1CB.008.0x

Reference

This test refers to requirements in [D01], section 5.5.2.2, Table 11.

Test Conditions

Use Table 12 for the test conditions during verifications of the signal voltage interpretation on the I/O contact during reception.

Value of x	I_{CC}	I/O V_{OL}	I/O V_{OH}
1	2 mA ± 2% ± 0.1 mA	0.0 V DC ± 30 mV	V_{CC} ± 30 mV
2	54 mA ± 2% ± 0.1 mA	0.0 V DC ± 30 mV	V_{CC} ± 30 mV
3	2 mA ± 2% ± 0.1 mA	[(0.2 × V_{CC}) - 30 mV] ± 30 mV	[(0.6 × V_{CC}) + 30 mV] ± 30 mV
4	54 mA ± 2% ± 0.1 mA	[(0.2 × V_{CC}) - 30 mV] ± 30 mV	[(0.6 × V_{CC}) + 30 mV] ± 30 mV

Table 12 – Test conditions for 1CB.008.0x

When generated by the Test Bench, the rise and fall times of the I/O signal shall be less than or equal to 100 ns of the concerned V_{OL} to V_{OH} range.

Procedure

Follow this procedure to verify the signal voltage interpretation on the I/O contact during reception :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 12.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Set the test conditions as listed in the next line of Table 12 and repeat steps 3 and 4. Repeat this step until the end of the table.
6. Repeat steps 1 to 5 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. Each sequence of commands and answers is performed correctly.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.10 1CB.009.0x - I/O reception rise and fall times

This test verifies that the DUT is able to correctly interpret the signal from an ICC that generates rise and fall times which are on the boundaries of the acceptable timing specifications.

Test Code

1CB.009.0x

Reference

This test refers to requirements in [D01], section 5.5.2.2, Table 11.

Test Conditions

Use Table 13 for the test conditions during verifications of the signal rise and fall times interpretation on the I/O contact during reception.

Value of x	I_{CC}	I/O t_R and t_F
1	2 mA ± 2% ± 0.1 mA	≤ 100 ns
2	54 mA ± 2% ± 0.1 mA	≤ 100 ns
3	2 mA ± 2% ± 0.1 mA	1075 ns ± 125 ns
4	54 mA ± 2% ± 0.1 mA	1075 ns ± 125 ns

Table 13 – Test conditions for 1CB.009.0x

When generated by the Test Bench, the voltages of the I/O signal shall be as follows :

- I/O V_{OL} = 0.0 V DC ± 30 mV
- I/O V_{OH} = V_{CC} ± 30 mV if controlled by the Test Tool, else floating
- The rise time is 10% to 90% of 0.0 V DC to V_{CC}
- The fall time is 90% to 10% of V_{CC} to 0.0 V DC

Procedure

Follow this procedure to verify the signal rise and fall times interpretation on the I/O contact during reception :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 13.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Set the test conditions as listed in the next line of Table 13 and repeat steps 3 and 4. Repeat this step until the end of the table.
6. Repeat steps 1 to 5 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. Each sequence of commands and answers is performed correctly.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.11 1CB.010.0x - CLK voltage

This test verifies the voltage trends on the CLK contact.

Test Code

1CB.010.0x

Reference

This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions

Use Table 14 for the test conditions during verifications of the voltage trends on the CLK contact.

Value of x	I_{CC}	I_{CLK}	Trigger delay
1	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA	60 ns
2	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA	60 ns

Table 14 – Test conditions for 1CB.010.0x

Procedure

Follow this procedure to verify the voltage trends on the CLK contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 14.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK voltage between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 14 and repeat steps 3 to 5.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-\ 50\ mV - \varepsilon V) \leq$ Low state CLK voltage $\leq ((0.15 \times V_{CC}) + \varepsilon VV)$
2. $((0.8 \times V_{CC}) - \varepsilon VV) \leq$ High state CLK voltage $\leq (V_{CC} + 50\ mV + \varepsilon VV)$

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.12 1CB.011.0x - CLK rise and fall times

This test verifies the rise and fall times on the CLK contact.

Test Code

1CB.011.0x

Reference

This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions

Use Table 15 for the test conditions during verifications of the rise and fall times on the CLK contact.

Value of x	I_{CC}	I_{CLK}
1	2 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA
4	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA

Table 15 – Test conditions for 1CB.011.0x

Procedure

Follow this procedure to verify the rise and fall times on the CLK contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 15.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK rise time (10% to 90% of ($0.2 \times V_{CC}$) to ($0.7 \times V_{CC}$)) and the CLK fall time (90% to 10% of ($0.7 \times V_{CC}$) to ($0.2 \times V_{CC}$)) between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 15 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. CLK rise time ≤ (8% of clock period + εs)
2. CLK fall time ≤ (8% of clock period + εs)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.13 1CB.012.0x - CLK signal perturbations

This test verifies the voltage perturbations on the CLK contact.

Test Code

1CB.012.0x

Reference

This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions

Use Table 16 for the test conditions during verifications of the voltage perturbations on the CLK contact.

Value of x	I_{CC}	I_{CLK}
1	2 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA
4	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA

Table 16 – Test conditions for 1CB.012.0x

Procedure

Follow this procedure to verify the voltage perturbations on the CLK contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 16.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK voltage between contacts C3 (CLK) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 16 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-0.25\ V - \varepsilon V) \leq$ CLK voltage $\leq (V_{CC} + 0.25\ V + \varepsilon VV)$
2. Each time that the CLK voltage increases over $((0.2 \times V_{CC}) + \varepsilon VV)$, it reaches next $((0.7 \times V_{CC}) - \varepsilon VV)$ or above before decreasing again under $((0.2 \times V_{CC}) + \varepsilon VV)$.
3. Each time that the CLK voltage decreases under $((0.7 \times V_{CC}) - \varepsilon VV)$, it reaches next $((0.2 \times V_{CC}) + \varepsilon VV)$ or below before increasing again over $((0.7 \times V_{CC}) - \varepsilon VV)$.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.14 1CB.013.0x - CLK frequency and duty cycle

This test verifies the frequency and duty cycle on the CLK contact.

Test Code

1CB.013.0x

Reference

This test refers to requirements in [D01], section 5.5.4, Table 12.

Test Conditions

Use Table 17 for the test conditions during verifications of the voltage perturbations on the CLK contact.

Value of x	I_{CC}	I_{CLK}
1	2 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA
4	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA

Table 17 – Test conditions for 1CB.013.0x

Procedure

Follow this procedure to verify the voltage trends on the CLK contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 17.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the CLK frequency and duty cycle between contacts C3 (CLK) and C5 (GND) when RST is at high state. Retain the minimum, maximum and average frequencies.

   If the measurement system is limited to observations shorter than the whole transaction, the measurements shall be done at least 10 times, during at least 50 ms each and at intervals of at least 50 ms, when RST is at high state during the transaction. For each interval, the average CLK frequency for this interval (f_i) shall be computed. At the end of the test, the CLK average frequency shall be computed as the mathematical average of the results for all intervals :

   $$CLK\ average\ frequency = \frac{1}{n} \times \sum_{i=1}^{n} f_i$$

6. Set the test conditions as listed in the next line of Table 17 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met at any time when RST is at high state during the whole monitoring duration and under all environmental and test conditions :

1. (1 MHz – εHz) ≤ CLK frequency ≤ (5 MHz + εHz)
2. [Max(f_i) - εHz] ≤ (101% of CLK average frequency)
3. [Min(f_i) + εHz] ≥ (99% of CLK average frequency)
4. (45% - ε%) ≤ CLK duty cycle ≤ (55% + ε%)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.15 1CB.014.0x - RST voltage

This test verifies the voltage trends on the RST contact.

Test Code

1CB.014.0x

Reference

This test refers to requirements in [D01], section 5.5.5, Table 13.

Test Conditions

Use Table 18 for the test conditions during verifications of the voltage trends on the RST contact.

Value of x	I_{CC}	I_{RST}	Trigger delay
1	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA	320 ns
2	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA	320 ns

Table 18 – Test conditions for 1CB.014.0x

Procedure

Follow this procedure to verify the voltage trends on the RST contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 18.
3. Initiate cold reset.
4. Wait for V_{CC} to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for V_{CC} to be deactivated.
7. During steps 4 to 6, monitor the RST voltage between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 18 and repeat steps 3 to 7.
9. Repeat steps 1 to 8 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-\ 50\ mV - \varepsilon V) \leq$ Low state RST voltage $\leq ((0.15 \times V_{CC}) + \varepsilon VV)$
2. $((0.8 \times V_{CC}) - \varepsilon VV) \leq$ High state RST voltage $\leq (V_{CC} + 50\ mV + \varepsilon VV)$

To be recognized as a failed test, a non-compliance situation shall last at least for the trigger delay duration.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.16 1CB.015.0x - RST rise and fall times

This test verifies the rise and fall times on the RST contact.

Test Code

1CB.015.0x

Reference

This test refers to requirements in [D01], section 5.5.5, Table 13.

Test Conditions

Use Table 19 for the test conditions during verifications of the rise and fall times on the RST contact.

Value of x	I_{CC}	I_{RST}
1	2 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA
4	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA

Table 19 – Test conditions for 1CB.015.0x

Procedure

Follow this procedure to verify the rise and fall times on the RST contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 19.
3. Initiate cold reset.
4. Wait for V_{CC} to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for V_{CC} to be deactivated.
7. During steps 4 to 6, monitor the RST rise time (10% to 90% of ($0.2 \times V_{CC}$) to ($0.7 \times V_{CC}$)) and the RST fall time (90% to 10% of ($0.7 \times V_{CC}$) to ($0.2 \times V_{CC}$)) between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 19 and repeat steps 3 to 7. Repeat this step until the end of the table.
9. Repeat steps 1 to 8 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. RST rise time ≤ (800 ns + εs)
2. RST fall time ≤ (800 ns + εs)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.17 1CB.016.0x - RST signal perturbations

This test verifies the voltage perturbations on the RST contact.

Test Code

1CB.016.0x

Reference

This test refers to requirements in [D01], section 5.5.5, Table 13.

Test Conditions

Use Table 20 for the test conditions during verifications of the voltage perturbations on the RST contact.

Value of x	I_{CC}	I_{RST}
1	2 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
2	54 mA ± 2% ± 0.1 mA	+10 µA ± 1 µA -10 µA ± 1 µA
3	2 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA
4	54 mA ± 2% ± 0.1 mA	+49 µA ± 1 µA -49 µA ± 1 µA

Table 20 – Test conditions for 1CB.016.0x

Procedure

Follow this procedure to verify the voltage perturbations on the RST contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 20.
3. Initiate cold reset.
4. Wait for V_{CC} to be activated.
5. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
6. Wait for V_{CC} to be deactivated.
7. During steps 4 to 6, monitor the RST voltage between contacts C2 (RST) and C5 (GND).
8. Set the test conditions as listed in the next line of Table 20 and repeat steps 3 to 7. Repeat this step until the end of the table.
9. Repeat steps 1 to 8 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. $(-0.25\ V - \varepsilon V) \leq$ RST voltage $\leq (V_{CC} + 0.25\ V + \varepsilon VV)$
2. Each time that the RST voltage increases over $((0.2 \times V_{CC}) + \varepsilon VV)$, it reaches next $((0.7 \times V_{CC}) - \varepsilon VV)$ or above before decreasing again under $((0.2 \times V_{CC}) + \varepsilon VV)$.
3. Each time that the RST voltage decreases under $((0.7 \times V_{CC}) - \varepsilon VV)$, it reaches next $((0.2 \times V_{CC}) + \varepsilon VV)$ or below before increasing again over $((0.7 \times V_{CC}) - \varepsilon VV)$.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.18 1CB.017.xx - V_{CC} voltage

This test verifies the voltage on the VCC contact.

Test Code

1CB.017.0x

Reference

This test refers to requirements in [D01], section 5.5.6, Table 14.

Test Conditions

Use Table 21 for the test conditions during verifications of the voltage on the VCC contact.

Value of xx	DUT input power supply	I_{CC}
01	Nominal (as per ICS)	≤ 0.2 mA
02	Nominal (as per ICS)	1 mA ± 2% ± 0.1 mA
03	Nominal (as per ICS)	25 mA ± 2% ± 0.1 mA
04	Nominal (as per ICS)	54 mA ± 2% ± 0.1 mA
05	Minimum (as per ICS)	≤ 0.2 mA
06	Minimum (as per ICS)	1 mA ± 2% ± 0.1 mA
07	Minimum (as per ICS)	25 mA ± 2% ± 0.1 mA
08	Minimum (as per ICS)	54 mA ± 2% ± 0.1 mA
09	Maximum (as per ICS)	≤ 0.2 mA
10	Maximum (as per ICS)	1 mA ± 2% ± 0.1 mA
11	Maximum (as per ICS)	25 mA ± 2% ± 0.1 mA
12	Maximum (as per ICS)	54 mA ± 2% ± 0.1 mA

Table 21 – Test conditions for 1CB.017.0x

Procedure

Follow this procedure to verify the voltage on the VCC contact :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 21.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.

5. During step 4, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 21 and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. For Class A :
    a. $(-0.25\ V - \varepsilon V) \leq$ Vcc voltage $\leq (5.40\ V + \varepsilon V)$
    b. When CLK is active : $(4.60\ V - \varepsilon V) \leq$ Vcc voltage
2. For Class B :
    a. $(-0.25\ V - \varepsilon V) \leq$ Vcc voltage $\leq (3.24\ V + \varepsilon V)$
    b. When CLK is active : $(2.76\ V - \varepsilon V) \leq$ Vcc voltage

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

6.19 1CB.018.xx - Transients neutralization on VCC

This test verifies the voltage on the VCC contact under dynamic load conditions.

Test Code

1CB.018.0x

Reference

This test refers to requirements in [D01], section 5.5.6, Table 14.

Test Conditions

Use Table 22 for the test conditions during verifications of the voltage on the VCC contact of a Class A DUT under dynamic load. All currents shall be generated with a maximum (± 2% ± 0.1 mA) uncertainty.

Value of xx	DUT input power supply (as per ICS)	Rest I_{CC}	Spike I_{CC}	Spike type
01	Nominal	≤ 0.2 mA	95 mA	Fixed
02	Nominal	≤ 0.2 mA	95 mA	Random
03	Nominal	1 mA	95 mA	Fixed
04	Nominal	1 mA	95 mA	Random
05	Nominal	25 mA	55 mA	Fixed
06	Nominal	25 mA	95 mA	Random
07	Nominal	40 mA	25 mA	Fixed
08	Nominal	54 mA	95 mA	Random
09	Minimum	≤ 0.2 mA	95 mA	Fixed
10	Minimum	≤ 0.2 mA	95 mA	Random
11	Minimum	1 mA	95 mA	Fixed
12	Minimum	1 mA	95 mA	Random
13	Minimum	25 mA	55 mA	Fixed
14	Minimum	25 mA	95 mA	Random
15	Minimum	40 mA	25 mA	Fixed

Value of xx	DUT input power supply (as per ICS)	Rest I_{CC}	Spike I_{CC}	Spike type
16	Minimum	54 mA	95 mA	Random
17	Maximum	≤ 0.2 mA	95 mA	Fixed
18	Maximum	≤ 0.2 mA	95 mA	Random
19	Maximum	1 mA	95 mA	Fixed
20	Maximum	1 mA	95 mA	Random
21	Maximum	25 mA	55 mA	Fixed
22	Maximum	25 mA	95 mA	Random
23	Maximum	40 mA	25 mA	Fixed
24	Maximum	54 mA	95 mA	Random

Table 22 – Class A test conditions for 1CB.018.0x

Use Table 23 for the test conditions during verifications of the voltage on the VCC contact of a Class B DUT under dynamic load. All currents shall be generated with a maximum (± 2% ± 0.1 mA) uncertainty.

Value of xx	DUT input power supply (as per ICS)	Rest I_{CC}	Spike I_{CC}	Spike type
01	Nominal	≤ 0.2 mA	45 mA	Fixed
02	Nominal	≤ 0.2 mA	45 mA	Random
03	Nominal	1 mA	45 mA	Fixed
04	Nominal	1 mA	45 mA	Random
05	Nominal	25 mA	45 mA	Fixed
06	Nominal	25 mA	45 mA	Random
07	Nominal	40 mA	25 mA	Fixed
08	Nominal	54 mA	45 mA	Random
09	Minimum	≤ 0.2 mA	45 mA	Fixed
10	Minimum	≤ 0.2 mA	45 mA	Random

Value of xx	DUT input power supply (as per ICS)	Rest I_{CC}	Spike I_{CC}	Spike type
11	Minimum	1 mA	45 mA	Fixed
12	Minimum	1 mA	45 mA	Random
13	Minimum	25 mA	45 mA	Fixed
14	Minimum	25 mA	45 mA	Random
15	Minimum	40 mA	25 mA	Fixed
16	Minimum	54 mA	45 mA	Random
17	Maximum	≤ 0.2 mA	45 mA	Fixed
18	Maximum	≤ 0.2 mA	45 mA	Random
19	Maximum	1 mA	45 mA	Fixed
20	Maximum	1 mA	45 mA	Random
21	Maximum	25 mA	45 mA	Fixed
22	Maximum	25 mA	45 mA	Random
23	Maximum	40 mA	25 mA	Fixed
24	Maximum	54 mA	45 mA	Random

Table 23 – Class B test conditions for 1CB.018.0x

In Table 22 and Table 23, the "Spike type" specifies the characteristics that the I_{CC} current shall have :

- "Fixed" spike type means that the I_{CC} current shall present a near-square waveform, having a frequency of 5 MHz ± 0.1 MHz, a duty cycle of 50% ± 10% and a slew rate of 1.0 mA/ns ± 20%.
- "Random" spike type means that the I_{CC} current shall present pulses with a fixed duration of 300 ns ± 30 ns for Class A and 350 ns ± 35 ns for Class B, measured at the half of the spike amplitude, then a random pause lasting between 0.1 ms and 500 ms ± 1%, and a slew rate of 1.0 mA/ns ± 20%.

In accordance with ISO 7816-3 and EMVCo Book 1 [D01], the "Spike I_{CC}" value is the additional current flowing in the VCC contact during the spike time (i.e. on top of the rest current), while the "Rest I_{CC}" value is the current flowing in the VCC contact in the absence of a current spike.

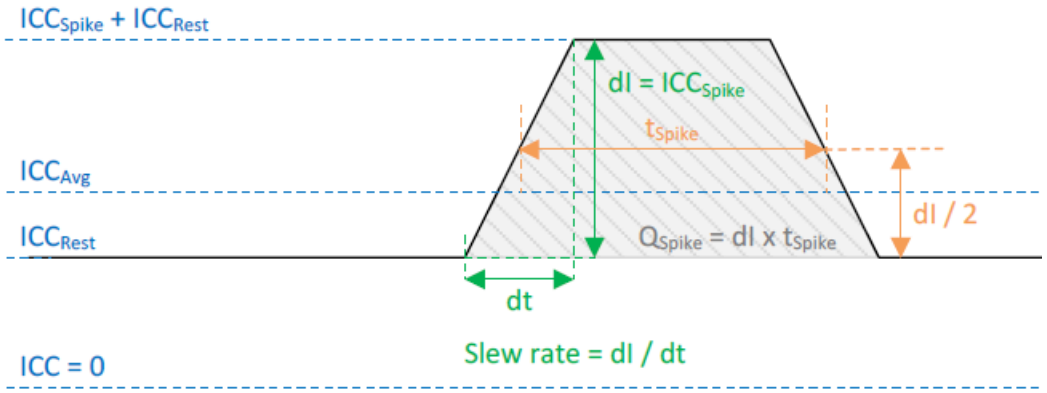


Figure 6 – Definition of ICC spikes

Procedure

Follow this procedure to verify the voltage on the VCC contact under dynamic load conditions :

1. Stabilize the DUT at the appropriate environmental conditions.
2. For a Class A DUT, set the test conditions as listed in the first line of Table 22. For a Class B DUT, set the test conditions as listed in the first line of Table 23.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. During step 4, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND).
6. Set the test conditions as listed in the next line of Table 22 (for a Class A DUT) or Table 23 (for a Class B DUT) and repeat steps 3 to 5. Repeat this step until the end of the table.
7. Repeat steps 1 to 6 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met during the whole monitoring duration and under all environmental and test conditions :

1. For Class A :
   a. (-0.25 V - εV) ≤ Vcc voltage ≤ (5.40 V + εV)
   b. When CLK is active : (4.60 V - εV) ≤ Vcc voltage
2. For Class B :
   a. (-0.25 V - εV) ≤ Vcc voltage ≤ (3.24 V + εV)
   b. When CLK is active : (2.76 V - εV) ≤ Vcc voltage

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

7 Card Session Test Cases

7.1 1CC.001.0x - Contacts activation sequence

This test verifies the contacts activation sequence.

Test Code

1CC.001.0x

Reference

This test refers to requirements in [D01], section 6.1.2.

Test Conditions

Use Table 24 for the test conditions during verifications of the contacts activation sequence.

Value of x	I_{CC}
1	2 mA ± 2% ± 0.1 mA
2	54 mA ± 2% ± 0.1 mA

Table 24 – Test conditions for 1CC.001.0x

Procedure

Follow this procedure to verify the contacts activation sequence :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 24.
3. Insert the measurement probe into the DUT (notional time t_0, see Figure 7).
4. Record the notional time t_1 when Vcc rises for the first time above 0.4 V DC.
5. Record the notional time t_2 when Vcc rises for the first time above (4.60 V - εV) [For Class A] or (2.76 V - εV) [For Class B].
6. Record the notional time t_3 when I/O rises for the first time above ((0.2 × Vcc) + εVV).
7. Record the notional time t_4 when CLK rises for the first time above ((0.2 × Vcc) + εVV).
8. Record the notional time t_5 that is 200 clock cycles after t_2.
9. Record the notional time t_6 when RST rises for the first time above ((0.2 × Vcc) + εVV).
10. During steps 3 to 9, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND), the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
11. Set the test conditions as listed in the next line of Table 24 and repeat steps 3 to 10.
12. Repeat steps 1 to 10 for all other environmental conditions.

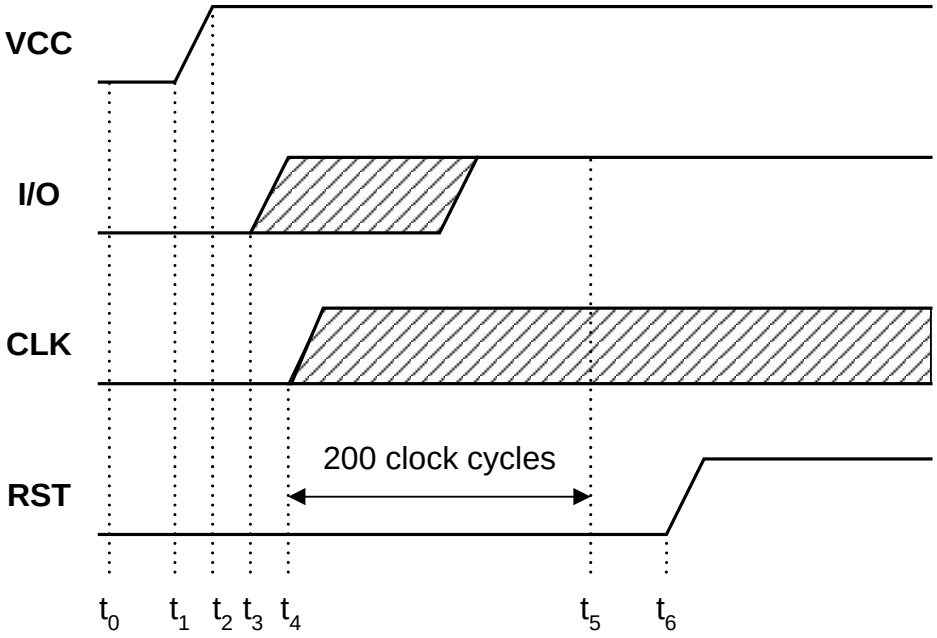


Figure 7 – Contacts Activation Sequence

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions :

1. The notional events appear in the correct time sequence :
   a. For VCC : $t_0 < t_1 < t_2$
   b. For I/O : $t_2 \leq t_3 < t_5$
   c. For CLK : $t_2 < t_4$
   d. For RST : $t_5 < t_6$

2. In the time interval from t_0 to t_2 :
   a. (- 0.25 V DC - εV) ≤ I/O voltage ≤ (V_{CC} + 0.25 V + εVV)
   b. (- 0.25 V DC - εV) ≤ CLK voltage ≤ (V_{CC} + 0.25 V + εVV)
   c. (- 0.25 V DC - εV) ≤ RST voltage ≤ (V_{CC} + 0.25 V + εVV)
   d. (- 0.25 V DC - εV) ≤ VCC voltage

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

7.2 1CC.002.0x - Contacts deactivation sequence

This test verifies the contacts deactivation sequence.

Test Code

1CC.002.0x

Reference

This test refers to requirements in [D01], section 6.1.5.

Test Conditions

Use Table 25 for the test conditions during verifications of the contacts deactivation sequence.

Value of x	I_{CC}
1	2 mA ± 2% ± 0.1 mA
2	54 mA ± 2% ± 0.1 mA

Table 25 – Test conditions for 1CC.002.0x

Procedure

Follow this procedure to verify the contacts activation sequence :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 25.
3. Initiate cold reset.
4. Send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of 5 seconds.
5. Record the notional time t_1 when RST falls for the first time below $((0.2 \times V_{CC}) - \varepsilon VV)$ at the end of the transaction (See Figure 8).
6. Record the notional time t_2 when I/O falls for the last time below $((0.2 \times V_{CC}) - \varepsilon VV)$ at the end of the transaction.
7. Record the notional time t_3 when CLK falls for the last time below $((0.2 \times V_{CC}) - \varepsilon VV)$ at the end of the transaction.
8. Record the notional time t_4 when V_{CC} falls below (4.60 V - εV) [For Class A] or (2.76 V - εV) [For Class B].
9. Record the notional time t_5 when V_{CC} falls for the first time below (0.40 V - εV).
10. Record the notional time t_6 that is 100 ms after t_1.
11. During steps 5 to 10, monitor the Vcc voltage between contacts C1 (VCC) and C5 (GND), the I/O voltage between contacts C7 (I/O) and C5 (GND), the CLK voltage between contacts C3 (CLK) and C5 (GND) and the RST voltage between contacts C2 (RST) and C5 (GND).
12. Set the test conditions as listed in the next line of Table 25 and repeat steps 3 to 11.
13. Repeat steps 1 to 12 for all other environmental conditions.

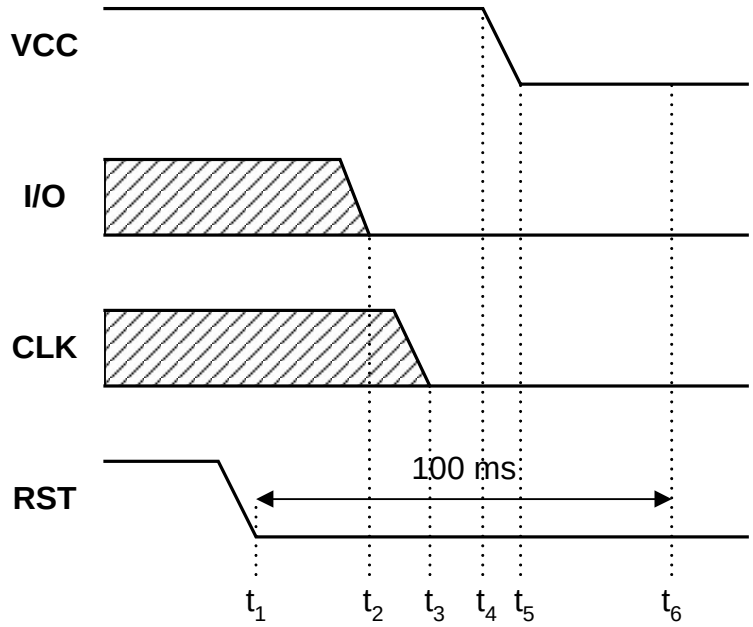


Figure 8 – Contacts Deactivation Sequence

Note : In the Figure 8, the relative position of t_2 and t_3 is indicative only, for the sake of the drawing clarity. It is allowed that $t_2 < t_3$, or $t_2 = t_3$, or $t_2 > t_3$.

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions :

1. The notional events appear in the correct time sequence :
   a. For VCC : $t_1 < t_4 < t_5 < t_6$
   b. For I/O : $t_1 < t_2 < t_4$
   c. For CLK : $t_1 < t_3 < t_4$

2. In the time interval from t_4 to t_5 :
   a. (- 0.25 V DC - εV) ≤ Vcc voltage
   b. (- 0.25 V DC - εV) ≤ I/O voltage ≤ (V_{CC} + 0.25 V + εVV)
   c. (- 0.25 V DC - εV) ≤ CLK voltage ≤ (V_{CC} + 0.25 V + εVV)
   d. (- 0.25 V DC - εV) ≤ RST voltage ≤ (V_{CC} + 0.25 V + εVV)

3. In the time interval from t_5 to t_6 :
   a. (- 0.25 V DC - εV) ≤ Vcc voltage ≤ (0.40 V + 0.25 V + εV)
   b. (- 0.25 V DC - εV) ≤ I/O voltage ≤ (V_{CC} + 0.25 V + εVV)
   c. (- 0.25 V DC - εV) ≤ CLK voltage ≤ (V_{CC} + 0.25 V + εVV)
   d. (- 0.25 V DC - εV) ≤ RST voltage ≤ (V_{CC} + 0.25 V + εVV)

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

7.3 1CC.003.0x - Cold reset

This test verifies the cold reset sequence.

Test Code

1CC.003.0x

Reference

This test refers to requirements in [D01], section 6.1.3.1.

Test Conditions

Use Table 26 for the test conditions during verifications of the cold reset sequence.

Value of x	I_{CC}	ATR delay	Delay uncertainty
1	2 mA ± 2% ± 0.1 mA	400 clock cycles	-0 +20 clock cycles
2	54 mA ± 2% ± 0.1 mA	400 clock cycles	-0 +20 clock cycles
3	2 mA ± 2% ± 0.1 mA	40'000 clock cycles	-20 + 0 clock cycles
4	54 mA ± 2% ± 0.1 mA	40'000 clock cycles	-20 +0 clock cycles

Table 26 – Test conditions for 1CC.003.0x

Procedure

Follow this procedure to verify the cold reset sequence :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 26.
3. Insert the measurement probe into the DUT. Initiate activation.
4. Record the notional time t_1 when CLK rises for the first time above ((0.7 × Vcc) - εVV).
5. Record the notional time t_2 when RST rises for the first time above ((0.7 × Vcc) - εVV).
6. Starting from t_2, wait for the delay specified in the "ATR delay" column of the concerned line of Table 26, then send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
7. Set the test conditions as listed in the next line of Table 26 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions :

1. The time between t_1 and t_2 is between 40'000 and 45'000 clock cycles.
2. Each sequence of commands and answers is performed correctly.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

7.4 1CC.004.0x - Warm reset

This test verifies the warm reset sequence.

Test Code

1CC.003.0x

Reference

This test refers to requirements in [D01], section 6.1.3.2.

Test Conditions

Use Table 27 for the test conditions during verifications of the warm reset sequence.

Value of x	I_{CC}	ATR delay	Delay uncertainty
1	2 mA ± 2% ± 0.1 mA	400 clock cycles	-0 +20 clock cycles
2	54 mA ± 2% ± 0.1 mA	400 clock cycles	-0 +20 clock cycles
3	2 mA ± 2% ± 0.1 mA	40'000 clock cycles	-20 + 0 clock cycles
4	54 mA ± 2% ± 0.1 mA	40'000 clock cycles	-20 +0 clock cycles

Table 27 – Test conditions for 1CC.004.0x

Procedure

Follow this procedure to verify the warm reset sequence :

1. Stabilize the DUT at the appropriate environmental conditions.
2. Set the test conditions as listed in the first line of Table 27.
3. Initiate warm reset by sending the non-standard T=0 ATR "3B 60 05 00".
4. Record the notional time t_1 when RST falls below ((0.2 × Vcc) + εVV).
5. Record the notional time t_2 when RST rises above ((0.7 × Vcc) - εVV).
6. Starting from t_2, wait for the delay specified in the "ATR delay" column of the concerned line of Table 27, then send the default T=0 ATR and complete processing of a command sequence between the Test Bench and IUT with a minimum duration of one second.
7. Set the test conditions as listed in the next line of Table 27 and repeat steps 3 to 6. Repeat this step until the end of the table.
8. Repeat steps 1 to 7 for all other environmental conditions.

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions :

1. The time between t_1 and t_2 is between 40'000 and 45'000 clock cycles.

2. In the time interval from t_1 to t_2 :
   a. For Class A : (4.60 V - εV) ≤ Vcc voltage ≤ (5.40 V + εV)
      For Class B : (2.76 V - εV) ≤ Vcc voltage ≤ (3.24 V + εV)
   b. ((0.7 × V_{CC}) - εVV) ≤ I/O voltage ≤ (V_{CC} + 0.25 V + εVV)
   c. The clock is active with no interruption.

3. Each sequence of commands and answers is performed correctly.

Expected Results

Results are recorded with one of two statements :

- Pass message
- Fail message including a list of all failed conditions and reference details of the acceptance item(s) not met.

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