

# HN62418 Series

## HN62428 Series

### 8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

#### ■ DESCRIPTION

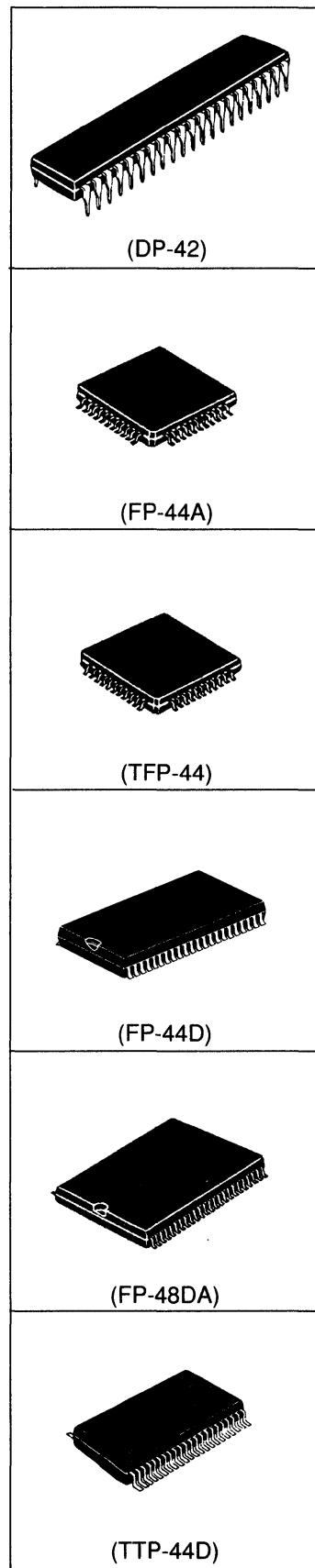
The Hitachi HN62418/428 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62418/428 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic QFP packages. The HN62418 is also packaged in a 44-lead TQFP, a 44-lead Plastic SOP and TSOP and a 48-lead Plastic SOP.

#### ■ FEATURES

- Single Power Supply  
 $V_{CC} = 5 \text{ V} \pm 10\%$
- Fast Access Time:  
150 ns (max)
- Low Power Consumption:  
Active Current: 100 mW (typ)  
Standby Current: 5  $\mu\text{W}$  (typ)
- User Selectable Organization:  
1M x 16-bit (Word-Wide)  
2M x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:  
42-pin Plastic DIP  
44-lead Plastic QFP  
44-lead TQFP  
44-lead Plastic SOP  
48-lead Plastic SOP  
44-lead Plastic TSOP (Type II)



3

**HITACHI**

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

3-65

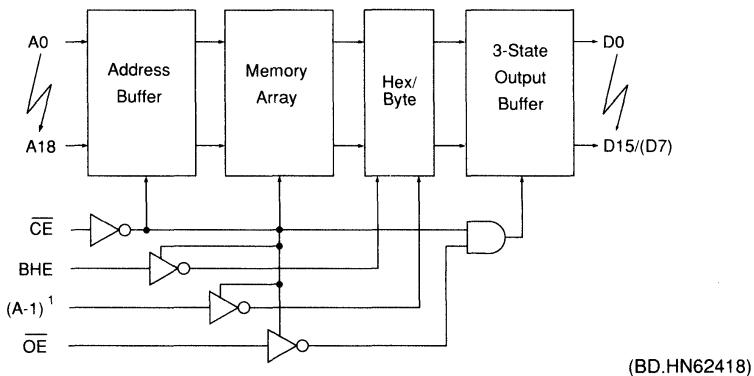
**■ ORDERING INFORMATION**

Type No.	Access Time	Package
HN62418/428P	150 ns/200 ns	42-pin Plastic DIP (DP-42)
HN62418/428FP	150 ns/200 ns	44-lead Plastic QFP (FP-44A)
HN62418/428TFP	150 ns/200 ns	44-lead TQFP (TFP-44)
HN62418/428FB	150 ns/200 ns	44-lead Plastic SOP (FP-44D)
HN62418/428F	150 ns/200 ns	48-lead Plastic SOP (FP-48DA)
HN62418/428TT	150 ns/200 ns	44-lead Plastic TSOP (TTP-44D)

**■ PIN DESCRIPTION**

Pin Name	Function
$A_0 - A_{18}$	Address
$A_{.1}$	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\bar{CE}$	Chip Enable
$\bar{OE}$	Output Enable
BHE	Byte Enable
$V_{cc}$	Power Supply
$V_{ss}$	Ground
NC	No Connection

**■ BLOCK DIAGRAM**



(BD.HN62418)

- Notes:
- \* :  $A_{.1}$  is the Least Significant Address bit in Byte-Wide Mode.
  - $BHE = V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE = V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
When BHE is low,  $D_{14} - D_8$  are in high impedance states.

**HITACHI**

**■ PIN ARRANGEMENT**

HN62418/428P Series

A18	1	O	42	NC
A17	2		41	A8
A7	3		40	A9
A6	4		39	A10
A5	5		38	A11
A4	6		37	A12
A3	7		36	A13
A2	8		35	A14
A1	9		34	A15
A0	10	42-PIN DIP	33	A16
CE	11	TOP VIEW	32	BHE
V <sub>SS</sub>	12		31	V <sub>SS</sub>
OE	13		30	D15/A-1
D0	14		29	D7
D8	15		28	D14
D1	16		27	D6
D9	17		26	D13
D2	18		25	D5
D10	19		24	D12
D3	20		23	D4
D11	21		22	V <sub>CC</sub>

(PinD42.HN62418)

HN62418/428FB Series

HN62418/428TT Series

NC	1	O	44	NC
A18	2		43	NC
A17	3		42	A8
A7	4		41	A9
A6	5		40	A10
A5	6		39	A11
A4	7		38	A12
A3	8		37	A13
A2	9		36	A14
A1	10	44-LEAD SOP	35	A15
A0	11	44-LEAD TSOP	34	A16
CE	12	TOP VIEW	33	BHE
V <sub>SS</sub>	13		32	V <sub>SS</sub>
OE	14		31	D15/A-1
D0	15		30	D7
D8	16		29	D14
D1	17		28	D6
D9	18		27	D13
D2	19		26	D5
D10	20		25	D12
D3	21		24	D4
D11	22		23	V <sub>CC</sub>

(PinD44.HN62418)

3

**HITACHI**

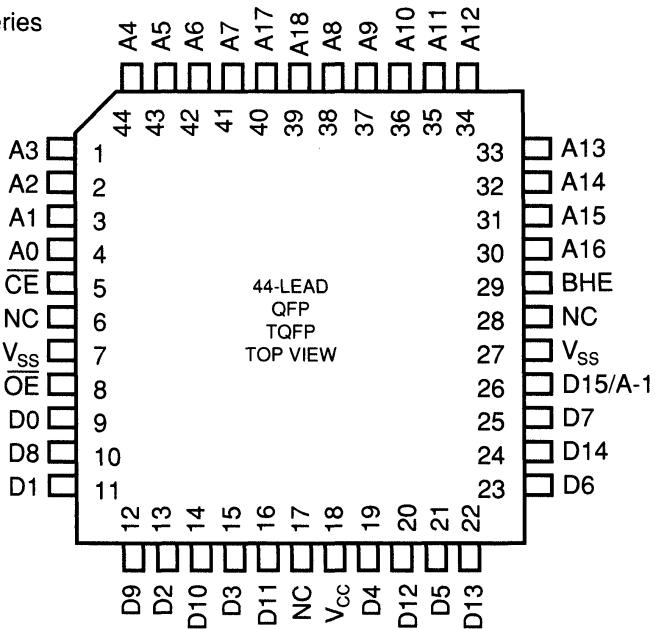
Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

## ■ PIN ARRANGEMENT (cont.)

HN62418/428F Series			
A18	1	48	NC
A17	2	47	A8
A7	3	46	A9
A6	4	45	A10
A5	5	44	A11
A4	6	43	A12
A3	7	42	A13
A2	8	41	A14
A1	9	40	A15
A0	10	39	A16
NC	11	38	NC
NC	12	37	NC
NC	13	36	NC
CE	14	35	BHE
<u>V<sub>SS</sub></u>	15	34	V <sub>SS</sub>
OE	16	33	D15/A-1
D0	17	32	D7
D8	18	31	D14
D1	19	30	D6
D9	20	29	D13
D2	21	28	D5
D10	22	27	D12
D3	23	26	D4
D11	24	25	V <sub>CC</sub>
48-LEAD SOP TOP VIEW			

(PinT248.HN62418)

## **HN62418/428FP Series**



(PinQ44.HN62418)

### ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	V <sub>CC</sub>	-0.3 to +7.0	V
All Input and Output Voltage <sup>1</sup>	V <sub>T</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operating Temperature Range	T <sub>OPR</sub>	0 to +70	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to +125	°C
Temperature Under Bias	T <sub>BIA</sub> S	-20 to +85	°C

Notes: 1. With respect to V<sub>SS</sub>.

### ■ CAPACITANCE

(V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 25°C, V<sub>IN</sub> = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	-	15	pF
Output Capacitance <sup>1</sup>	C <sub>OUT</sub>	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

### ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0 V, T<sub>a</sub> = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I <sub>LI</sub>	-	10	µA	V <sub>IN</sub> = 0 to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	-	10	µA	CĒ = 2.2 V, V <sub>OUT</sub> = 0 to V <sub>CC</sub>
Operating V <sub>CC</sub> Current	I <sub>CC</sub>	-	50	mA	V <sub>CC</sub> = 5.5 V, I <sub>DOUT</sub> = 0 mA, t <sub>RC</sub> = Min.
Standby V <sub>CC</sub> Current	I <sub>SB</sub>	-	30	µA	V <sub>CC</sub> = 5.5 V, CĒ ≥ V <sub>CC</sub> - 0.2V
Input Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.3	V	
	V <sub>IL</sub>	-0.3	0.8	V	
Output Voltage	V <sub>OH</sub>	2.4	-	V	I <sub>OH</sub> = -205 µA
	V <sub>OL</sub>	-	0.4	V	I <sub>OL</sub> = 1.6 mA

## ■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0 V$ ,  $T_a = 0$  to  $70^\circ C$ )

### Test Conditions

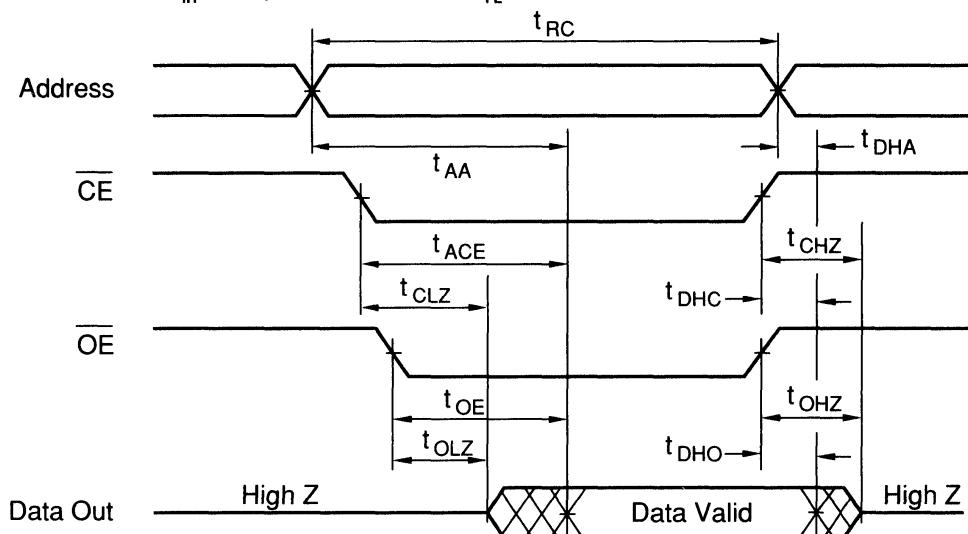
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate +  $CL = 100$  pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62418		HN62428		Unit
		Min.	Max.	Min.	Max	
Read Cycle Time	$t_{RC}$	150	-	200	-	ns
Address Access Time	$t_{AA}$	-	150	-	200	ns
CE Access Time	$t_{ACE}$	-	150	-	200	ns
OE Access Time	$t_{OE}$	-	70	-	100	ns
BHE Access Time	$t_{BHE}$	-	150	-	200	ns
Output Hold Time from Address Change	$t_{DHA}$	0	-	0	-	ns
Output Hold Time from CE	$t_{DHC}$	0	-	0	-	ns
Output Hold Time from OE	$t_{DHO}$	0	-	0	-	ns
Output Hold Time from BHE	$t_{DHB}$	0	-	0	-	ns
CE to Output in High Z	$t_{CHZ}$ <sup>1</sup>	-	70	-	70	ns
OE to Output in High Z	$t_{OHZ}$ <sup>1</sup>	-	70	-	70	ns
BHE to Output in High Z	$t_{BHZ}$ <sup>1</sup>	-	70	-	70	ns
CE to Output in Low Z	$t_{CLZ}$ <sup>1</sup>	10	-	10	-	ns
OE to Output in Low Z	$t_{OLZ}$ <sup>1</sup>	10	-	10	-	ns
BHE to Output in Low Z	$t_{BLZ}$ <sup>1</sup>	10	-	10	-	ns

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

Word Mode ( $BHE = V_{IH}$ ) or Byte Mode ( $BHE = V_{IL}$ )

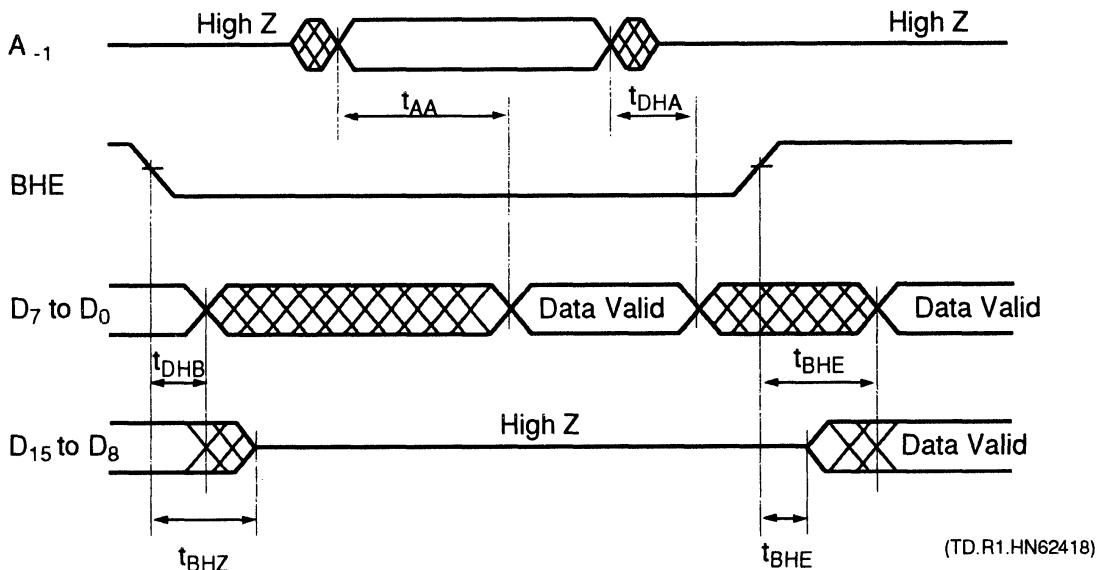


(TD.R.HN62418)

- Note:
- $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$  are determined by the faster time.
  - $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$  are determined by the slower time.
  - $t_{CLZ}$ ,  $t_{OLZ}$  are determined by the slower time.

Word Mode/Byte Mode Switch

3



(TD.R1.HN62418)

- Note:
- $\overline{CE}$  and  $\overline{OE}$  are of select status.  $A_{15}$  to  $A_0$  are fixed.
  - $D_{15}/A-1$  terminal is of output state when  $BHE = V_{IH}$ ,  $\overline{CE}$  and  $\overline{OE}$  are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

**HITACHI**

# HN62W428 Series

## 8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

### ■ DESCRIPTION

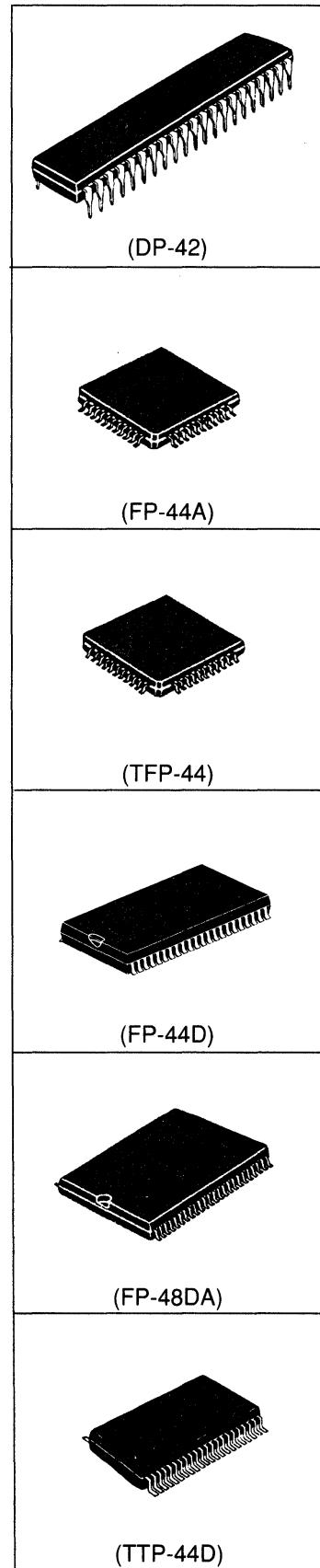
The Hitachi HN62W428 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The low voltage and low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62W428 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic QFP packages. The HN62W428 is also packaged in a 44-lead TQFP, a 44-lead Plastic SOP and TSOP and a 48-lead Plastic SOP.

### ■ FEATURES

- Single Power Supply  
 $V_{CC} = 3.0$  to 5.5V
- Access Time:  
300 ns (max)
- Low Power Consumption:  
Active Current: 100 mW (typ)  
Standby Current: 5  $\mu$ W (typ)
- User Selectable Organization:  
1M x 16-bit (Word-Wide)  
2M x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:  
42-pin Plastic DIP  
44-lead Plastic QFP  
44-lead TQFP  
44-lead Plastic SOP  
48-lead Plastic SOP  
44-lead Plastic TSOP (Type II)



**HITACHI**

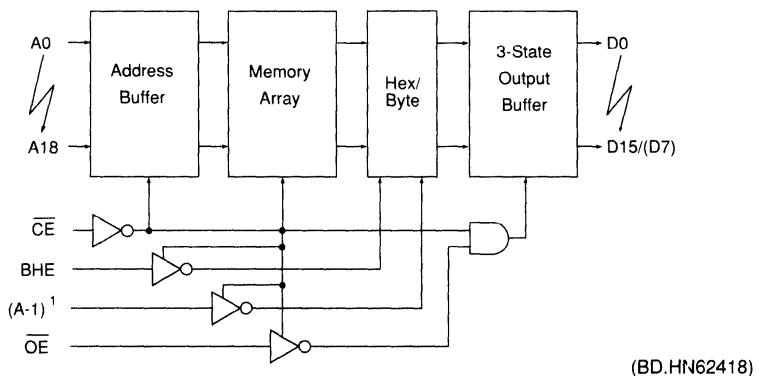
**■ ORDERING INFORMATION**

Type No.	Access Time	Package
HN62W428P	300 ns	42-pin Plastic DIP (DP-42)
HN62W428FP	300 ns	44-lead Plastic QFP (FP-44A)
HN62W428TFP	300 ns	44-lead TQFP (TFP-44)
HN62W428FB	300 ns	44-lead Plastic SOP (FP-44D)
HN62W428F	300 ns	48-lead Plastic SOP (FP-48DA)
HN62W428TT	300 ns	44-lead Plastic TSOP (TTP-44D)

**■ PIN DESCRIPTION**

Pin Name	Function
$A_0 - A_{18}$	Address
$A_{.1}$	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
$V_{CC}$	Power Supply
$V_{SS}$	Ground
NC	No Connection

3

**■ BLOCK DIAGRAM**

(BD.HN62418)

- Notes:
- \* :  $A_{.1}$  is the Least Significant Address bit in Byte-Wide Mode.
  - $BHE = V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE = V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
When BHE is low,  $D_{14} - D_8$  are in high impedance states.

**HITACHI**

■ PIN ARRANGEMENT

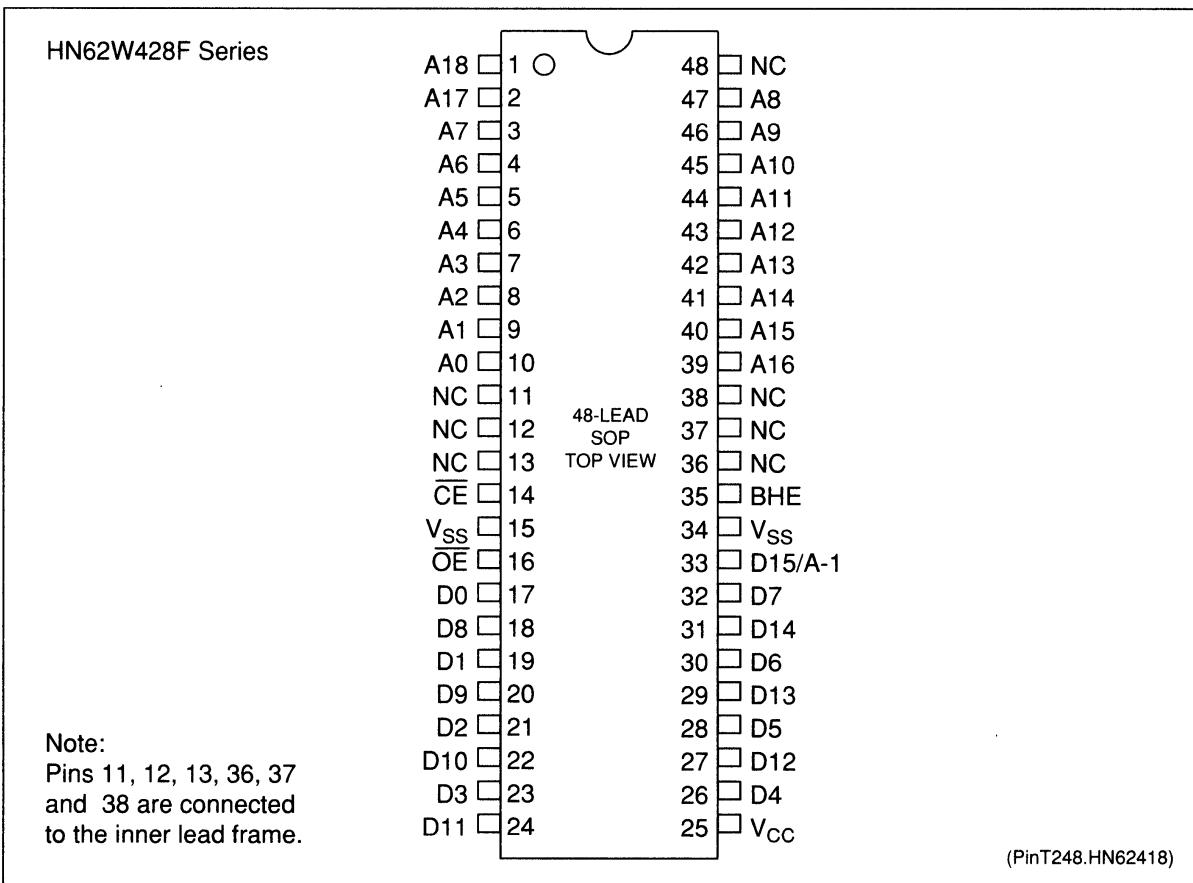
HN62W428P Series	
A18	1 ○
A17	2
A7	3
A6	4
A5	5
A4	6
A3	7
A2	8
A1	9
A0	10
CE	11
V <sub>SS</sub>	12
OE	13
D0	14
D8	15
D1	16
D9	17
D2	18
D10	19
D3	20
D11	21
	42-PIN DIP TOP VIEW
42	NC
41	A8
40	A9
39	A10
38	A11
37	A12
36	A13
35	A14
34	A15
33	A16
32	BHE
31	V <sub>SS</sub>
30	D15/A-1
29	D7
28	D14
27	D6
26	D13
25	D5
24	D12
23	D4
22	V <sub>CC</sub>
(PinD42.HN62418)	

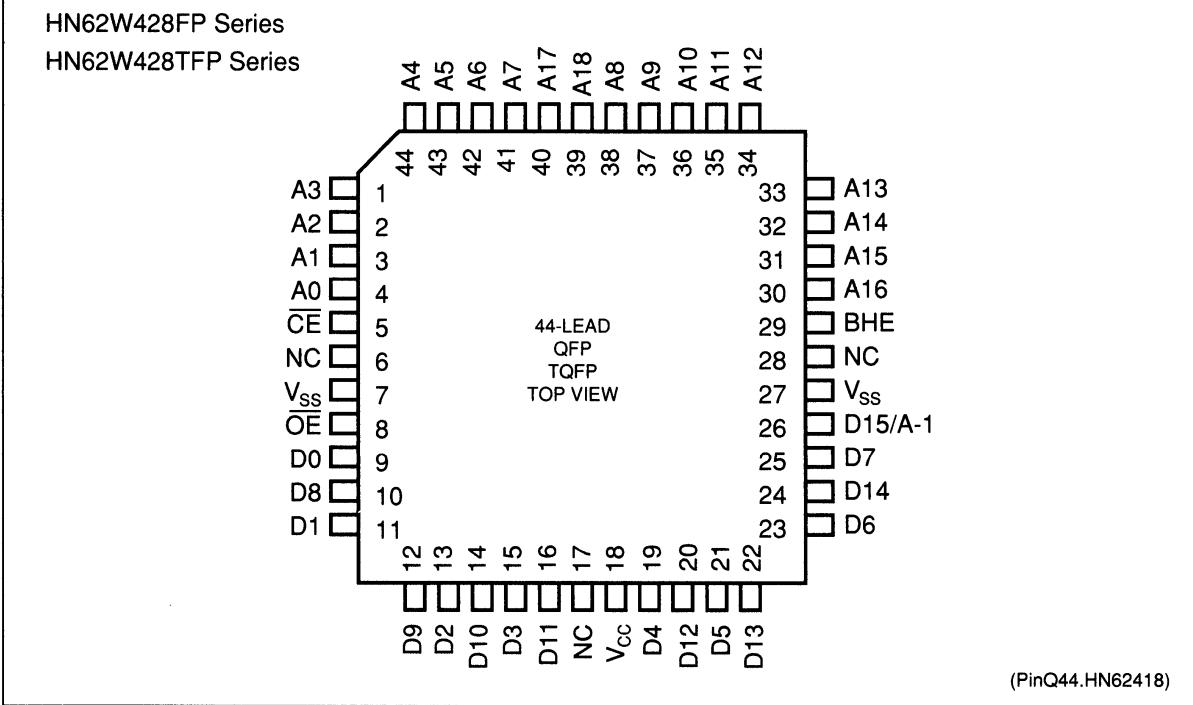
HN62W428FB Series	
HN62W428TT Series	
NC	1 ○
A18	2
A17	3
A7	4
A6	5
A5	6
A4	7
A3	8
A2	9
A1	10
A0	11
CE	12
V <sub>SS</sub>	13
OE	14
D0	15
D8	16
D1	17
D9	18
D2	19
D10	20
D3	21
D11	22
	44-LEAD SOP TOP VIEW
44	NC
43	NC
42	A8
41	A9
40	A10
39	A11
38	A12
37	A13
36	A14
35	A15
34	A16
33	BHE
32	V <sub>SS</sub>
31	D15/A-1
30	D7
29	D14
28	D6
27	D13
26	D5
25	D12
24	D4
23	V <sub>CC</sub>
(PinD44.HN62418)	

**HITACHI**

## ■ PIN ARRANGEMENT (cont.)



3

**HITACHI**

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

3-75

**■ ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	V <sub>CC</sub>	-0.3 to +7.0	V
All Input and Output Voltage <sup>1</sup>	V <sub>T</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operating Temperature Range	T <sub>OPR</sub>	0 to +70	°C
Storage Temperature Range	T <sub>STG</sub>	-55 to +125	°C
Temperature Under Bias	T <sub>BIA</sub> S	-20 to +85	°C

Notes: 1. With respect to V<sub>SS</sub>.

**■ CAPACITANCE**

(V<sub>CC</sub> = 3.0 to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = 25°C, V<sub>IN</sub> = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	-	15	pF
Output Capacitance <sup>1</sup>	C <sub>OUT</sub>	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

**■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**

(V<sub>CC</sub> = 3.0 to 5.5V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I <sub>LI</sub>	-	10	µA	V <sub>IN</sub> = 0 to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	-	10	µA	CĒ = 2.2 V, V <sub>OUT</sub> = 0 to V <sub>CC</sub>
Operating V <sub>CC</sub> Current	I <sub>CC</sub>	-	25	mA	V <sub>CC</sub> = 3.5 V, I <sub>DOUT</sub> = 0 mA, t <sub>RC</sub> = Min.
Standby V <sub>CC</sub> Current	I <sub>SB</sub>	-	30	µA	V <sub>CC</sub> = 5.5 V, CĒ ≥ V <sub>CC</sub> - 0.2V
Input Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.3	V	
	V <sub>IL</sub>	-0.3	0.8	V	
Output Voltage	V <sub>OH</sub>	2.4	-	V	I <sub>OH</sub> = -205 µA
	V <sub>OL</sub>	-	0.4	V	I <sub>OL</sub> = 1.6 mA

**HITACHI**

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 3.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = 0$  to  $70^\circ\text{C}$ )

**Test Conditions**

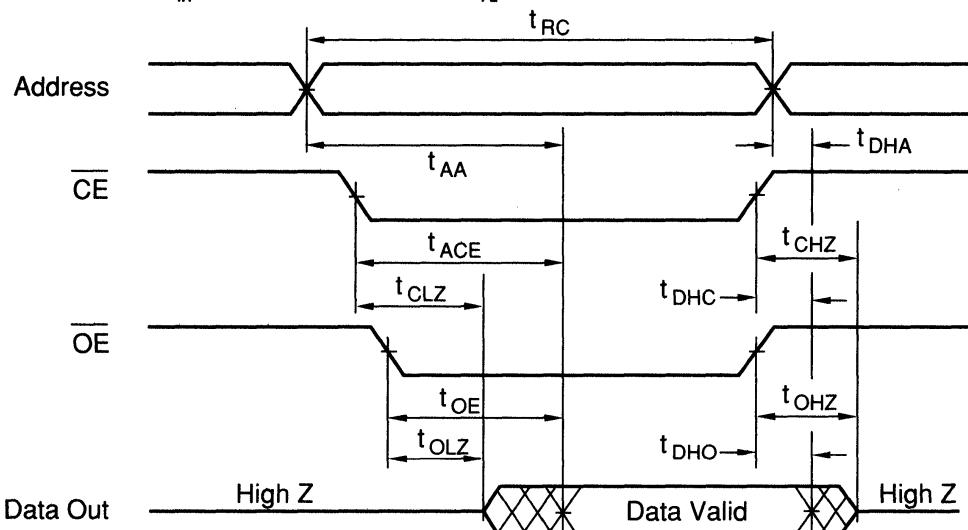
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate +  $CL = 100$  pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62W428		
		Min.	Max.	Unit
Read Cycle Time	$t_{RC}$	300	-	ns
Address Access Time	$t_{AA}$	-	300	ns
CE Access Time	$t_{ACE}$	-	300	ns
OE Access Time	$t_{OE}$	-	150	ns
BHE Access Time	$t_{BHE}$	-	300	ns
Output Hold Time from Address Change	$t_{DHA}$	0	-	ns
Output Hold Time from CE	$t_{DHC}$	0	-	ns
Output Hold Time from OE	$t_{DHO}$	0	-	ns
Output Hold Time from BHE	$t_{DHB}$	0	-	ns
CE to Output in High Z	$t_{CHZ}^1$	-	100	ns
OE to Output in High Z	$t_{OHZ}^1$	-	100	ns
BHE to Output in High Z	$t_{BHZ}^1$	-	100	ns
CE to Output in Low Z	$t_{CLZ}^1$	10	-	ns
OE to Output in Low Z	$t_{OLZ}^1$	10	-	ns
BHE to Output in Low Z	$t_{BLZ}^1$	10	-	ns

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ **READ TIMING WAVEFORM**

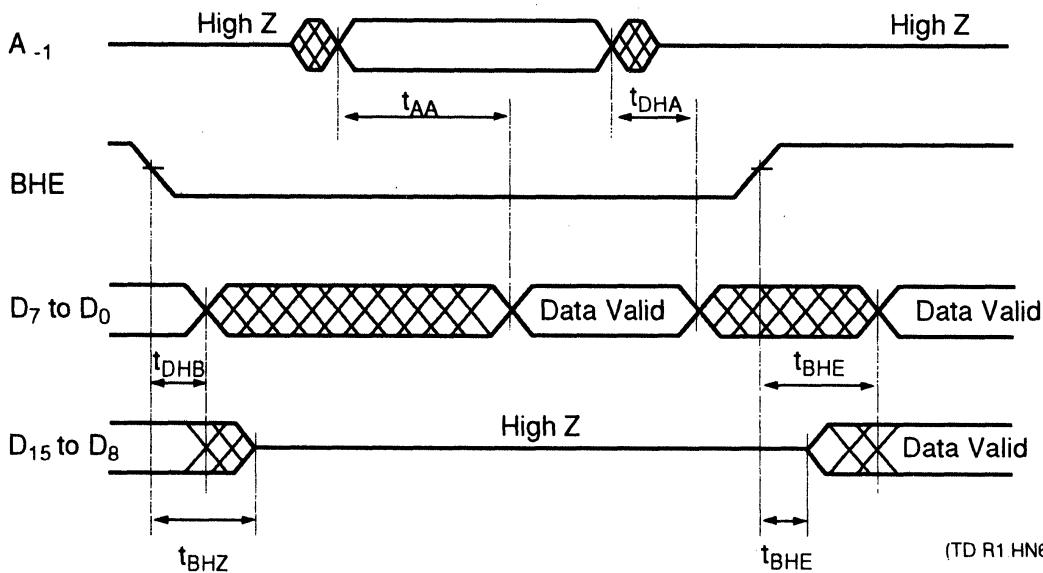
**Word Mode ( $BHE = V_{IH}$ ) or Byte Mode ( $BHE = V_{IL}$ )**



(TD.R.HN62418)

- Note:
1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$  are determined by the faster time.
  2.  $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$  are determined by the slower time.
  3.  $t_{CLZ}$ ,  $t_{OLZ}$  are determined by the slower time.

**Word Mode/Byte Mode Switch**



(TD R1 HN62418)

- Note:
1.  $\overline{CE}$  and  $\overline{OE}$  are of select status.  $A_{18}$  to  $A_0$  are fixed.
  2.  $D_{15}/A_1$  terminal is of output state when  $BHE = V_{IH}$ .  $\overline{CE}$  and  $\overline{OE}$  are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

**HITACHI**

## 8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

### ■ DESCRIPTION

The Hitachi HN62438 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

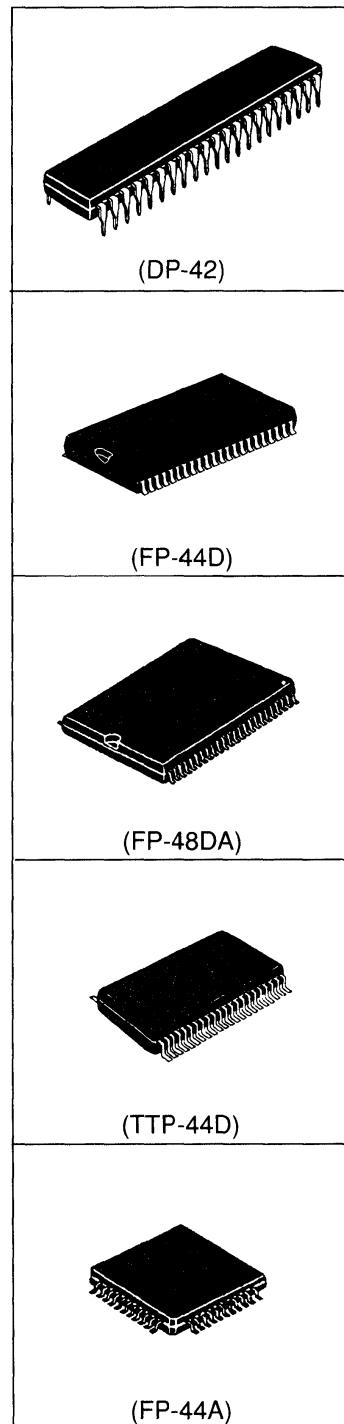
Hitachi's HN62438 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62438 is also packaged in a 48-lead Plastic SOP.

### ■ FEATURES

- Single Power Supply  
 $V_{CC} = 5\text{ V} \pm 10\%$
- Fast Access Times:  
100 ns/120 ns (max)
- Low Power Consumption:  
Active Current: 250 mW (typ)  
Standby Current: 5  $\mu\text{W}$  (typ)
- User Selectable Organization:  
512K x 16-bit (Word-Wide)  
1M x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:  
42-pin Plastic DIP  
44-lead Plastic SOP  
44-lead Plastic TSOP (Type II)  
48-lead Plastic SOP  
44-pin Plastic QFP

### ■ ORDERING INFORMATION

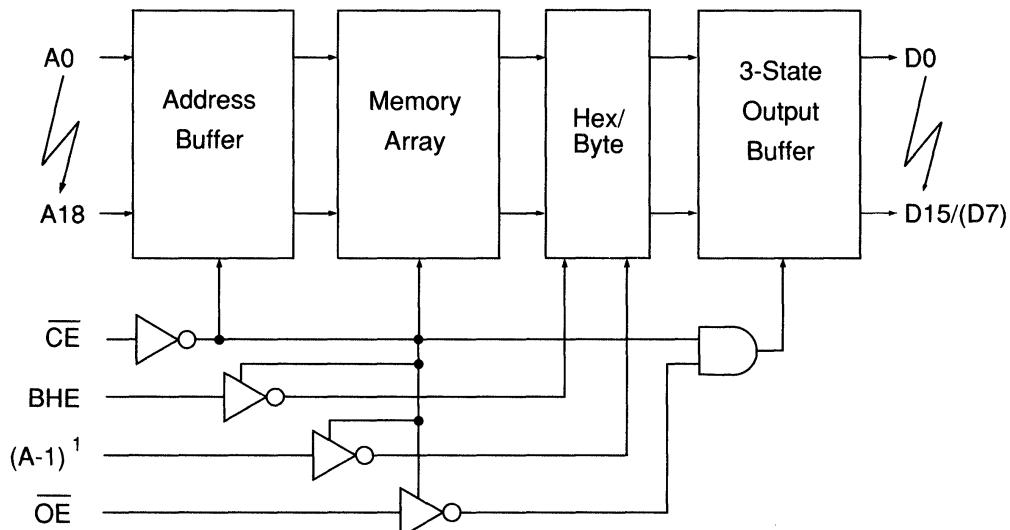
Type No	Access Time	Package
HN62438P	100 ns	42-pin Plastic DIP
	120 ns	(DP-42)
HN62438FB	100 ns	44-lead Plastic SOP
	120 ns	(FP-44D)
HN62438TT	100 ns	44-lead Plastic TSOP
	120 ns	(TTP-44D)
HN62438F	100 ns	48-lead Plastic SOP
	120 ns	(FP-48DA)
HN62438FP	100 ns	44-pin Plastic QFP
	120 ns	(FP-44A)



## ■ PIN DESCRIPTION

Pin Name	Function
$A_0 - A_{18}$	Address
$A_{-1}$	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
$V_{cc}$	Power Supply
$V_{ss}$	Ground
NC	No Connection

## ■ BLOCK DIAGRAM



(BD.HN62418)

- Notes:
1. \* :  $A_{-1}$  is the Least Significant Address bit in Byte-Wide Mode.
  2.  $BHE=V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE=V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
When BHE is low,  $D_{14} - D_8$  are in high impedance states.

**HITACHI**

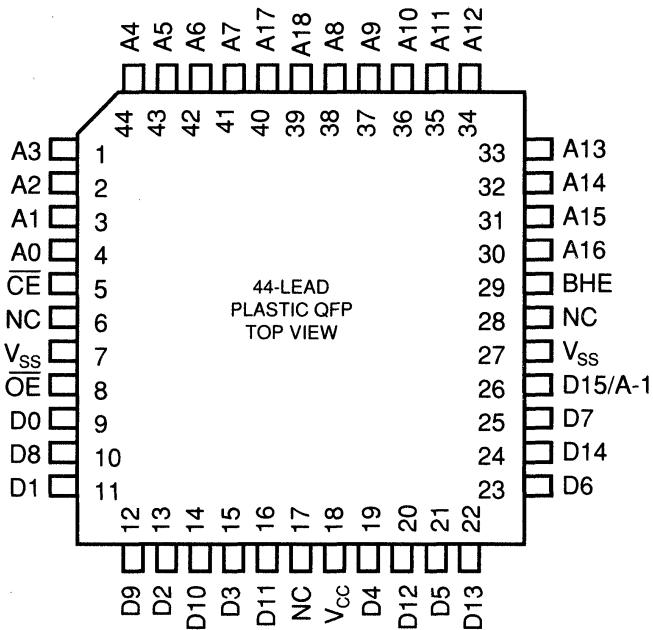
## ■ PIN ARRANGEMENT

HN62438P Series		HN62438FB Series HN62438TT Series			
A18	1 O	42	NC		
A17	2	41	A8		
A7	3	40	A9		
A6	4	39	A10		
A5	5	38	A11		
A4	6	37	A12		
A3	7	36	A13		
A2	8	35	A14		
A1	9	34	A15		
A0	10	33	A16		
CE	11	32	BHE		
V <sub>SS</sub>	12	31	V <sub>SS</sub>		
OE	13	30	D15/A-1		
D0	14	29	D7		
D8	15	28	D14		
D1	16	27	D6		
D9	17	26	D13		
D2	18	25	D5		
D10	19	24	D12		
D3	20	23	D4		
D11	21	22	V <sub>CC</sub>		
42-PIN DIP		44-LEAD SOP 44-LEAD TSOP			
TOP VIEW		TOP VIEW			
(PinD42.HN62438N)					
3					
HN62438F Series					
A18	1 O	48	NC		
A17	2	47	A8		
A7	3	46	A9		
A6	4	45	A10		
A5	5	44	A11		
A4	6	43	A12		
A3	7	42	A13		
A2	8	41	A14		
A1	9	40	A15		
A0	10	39	A16		
NC	11	38	NC		
NC	12	48-LEAD SOP	NC		
NC	13	36	NC		
CE	14	TOP VIEW	BHE		
V <sub>SS</sub>	15		V <sub>SS</sub>		
OE	16		D15/A-1		
D0	17		D7		
D8	18		D14		
D1	19		D6		
D9	20		D13		
D2	21		D5		
D10	22		D12		
D3	23		D4		
D11	24		V <sub>CC</sub>		
48-LEAD SOP					
TOP VIEW					
(PinT248.HN62438N)					
Note: Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.					

**HITACHI**

## ■ PIN ARRANGEMENT, contd.

HN62438FP Series



(PinQ44.HN62418)

## ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$ )

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	10	$\mu A$	$V_{IN} = 0$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-	10	$\mu A$	$\bar{CE} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$
Operating $V_{CC}$ Current	$I_{CC}$	-	80	$mA$	$V_{CC} = 5.5V$ , $I_{DOUT} = 0mA$ , $t_{RC}$ = Min.
Standby $V_{CC}$ Current	$I_{SB1}$	-	30	$\mu A$	$V_{CC} = 5.5V$ , $\bar{CE} \geq V_{CC} - 0.2V$ = Min.
Input Voltage	$V_{IH}$	2.4	$V_{CC} + 0.3$	V	
	$V_{IL}$	-0.3	0.45	V	
Output Voltage	$V_{OH}$	2.4	-	V	$I_{OH} = -205 \mu A$
	$V_{OL}$	-	0.4	V	$I_{OL} = 1.6 mA$

HITACHI

### ■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0 V$ ,  $T_a = 0$  to  $70^\circ C$ )

#### Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate +  $CL = 100$  pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62438-10		HN62438-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	100	-	120	-	ns
Address Access Time	$t_{AA}$	-	100	-	120	ns
$\bar{CE}$ Access Time	$t_{ACE}$	-	100	-	120	ns
$\bar{OE}$ Access Time	$t_{OE}$	-	55	-	60	ns
BHE Access Time	$t_{BHE}$	-	100	-	120	ns
Output Hold Time from Address Change	$t_{DHA}$	0	-	0	-	ns
Output Hold Time from $\bar{CE}$	$t_{DHC}$	0	-	0	-	ns
Output Hold Time from $\bar{OE}$	$t_{DHO}$	0	-	0	-	ns
Output Hold Time from BHE	$t_{DHB}$	0	-	0	-	ns
$\bar{CE}$ to Output in High Z	$t_{CHZ}^1$	-	40	-	40	ns
$\bar{OE}$ to Output in High Z	$t_{OHZ}^1$	-	40	-	40	ns
BHE to Output in High Z	$t_{BHZ}^1$	-	40	-	40	ns
$\bar{CE}$ to Output in Low Z	$t_{CLZ}$	5	-	5	-	ns
$\bar{OE}$ to Output in Low Z	$t_{OLZ}$	5	-	5	-	ns
BHE to Output in Low Z	$t_{BLZ}$	5	-	5	-	ns

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	$V_{CC}$	-0.3 to +7.0	V
All Input and Output Voltage <sup>1</sup>	$V_T$	-0.3 to $V_{CC} + 0.3$	V
Operating Temperature Range	$T_{OPR}$	0 to +70	°C
Storage Temperature Range	$T_{STG}$	-55 to +125	°C
Temperature Under Bias	$T_{BIAS}$	-20 to +85	°C

Notes: 1. With respect to  $V_{SS}$ .

■ CAPACITANCE

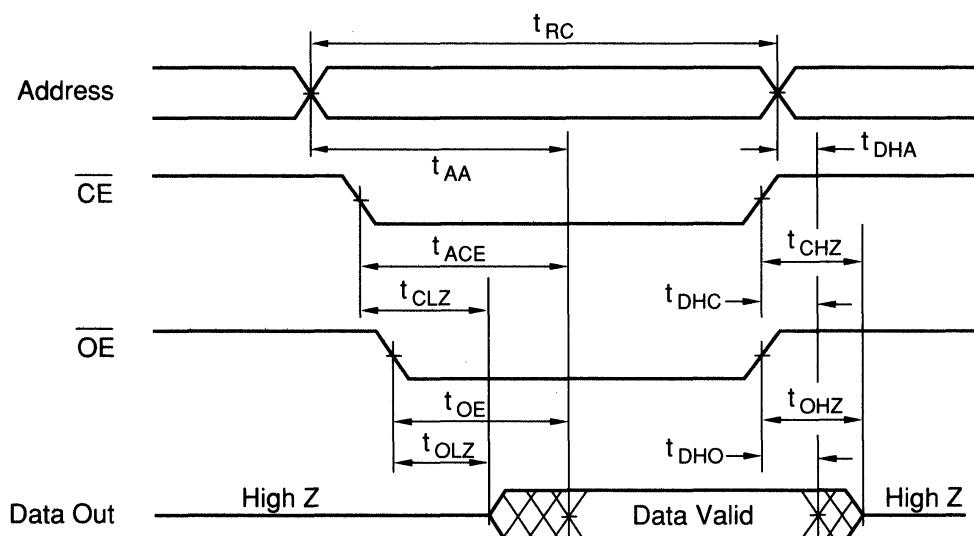
( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $V_{IN} = 0 V$ ,  $f = 1 MHz$ )

Item	Symbol	Min.	Max.	Unit
Input Capacitance <sup>1</sup>	$C_{IN}$	-	15	pF
Output Capacitance <sup>1</sup>	$C_{OUT}$	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ READ TIMING WAVEFORM

Word Mode ( $BHE = V_{IH}$ ) or Byte Mode ( $BHE = V_{IL}$ )

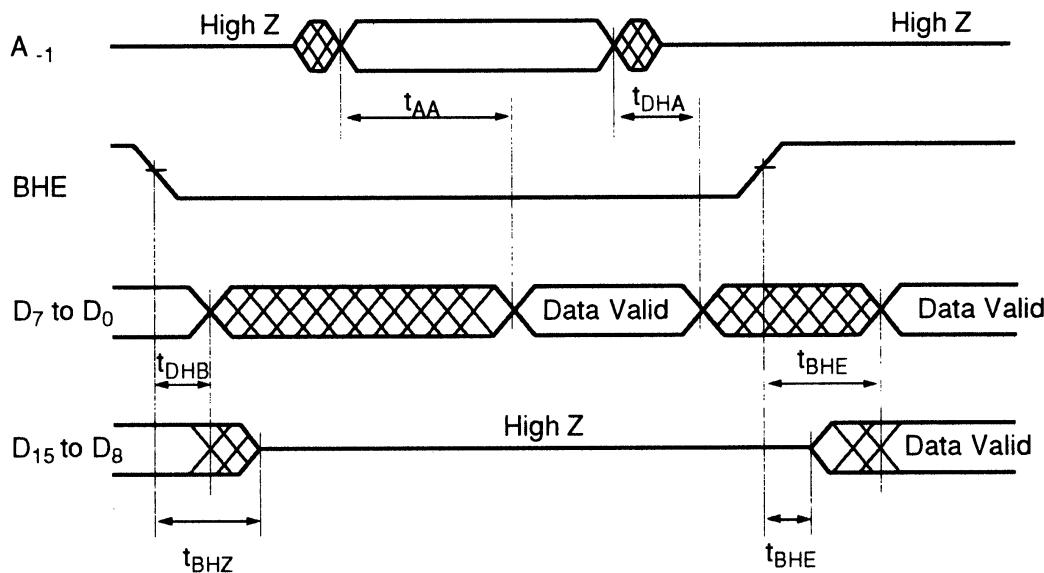


(TD.R.HN62438N)

- Note:
1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$  are determined by the faster time.
  2.  $t_{AA}$ ,  $t_{ACE}$ ,  $t_{OE}$  are determined by the slower time.
  3.  $t_{CLZ}$ ,  $t_{OLZ}$  are determined by the slower time.

**HITACHI**

■ READ TIMING WAVEFORM  
Word Mode/Byte Mode Switch



(TD.R1.HN62438N)

- Note:
1.  $\overline{CE}$  and  $\overline{OE}$  are of select status.  $A_{18}$  to  $A_0$  are fixed.
  2.  $D_{15}/A_{18}$  terminal is of output state when  $BHE = V_{IH}$ ,  $\overline{CE}$  and  $\overline{OE}$  are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

3

**HITACHI**

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

3-85

## 8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

### ■ DESCRIPTION

The Hitachi HN62438N Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

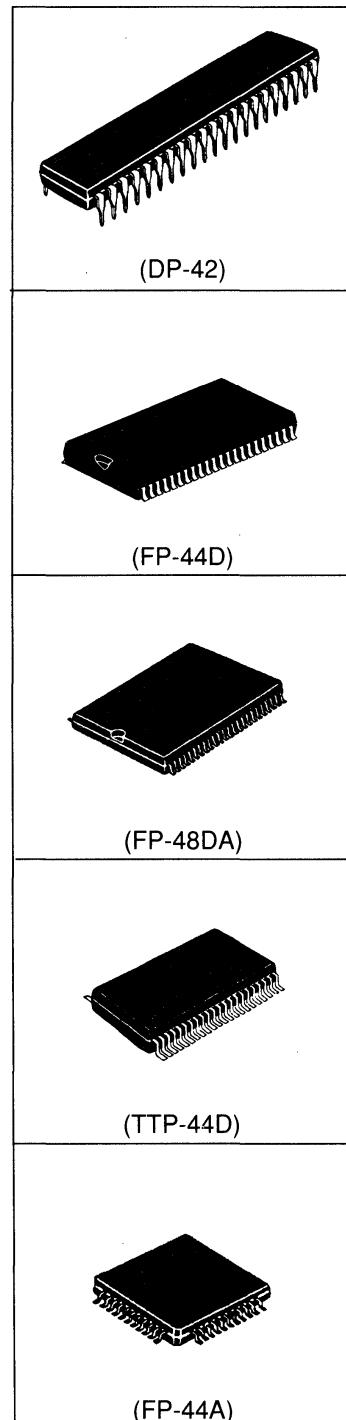
Hitachi's HN62438N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62438N is also packaged in a 48-lead Plastic SOP.

### ■ FEATURES

- Single Power Supply  
 $V_{CC} = 5 \text{ V} \pm 10\%$
- Fast Access Times:  
120 ns/150 ns (max)
- Fast Address Access Times ( $A_0, A_1$ ):  
60 ns/70 ns (max)
- Low Power Consumption:  
Active Current: 250 mW (typ)  
Standby Current: 5  $\mu\text{W}$  (typ)
- User Selectable Organization:  
512K x 16-bit (Word-Wide)  
1M x 8-bit (Byte-Wide)  
Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:  
JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:  
42-pin Plastic DIP  
44-lead Plastic SOP  
44-lead Plastic TSOP (Type II)  
48-lead Plastic SOP  
44-pin Plastic QFP

### ■ ORDERING INFORMATION

Type No	Access Time	Package
HN62438NP	120 ns	42-pin Plastic DIP
	150 ns	(DP-42)
HN62438NFB	120 ns	44-lead Plastic SOP
	150 ns	(FP-44D)
HN62438NTT	120 ns	44-lead Plastic TSOP
	150 ns	(TTP-44D)
HN62438NF	120 ns	48-lead Plastic SOP
	150 ns	(FP-48DA)
HN62438NFP	120 ns	44-pin Plastic QFP
	150 ns	(FP-44A)

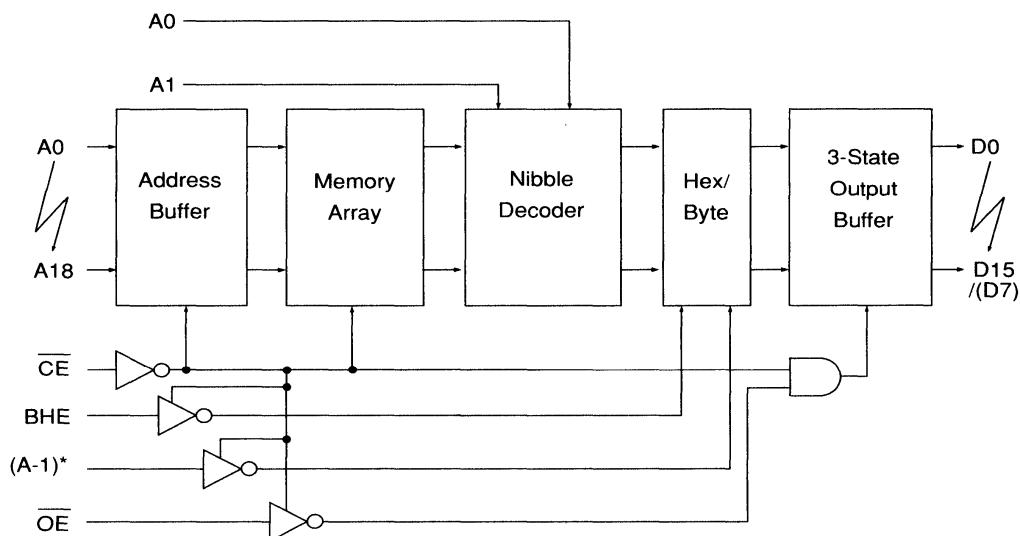


**HITACHI**

### ■ PIN DESCRIPTION

Pin Name	Function
$A_0 - A_{18}$	Address
$A_{.1}$	Address (Word-Wide)
$D_0 - D_{15}$	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
$V_{cc}$	Power Supply
$V_{ss}$	Ground
NC	No Connection

### ■ BLOCK DIAGRAM



3

(BD.HN62438N)

- Notes:
- \* :  $A_{.1}$  is the Least Significant Address bit in Byte-Wide Mode.
  - $BHE = V_{IH}$  : 16-bit ( $D_{15} - D_0$ )  
 $BHE = V_{IL}$  : 8-bit ( $D_7 - D_0$ )  
When BHE is low,  $D_{14} - D_8$  are in high impedance states.

**HITACHI**

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

3-87

## **HN62438N Series**

## ■ PIN ARRANGEMENT

HN62438NP Series		HN62438NFB Series		HN62438NTT Series					
A18	1	42	NC	NC	1				
A17	2	41	A8	A18	2				
A7	3	40	A9	A17	3				
A6	4	39	A10	A7	4				
A5	5	38	A11	A6	5				
A4	6	37	A12	A5	6				
A3	7	36	A13	A4	7				
A2	8	35	A14	A3	8				
A1	9	34	A15	A2	9				
A0	10	33	A16	A1	10				
CE	11	32	BHE	A0	11				
V <sub>SS</sub>	12	31	V <sub>SS</sub>	CE	12				
OE	13	30	D15/A-1	V <sub>SS</sub>	13				
D0	14	29	D7	OE	14				
D8	15	28	D14	D0	15				
D1	16	27	D6	D8	16				
D9	17	26	D13	D1	17				
D2	18	25	D5	D9	18				
D10	19	24	D12	D2	19				
D3	20	23	D4	D10	20				
D11	21	22	V <sub>CC</sub>	D3	21				
42-PIN DIP		44-LEAD SOP		44-LEAD TSOP					
TOP VIEW		TOP VIEW		TOP VIEW					
(PinD42_HN62438NP)									
(PinD44_HN62438NFB)									

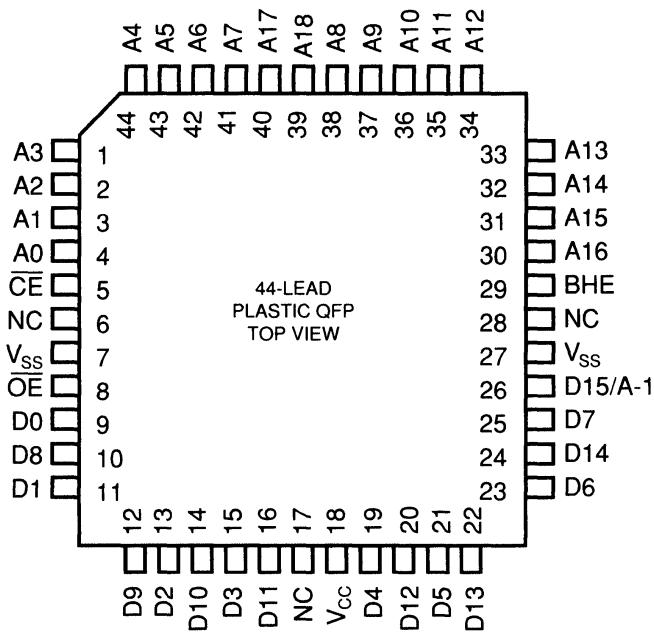
HN62438NF Series			
A18	1	48	NC
A17	2	47	A8
A7	3	46	A9
A6	4	45	A10
A5	5	44	A11
A4	6	43	A12
A3	7	42	A13
A2	8	41	A14
A1	9	40	A15
A0	10	39	A16
NC	11	38	NC
NC	12	48-LEAD	NC
NC	13	SOP	NC
CE	14	TOP VIEW	BHE
V <sub>SS</sub>	15	34	V <sub>SS</sub>
OE	16	33	D15/A-1
D0	17	32	D7
D8	18	31	D14
D1	19	30	D6
D9	20	29	D13
D2	21	28	D5
D10	22	27	D12
D3	23	26	D4
D11	24	25	V <sub>CC</sub>

**Note:**  
Pins 11, 12, 13, 36, 37  
and 38 are connected  
to the inner lead frame.

HITACHI

■ PIN ARRANGEMENT, contd.

HN62438NFP Series



(PinQ44.HN62418)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	$V_{CC}$	-0.3 to +7.0	V
All Input and Output Voltage <sup>1</sup>	$V_T$	-0.3 to $V_{CC} + 0.3$	V
Operating Temperature Range	$T_{OPR}$	0 to +70	°C
Storage Temperature Range	$T_{STG}$	-55 to +125	°C
Temperature Under Bias	$T_{BIAS}$	-20 to +85	°C

Notes: 1. With respect to  $V_{SS}$ .

3

■ CAPACITANCE

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $V_{IN} = 0 V$ ,  $f = 1MHz$ )

Item	Symbol	Min.	Max.	Unit
Input Capacitance <sup>1</sup>	$C_{IN}$	-	15	pF
Output Capacitance <sup>1</sup>	$C_{OUT}$	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

3-89

### ■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0 V$ ,  $T_a = 0$  to  $70^\circ C$ )

#### Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate +  $CL = 100$  pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62438N-12		HN62438N-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	$t_{RC}$	120	-	120	-	ns
Fast Address Read Cycle Time	$t_{BC}$	60	-	70	-	ns
Address Access Time	$t_{AA}$	-	120	-	150	ns
Fast (Address Access) Time	$t_{BA}$	-	60	-	70	ns
CE Access Time	$t_{ACE}$	-	120	-	150	ns
OE Access Time	$t_{OE}$	-	60	-	70	ns
BHE Access Time	$t_{BHE}$	-	120	-	150	ns
Output Hold Time from Address Change	$t_{DHA}$	0	-	0	-	ns
Output Hold Time from CE	$t_{DHC}$	0	-	0	-	ns
Output Hold Time from OE	$t_{DHO}$	0	-	0	-	ns
Output Hold Time from BHE	$t_{DHB}$	0	-	0	-	ns
CE to Output in High Z	$t_{CHZ}$ <sup>1</sup>	-	60	-	70	ns
OE to Output in High Z	$t_{OHZ}$ <sup>1</sup>	-	60	-	70	ns
BHE to Output in High Z	$t_{BHZ}$ <sup>1</sup>	-	60	-	70	ns
CE to Output in Low Z	$t_{CLZ}$	10	-	10	-	ns
OE to Output in Low Z	$t_{OLZ}$	10	-	10	-	ns
BHE to Output in Low Z	$t_{BLZ}$	10	-	10	-	ns

Note: 1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{BHZ}$  define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

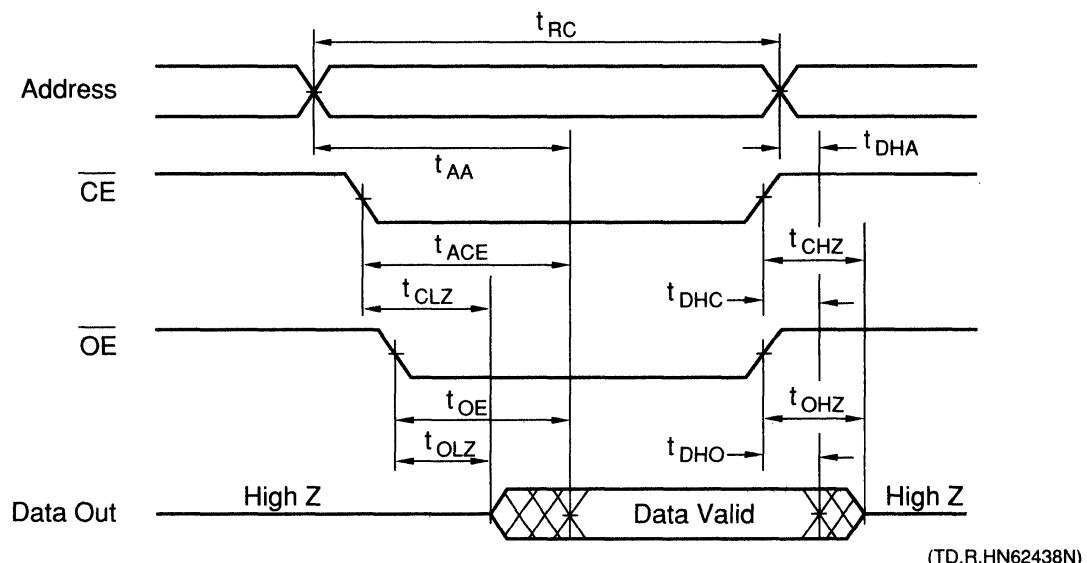
■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$ )

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	10	$\mu A$	$V_{IN} = 0$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-	10	$\mu A$	$\overline{CE} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$
Operating $V_{CC}$ Current	$I_{CC}$	-	100	mA	$V_{CC} = 5.5V$ , $I_{DOUT} = 0$ mA, $t_{RC}$ = Min.
Standby $V_{CC}$ Current	$I_{SB1}$	-	30	$\mu A$	$V_{CC} = 5.5V$ , $\overline{CE} \geq V_{CC} - 0.2V$ = Min.
	$I_{SB2}$	-	3	mA	$V_{CC} = 5.5V$ , $\overline{CE} \geq 2.4V$
Input Voltage	$V_{IH}$	2.4	$V_{CC} + 0.3$	V	
	$V_{IL}$	-0.3	0.45	V	
Output Voltage	$V_{OH}$	2.4	-	V	$I_{OH} = -205 \mu A$
	$V_{OL}$	-	0.4	V	$I_{OL} = 1.6$ mA

■ READ TIMING WAVEFORM

Word Mode ( $BHE = V_{IH}$ ) or Byte Mode ( $BHE = V_{IL}$ )



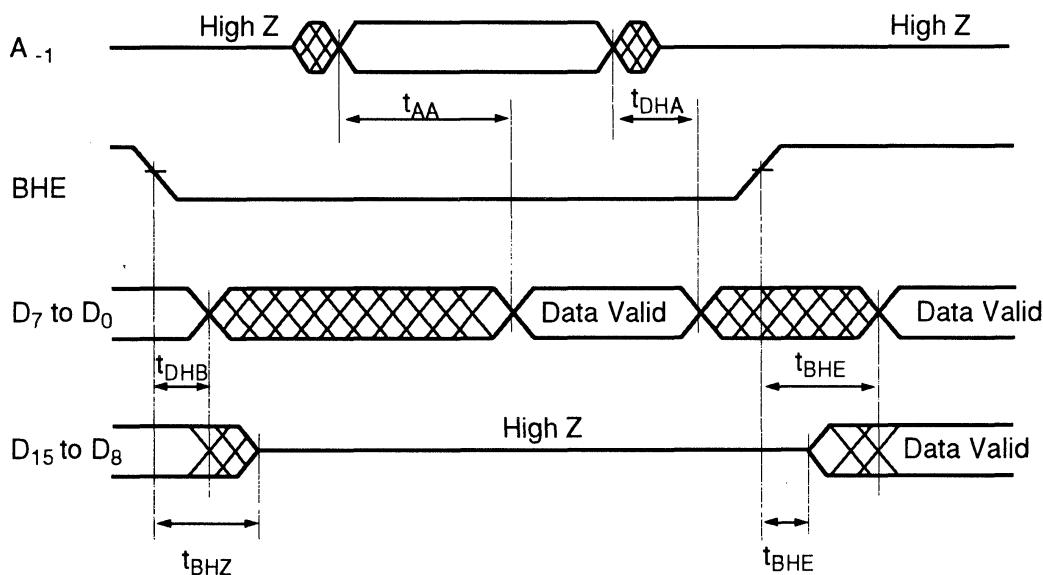
- Note:
1.  $t_{DHA}$ ,  $t_{DHC}$ ,  $t_{DHO}$  are determined by the faster time.
  2.  $t_{AA}$ ,  $t_{AEC}$ ,  $t_{OE}$  are determined by the slower time.
  3.  $t_{CLZ}$ ,  $t_{OLZ}$  are determined by the slower time.

3

HITACHI

■ **READ TIMING WAVEFORM**

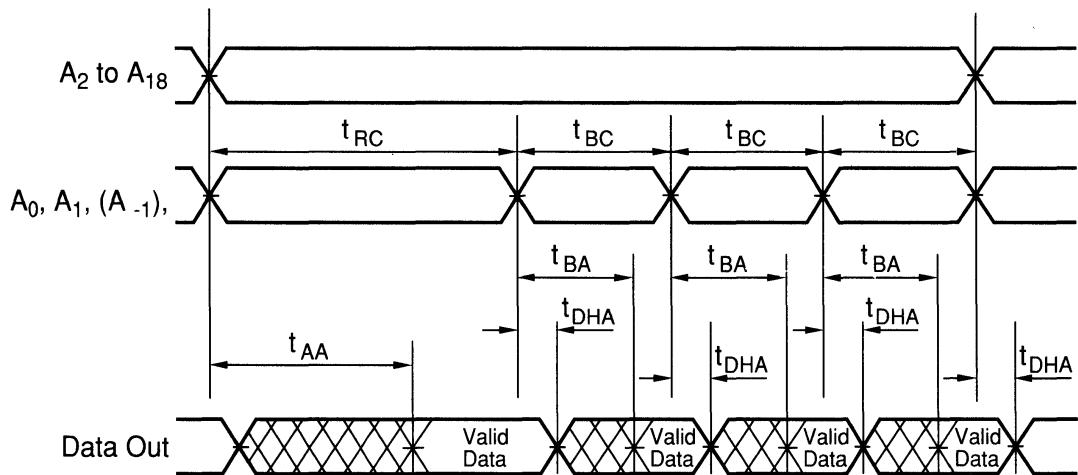
**Word Mode/Byte Mode Switch**



(TD.R1.HN62438N)

- Note:
1.  $\overline{CE}$  and  $\overline{OE}$  are of select status.  $A_{18}$  to  $A_0$  are fixed.
  2.  $D_{15}/A_{-1}$  terminal is of output state when  $BHE = V_{IH}$ ,  $\overline{CE}$  and  $\overline{OE}$  are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

**Fast Address Access**



(TD.RN.HN62438N)

- Note:  $\overline{CE}$  and  $\overline{OE}$  are enabled.

**HITACHI**