# HM51W17800 Series

2,097,152-word × 8-bit Dynamic RAM

HITACHI

ADE-203-664C (Z)
Rev. 3.0
Feb. 24, 1997

## Description

The Hitachi HM51W17800 is a CMOS dynamic RAM organized 2,097,152-word × 8-bit. It employs the most advanced CMOS technology for high performance and low power. The HM51W17800 offers Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM51W17800 to be packaged in standard 28-pin plastic SOJ and 28-pin TSOP.

## Features

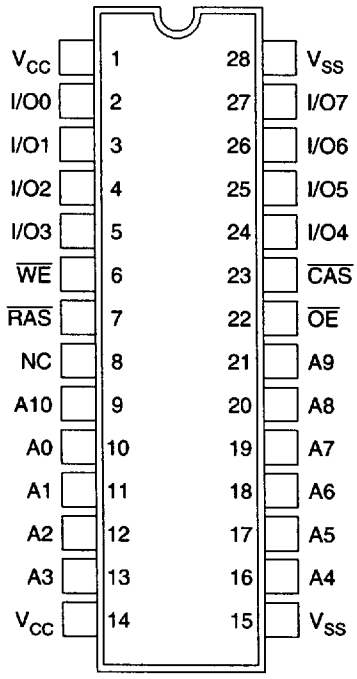
- Single 3.3 V (±0.3 V)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
  - — Active mode: 396 mW/360 mW/324 mW (max)
  - — Standby mode
    - 7.2 mW (max)
    - 0.54 mW (max) (L-version)
- Fast page mode capability
- Refresh cycles
  - — 2048 refresh cycles
    - 32 ms
    - 128 ms (L-version)
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- Battery backup operation (L-version)

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM51W17800J-5 | 50 ns | 400-mil 28-pin plastic SOJ (CP-28DA) |
| HM51W17800J-6 | 60 ns | |
| HM51W17800J-7 | 70 ns | |
| HM51W17800LJ-5 | 50 ns | 400-mil 28-pin plastic SOJ (CP-28DA) |
| HM51W17800LJ -6 | 60 ns | |
| HM51W17800LJ -7 | 70 ns | |
| HM51W17800S-5 | 50 ns | 300-mil 28-pin plastic SOJ (CP-28DNA) |
| HM51W17800S-6 | 60 ns | |
| HM51W17800S-7 | 70 ns | |
| HM51W17800LS-5 | 50 ns | 300-mil 28-pin plastic SOJ (CP-28DNA) |
| HM51W17800LS-6 | 60 ns | |
| HM51W17800LS-7 | 70 ns | |
| HM51W17800TT-5 | 50 ns | 400-mil 28-pin plastic TSOP II (TTP-28DA) |
| HM51W17800TT-6 | 60 ns | |
| HM51W17800TT-7 | 70 ns | |
| HM51W17800LTT-5 | 50 ns | 400-mil 28-pin plastic TSOP II (TTP-28DA) |
| HM51W17800LTT-6 | 60 ns | |
| HM51W17800LTT-7 | 70 ns | |
| HM51W17800TS-5 | 50 ns | 300-mil 28-pin plastic TSOP II (TTP-28DB) |
| HM51W17800TS-6 | 60 ns | |
| HM51W17800TS-7 | 70 ns | |
| HM51W17800LTS-5 | 50 ns | 300-mil 28-pin plastic TSOP II (TTP-28DB) |
| HM51W17800LTS-6 | 60 ns | |
| HM51W17800LTS-7 | 70 ns | |

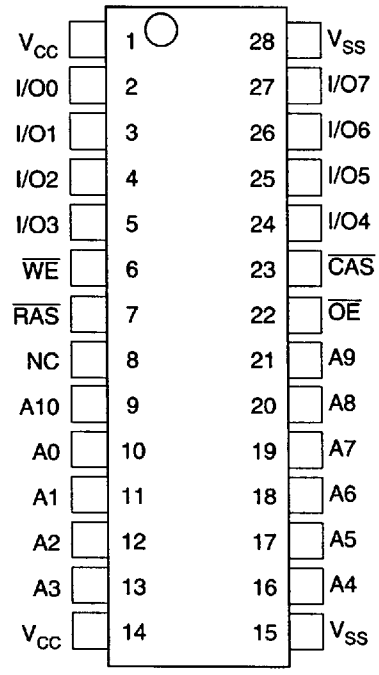
## Pin Arrangement

HM51W17800J/LJ Series
HM51W17800S/LS Series




(Top view)

HM51W17800TT/LTT Series
HM51W17800TS/LTS Series

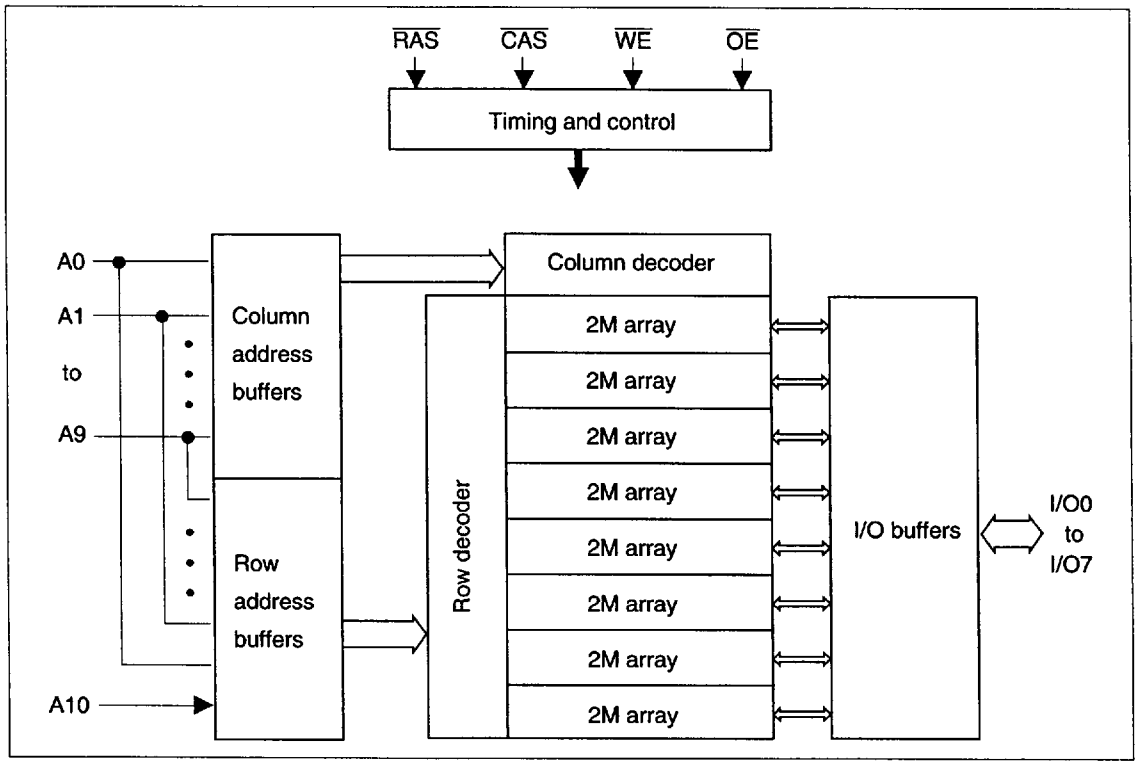



(Top view)

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A10 | Address input<br>Row/Refresh address A0 to A10<br>Column address A0 to A9 |
| I/O0 to I/O7 | Data input/data output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{CAS}$ | Column address strobe |
| $\overline{WE}$ | Read/Write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram




## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 to + 4.6 | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to + 4.6 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 1, 2 |
| Input high voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | –0.3 | — | 0.8 | V | 1 |

Notes: 1. All voltage referred to $V_{SS}$

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test conditions |
| Operating current*1, *2 | $I_{CC1}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | 2 | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$<br>Dout = High-Z |
| Standby current | | — | 1 | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | 150 | — | 150 | — | 150 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ – 0.2V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | 5 | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{CAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | 110 | — | 100 | — | 90 | mA | $t_{RC}$ = min |
| Fast page mode current*1, *3 | $I_{CC7}$ | — | 100 | — | 90 | — | 85 | mA | $t_{PC}$ = min |
| Battery backup current*4 (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | 400 | — | 400 | — | 400 | µA | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC}$ = 62.5 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | 250 | — | 250 | — | 250 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{CAS}$ ≤ 0.2V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ 4.6 V |
| Output leakage current | $I_{LO}$ | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vout ≤ 4.6 V<br>Dout = disable |
| Output high voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.
4. $\overline{CAS}$ = L (≤ 0.2 V) while $\overline{RAS}$ = L (≤ 0.2 V).

## Capacitance (Ta = 25°C, $V_{CC}$ = 3.3 V ± 0.3 V)

| Parameter | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output capacitance (Data-in, Data-out) | $C_{I/O}$ | — | 7 | pF | 1, 2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable Dout.

## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)[*1, *2, *18]

### Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + $C_L$ (100 pF) (Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles** (Common parameters)

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Random read or write cycle time | $t_{RC}$ | 90 | — | 110 | — | 130 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 30 | — | 40 | — | 50 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | 8 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 13 | 10000 | 15 | 10000 | 18 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | 0 | — | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | 8 | — | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | 0 | — | 0 | — | 0 | — | ns | |
| Column address hold time | $t_{CAH}$ | 8 | — | 10 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 18 | 37 | 20 | 45 | 20 | 52 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 13 | 25 | 15 | 30 | 15 | 35 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 13 | — | 15 | — | 18 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 50 | — | 60 | — | 70 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{OE}$ to Din delay time | $t_{OED}$ | 13 | — | 15 | — | 18 | — | ns | 5 |
| $\overline{OE}$ delay time from Din | $t_{DZO}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| $\overline{CAS}$ delay time from Din | $t_{DZC}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| Transition time (rise and fall) | $t_T$ | 3 | 50 | 3 | 50 | 3 | 50 | ns | 7 |

## Read Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | 50 | — | 60 | — | 70 | ns | 8, 9 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | 13 | — | 15 | — | 18 | ns | 9, 10, 17, |
| Access time from address | $t_{AA}$ | — | 25 | — | 30 | — | 35 | ns | 9, 11, 17, |
| Access time from $\overline{OE}$ | $t_{OEA}$ | — | 13 | — | 15 | — | 18 | ns | 9 |
| Read command setup time | $t_{RCS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | 0 | — | ns | 12 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 25 | — | 30 | — | 35 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | 25 | — | 30 | — | 35 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | 0 | — | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output data hold time from $\overline{OE}$ | $t_{OHO}$ | 3 | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | 13 | — | 15 | — | 15 | ns | 13 |
| Output buffer turn-off to $\overline{OE}$ | $t_{OEZ}$ | — | 13 | — | 15 | — | 15 | ns | 13 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | 13 | — | 15 | — | 18 | — | ns | 5 |

## Write Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Write command setup time | $t_{WCS}$ | 0 | — | 0 | — | 0 | — | ns | 14 |
| Write command hold time | $t_{WCH}$ | 8 | — | 10 | — | 15 | — | ns | |
| Write command pulse width | $t_{WP}$ | 8 | — | 10 | — | 10 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 13 | — | 15 | — | 18 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 13 | — | 15 | — | 18 | — | ns | |
| Data-in setup time | $t_{DS}$ | 0 | — | 0 | — | 0 | — | ns | 15 |
| Data-in hold time | $t_{DH}$ | 8 | — | 10 | — | 15 | — | ns | 15 |

### Read-Modify-Write Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Read-modify-write cycle time | $t_{RWC}$ | 131 | — | 155 | — | 181 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 73 | — | 85 | — | 98 | — | ns | 14 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 36 | — | 40 | — | 46 | — | ns | 14 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 48 | — | 55 | — | 63 | — | ns | 14 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | 13 | — | 15 | — | 18 | — | ns | |

### Refresh Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | 5 | — | 5 | — | 5 | — | ns | |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | 8 | — | 10 | — | 10 | — | ns | |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | 0 | — | 0 | — | 0 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | 8 | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | — | 5 | — | 5 | — | ns | |

### Fast Page Mode Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Fast page mode cycle time | $t_{PC}$ | 35 | — | 40 | — | 45 | — | ns | |
| Fast page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | 100000 | — | 100000 | — | 100000 | ns | 16 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | 30 | — | 35 | — | 40 | ns | 9, 17 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | 30 | — | 35 | — | 40 | — | ns | |

### Fast Page Mode Read-Modify-Write Cycle

| | | HM51W17800 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Fast page mode read-modify-write cycle time | $t_{PRWC}$ | 76 | — | 85 | — | 96 | — | ns | |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$ | 53 | — | 60 | — | 68 | — | ns | 14 |

### Refresh

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 32 | ms | 2048 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms | 2048 cycles |

**Self Refresh Mode** (L-version)

| Parameter | Symbol | HM51W17800L -5 Min | -5 Max | -6 Min | -6 Max | -7 Min | -7 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{RAS}$ pulse width (self refresh) | $t_{RASS}$ | 100 | — | 100 | — | 100 | — | µs | 19, 20, 21, 22 |
| $\overline{RAS}$ precharge time (self refresh) | $t_{RPS}$ | 90 | — | 110 | — | 130 | — | ns | |
| $\overline{CAS}$ hold time (self refresh) | $t_{CHS}$ | −50 | — | −50 | — | −50 | — | ns | |

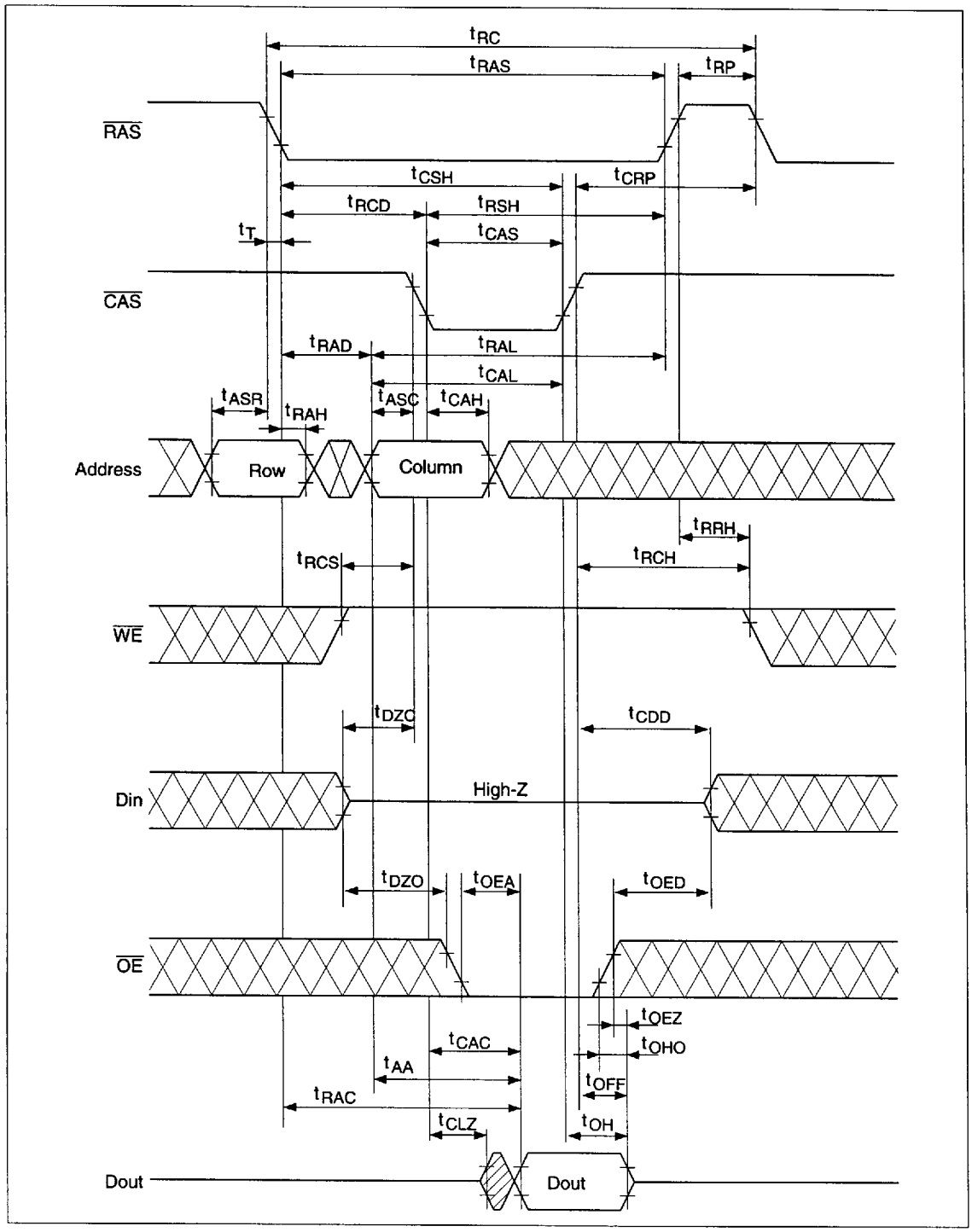
Notes: 1. AC measurements assume $t_T$ = 5 ns.

2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
4. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
5. Either $t_{OED}$ or $t_{CDD}$ must be satisfied.
6. Either $t_{DZO}$ or $t_{DZC}$ must be satisfied.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF. ($V_{OH}$ = 2.0 V, $V_{OL}$ = 0.8 V)
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.
13. $t_{OFF}$ (max) and $t_{OEZ}$ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. $t_{RASP}$ defines $\overline{RAS}$ pulse width in Fast page mode cycles.
17. Access time is determined by the longest among $t_{AA}$, $t_{CAC}$ and $t_{CPA}$.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. Please do not use $t_{RASS}$ timing, 10 µs $\leq t_{RASS} \leq$ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq$ 100 µs, then $\overline{RAS}$ precharge time should use $t_{RPS}$ instaed of $t_{RP}$.

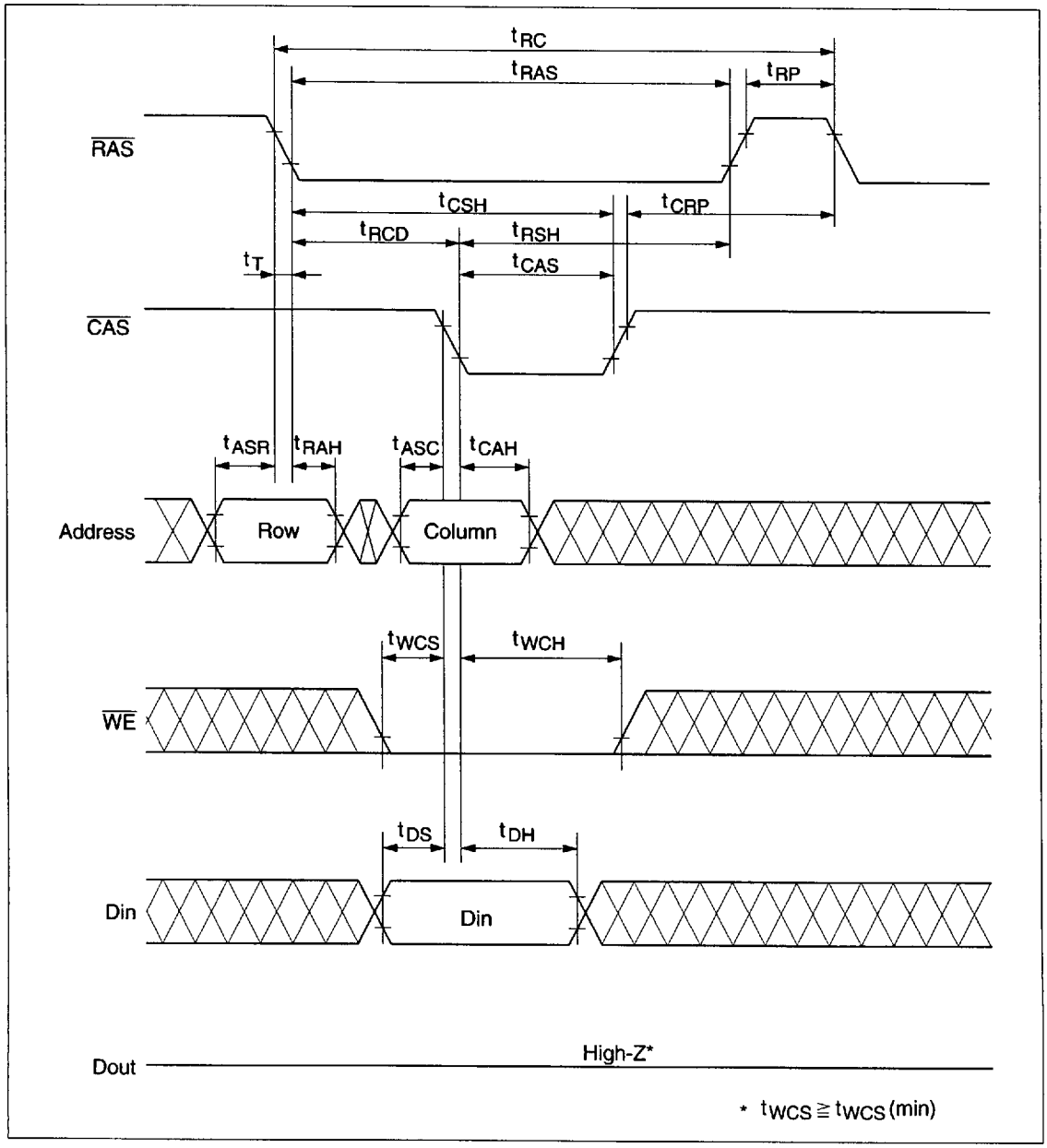
20. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycles, 2048 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
21. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
22. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
23. XXX: H or L (H: $V_{IH}$ (min) ≤ $V_{IN}$ ≤ $V_{IH}$ (max), L: $V_{IL}$ (min) ≤ $V_{IN}$ ≤ $V_{IL}$ (max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied $V_{IH}$ or $V_{IL}$.

## Timing Waveforms*[23]

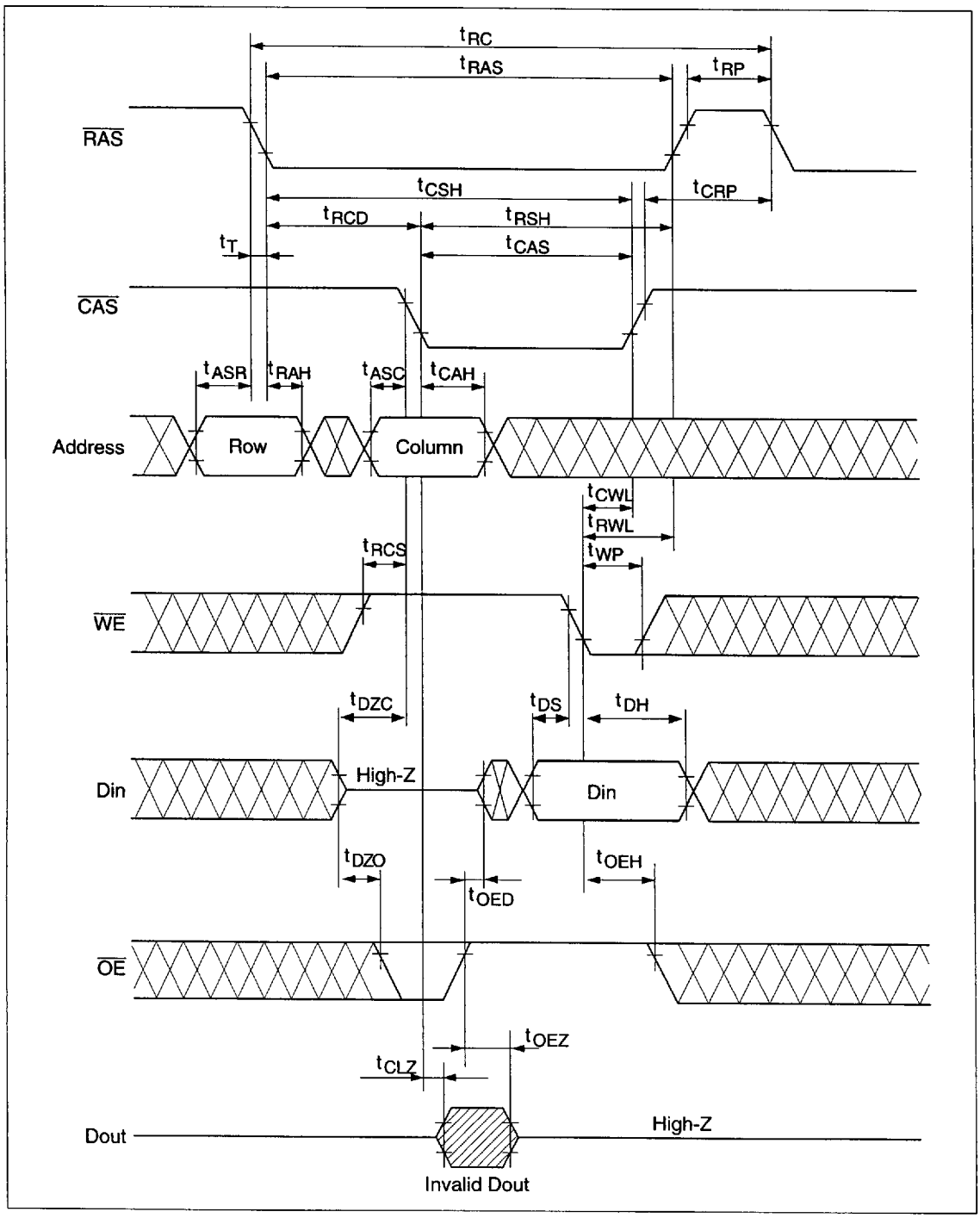
### Read Cycle



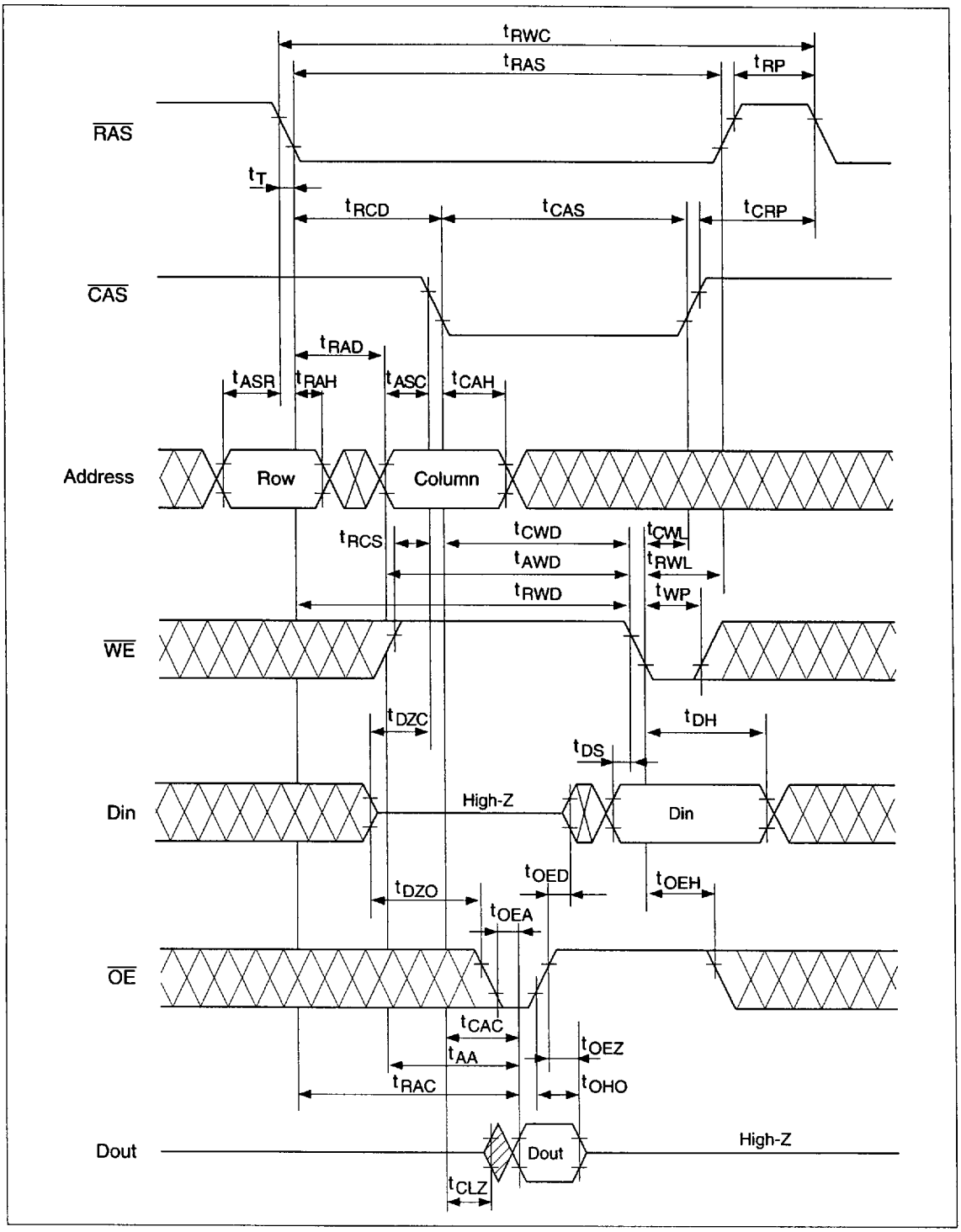

**Early Write Cycle**



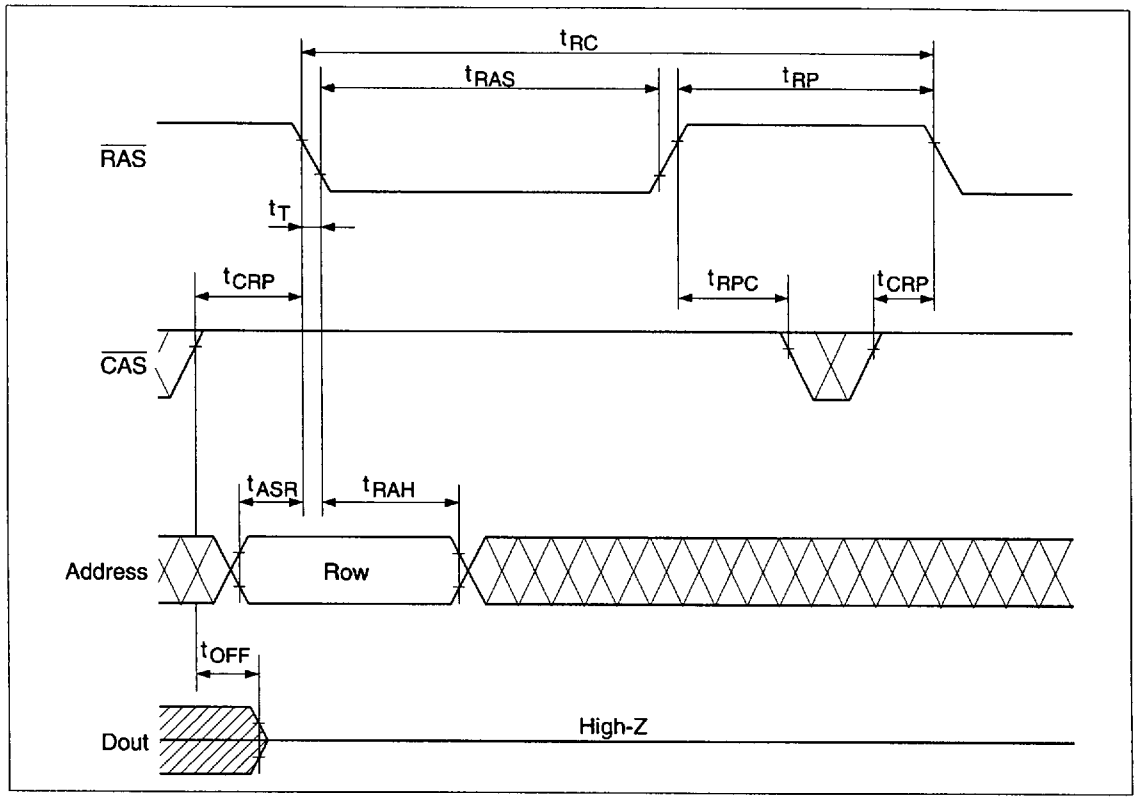
**Delayed Write Cycle*[18]**



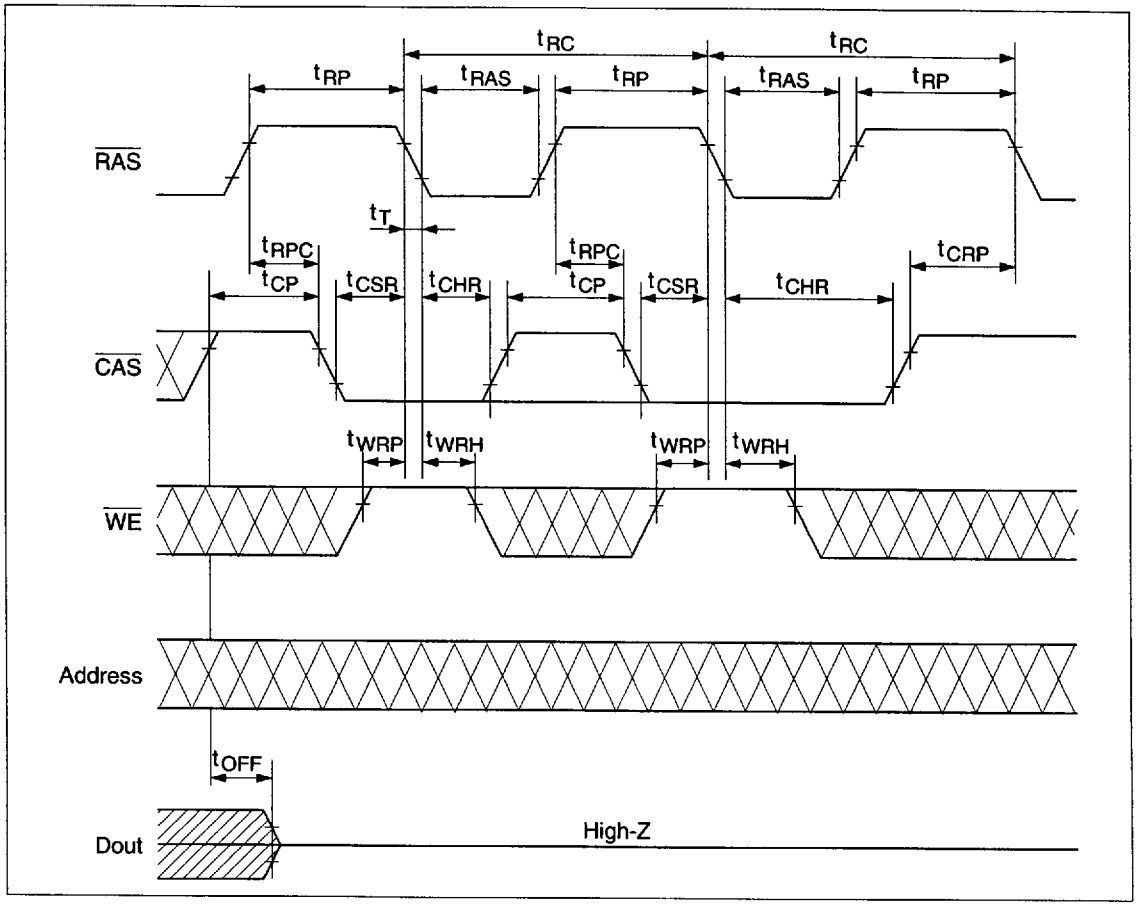

**Read-Modify-Write Cycle*[18]**



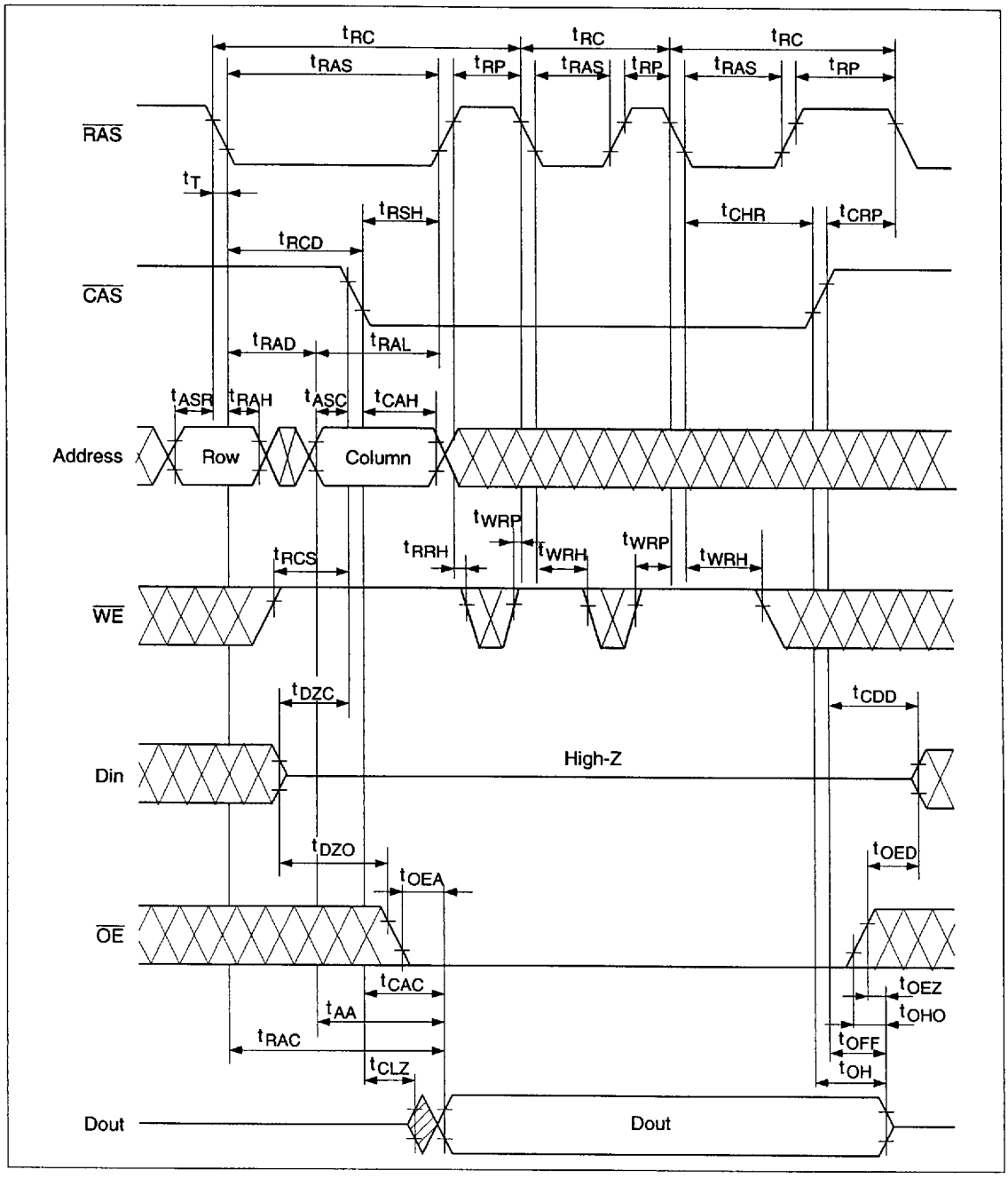

**RAS-Only Refresh Cycle**



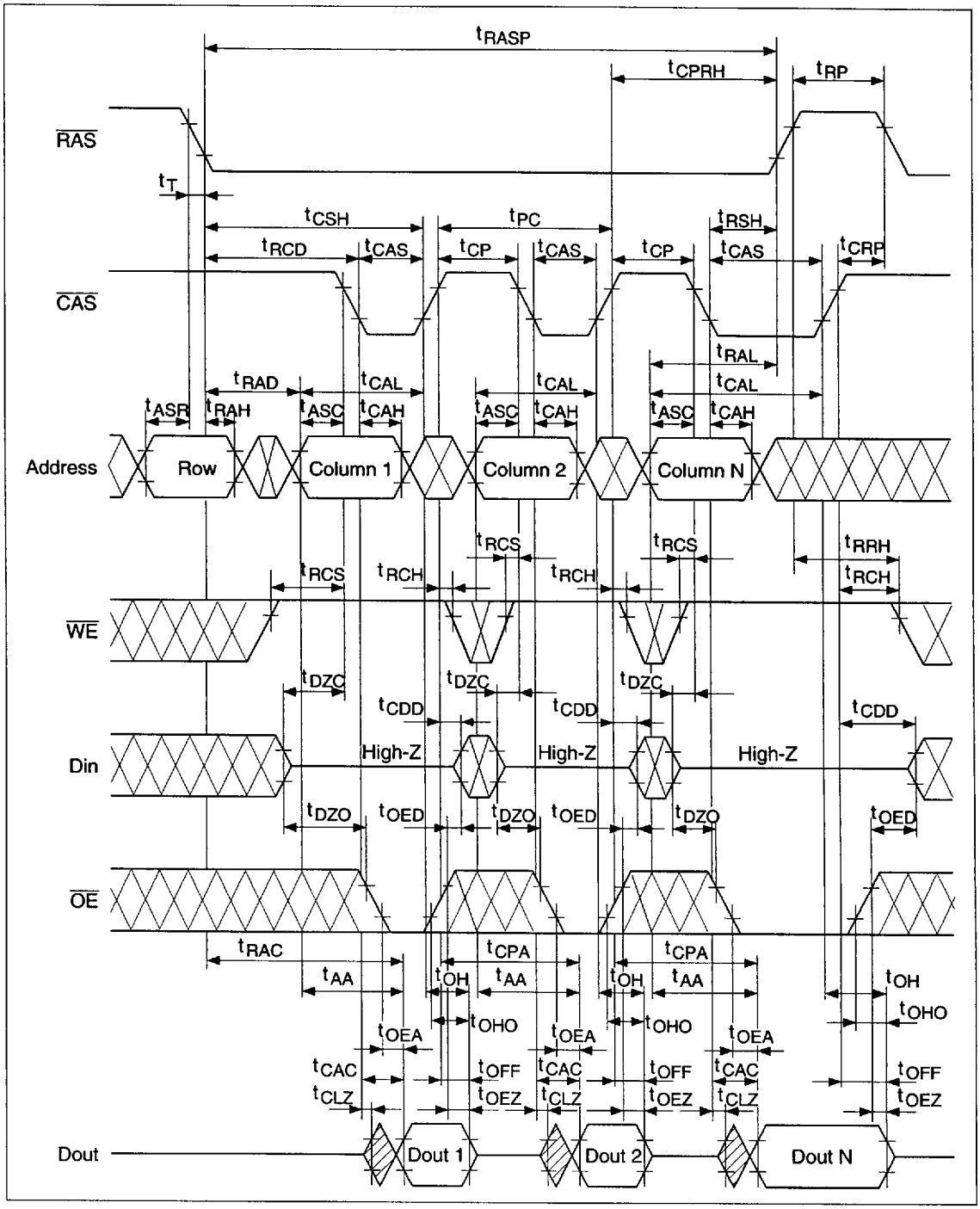
**$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle**



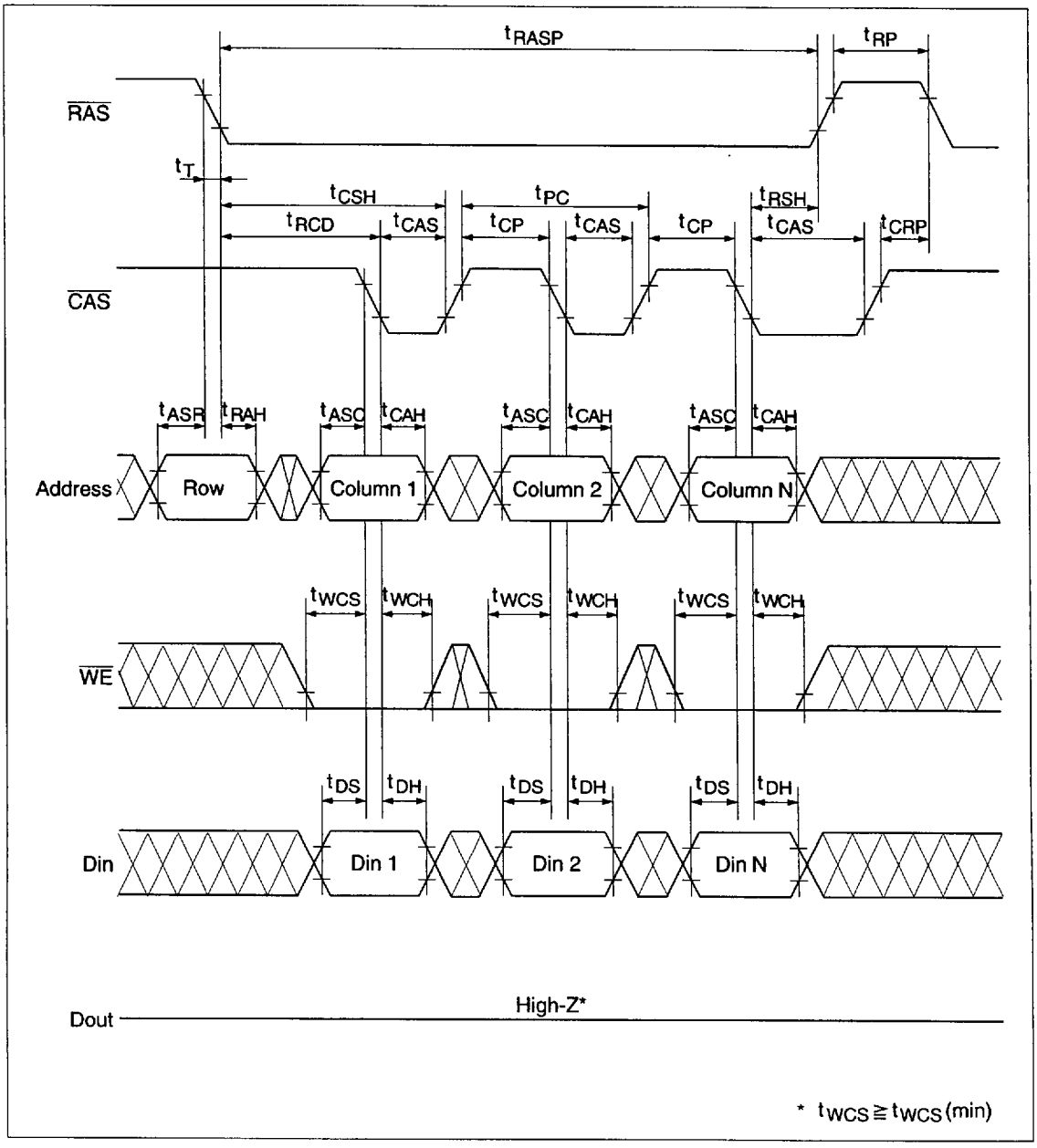
**Hidden Refresh Cycle**



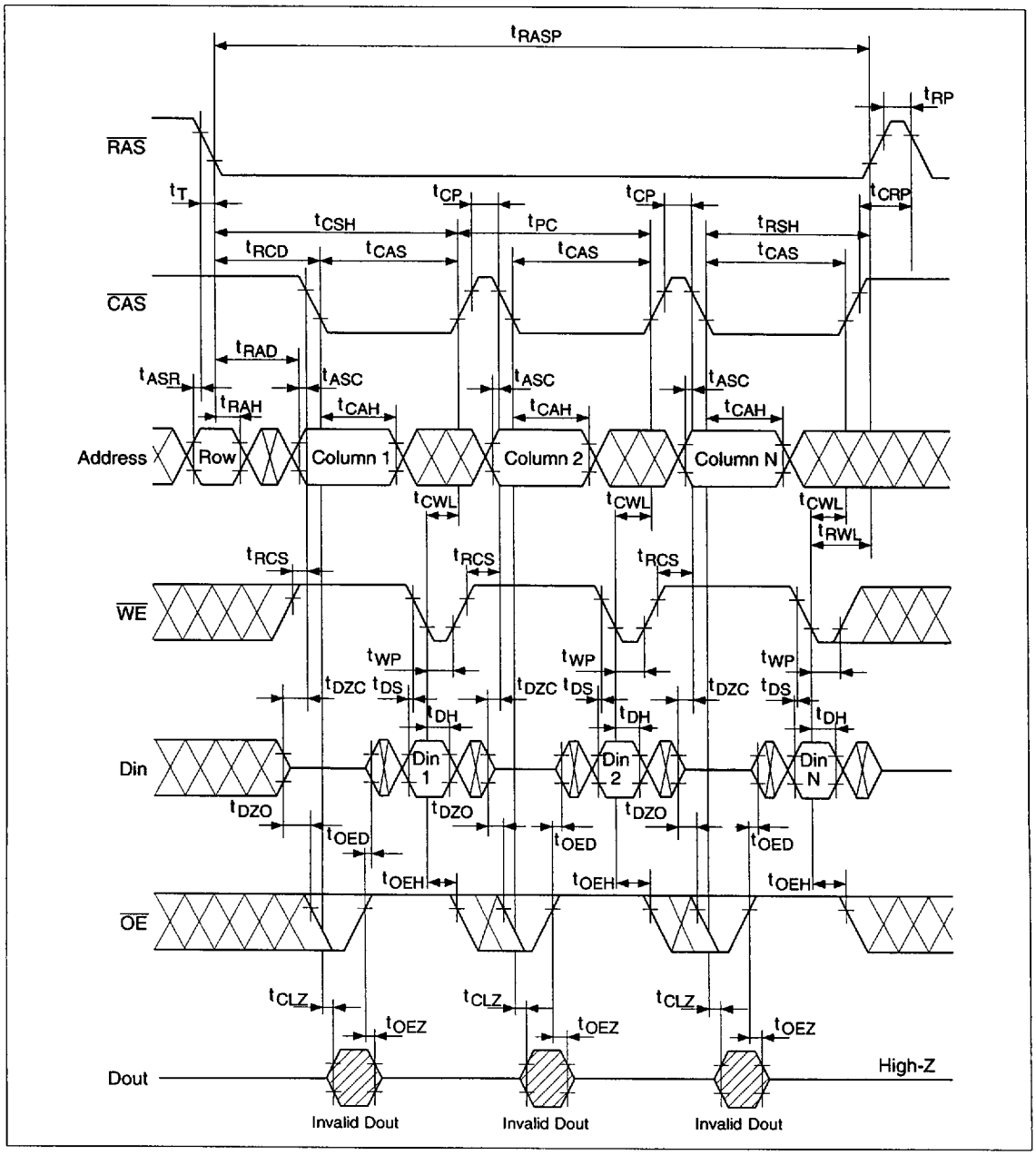

**Fast Page Mode Read Cycle**



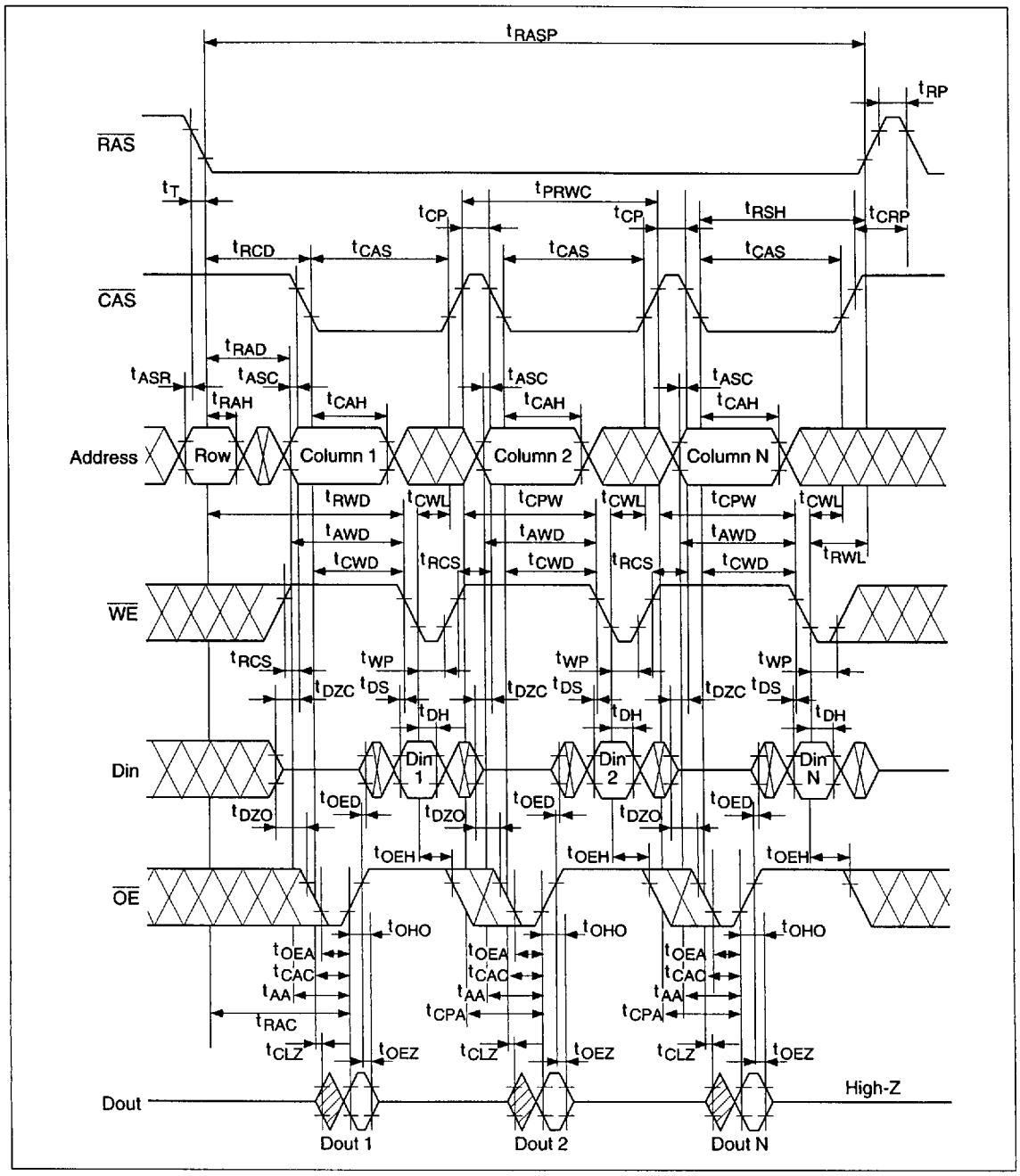

**Fast Page Mode Early Write Cycle**



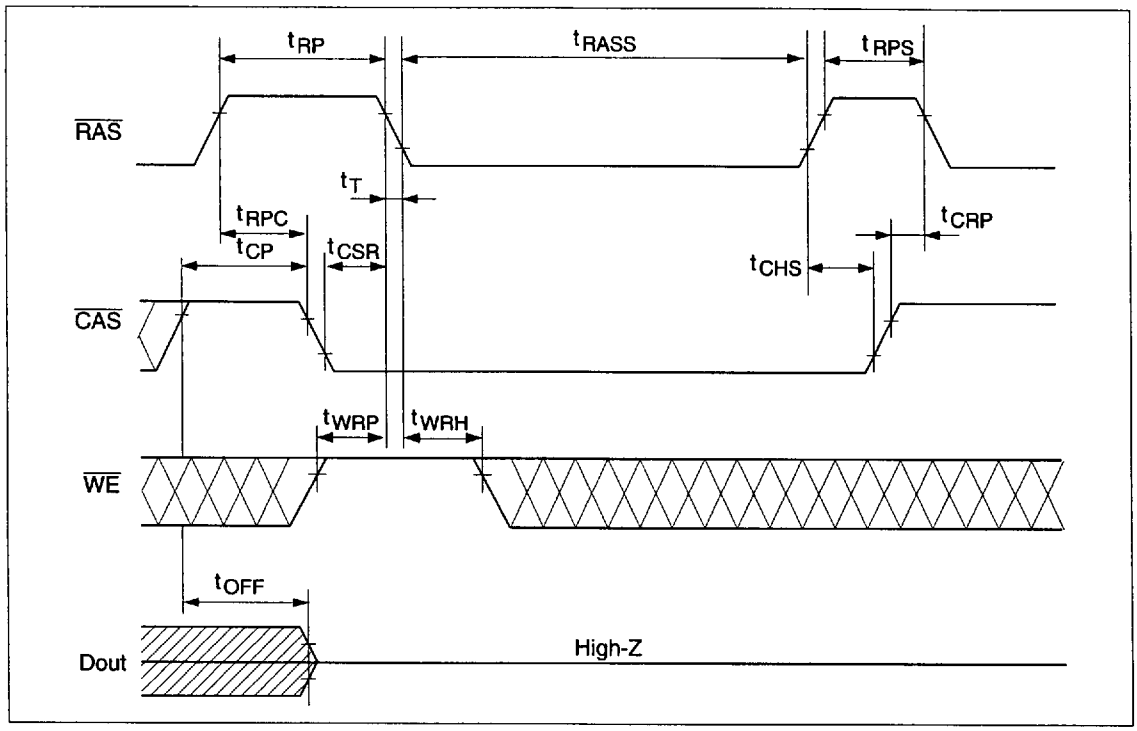
**Fast Page Mode Delayed Write Cycle*[18]**



**Fast Page Mode Read-Modify-Write Cycle*[18]**

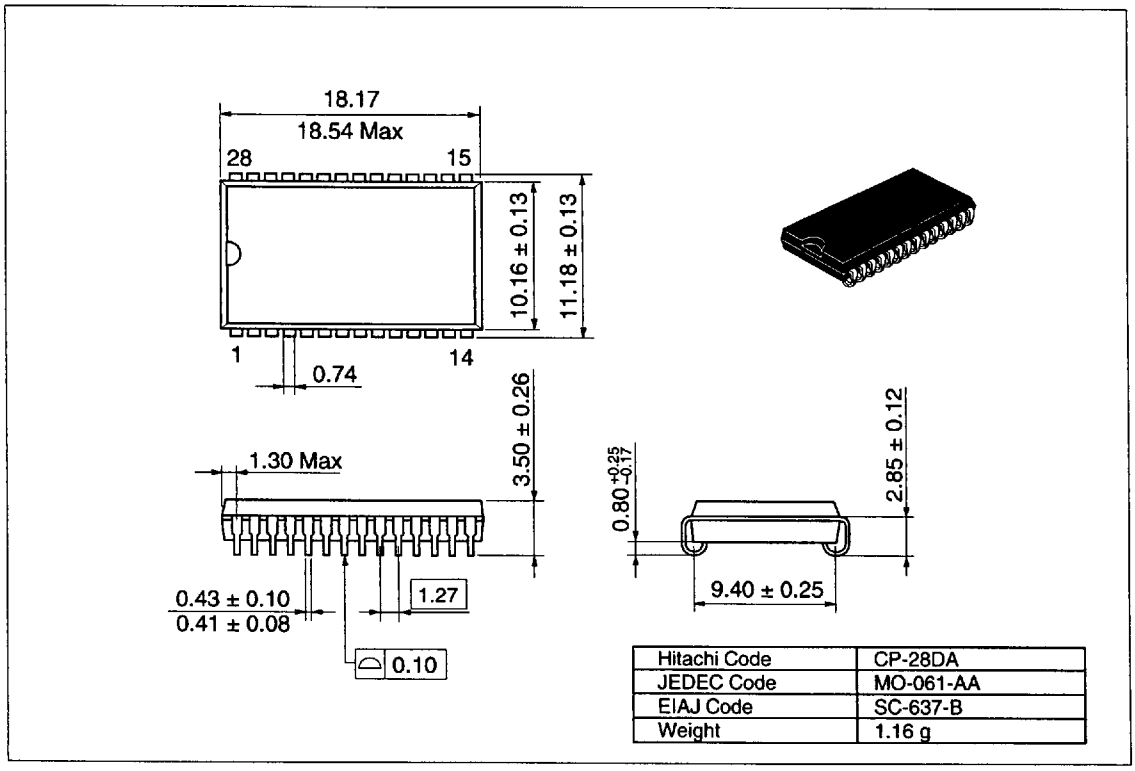


**Self Refresh Cycle** (L-version)*19, *20, *21, *22



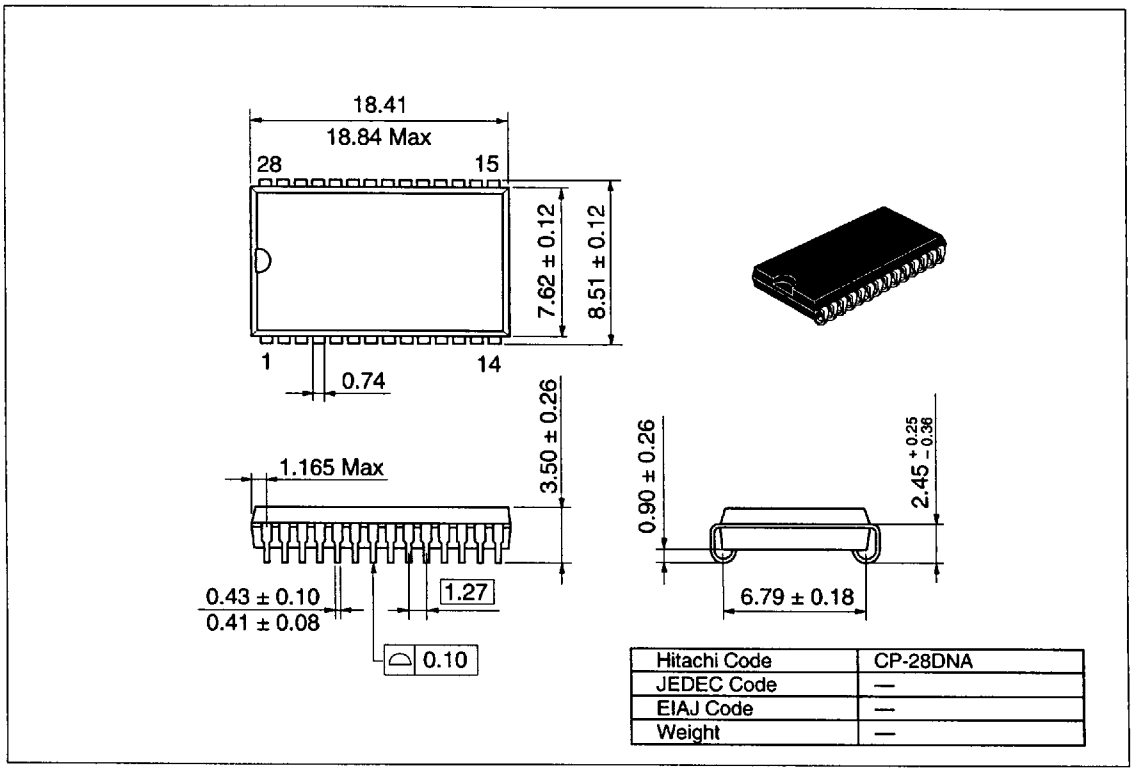
## Package Dimensions

**HM51W17800J/LJ Series** (CP-28DA)



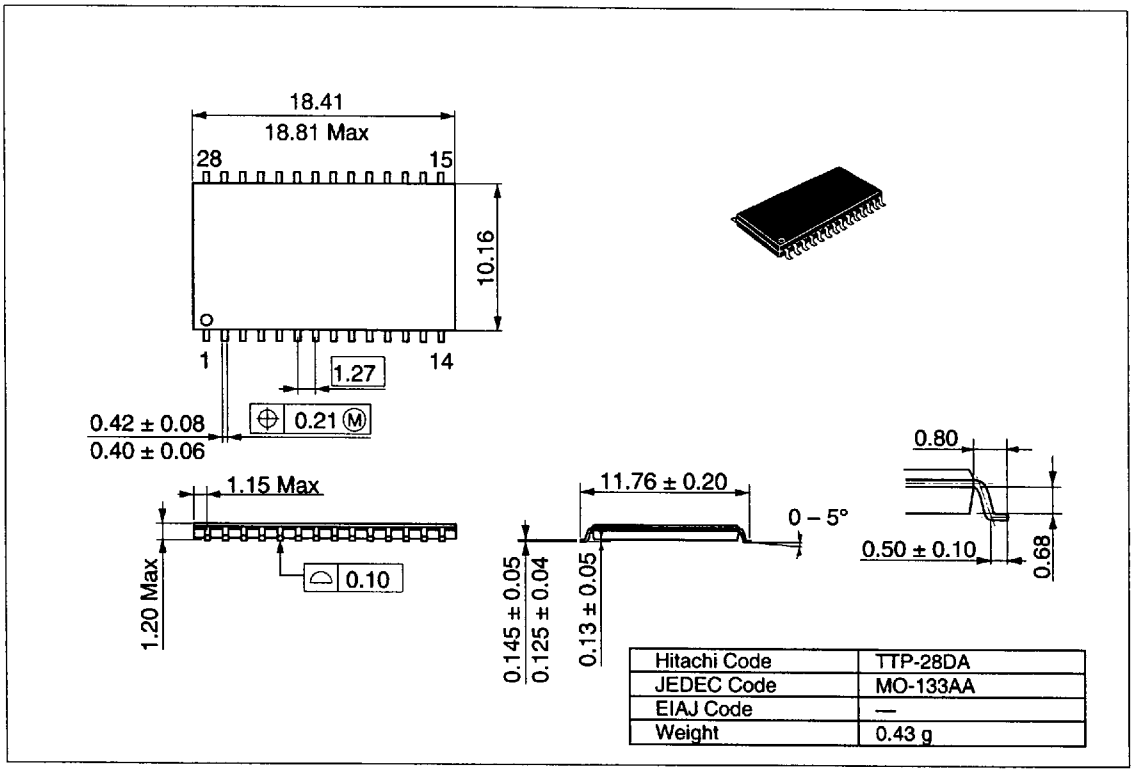

| | |
|---|---|
| Hitachi Code | CP-28DA |
| JEDEC Code | MO-061-AA |
| EIAJ Code | SC-637-B |
| Weight | 1.16 g |

**HM51W17800S/LS Series** (CP-28DNA)



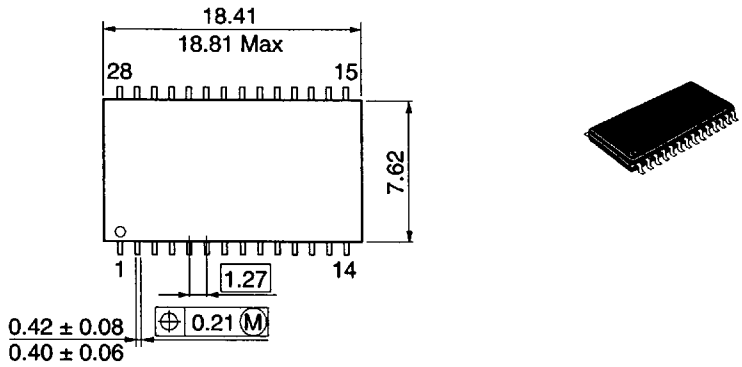

| | |
|---|---|
| Hitachi Code | CP-28DNA |
| JEDEC Code | — |
| EIAJ Code | — |
| Weight | — |

**HM51W17800TT/LTT Series** (TTP-28DA)




| | |
|---|---|
| Hitachi Code | TTP-28DA |
| JEDEC Code | MO-133AA |
| EIAJ Code | — |
| Weight | 0.43 g |

**HM51W17800TS/LTS Series** (TTP-28DB)




| | |
|---|---|
| Hitachi Code | TTP-28DB |
| JEDEC Code | — |
| EIAJ Code | — |
| Weight | — |

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## Revision Record

| Rev. | Date | Contents of Modification | Drawn by | Approved by |
|---|---|---|---|---|
| 1.0 | Sep. 30, 1996 | Initial issue | Y. Kasama | M. Mishima |
| 2.0 | Dec. 5, 1996 | Addition of HM51W17800-5 Series<br>Addition of HM51W17800S/LS Series (CP-28DNA)<br>Addition of HM51W17800TS/LTS Series (TTP-28DB)<br>Power dissipation (active)<br>432/396 mW(max) to 396/360/324 mW (max)<br>DC Characteristics<br>$I_{CC1}$ max: 120/110 mA to 110/100/90 mA<br>$I_{CC3}$ max: 120/110 mA to 110/100/90 mA<br>$I_{CC6}$ max: 120/110 mA to 110/100/90 mA<br>$I_{CC7}$ max: 100/90 mA to 100/90/85 mA<br>AC Characteristics<br>$t_{RRH}$ min: 0/0 ns to 5/5/5 ns<br>$t_{RPC}$ min: 0/0 ns to 5/5/5 ns | Y. Kasama | M. Mishima |
| 3.0 | Feb. 24, 1997 | AC Characteristics<br>$t_{RRH}$ min: 5/5/5 ns to 0/0/0 ns | | |