MN195001

Single-Chip Fax Engine LSI

■ Overview

The MN195001 reduces to a single chip CPU functions related to facsimile control, peripheral device control functions, and modem functions. The last include complete fax/modem support for the ITU-T G3 recommandations V.29, V.27ter, and V.21 Channels 1 and 2.

The MN195001 consists of the following blocks: digital signal processor (DSP), facsimile peripheral circuits, analog circuits, DTE interface, clock generator, and dual-port RAM. Changing the contents of an external ROM tailors the chip for a wide variety of facsimile applications.

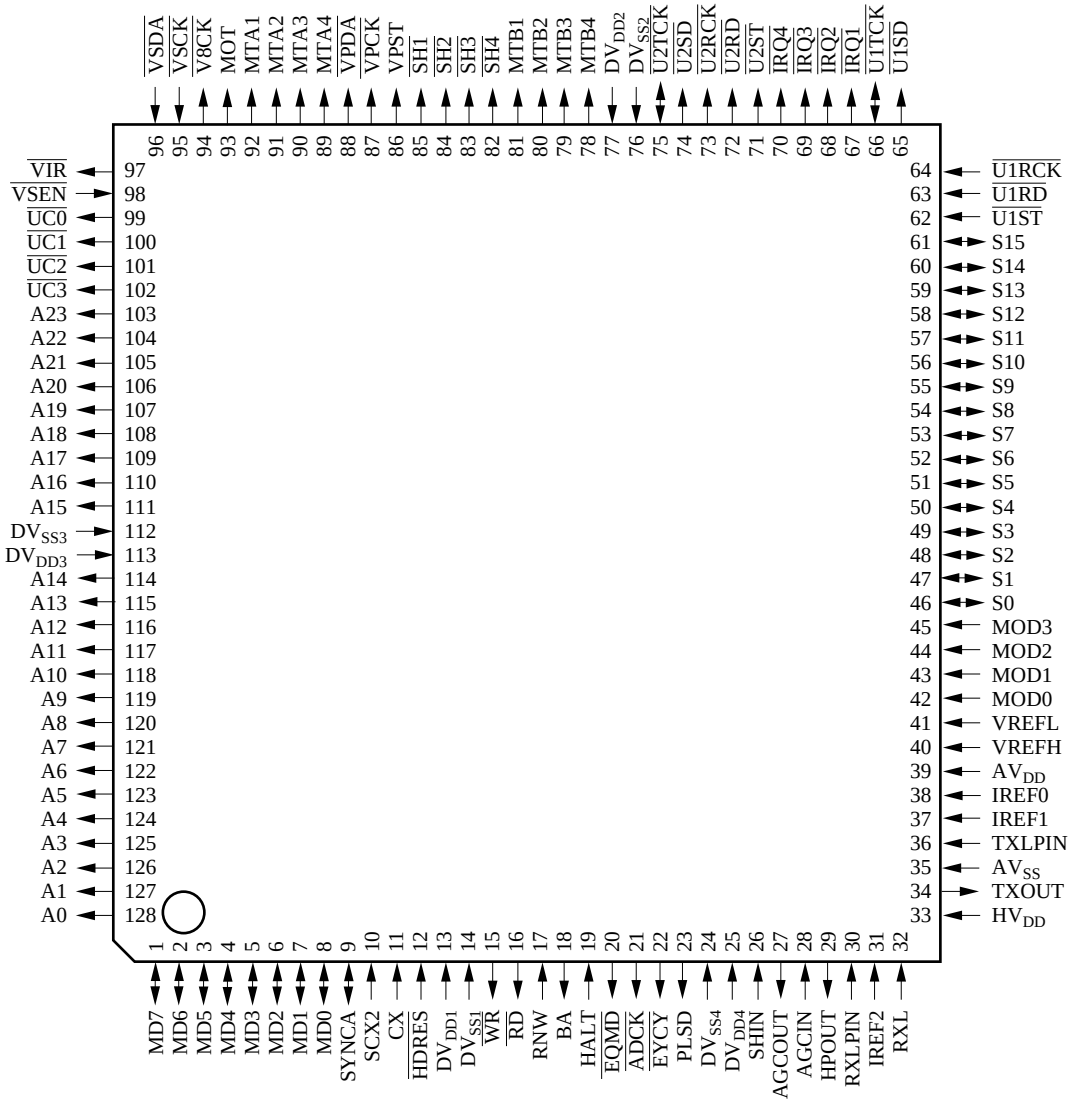
■ Features

- Digital signal processor (DSP) block
  - Micro ROM: 4096 × 32 bits
  - Data RAM: 512 × 16 bits × 2 sets
  - Machine cycle: 90 ns
  - Parallel multiplier:
    16 bits × 16 bits × → 32 bits
  - Arithmetic and logic unit (ALU): 32-bit
- Facsimile peripheral circuit block
  - Scanner/plotter interface
  - Two USART channels
  - Two motor control channels
  - One thermal head control channel
  - Programmable chip select
- Analog circuit block
  - Built-in 8-bit D/A converter, A/D converter, and filters
- DTE interface block
  - Built-in 8-bit I/O interface and serial interface
- Clock generator block
  - Sampling clock and baud rate clock generators
- Dual-port RAM block
  - 1024 × 8 bits
- Single 5 volt power supply

■ Applications

- Facsimile equipment

■ Pin Assignment



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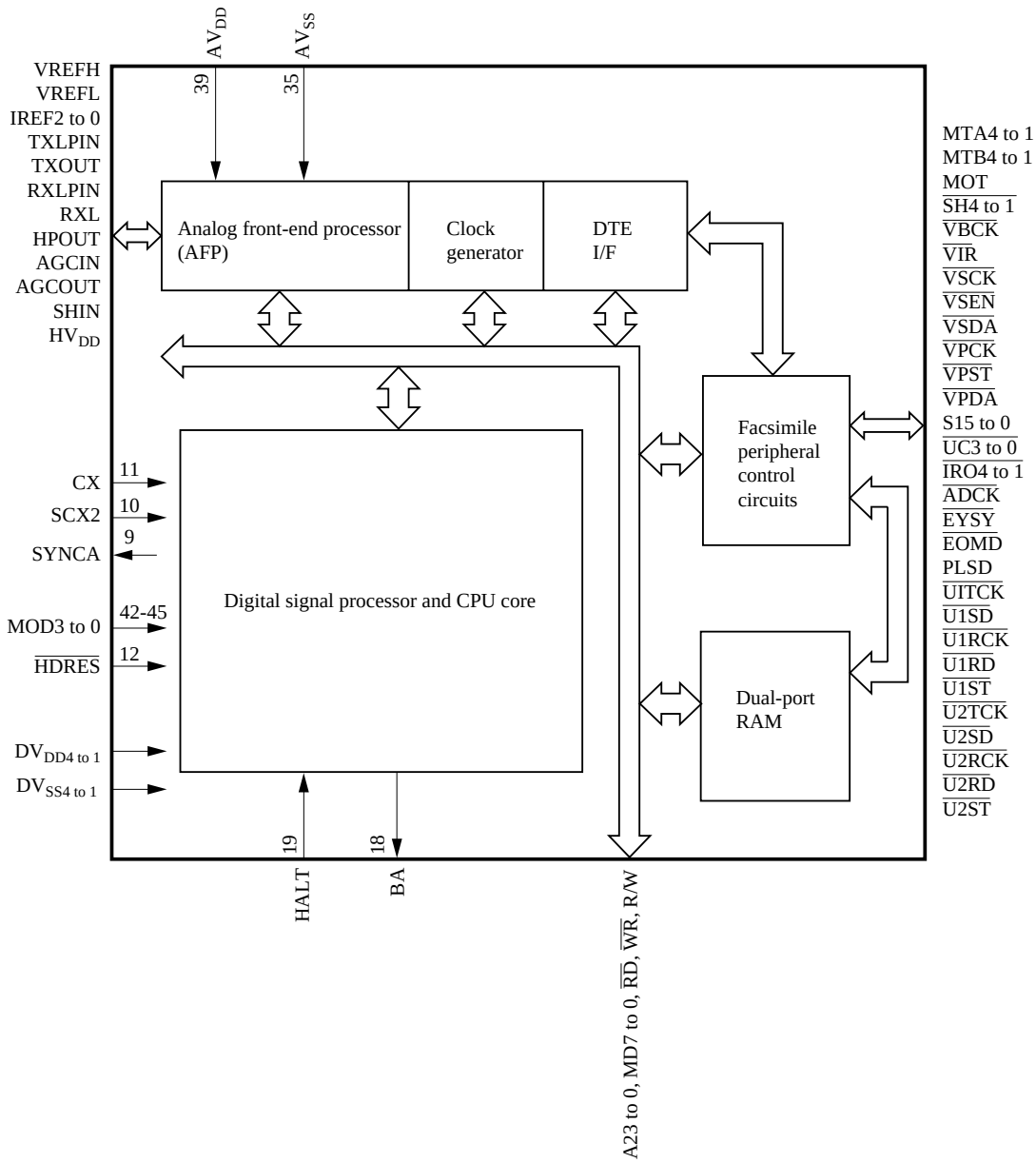
■ Block Diagram



■ Pin Descriptions

Functional Group	Symbol	Pin No.	I/O	Function Descreption
Memory Interface	A0 to 23	128 to 114, 111 to 103	O	External memory address bus
	MD0 to 7	8 to 1	I/O	External memory data bus
	$\overline{RD}$	16	O	External memory read signal
	$\overline{WR}$	15	O	External memory write signal
	R/W	17	I	External memory read/write control
Control Interface	CX	11	I	Basic clock input
	SCX2	10	I	Basic clock frequency selection
	SYNCA	9	O	System clock output
	$\overline{HDRES}$	12	I	Reset signal
	MOD0 to 3	42 to 45	I	Mode setting inputs
	HALT	19	I	HALT signal for internal digital signal processor
	BA	18	O	External memory bus available signal
Analog Interface	IREF0	38	AI	D/A converter input
	IREF1	37	AI	Reference voltage for transmit circuits
	TXLPIN	36	AI	Transmit low-pass filter input
	TXOUT	34	AO	Analog transmit signal output
	RXL	32	AI	Analog receive signal input
	IREF2	31	AI	Reference voltage for receive circuit
	RXLPIN	30	AI	Receive low-pass filter input
	HPOUT	29	AO	Receive high-pass filter output
	AGCIN	28	AI	Receive automatic gain control input
	AGCOUT	27	AO	Receive automatic gain control output
	SHIN	26	AI	A/D converter sample-and-hold circuit input
	VREFH	40	AI	A/D converter reference "H" level
	VREFL	41	AI	A/D converter reference "L" level
	PLSD	23	O	External amplifier gain control signal
Fax control Signals	SO to 15	46 to 61	I/O	General-purpose I/O port
	$\overline{UC0 \text{ to } 3}$	99 to 102	O	Programmable chip select
	$\overline{IRO1 \text{ to } 4}$	67 to 70	I	External interrupts
	$\overline{U1ST}$	62	I	USART (CH1) external synchronization clock
	$\overline{U1RD}$	63	I	USART (CH1) receive data
	$\overline{U1RCK}$	64	I	USART (CH1) receive clock
	$\overline{U1SD}$	65	O	USART (CH1) transmit data
	$\overline{U1TCK}$	66	I/O	USART (CH1) transmit clock
	$\overline{U2ST}$	71	I	USART (CH2) external synchronization clock
	$\overline{U2RD}$	72	I	USART (CH2) receive data
	$\overline{U2RCK}$	73	I	USART (CH2) receive clock
	$\overline{U2SD}$	74	O	USART (CH2) transmit data
	$\overline{U2TCK}$	75	I/O	USART (CH2) transmit clock
	$\overline{SH1 \text{ to } 4}$	85 to 82	O	Thermal head control signals
	MTA1 to 4	92 to 89	O	Motor A control signals

■ Pin Descriptions (continued)

Functional Group	Symbol	Pin No.	I/O	Function Description
Fax Control Signals	MTB1 to 4	81 to 78	O	Motor B control signals
	MOT	93	O	Motor synchronization signal
	$\overline{\text{VPST}}$	86	O	Plotter data clock
	$\overline{\text{VPCK}}$	87	O	Plotter synchronization burst clock
	$\overline{\text{VPDA}}$	88	O	Plotter data
	$\overline{\text{V8CK}}$	94	O	Scanner clock
	$\overline{\text{VSCK}}$	95	I	Scanner data input clock
	$\overline{\text{VSDA}}$	96	I	Scanner data
	$\overline{\text{VIR}}$	97	O	Scanner input ready
	$\overline{\text{VSEN}}$	98	I	Scanner data input enable
EYE I/F	$\overline{\text{ADCK}}$	21	O	Eye pattern data clock
	$\overline{\text{EYSY}}$	22	O	Eye pattern data synchronization signal
	$\overline{\text{EQMD}}$	20	O	Eye pattern data
Power Supply Interface	$DV_{DD1\ to\ 4}$	13, 77, 114, 25	DP	Power supply for digital circuits +5 V
	$DV_{SS1\ to\ 4}$	14, 76, 112, 24	DP	Power supply for digital circuits GND
	AV_{DD}	39	AP	Power supply for analog circuits +5 V
	AV_{SS}	35	AP	Power supply for analog circuits GND
	HV_{DD}	33	AO	HVDD output

■ Package Dimensions (Unit: mm)

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