RTL

Introduction to Resistor Transistor Logic (RTL)

RTL circuits use resistor as the input network and transistors as switching device for logical operations. Thereby, it is named as Resistor Transistor Logic circuit

Features:

1. Resistor Transistor Logic was used in the construction of the first digital integrated circuits.

2. It requires minimum number of transistors

3. It is a saturated logic (operates either cutoff or saturation).

4. Input variables are applied via base resistor of the transistors. The values were chosen so that the inputs would depending upon voltage levels, either cut off or saturation of the transistor.

5. The collector of the transistors are tied together with a common resistor to the V_{cc} supply.

6. The circuit uses common emitter configuration of transistor.

Disadvantages:

1. relatively slow speed.

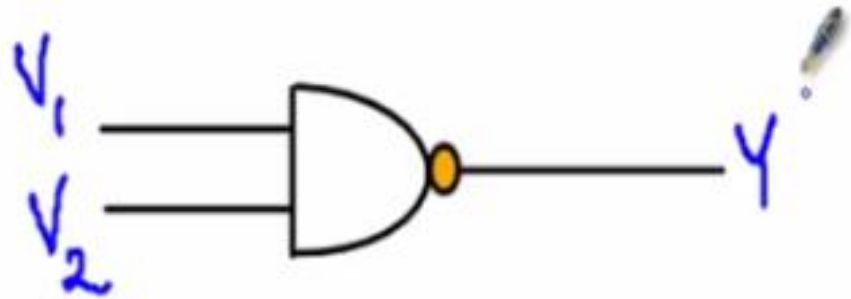
2. low fan-in and fan-out of 3

3. poor noise immunity or low noise margin

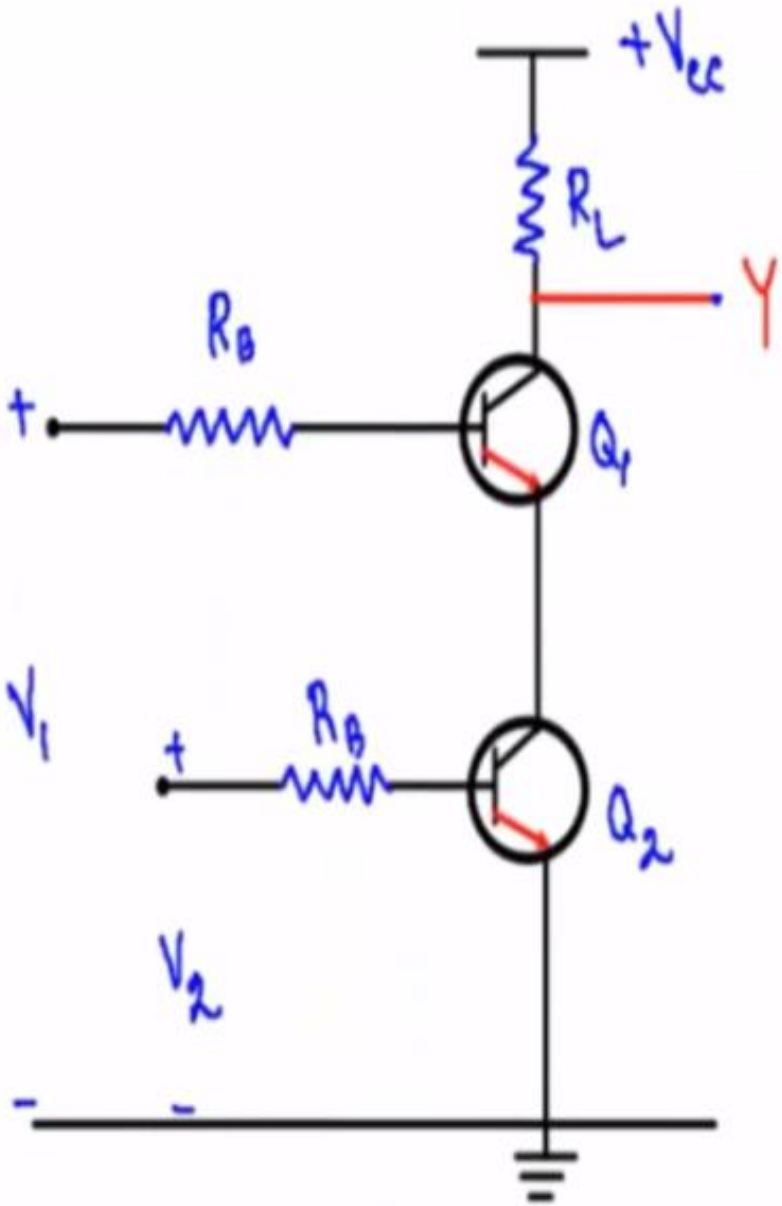
4. expensive since resistors are required to be fabricated

5. cannot operate at speed above 4 MHz

RTL NAND Gate

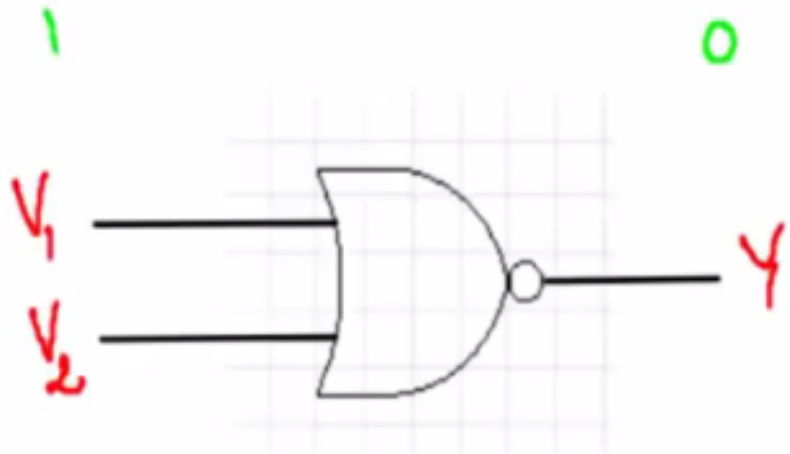


V_1	V_2	Y
0	0	1
0	1	1
1	0	1
1	1	0

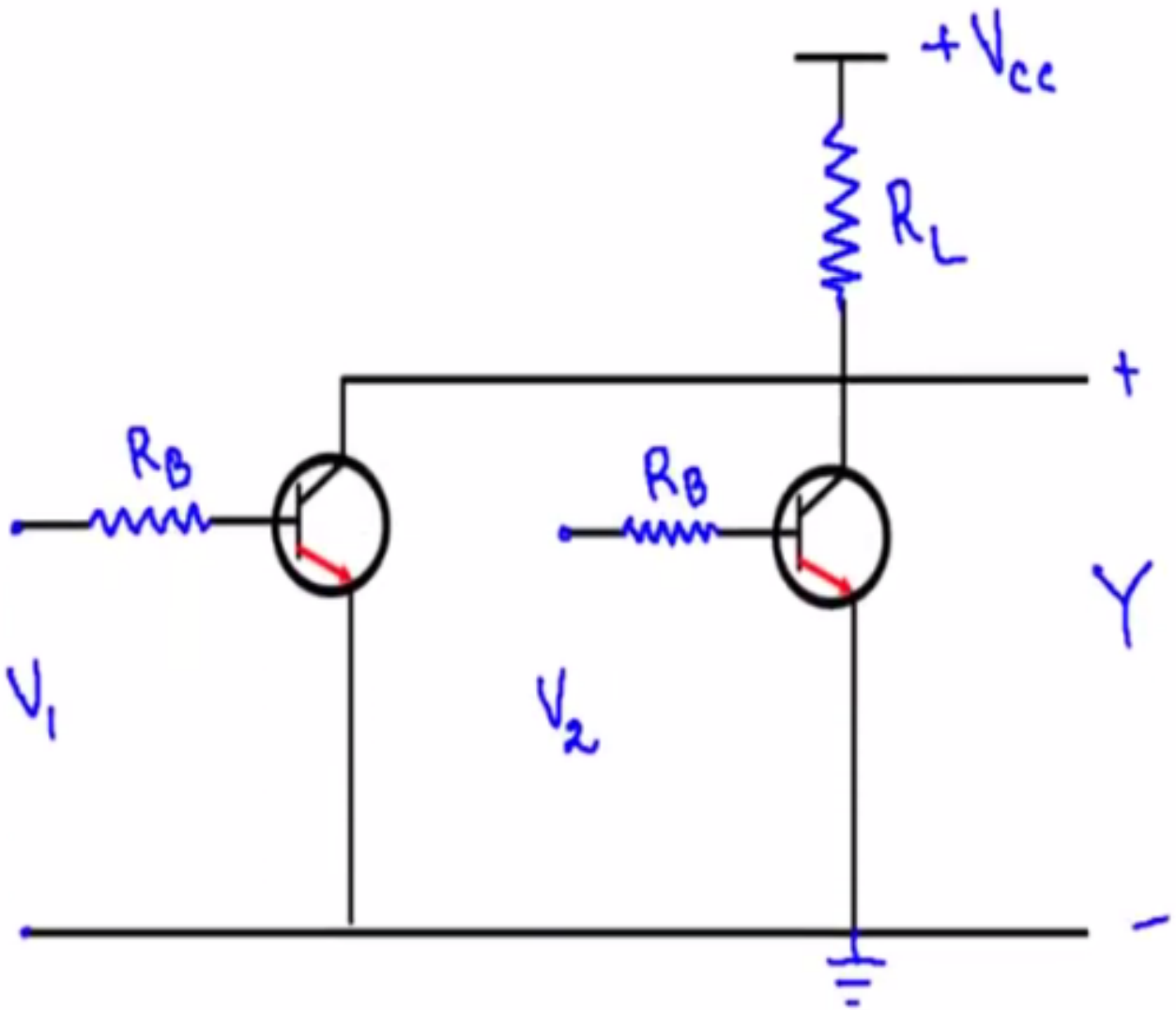


V_1	V_2	Y
0	0	1
0	1	1
1	0	1
1	1	0

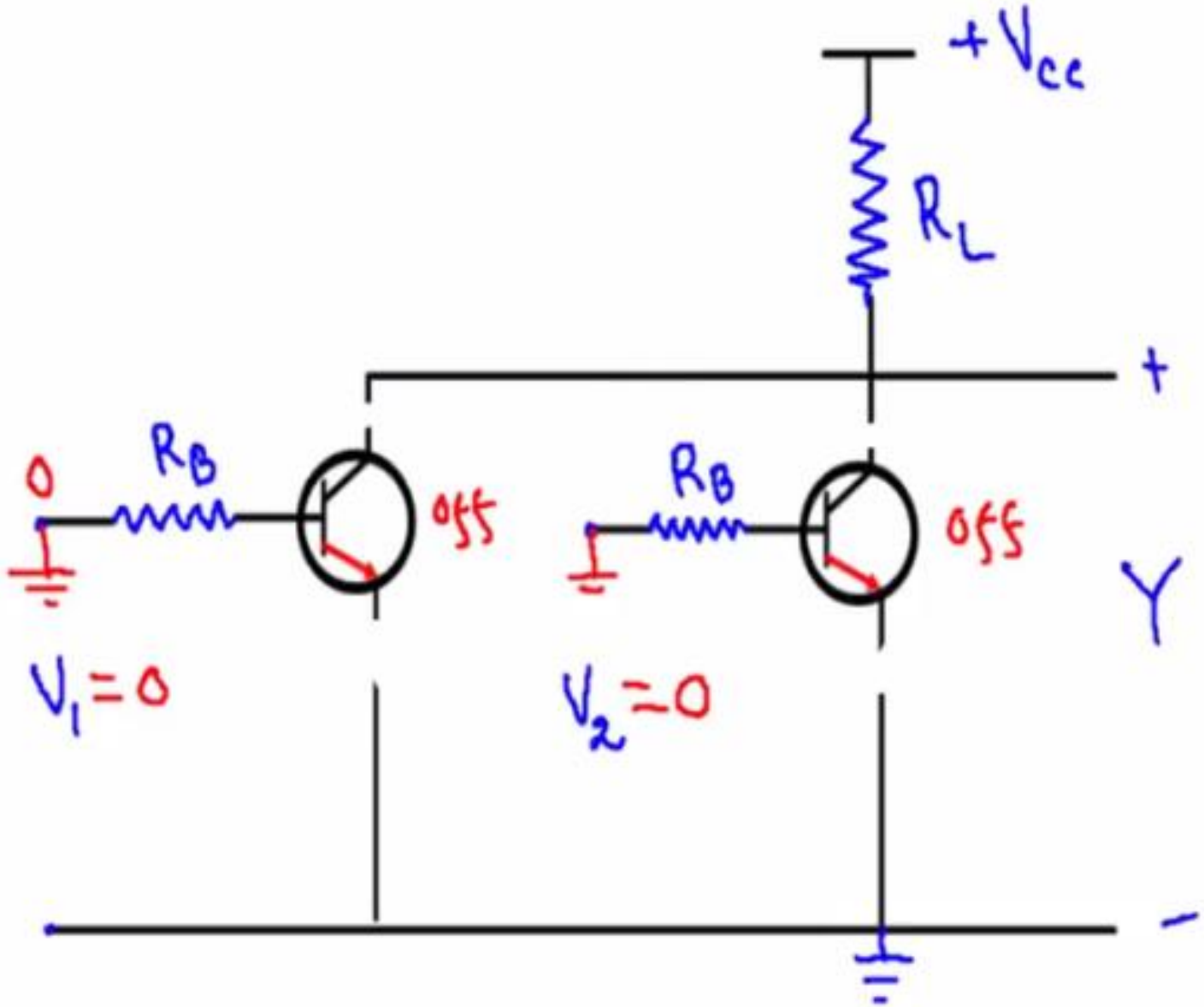
RTL NOR Gate



V_1	V_2	Y
0	0	1
0	1	0
1	0	0
1	1	0



V_1	V_2	Y
0	0	1
0	1	0
1	0	0
1	1	0


+Vcc
RL
+
RB
0
off
RB
off
Y
V1 = 0
V2 = 0
-

DTL

Introduction to DTL logic Family

Diode transistor logic circuits use diodes as input network and transistor as switching devices. Thats why this circuit is known as Diod transistor logic.

Features:

1. It consists of diodes, resistors and transistors.

2. It was the next family to be introduced after RTL.

3. It is a saturated logic circuit that means it operates between cut-off and saturation region.

4. Comparatively better noise immunity.

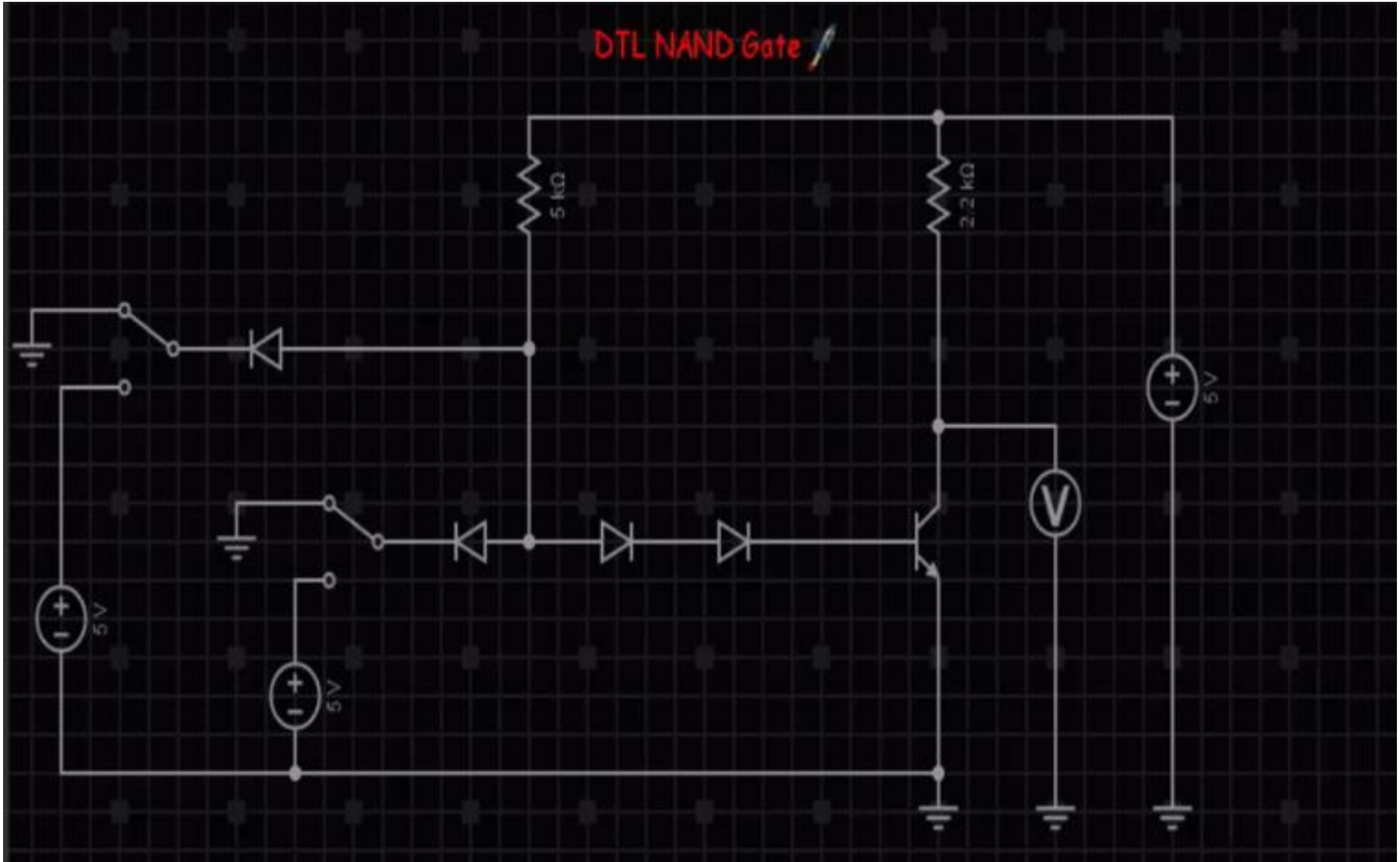
5. A fan out of 5.

Disadvantages:

1. Relatively lower speed.

2. Propagation delay of 30 nS.

As DTL gates use saturated logic, when transistor is in saturation base terminal is flooded with minority carriers. When it comes out of saturation (off), it takes sometime for the minority carriers to leave the base terminal. This is why there is a propagation delay in DTL circuits


DTL NAND Gate
5 kΩ
2.2 kΩ
5V
5V
5V
V

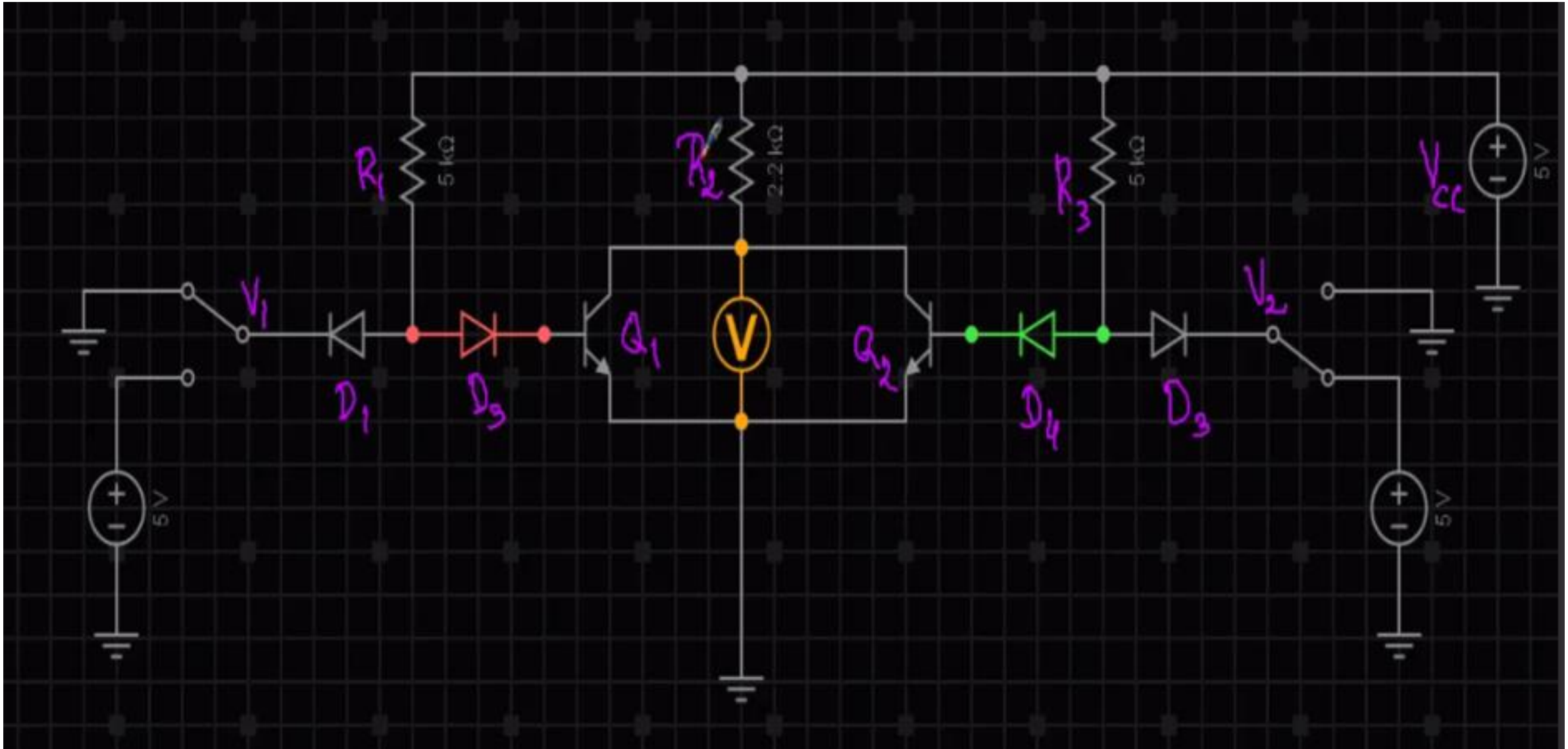
DTL NAND Gate

$$V_x = V_{D_3} + V_{D_4} + V_{BE}$$

$$= 0.7 + 0.7 + 0.8$$

$$\simeq 2.2V$$

DTL NOR Gate



DCTL

Introduction to Direct Coupled Transistor Logic

Direct coupled transistor logic that means inputs are directly coupled to the base terminals of the transistors without any base resistors.

Features:

1. It is a modified version of RTL logic circuits. Remove the base resistors R_B, we will get DCTL circuit

2. Circuit uses transistors as switching elements which requires low voltages to operate the logic circuits.

3. DCTL circuit has fast switching speed.

4. DCTL circuits use

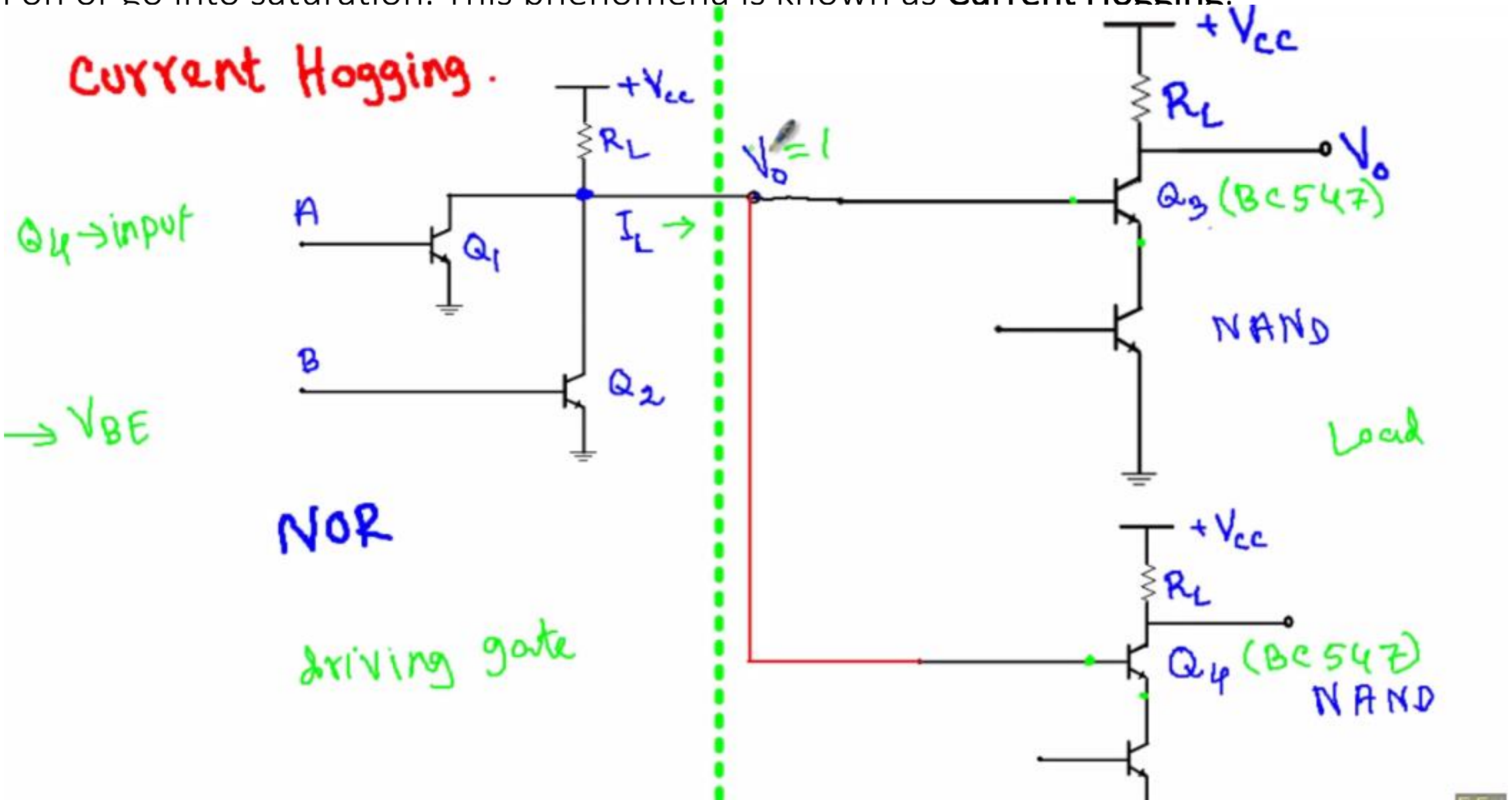
   0.8V (V_{BEsat}) as logic 1
   0.2V (V_{CEsat}) as logic 0

Disadvangtages:

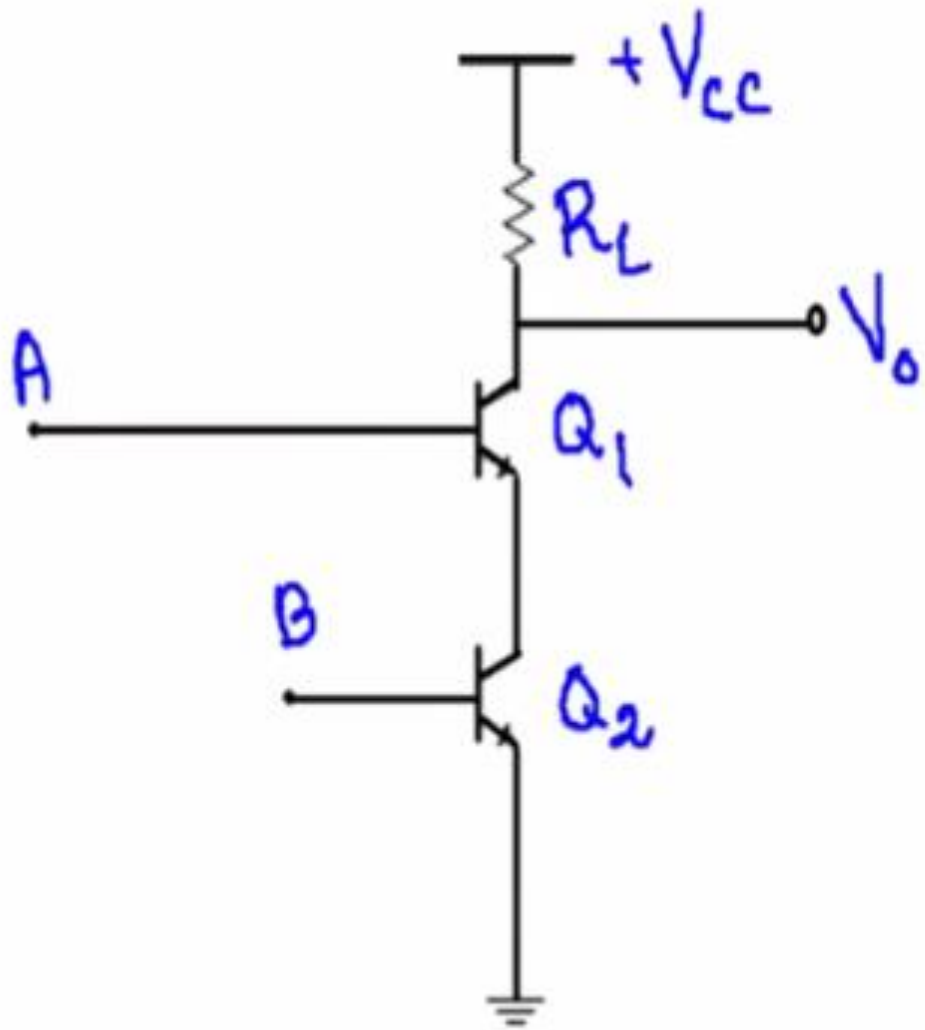
1. Separation of logic 1 and logic 0 voltage levels = logic swing = $V_{BEsat} - V_{CEsat}$ = (0.8 - 0.2) = 0.6V so noise margin for DCTL is very poor

2. DCTL circuits suffer from current hogging.

When output of one **DCTL** gate drives several base terminals of other **DCTL** gates, the transistor with lowest B-E junction voltage will go into saturation first. This prevents other transistors to turn on or go into saturation. This phenomena is known as **Current Hogging**.



DCTL NAND Gate



TTL

Introduction to Transistor Transistor Logic

TTL - Transistor Transistor Logic

Features:

1. It is a saturated logic.

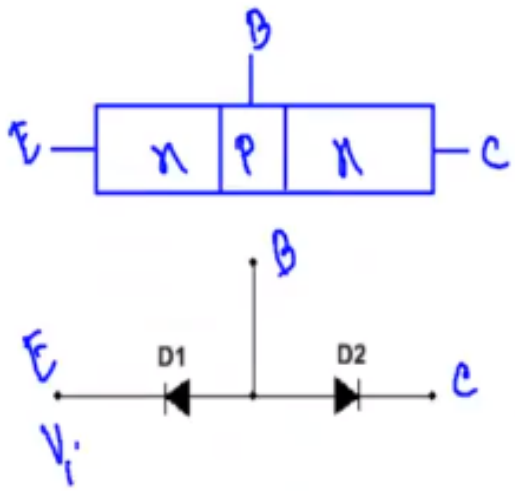
2. It uses multiemitter transistor at input which eliminates the need of input diodes like DTL.

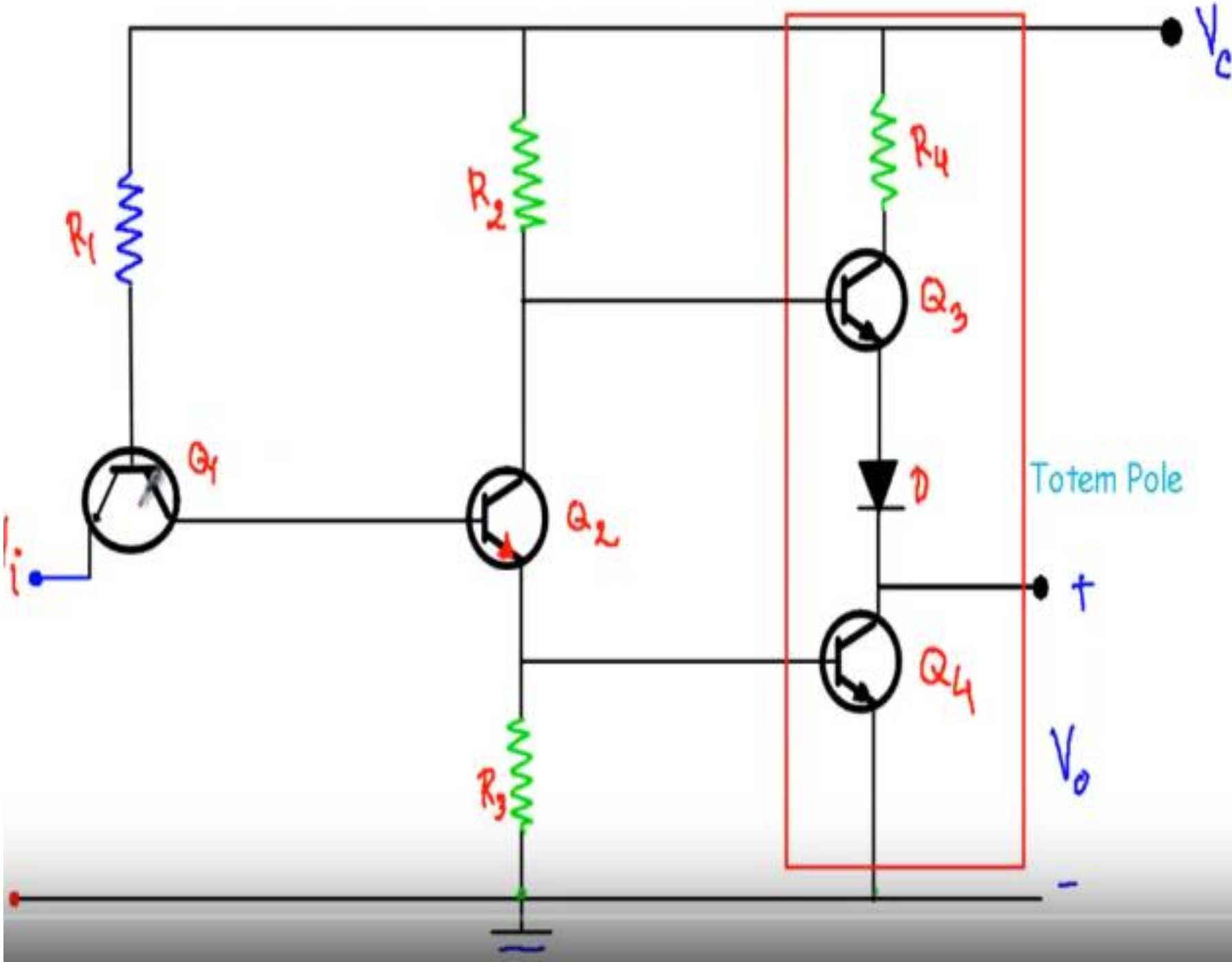
3. The number of emitters will be equal to the number of emitter terminals (limited to 8).

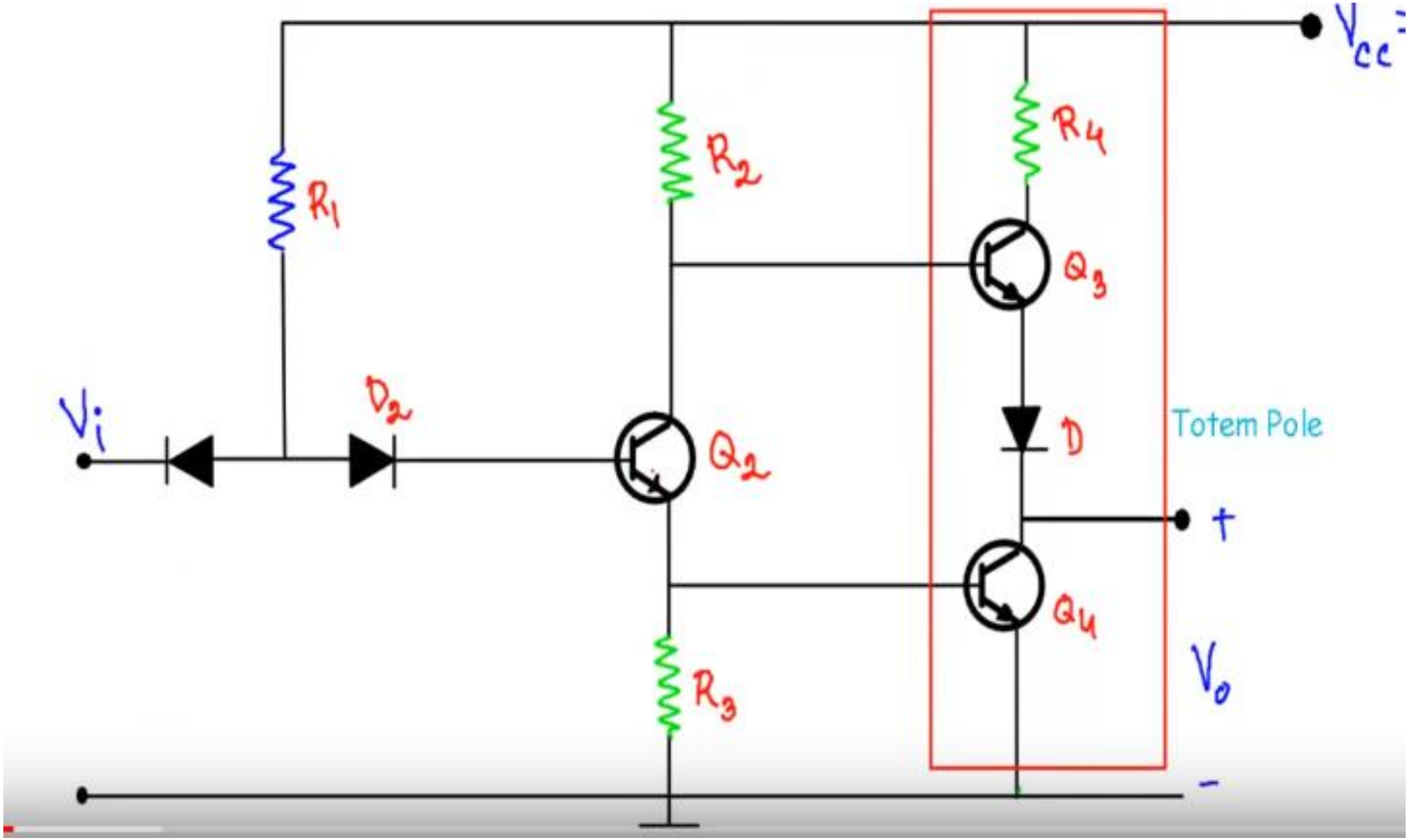
4. As we don't need the diodes at input, this reduces silicon chip area.

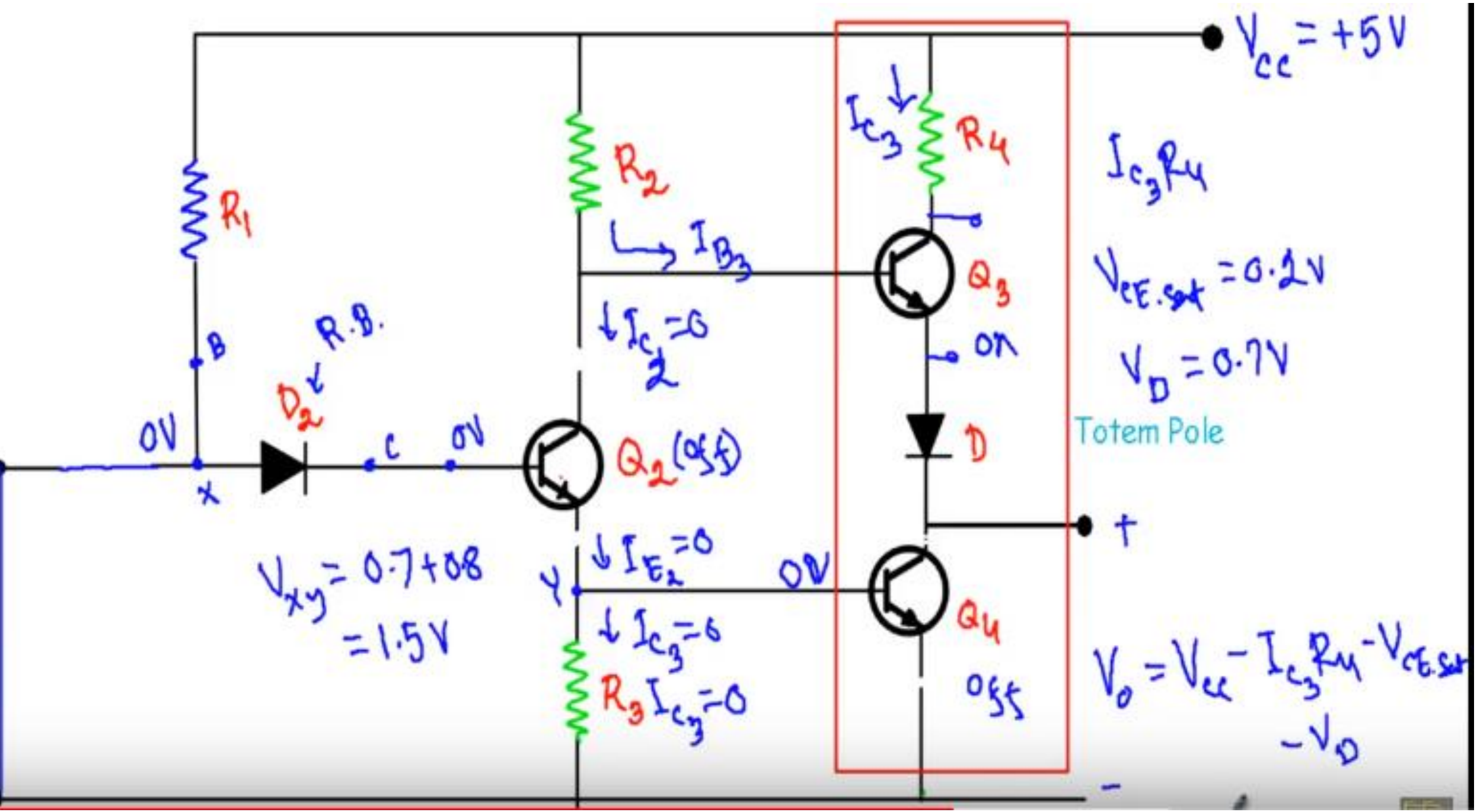
5. Output structure can be classified as totem pole, open collector, and tristate structure

TTL Inverter

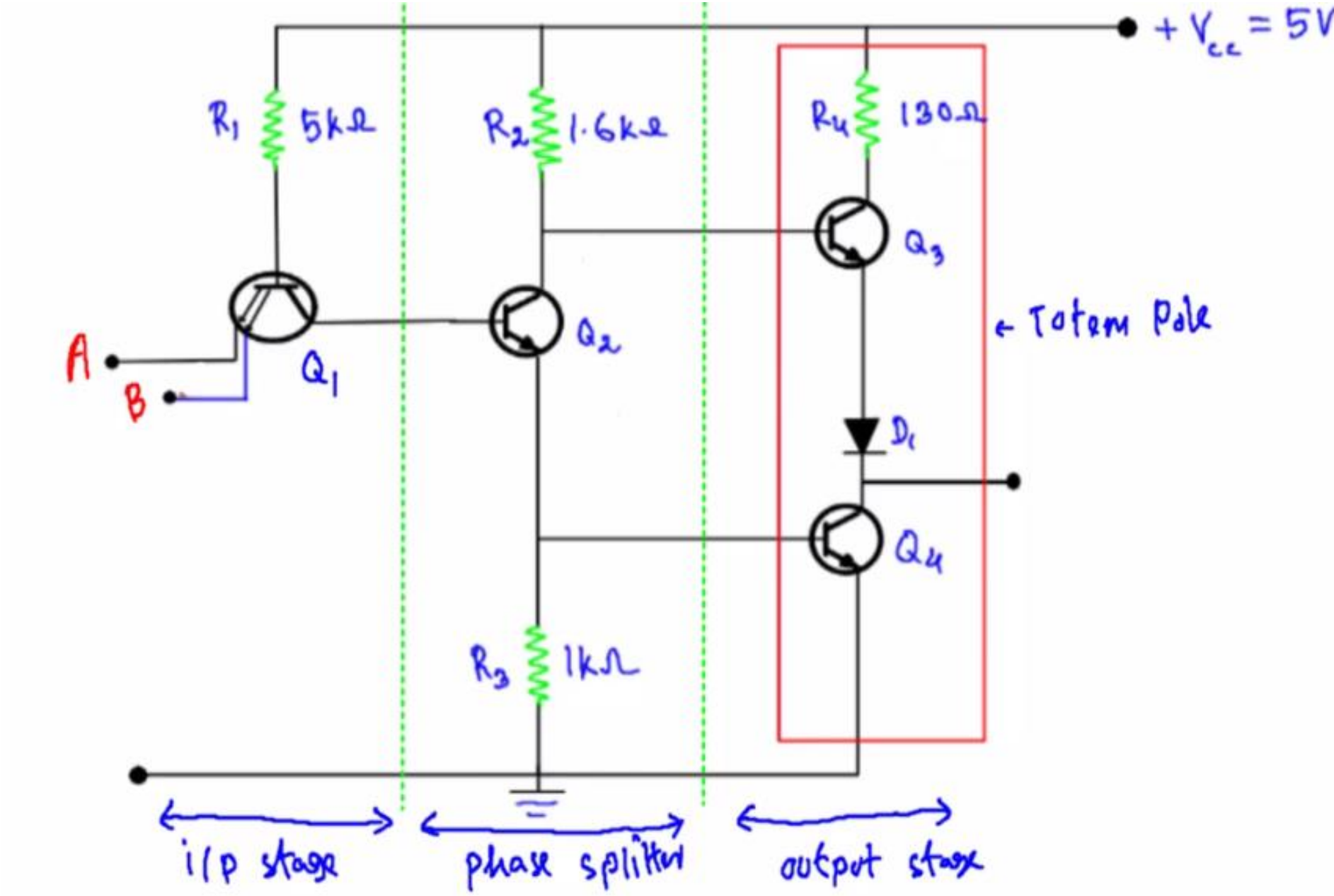


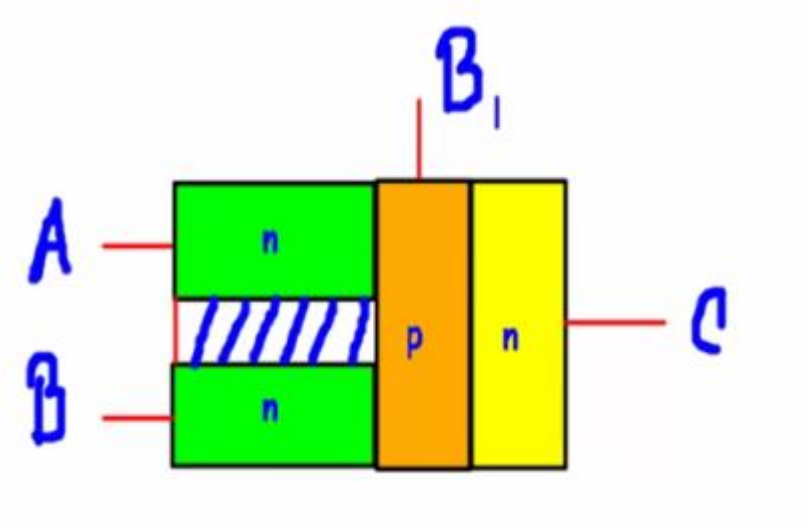



V_{cc}
R_1
R_2
R_4
Q_3
V_i
D_2
Q_2
D
Totem Pole
t
Q_4
R_3
V_o
-


$V_{cc} = +5V$
R_1
R_2
I_{B_3}
I_{C_3}
R_4
$I_{C_3}R_4$
$V_{CE.sat} = 0.2V$
$V_D = 0.7V$
Q_3
ON
D
Totem Pole
B
R.B.
D_2
OV
x
C
OV
Q_2 (off)
$I_{C_2} = 0$
$I_{E_2} = 0$
$V_{xy} = 0.7 + 0.8$
$= 1.5V$
y
OV
$I_{C_3} = 0$
$R_3 I_{C_3} = 0$
Q_4
off
+
−
$V_o = V_{cc} - I_{C_3}R_4 - V_{CE.sat} - V_D$

TTL NAND


+ Vcc = 5V
R1 5kΩ
R2 1.6kΩ
R4 130Ω
Q3
Totem Pole
A
B
Q1
Q2
D1
Q4
R3 1kΩ
i/p stage
phase splitter
output stage



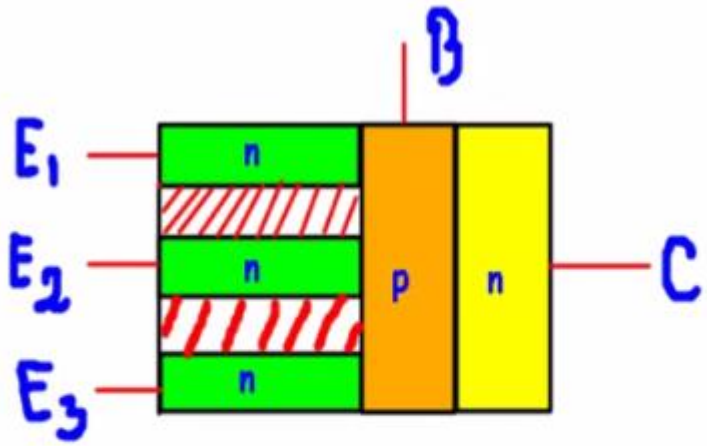
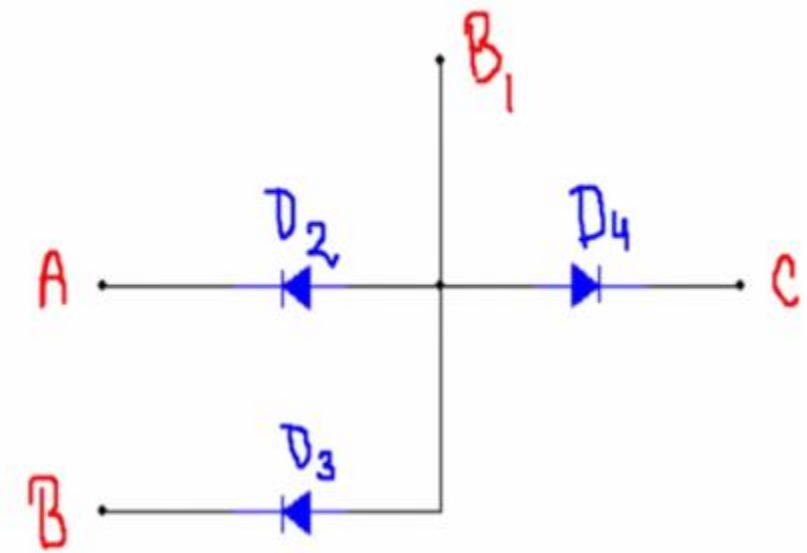
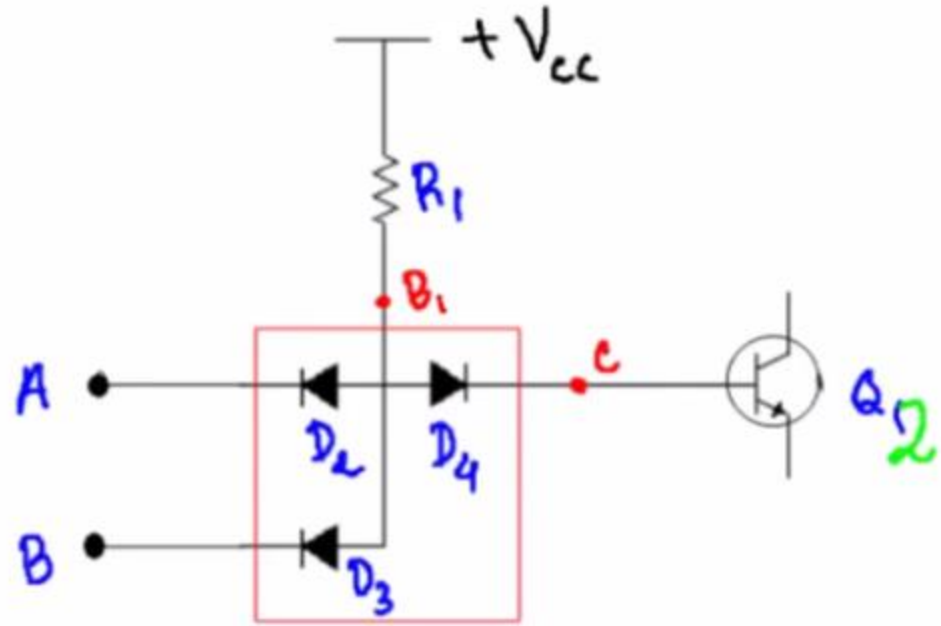


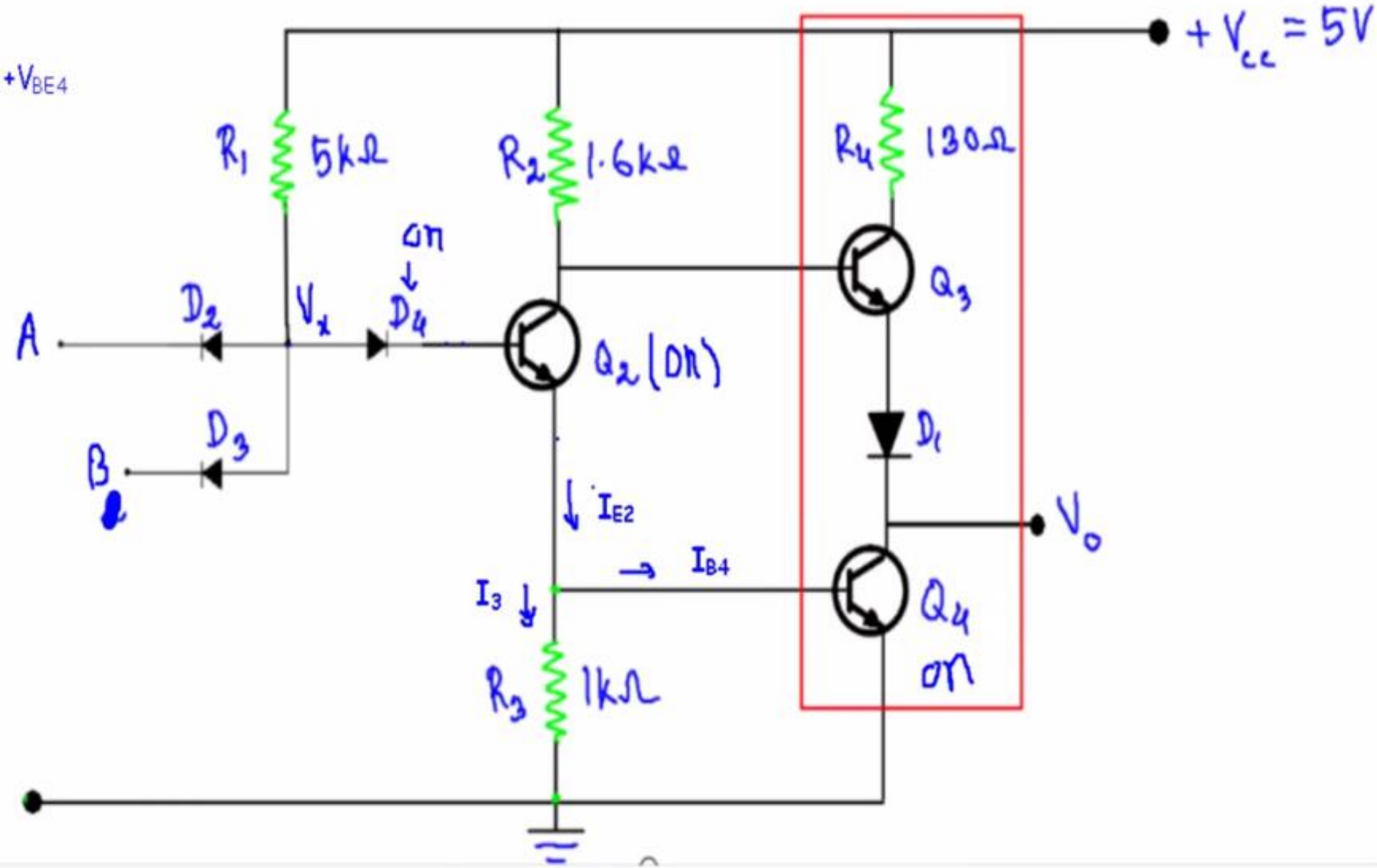
Fig. Configuration of Q_1 as multi-emitter transistor





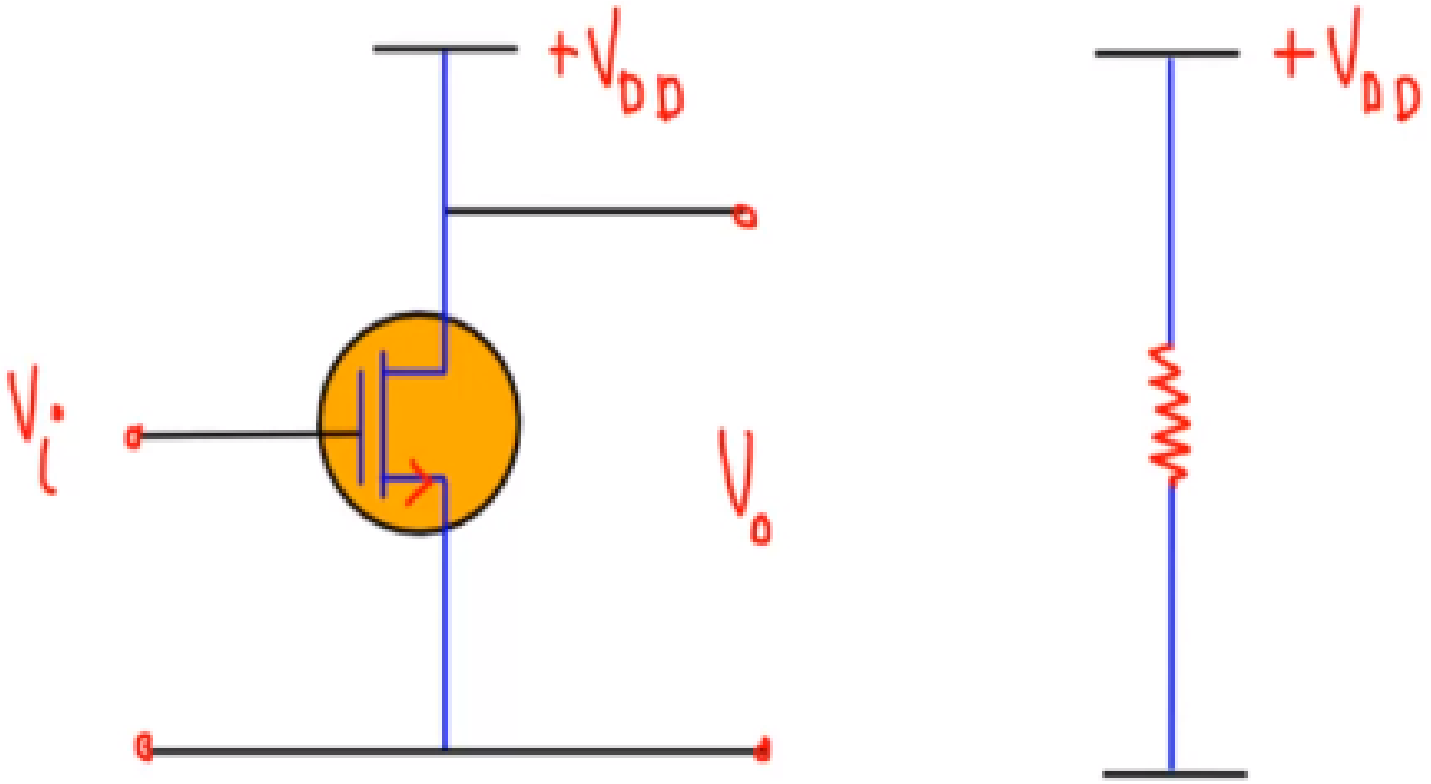
Diode Equivalent for Q_1

$V_X = V_{BC1} + V_{BE2} + V_{BE4}$

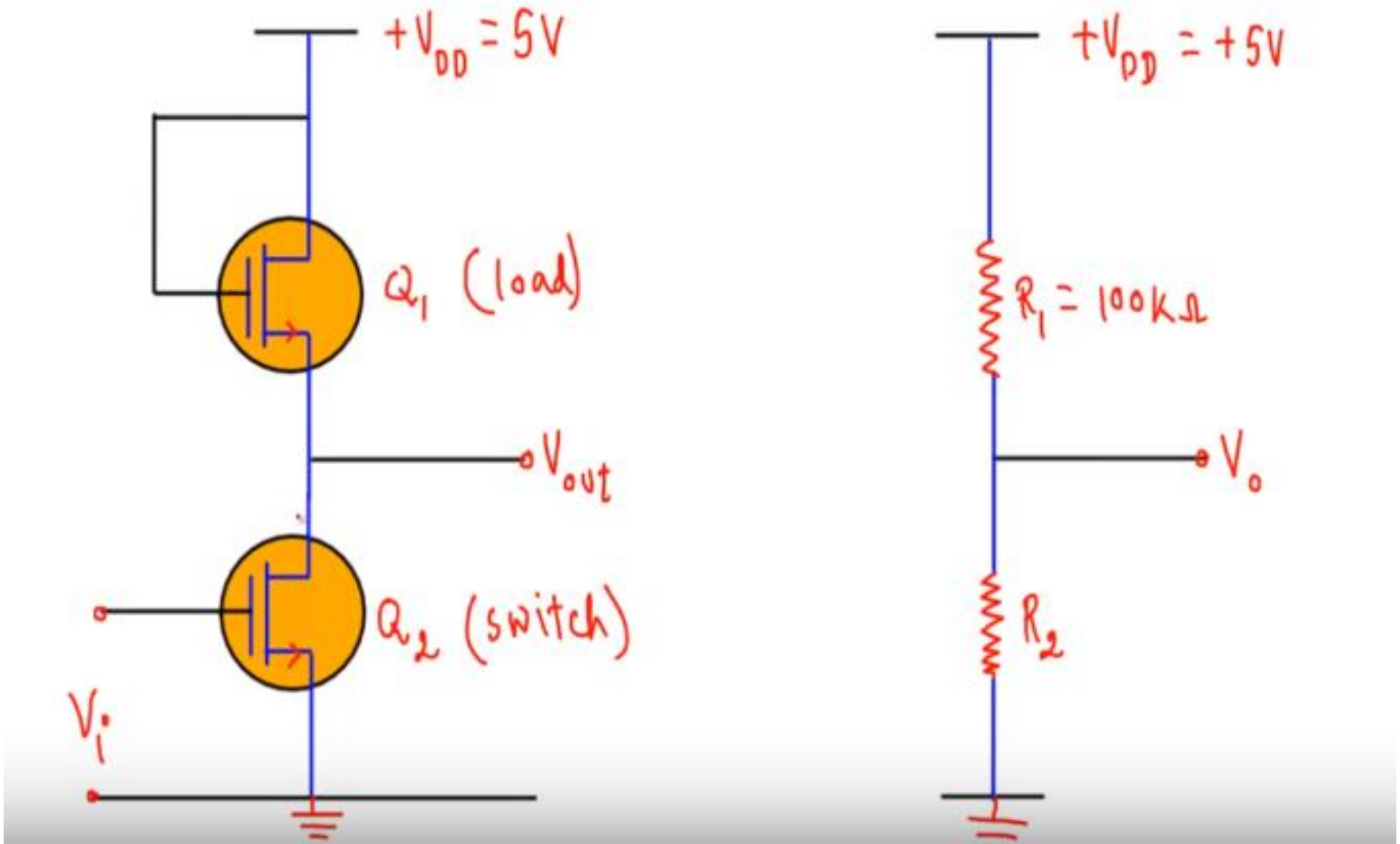


Basic Operation of NMOS

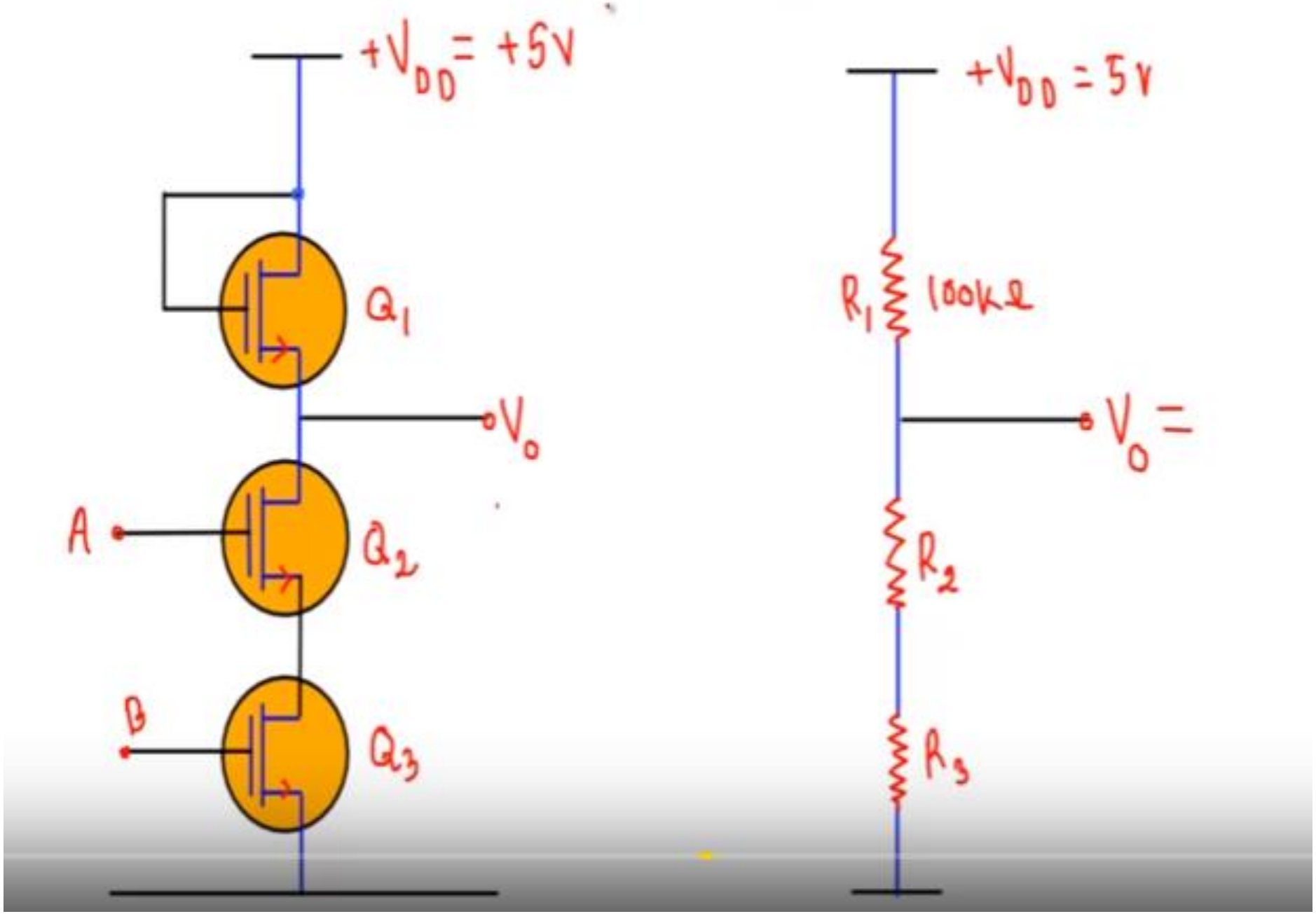
V_{th} = 1V



NMOS Inverter



NMOS NAND Gate



NMOS NOR Gate