University of Dhaka
Dept. of Computer Science and Engineering
3rd Year 1st Semester Incourse Examination, 2024

Answer all the questions. Marks are indicated at the left side bracket of each question.

Time: 90 Minutes | CSE 3101 - Computer Networking | Total Mark: 20

1. (a) (1 point) A network link has a bandwidth of 10 Mbps and a round-trip time (RTT) of 100 milliseconds. Calculate the BDP and explain what it means in this context.

   (b) (2 points) How does CNAME record of DNS help to distribute loads of web servers of a company? Illustrate with an example.

   (c) (2 points) Suppose a user's network bandwidth drops significantly during video playback. Describe how DASH responds to this situation to maintain a smooth viewing experience.

2. (a) (1 point) Mention one potential drawback of web caching and how it can be mitigated.

   (b) (2 points) Describe the typical sequence of events that occurs when a user sends an email from an email client and another user retrieves it using an IMAP-based client.

   (c) (1 point) Explain why IMAP is generally preferred over POP3 in modern email services.

3. (a) (2 points) Explain how TCP implements flow control using the sliding window mechanism.

   (b) (2 points) Consider a scenario where the receiver's buffer size is 32 KB and the sender has 200 KB of data to send. Describe how TCP would manage the transmission of data in this case, assuming no packet loss or retransmission is needed.

   (c) (1 point) How does TCP adjust its behavior when the receiver's advertised window size becomes zero?

4. (a) (1 point) State the key differences between TCP Tahoe and TCP Reno in terms of how they handle packet loss.

   (b) (2 points) Explain the Fast Retransmit and Fast Recovery mechanisms in TCP Reno. Illustrate your explanation with a congestion window (cwnd) vs. time diagram.

   (c) (1 point) Draw a diagram illustrating the flow of TCP segments between a sender and a receiver, showing how cumulative acknowledgments are sent as segments are received out of order.

   (d) (2 points) Describe how TCP Cubic overcomes the limitations of TCP Reno, particularly for high-bandwidth and high-delay networks.

Department of Computer Science and Engineering
University of Dhaka
CSE-3104: Database Management Systems-II
3rd Year 1st Semester Incourse Examination, 2024

Time: 1 Hour 10 Minutes	Marks: 30 25

Answer all the questions.

1 [1+3+3] =7

You are given the following tabular relation, where clustering indexing was based on the organization ID.

Name	Organization ID	Class	Address
AA	C-11	5	Dhaka
AB	F-10	2	Barisal
BA	G-12	3	Aftabnagar
BB	C-13	5	Mongla
CA	A-05	4	Khulna
CB	B-06	6	Barisal
D	A-08	4	Aftabnagar
EF	M-09	7	Dhaka

a) Define the differences between Secondary and Clustering Index.
b) Discuss how the search will be conducted if a secondary indexing is created on the *Name* attribute.
c) Present a mathematical formulation of the associated costs of seeking and transferring the blocks from disk to resolving the queries.

2 [3+3+3] =9

For the given tabular relation in Question 1, we want to extract the tuples/files/entries that satisfy the following query:

$$\sigma(\text{Class} >= 3) \wedge \sigma(\text{Class} <= 5) \wedge \sigma(\text{Address}=\text{Dhaka})$$

a) Apply the Linear Scan selection algorithm and discuss the associated cost of extracting the tuples
b) Apply the indexing-based selection algorithm and discuss the associated cost of extracting the tuples
c) Discuss the possible optimization strategies to reduce the number of disk accesses for the given problem setup.

3	You are given the following operations to maintain a B+ Tree. For each operation, state your strategy and show the updated B+ Tree. You can keep at most 3 keys in each leaf and non-leaf node. Initially, there is no node in the B+ Tree. a) Insert Mango b) Insert Apple c) Insert Orange d) Delete Mango e) Insert Guava f) Insert Lemon g) Delete Guava h) Delete Apple Explain the differences that can be observed between B+-Tree and B-Tree for the aforementioned problem setup.	[8+1] =9

A B C D E F G H I J K L M N O P

Mid Term Examination
CSE 3102- Software Engineering
Total Marks: 30, Time: 1.5 hours

1. What are the main drawbacks of the Waterfall model? Explain how the Iterative model solves those problems. Give examples of applications that are best suited to the Waterfall model and the Iterative model, respectively. 5

2. The Rational Unified Process (RUP) is a widely used iterative software development framework. List and briefly describe the four phases of RUP, including their primary objectives. 5

3. Consider a Library Management System where librarians manage books, members, and borrowing processes. One of the key functionalities is *"Borrow a Book."* Write a detailed use case description for the "Borrow a Book" scenario, including the following sections: 10
   - Use Case Name (1 Mark)
   - Actors (Primary and Secondary, if any) (1 Mark)
   - Preconditions (What must be true before the use case starts) (1 Mark)
   - Basic Flow (Main Success Scenario) (3 Marks)
   - Alternative Flows / Exceptions (e.g., book unavailable, member has fines) (4 Marks)

4. Consider an *Online Bookstore* System where users can browse, search, and purchase books. The system also handles inventory management, order processing, and customer accounts. 10
   i. Identify the key domain entities and attributes.
   ii. Draw a Domain Model diagram to show the relationships between these entities.

CSE 3103– Microprocessor and Microcontroller
MidTerm Exam, 2025
Computer Science and Engineering
University of Dhaka

Professor Upama Kabir, PhD

Time = 1.5 Hours **Total marks is 40**

[Answer all the following questions]

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1. (a) (5 points) Shift the contents of the 16-bit variable **Value** to the left one bit. Store the result back in **Result.**
   Sample Problems
   Input: **Value** = 4242(0100001001000010_2)
   Output: **Result** = 8484(1000010010000100_2)

   (b) (5 points) Find the larger of two 32-bit variables **Value1** and **Value2**. Place the result in the variable **Result.**
   Sample Problems
   Input: **Value1**= 12345678
   Value2= 87654321
   Output: **Result** = 87654321

2. (a) (2 points) Assuming that the registers R1, R2, R3, R4 contain the values 0x11aa, 0x22bb, 0x33cc, 0x44dd respectively, and that the register R5 contains the value 0x1000, what is the value in R5 after each of the following ARM instructions in this program fragment and what byte value is stored in each affected memory location? (Assume a little-endian configuration.)
   STR R2, [R5, #4]
   STR R3, [R5], #4

   (b) (2 points) What are the three registers that are initialized on Reset in cortex M4?

   (c) (2 points) Register *R1* has the value 0x80008001, what is its value of *R1* after the following operations are performed independently:
   i. LSR R1,R1,#3
   ii. LSL R1,R1,#4

   (d) (2 points) Mention the bitfields of APSR with proper diagram.

   (e) (2 points) Consider the following 8-bit addition (assume registers are 8 bits wide)
   Load 0x40 into R1
   Load 0x4B into R2
   Add R3 = R1+R2
   1. What will be the 8-bit result in Register R3 (in hex)?
   2. What is 8-bit result in Register R3 (as unsigned decimal)?

3. (20 points) Multiple Choice Questions.
   1. Which one is the highest priority interrupt in the Cortex M4 processor
   (a) NMI (b) Reset (c) SVC (d) PendSV
   2. The interrupt which cannot be delayed and require the processor to process them immediately
      (a) Maskable Interrupts
      (b) Periodic Interrupts
      (c) Non-maskable Interrupts
      (d) Software Interrupts

3. Consider a four bit ALU which does four bit arithmetic. When the following four bit numbers are added, what is the status of NZCV flags? 1101+ 1011
(a) NZCV = 0111 (b) NZCV = 1000 (c) NZCV = 1001 (d) NZCV = 1010
4. The return address from the interrupt-service routine is stored on the
(a) Processor register (b) Memory (c) System Heap (d) Processor Stack
5. Reset vector is the location of the first instruction executed by the processor when power is applied. This instruction branches to the initialization code.
(a) True (b) False
6. Instruction CPSIE I does
(a) set PRIMASK =0
(b) set BASEPRI =0
(c) set PRIMASK =1
(d) set BASEPRI =1
7. Fixed instruction length is a feature of one of the following architecture.
(a) CISC (b) RISC (c) X86 (d) None
8. Processors that are typically used in mobile phone, mobile computing devices, television, and some of the energy efficient servers are
(a) Cortex-R processors
(b) Cortex-A processors
(c) Cortex-M processors
(d) ARM9E series
9. How many bits are required to specify the Register operands in an Cortex M4 instruction?
(a) 32 bits (b) 8 bits (c) 16 bits (d) 12 bits
10. If an instruction takes 3 cycles for execution, then how many cycles are needed for executing 4 instructions of the same type in a sequence using a 3-stage pipeline? Assume that there are no interrupts or exceptions while executing them.
(a) 12 cycles (b) 9 cycles (c) 6 cycles (d) 4 cycles
11. Which of the following register in ARM7 is used to point to the location of currently executing instruction in a program?
(a) R1 (b) R5 (c) R15 (d) R8
12. Evaluate the following statements:
I. R13 is traditionally used as the stack pointer and stores the head of the stack in the current processor mode
II. R14 is the link register where the core puts the return address on executing a subroutine
III. R15 is the program counter and contains the address of the next instruction to be fetched
(a) All the options are true
(b) I and II are true
(c) II and III are true
(d) I and III are true
13. Instruction used to multiply R5 contents by R4 and to store the result into R6 is called
(a) MUL R6, R5, LSL #2
(b) MUL R6, R5, R4
(c) MUL R6, R5, LSR #2
(d) None of the above
14. Which of the following instructions corresponds to a Multiply Accumulate instruction in ARM architecture?
(a) MUL (b) UMULL (c) SMULL (d) SMLAL
15. Which of the following is a valid multiplication (not multiply accumulate) instruction in ARM architecture?
(a) MUL r15, r0, r3
(b) MLA r1, r1, r6
(c) MUL r10, r2, r5
(d) MLA r10, r2, r1, r5
16. How many registers does ARM have?
(a) Four (b) Eight (c) Sixteen (d) Thirty-seven
17. How many operating modes does ARM have?
(a) Four (b) Eight (c) Sixteen (d) Thirty-seven
18. What is the standard form of NVIC?
(a) Nested Vectored Internal Controller
(b) Nested Vectored Interface Controller
(c) Nested Vectored Interrupt Controller
(d) None of the above
19. An instruction that is used to move data from an ARM Register to a Status Register (CPSR or SPSR) is called
(a) MRC (b) MRS (c) MSR (d) MCS
20. Which of the following is not the configurable options in Cortex-M4?
(a) FPU (b) MPU (c) NVIC (d) WIC