CSE-3103: Microprocessor and Microcontroller

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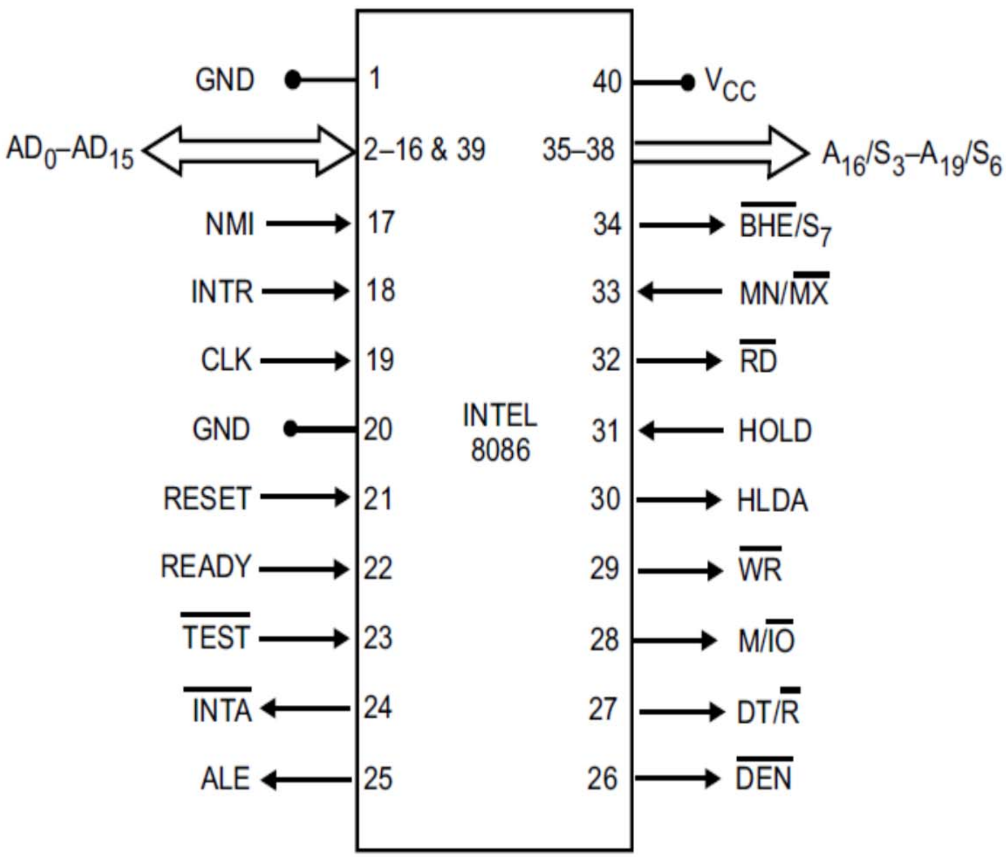
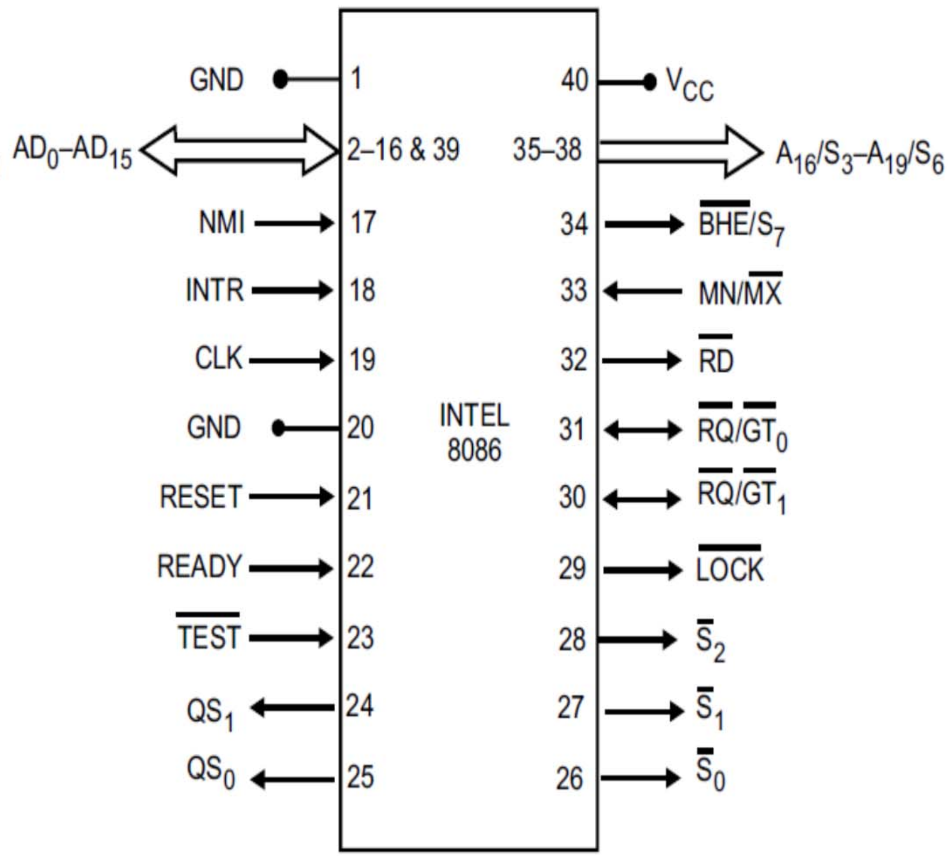
Pin Diagram of 8086 Microprocessor



MIN mode



MAX mode

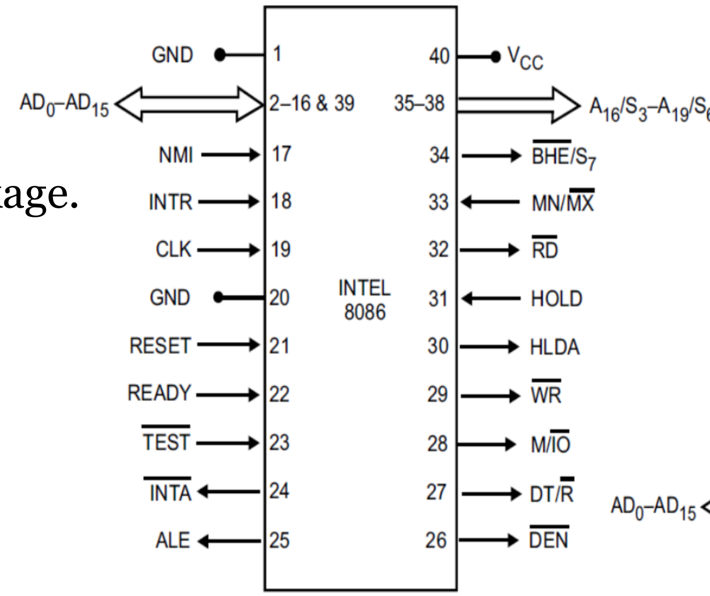
Pin Diagram of 8086 Microprocessor

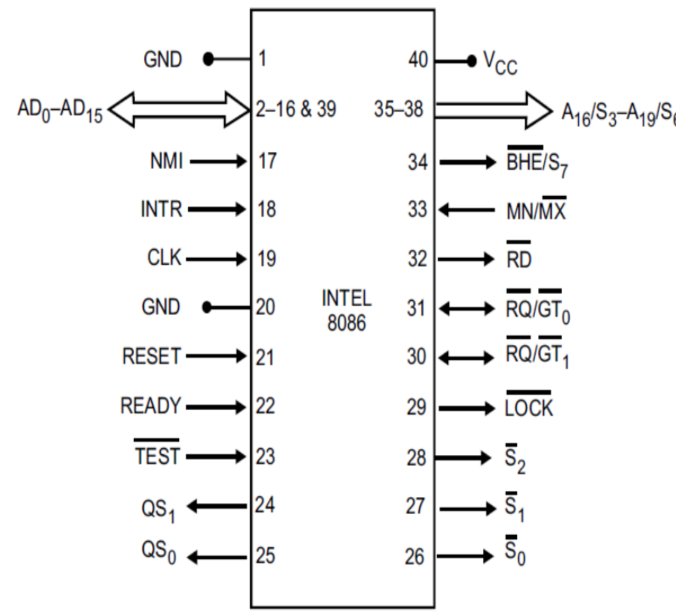
Intel 8086 microprocessor →
- HMOS technology.
- 29,000 transistors
- housed in 40-pin DIP package.

2 pin diagrams →
- MIN mode,
- MAX mode.
- differ: pin 24 to pin 31.

MIN mode (uniprocessor) →
- pin 33 high
- CPU issues control signals.

MAX mode (multiprocessor) →
- pin 33 low
- bus controller IC (8288) generates control signals.





Pin Diagram of 8086 Microprocessor

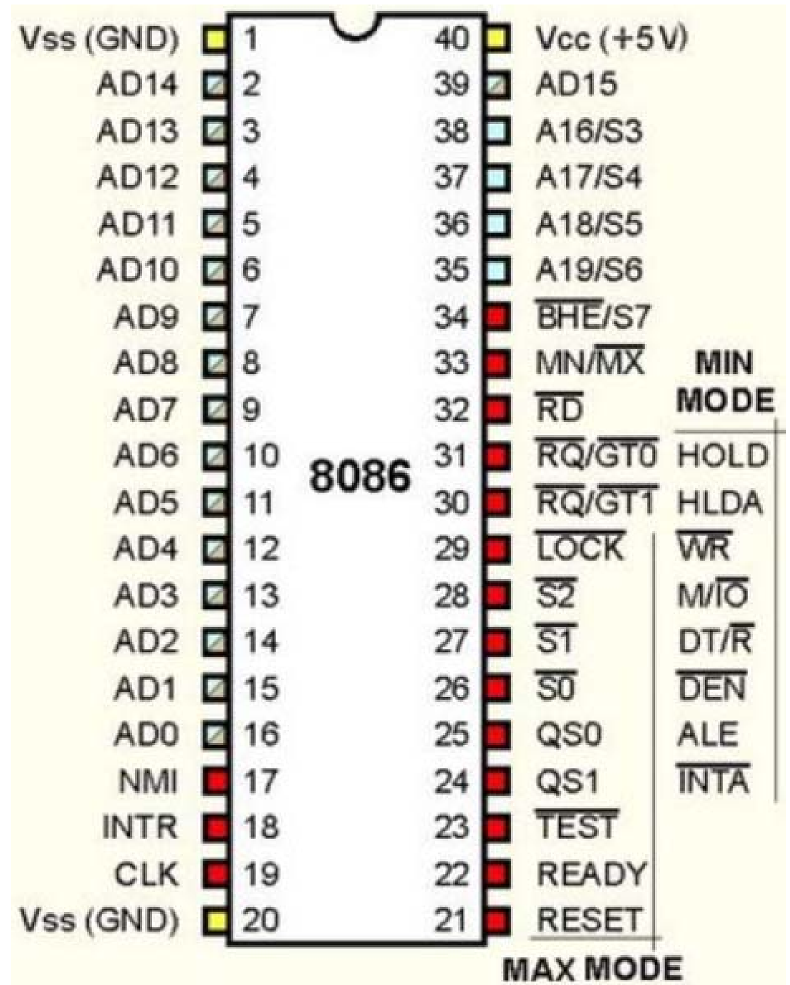
(AD_0–AD_{15}) = multiplexed lower 16 address lines.
(AD_{16}/S_3–AD_{19}/S_6) = multiplexed upper 4 address lines.

(AD_0–AD_{15}) →
carry address during T_1,
carry data during T_2, T_3, T_4.

(AD_{16}–AD_{19}) →
carry address during T_1,
carry status signals during T_2, T_3, T_4.

AD_0–AD_{19} →
address lines for accessing memory.
can address 2^{20} = 1 MB memory.

AD_0–AD_{15} →
address lines for accessing I/O's.
can access 2^{16} = 64kB of I/O's.



Pin Diagram of 8086 Microprocessor

pin 40 → +5 V DC supply at V_{CC},
pin 1 and 20 → ground at V_{SS}.

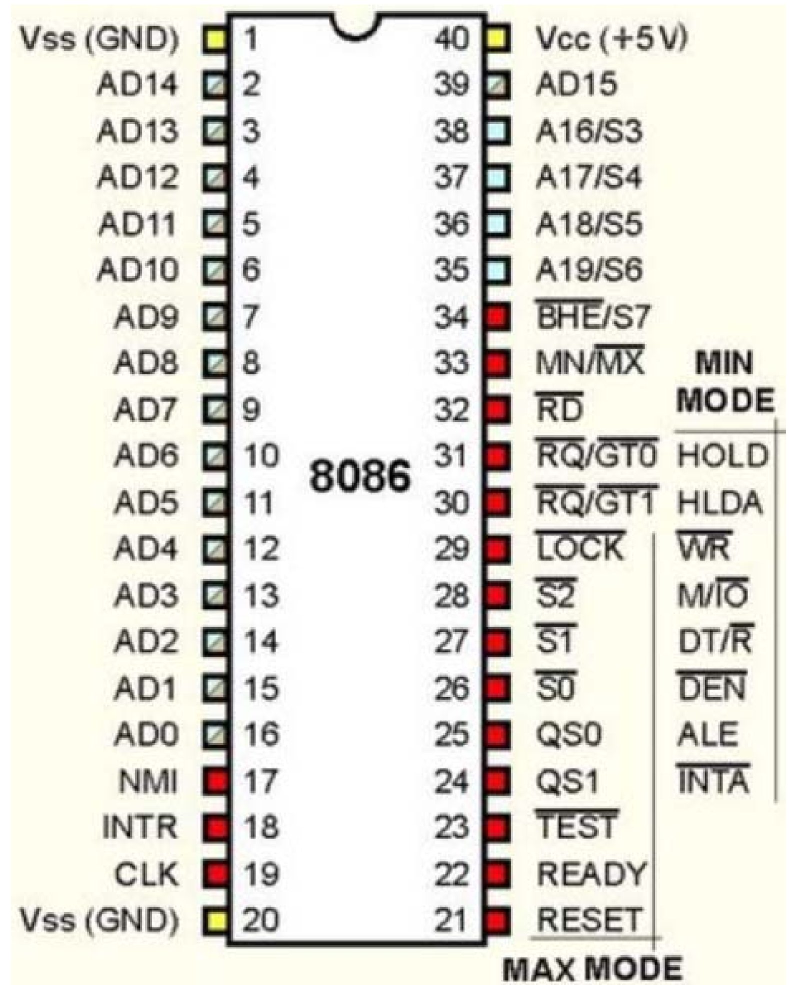
pin 19 →
clock signal.
5 MHz, 8 MHz or 10 MHz for different versions.

AD_{16}/S_3—AD_{19}/S_6 →
time multiplexed signals.

AD_{19}–AD_{16} →
address lines during T_1 for memory operation.
remain low during I/O operations.
carry status signals during T_2–T_4.

S_4 and S_3 →
identify segment register for
20-bit physical address generation.

S_5 → interrupt enable status.
S_6 → remains low during T_2 to T_4.



Pin Diagram of 8086 Microprocessor

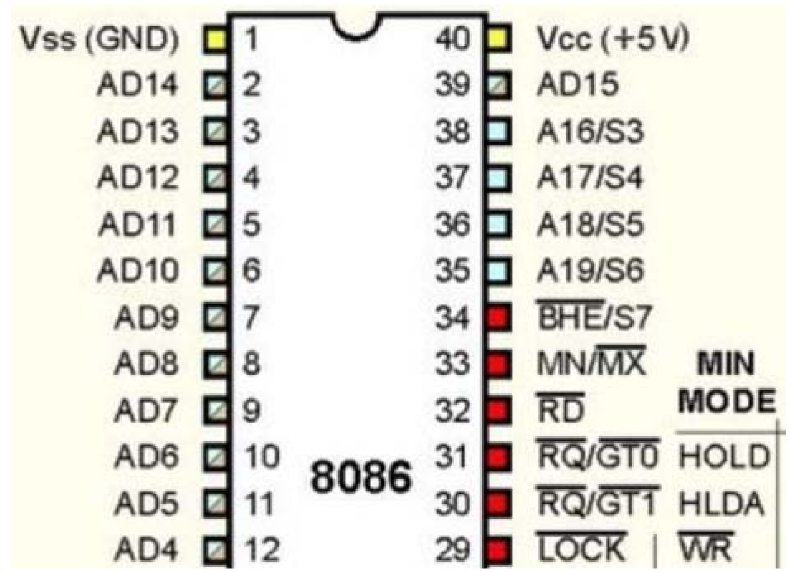
pin 34 →

$\overline{BHE}/S_7$ signal,

Bus High Enable signal during T_1, remains low.

chip select signal on AD_{15}–AD_8.

status signal S_7 during T_2 to T_4 remains high.



$\overline{BHE}$ and A_0 →

determine references to memory.

$\overline{BHE}$	A_0	Word/byte access
0	0	Both banks active, 16-bit word transfer on AD_{15}–AD_0
0	1	Only high bank active, upper byte from/to odd address on AD_{15}–AD_8
1	0	Only low bank active, lower byte from/to even address on AD_7–AD_0
1	1	No bank active

Pin Diagram of 8086 Microprocessor

pin 22 →

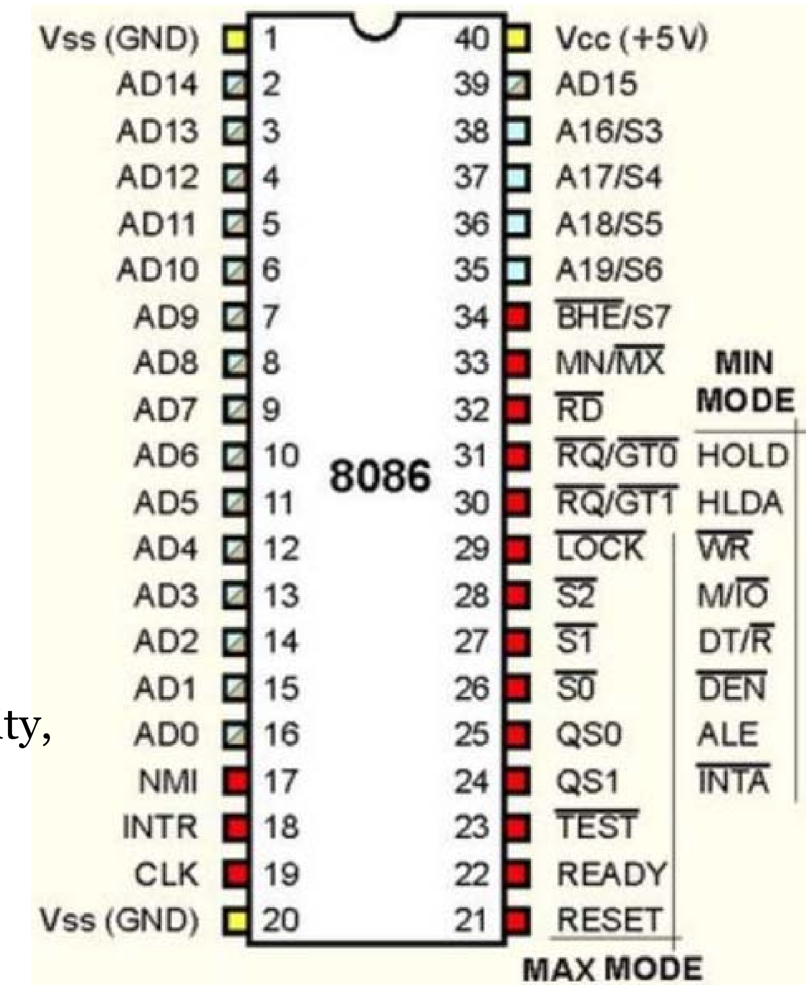
READY signal,
high = device is ready to transfer data.
low = wait state.

pin 21 →

RESET signal,
applied after 50 µS of power on.
active for ≥ 4 CLK cycles.
execution starts after RESET returns to low value.
three buses = tristated,
ALE and HLDA = low.

During resetting →

processor immediately terminates its present activity,
all internal register contents = 0000H,
CS = F000H and IP = FFF0H.
execution starts from physical address FFFF0H.
EPROM = FFFF0H to FFFFFH



Pin Diagram of 8086 Microprocessor

pin 18 →

INTR = interrupt request signal,
sampled during last clock cycle of each instruction.

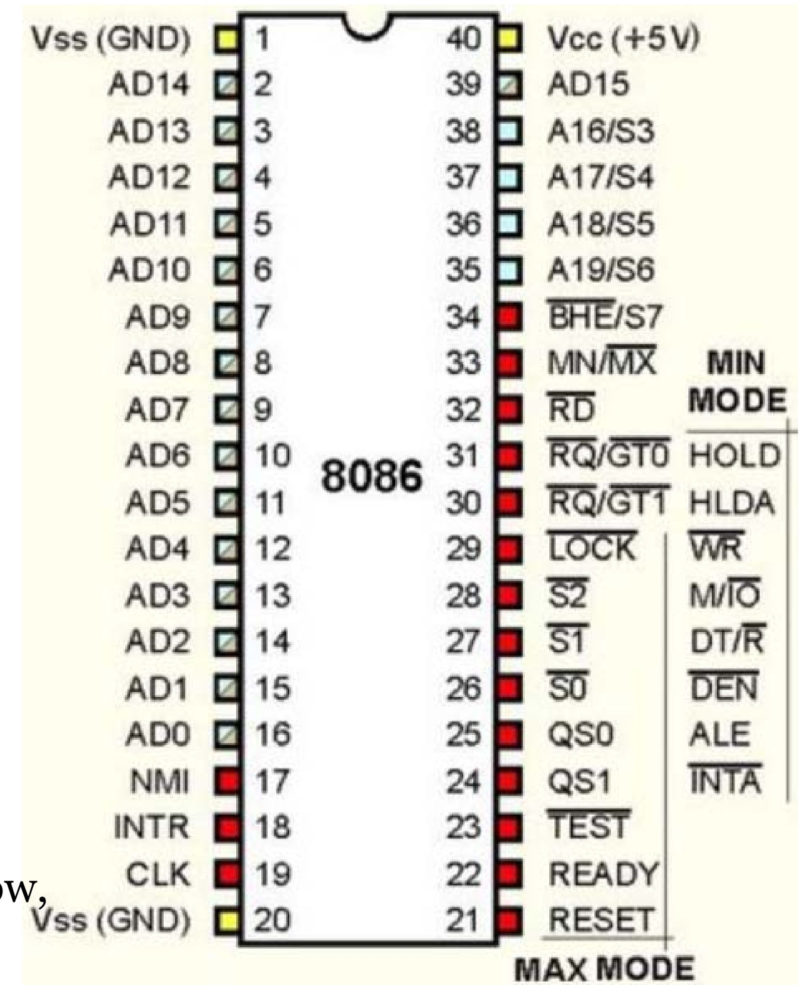
pin 17 →

NMI = non-maskable interrupt signal,
edge triggered input,
causes interrupt request to microprocessor.

pin 23 →

BUSY output pin of 8087 NDP is connected to
$\overline{\text{TEST}}$ input pin.
8087 is busy →

pulls $\overline{\text{TEST}}$ signal high,
8086 is made to WAIT,
8087 completes its instruction executions.
BUSY signal goes low = $\overline{\text{TEST}}$ input goes low,
8086 goes for execution of its program.



Pin Diagram of 8086 Microprocessor

pin 33 →

MN/$\overline{\text{MX}}$ = minimum/maximum mode,
High = works in minimum mode;
Low = works in maximum mode.

pin 24 →

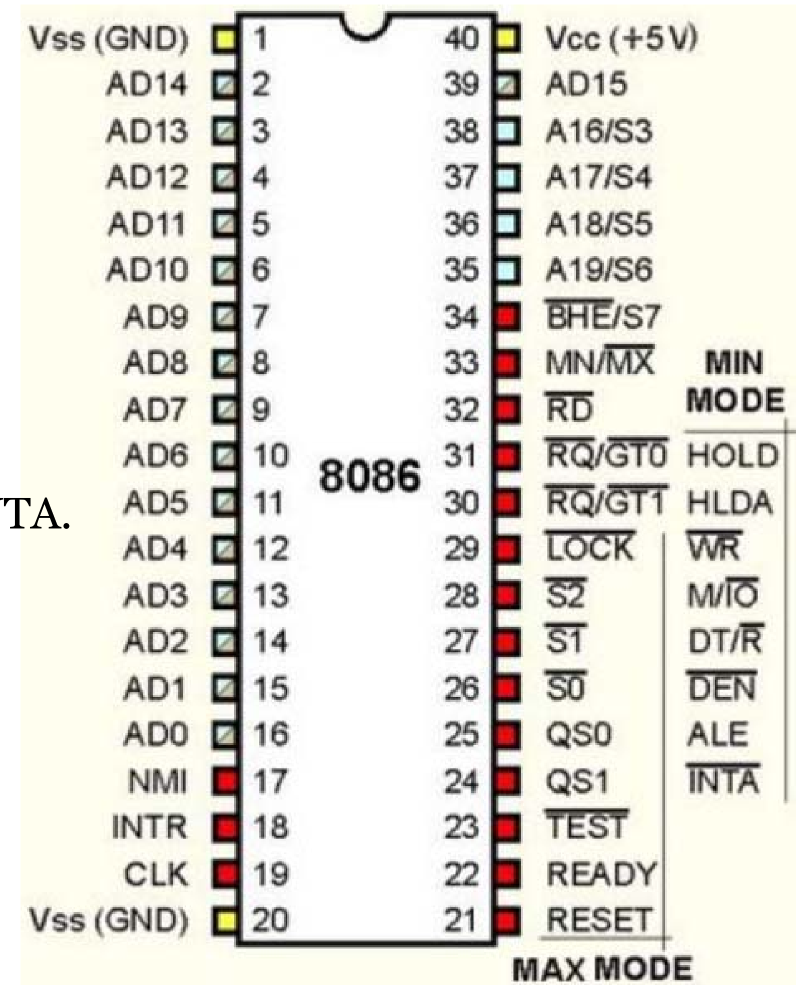
INTA = interrupt acknowledge signal (MIN Mode).
microprocessor receives interrupt request through NMI/INTR,
acknowledges interrupt through INTA.

pin 25 →

ALE = address latch enable signal (MIN mode),
+ve pulse = availability of valid address on address/data lines.

pin 28 →

M/$\overline{\text{IO}}$ pin (MIN mode),
distinguish between memory and I/O operations.



Pin Diagram of 8086 Microprocessor

pin 27 →

DT/$\overline{R}$ = data transmit/receive output pin (MIN mode),
decides directions of data flow through transceivers.
1 = processor sends out data;
0 = processor receives data.

pin 26 →

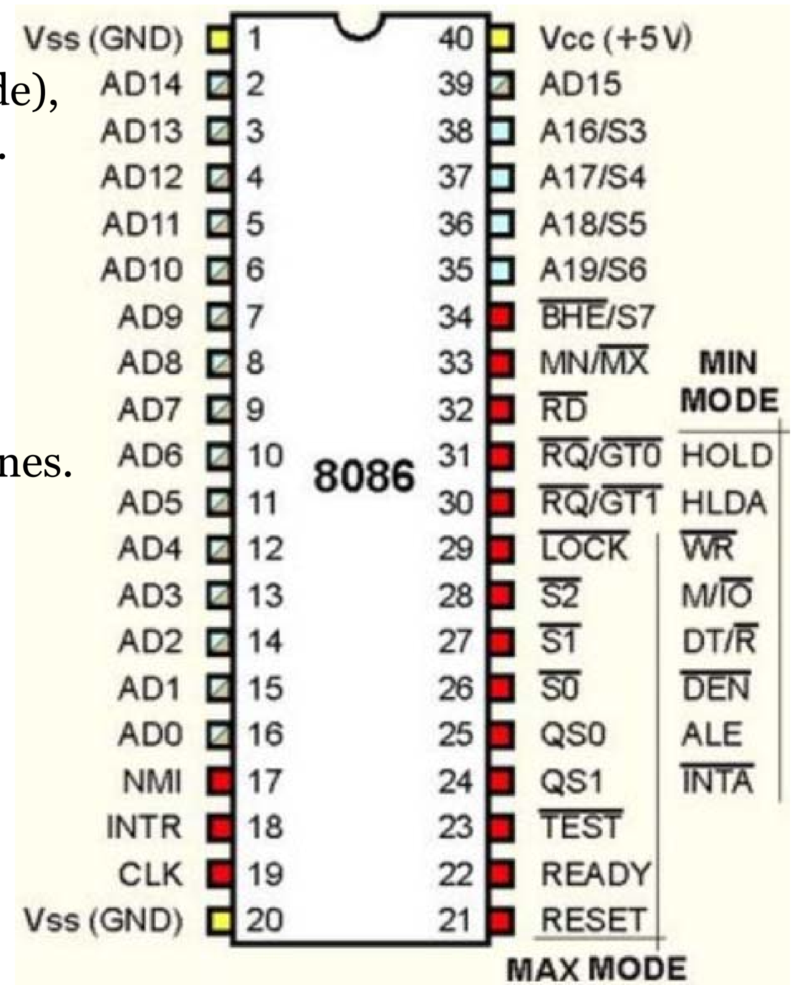
$\overline{DEN}$ = data enable signal (MIN mode),
availability of data over multiplexed address/data lines.
active from middle of T_2 until middle of T_4.

pin 29 →

$\overline{WR}$ = write signal (MIN mode),
write data into memory or output device.

pin 32 →

$\overline{RD}$ = read signal,
read operation from memory or input device.



Pin Diagram of 8086 Microprocessor

pin 31 →

HOLD = hold signal to processor (MIN mode), external devices request to access address/data buses.

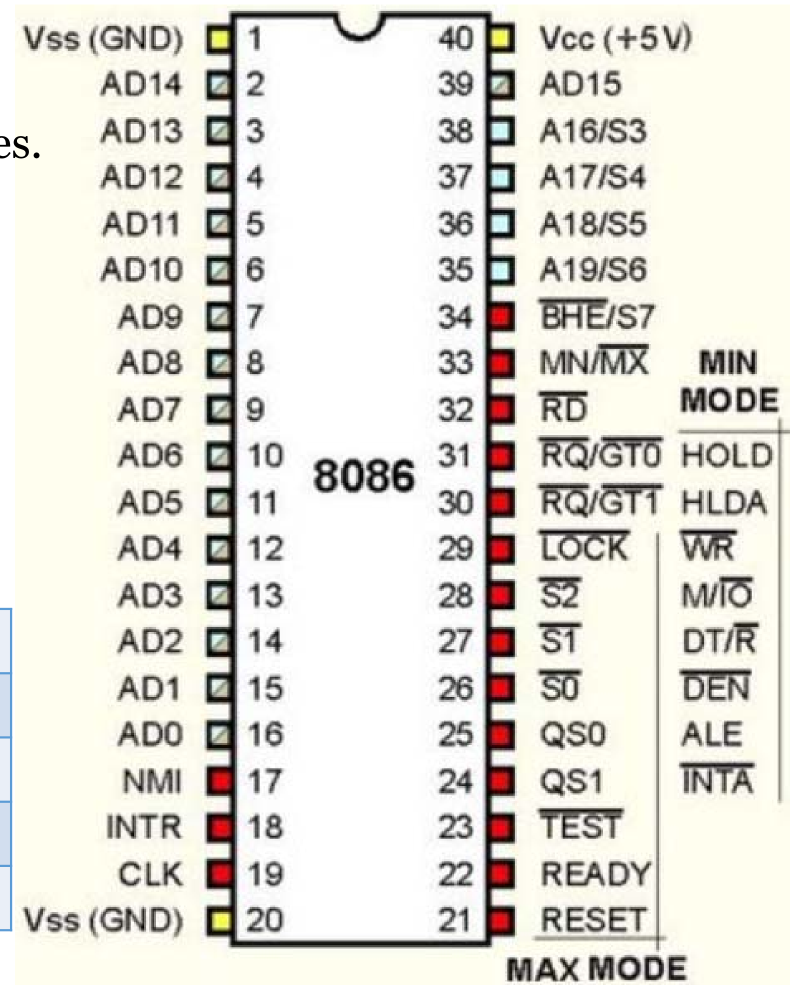
pin 30 →

HLDA = hold acknowledgement (MIN mode), acknowledges HOLD signal.

pins 24 and 25 →

QS_1 and QS_0 = queue status signals (MAX mode) provide status of instruction queue.

QS_0	QS_1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

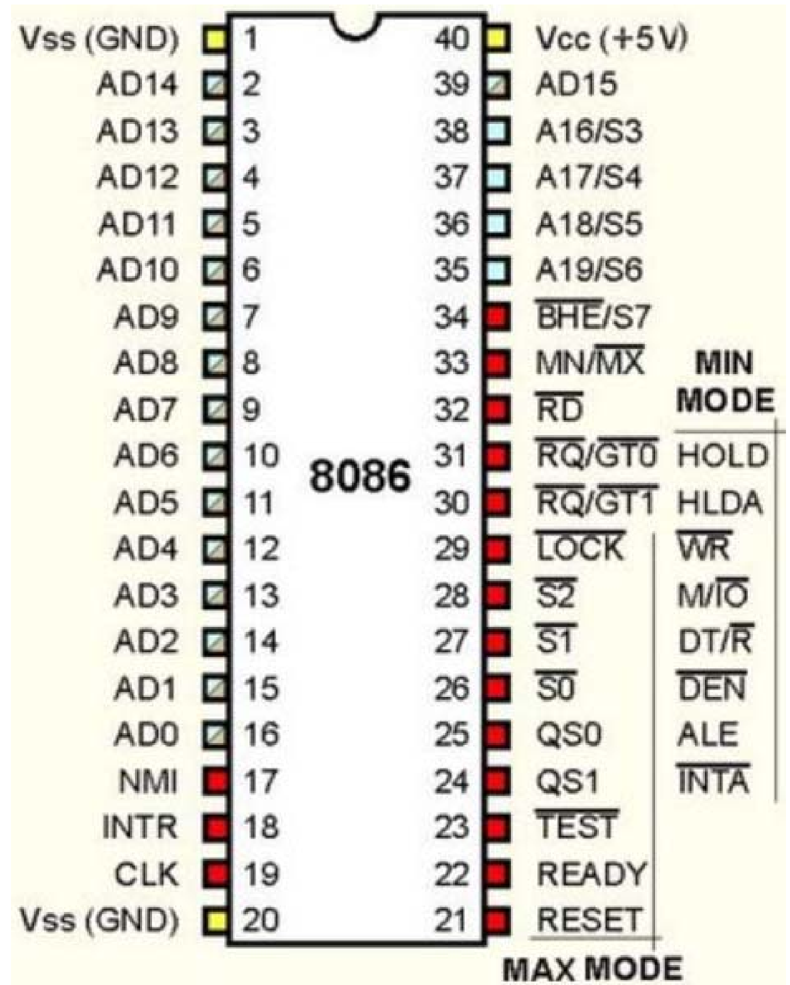


Pin Diagram of 8086 Microprocessor

pin 26 – pin 28 →

$\overline{S_2}, \overline{S_1}, \overline{S_0}$ = output status signals (MAX mode).
indicates type of operation carried out by processor.
active during T_4 of previous cycle and
T_1 and T_2 of current cycle.
passive state during T_3 of current bus cycle.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	**CPU Cycle**
0	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	HALT
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive



Pin Diagram of 8086 Microprocessor

pin 29 →

$\overline{\text{LOCK}}$ signal (MAX mode),
activated by LOCK prefix instruction,
remains active until completion of next instruction.
$\overline{\text{LOCK}}$ = low → all interrupts get masked,
HOLD request is not granted.

pin 30 and 31 →

$\overline{\text{RQ}}/\overline{\text{GT}_1}$ and $\overline{\text{RQ}}/\overline{\text{GT}_0}$ =
request/grant signals (MAX mode),
other processors request CPU to release system bus.
when signal is received, CPU sends acknowledgment.