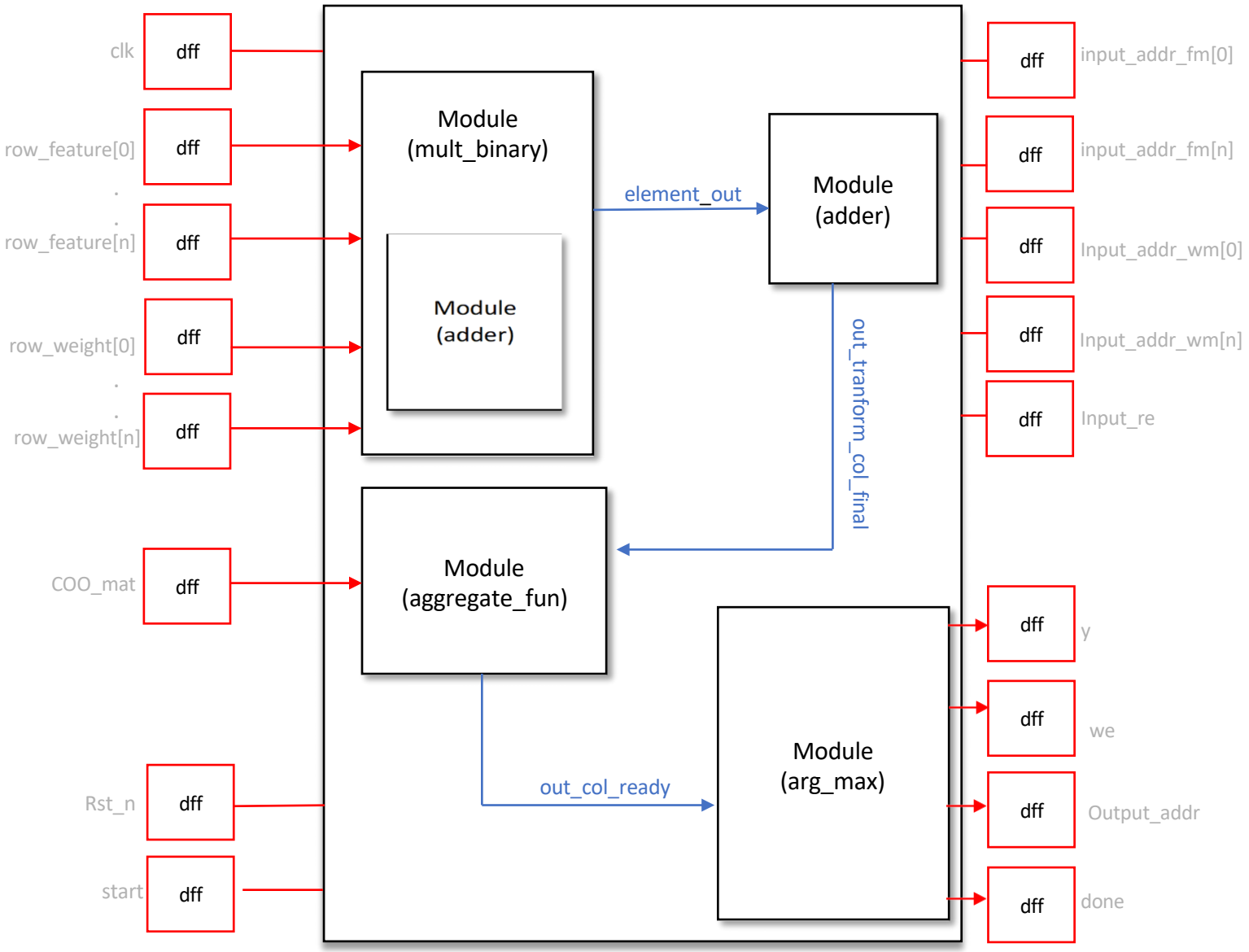
Name: XXXX
ASU ID: XXX

EEE 525 LAB 4

Milestone 1

Architecture/High-level Block Diagram:

Module (gcn)



High-level block diagram

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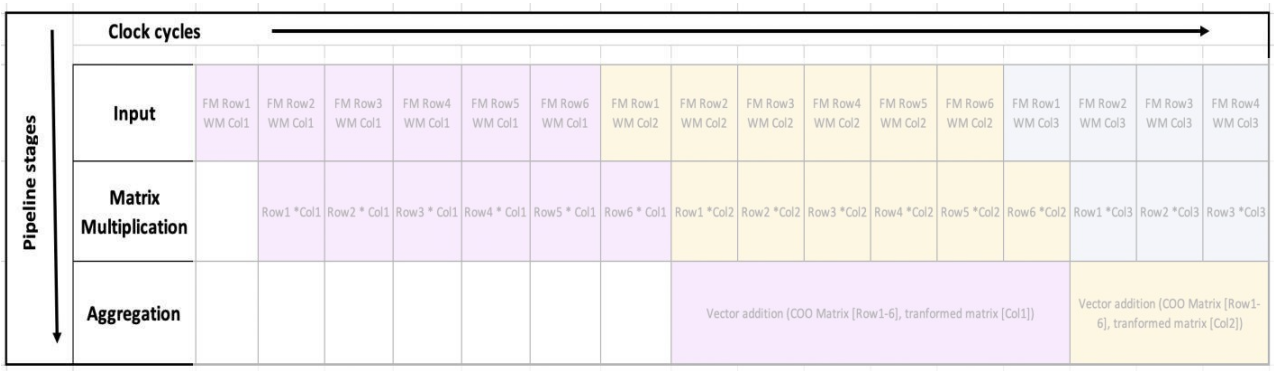
Design decisions: (with 1-2 appropriate figures)

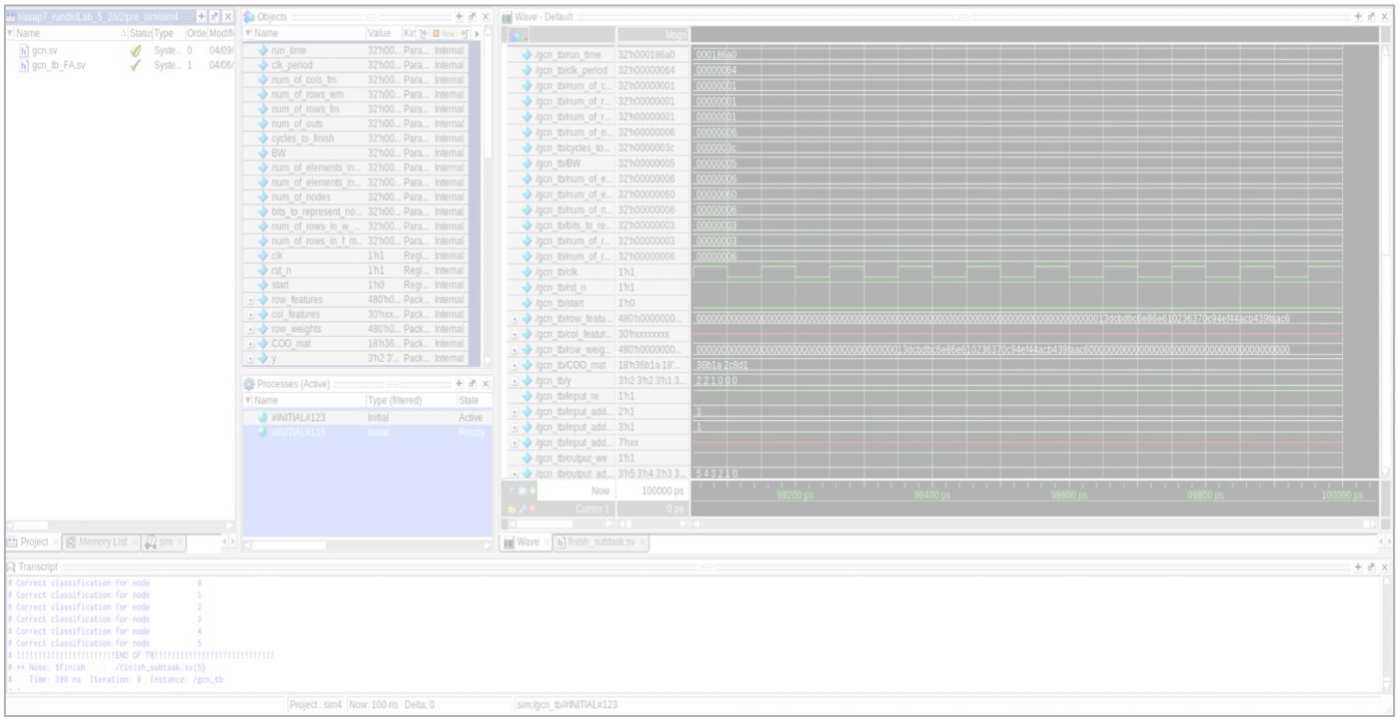
We have designed the GCN module for a node classification application as follows:

- xxx.
- xxx:



- *Representation of pipeline stages in design*

Behavioral Verilog – Simulation:



Correctness of the module with behavioral Verilog

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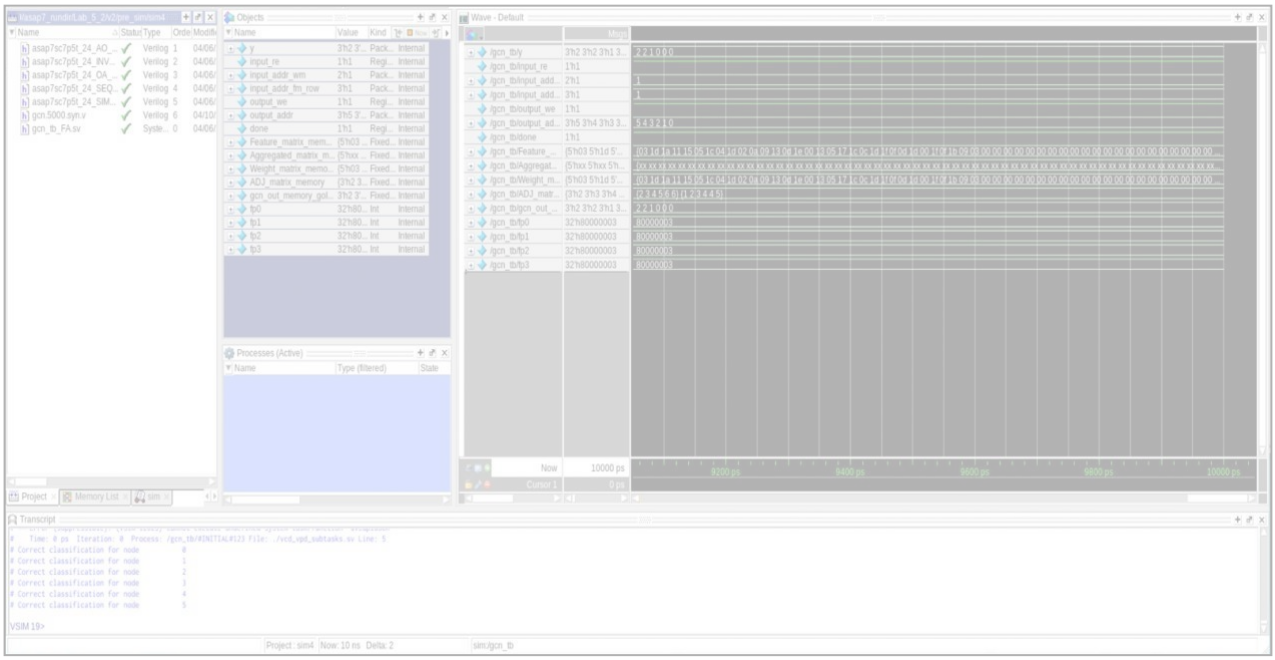
Post_Synthesis – Simulation:

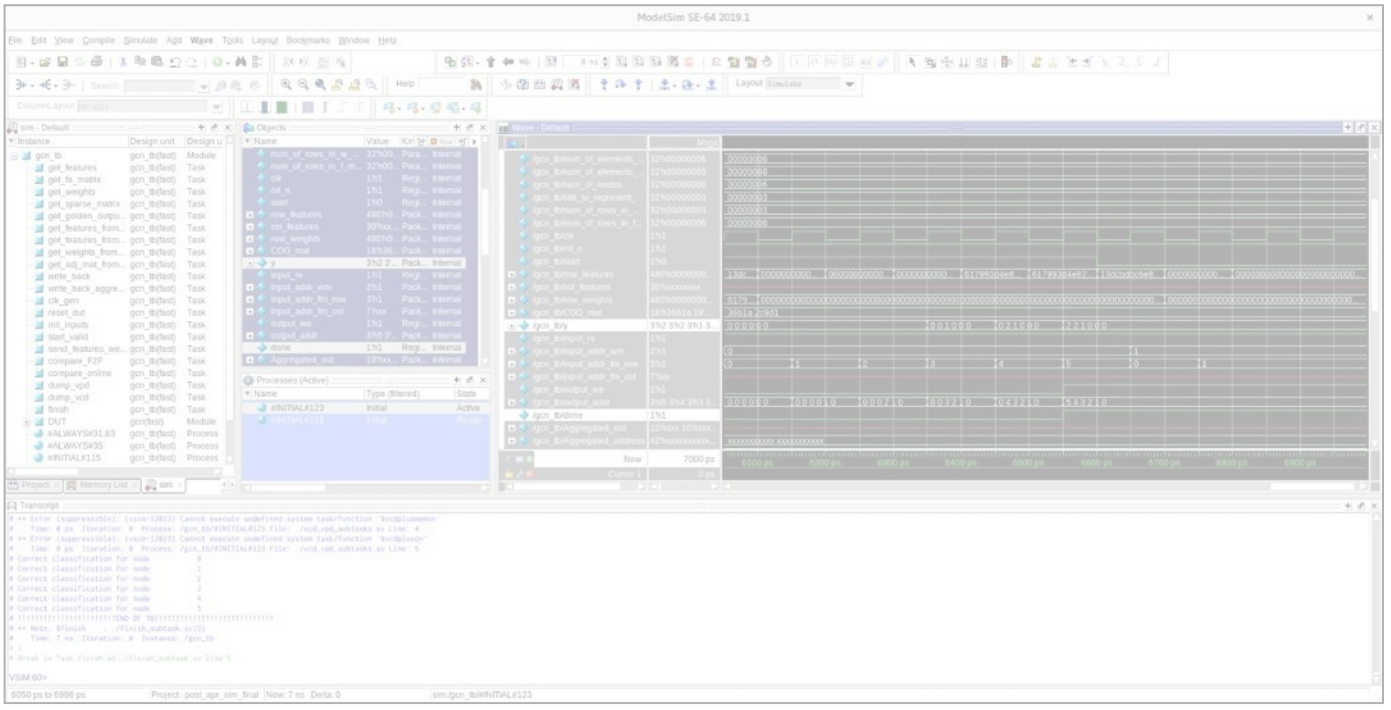


Correctness of the module with post-synthesis Verilog netlist

Milestone 2

Total Latency:

- Total Latency: **xxx ns**, at the clock frequency of **xxx MHz**.
- Screenshot of Modelsim:



post APR simulations screenshot

Name: XXXX
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Power:

- Total Power (From Innovus): **xx mW**

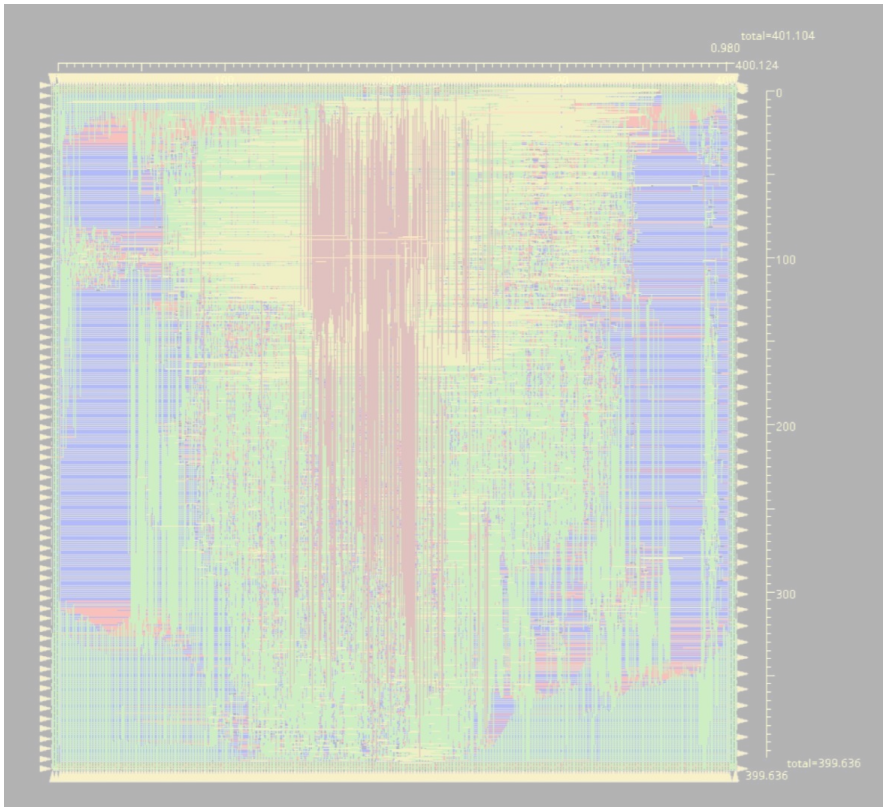
```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:
Total Switching Power:
Total Leakage Power:
Total Power:
-----------------------------------------------------------------------------------------
```

Area:

- Standard cells + Filler cells: **xxx mm^2**

```
================================
Floorplan/Placement Information
================================
Total area of Standard cells
Total area of Standard cells
Total area of Macros:
Total area of Blockag
Total area of Pad cel
Total area of Core: 1
Total area of Chip: 1
```

Snippet from log



Design x and y dimensions screenshot

Name: XXXX
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Innovus density:

- Before filler cell insertion: **XXX**

```
Density

Routing Overflow:
-------------------------------------------------------------
**optDesign ...
*** Finished optDesign ***
```

Number of gates:

- Gates = **xxx**
- Cells = **xxx**

Post_APR – DRC Check:

Post_APR – LVS Check:

(Submit your geom.rpt and conn.rpt, as well as attach your screenshot of them here)

Screenshot of your timing report for the worstcase hold and setup path

One screenshot of the timing report for the worst setup and worst hold. Do not need the top 3 here.

Note:
If you have any additional comments, you can briefly document them here.