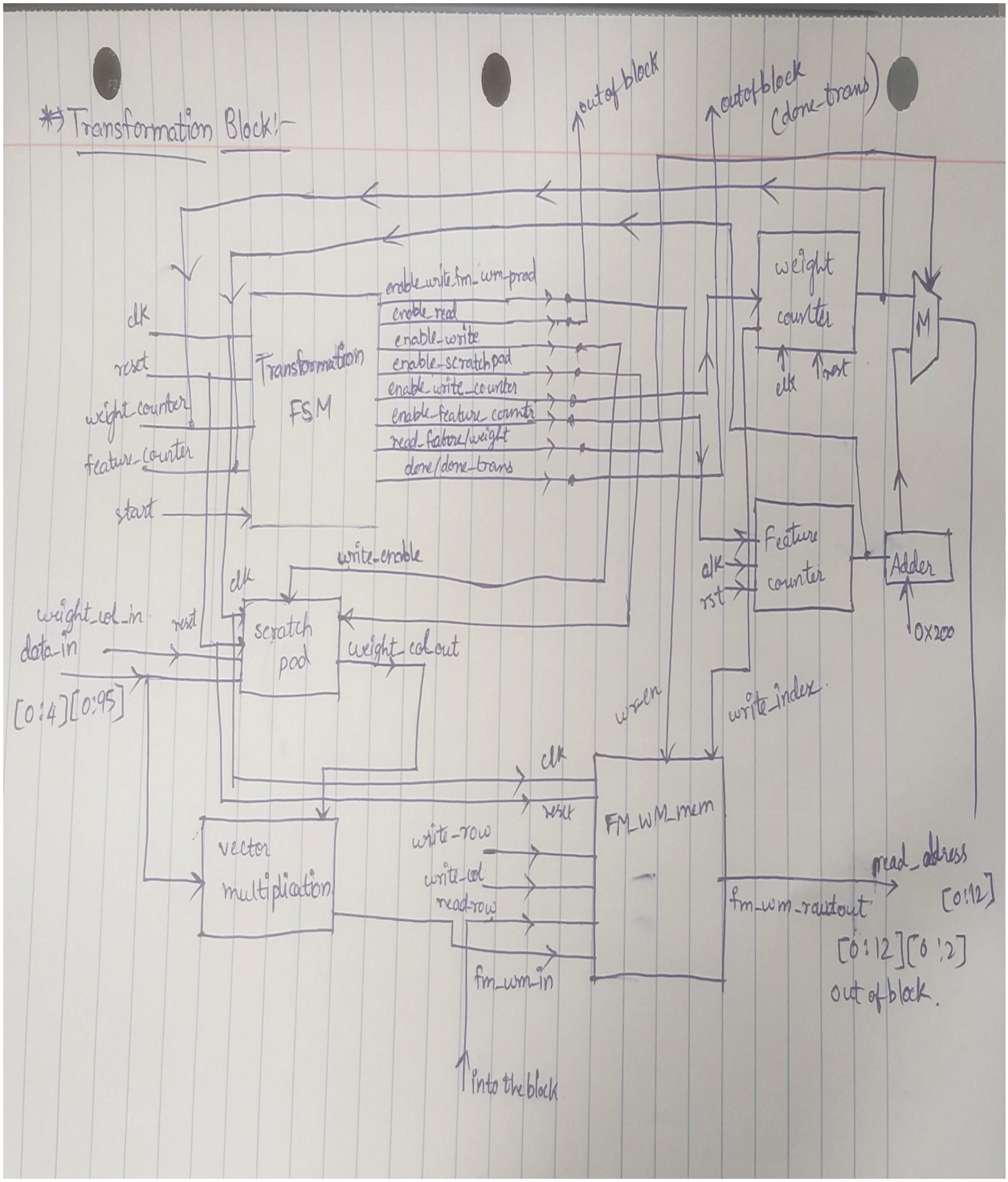
NAME:- ANANTHA SAI CHENNOJU
ASU ID:- 1229918692

EEE 525 LAB4-1

1. Architecture/High-level Block Diagram:

i)



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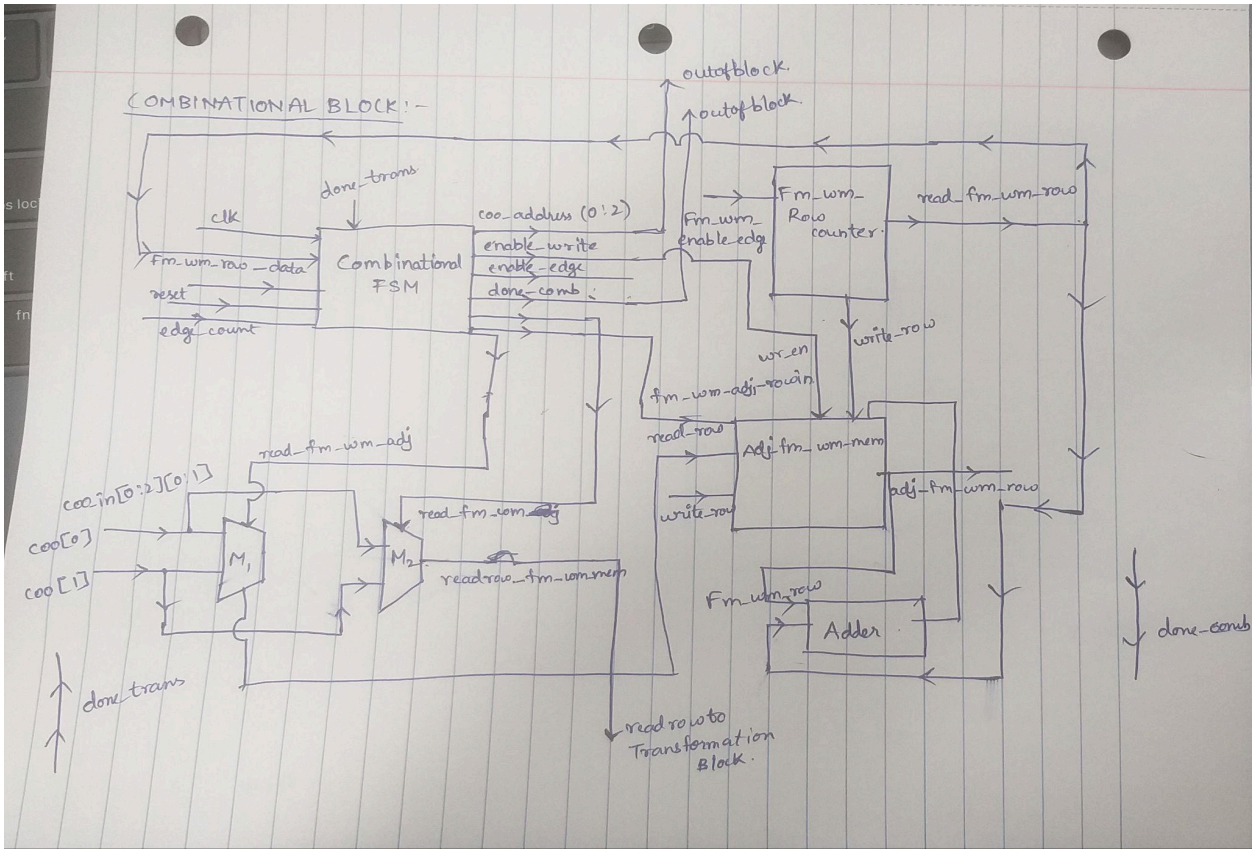
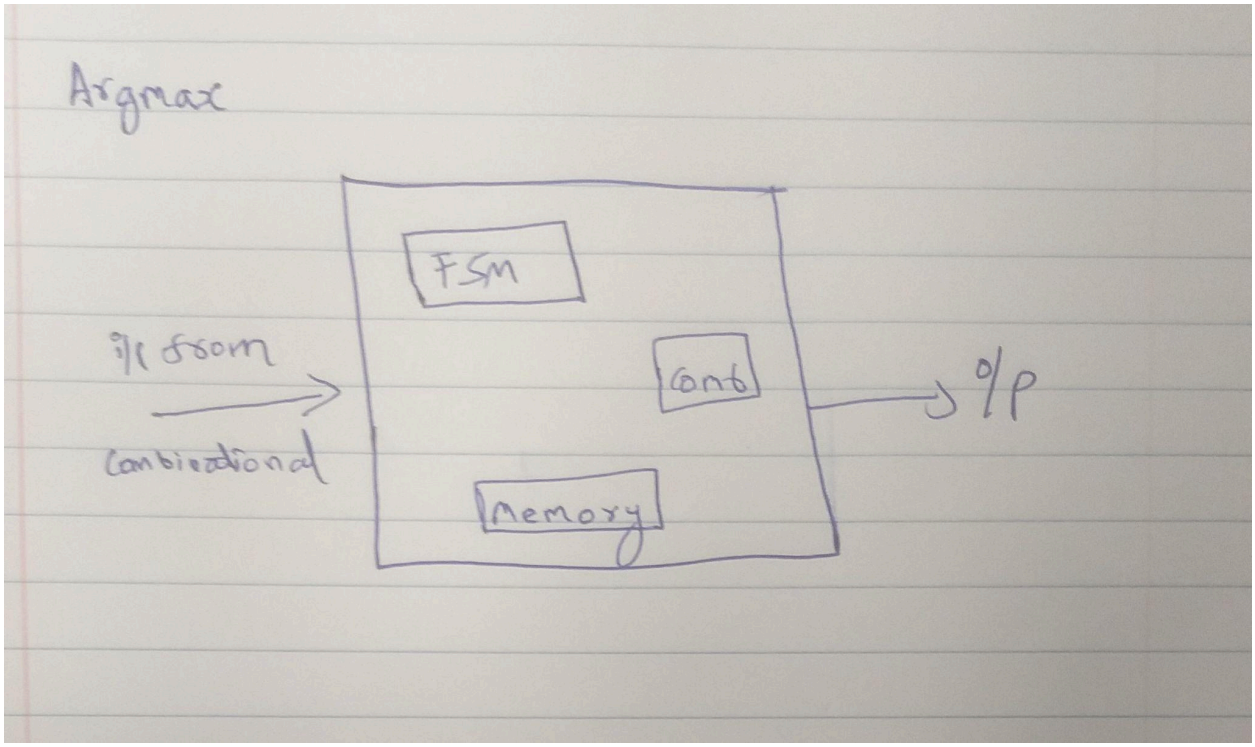
ii)



iii)



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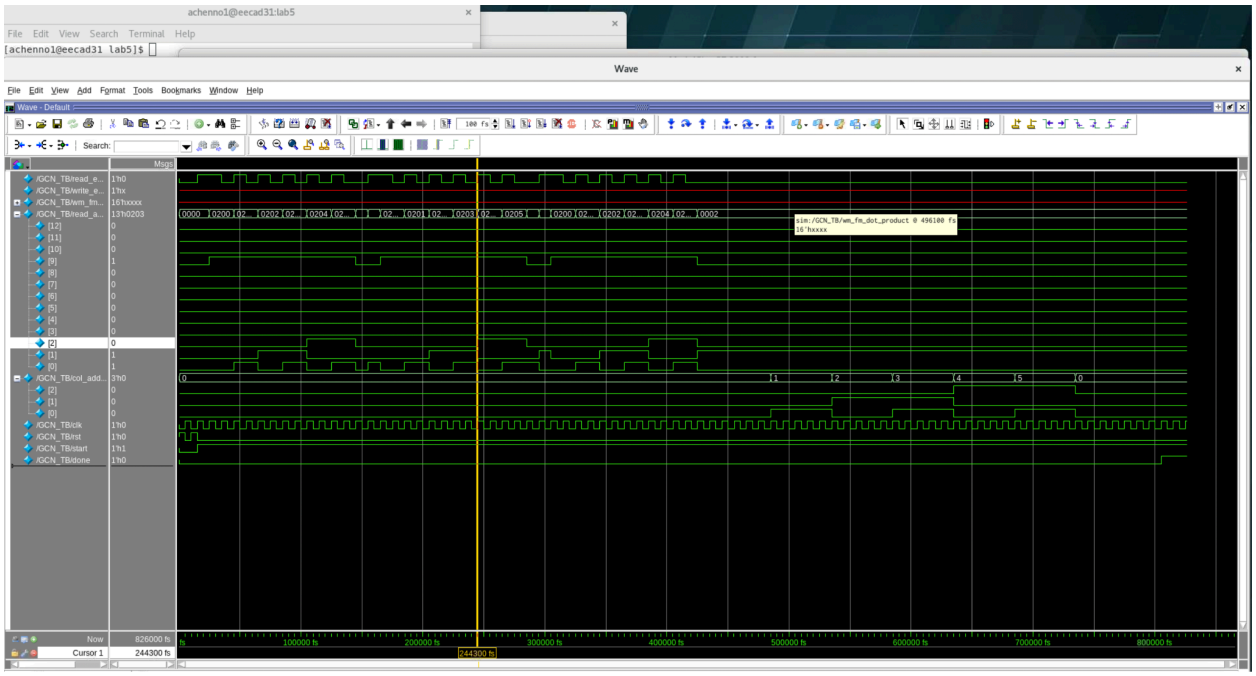
Design decisions

Feature Matrix	1st row	2nd row	3	4	5	6
Weight Matrix	1st col	2nd col	3	4	5	6

Multi-Plication	row1 x col1 ..... row6 x col6

Translate addition	translate COO matrix and add to adj matrix

Behavioral Verilog – Simulation:



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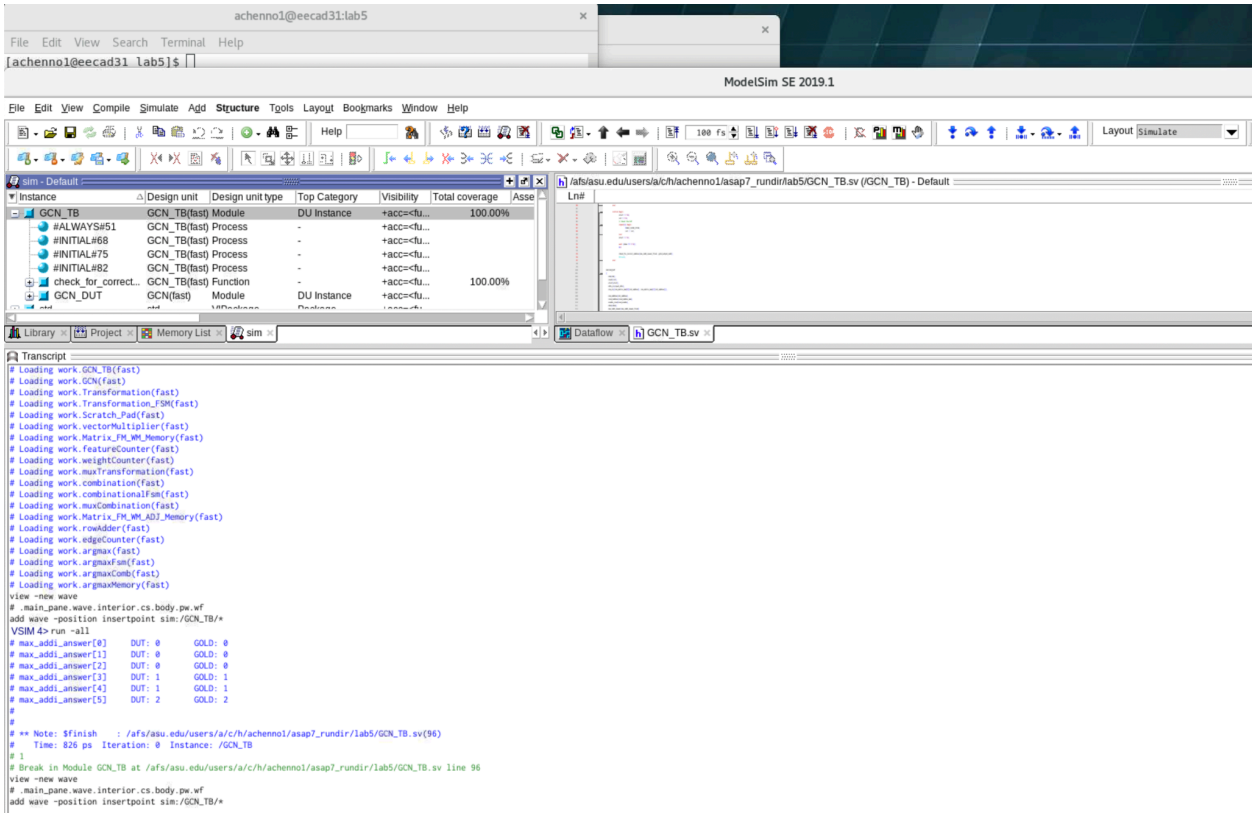
Transcript



Post_Synthesis – Simulation: