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The Significance of Thermal-Aware Universal Chiplet Interconnect Express (UCIe) Interface Design in 2.5D/3D ICs

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***Abstract*— In this paper, signal integrity analysis of universal chiplet interconnect express-advanced (UCIe-A) interface in terms of crosstalk and thermal effects was carried out. As the demands of chiplet systems increase, the need for strong interconnectivity with each chiplet intensifies. UCIe-A is the chiplet-to-chiplet interconnect on advanced package which supports high datarate of 32 Gb/s within small PHY dimension. Therefore, the crosstalk of UCIe-A channel is the dominant signal integrity design issue. Furthermore, as the power consumption of chiplet increases, thermal management of chiplet system becomes more challenging, leading to an increase in temperature along the interconnect. Thermal issue is particularly severe in 2.5D/3D ICs, where the elevated temperatures can significantly degrade signal integrity. Hence, this research focused on the thermal effects on signal integrity of the UCIe-A interface, in terms of channel characteristics, voltage transfer function, and eye-diagrams. The results show that the thermal effect on UCIe-A interface surpasses the crosstalk effect at 80℃. This research validates the significance of thermal-aware UCIe-A interface design for chiplet systems.**

Keywords—Advanced package; Chiplet; Crosstalk; Thermal-aware; Universal chiplet interconnect express (UCIe);

I. INTRODUCTION

For tackling the reticle limitations and yield issues, the chiplet-based heterogeneous integrated system has emerged. The chiplet is a compact ICs that comprise a delineated set of functions, and it is integrated on PKG or interposer to unify with other chiplets. Also, the universal chiplet interconnect express (UCIe) emerges to interconnect between each chiplet. UCIe is the chiplet-to-chiplet interconnect and serial bus between chiplets as shown in Fig. 1. (a). It has two types, UCIe-standard (UCIe-S) for standard packages and UCIe-advanced (UCIe-A) for advanced packages, respectively. UCIe-A is in the UCIe interface for advanced package such as silicon interposer and it supports high datarate of 32 Gb/s [1]. Additionally, the silicon interposer channels have higher losses than standard package channels [2]. Therefore, to support high datarate, the UCIe-A interface design considering signal integrity (SI) is required.

Fig. 1. (b) shows the SI issues on UCIe-A interface. The UCIe-A is implemented within a compact PHY dimension, with 128 channels per 388.8 um. Therefore, the crosstalk of each UCIe-A channel is the dominant SI design issue due to its dense routing. Furthermore, the UCIe-A has a length limitation of less than 2 mm, necessitating the close placement of each chiplet on the silicon interposer, which in turn increases thermal coupling. With the increase in power consumption of chiplets, the

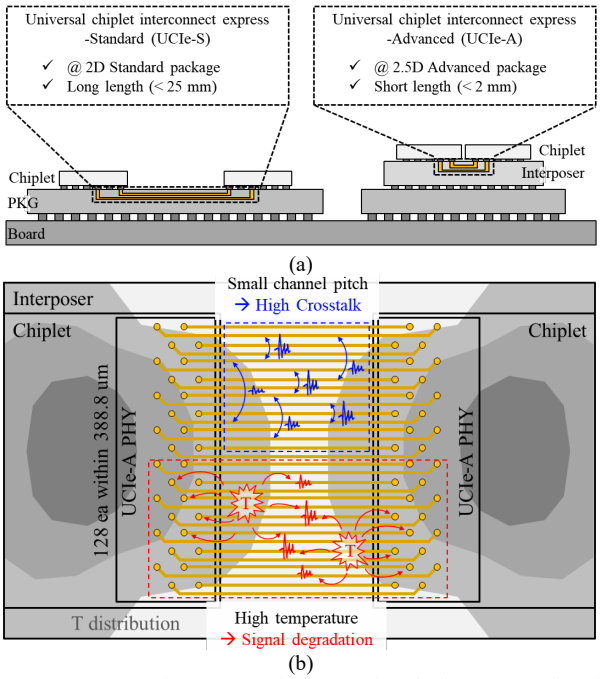

Fig. 1. (a) Concept of UCIe-S and UCIe-A for chiplet system. (b) Signal integrity issues on UCIe-A interface caused by crosstalk and temperature.

management of thermal aspects within the chiplet system becomes more challenging, resulting in elevated temperatures along the interconnect. Especially, this phenomenon is severe in 2.5D ICs, and the high temperature degrades the channel characteristics and driver strength [3], [4]. Therefore, the thermal effects on UCIe-A interface need to be analyzed to ensure guaranteed SI at high datarate.

In this paper, SI analysis of UCIe-A interface with crosstalk and thermal effects was carried out. To analyze the thermal-aware SI of UCIe-A interface, first, we designed the stripline channel on silicon interposer considering UCIe-A routability. Then, we analyzed the SI of channel considering thermal effects in terms of insertion loss and crosstalk. Also, we conducted sensitive analysis of thermal-aware eye-diagram simulation with crosstalk, thermal effects on channel, and thermal effects on input/output (I/O) driver. The results showed that the crosstalk is the dominant SI design issue, but also the thermal effects on UCIe-A interface is important; the thermal effects on UCIe-A interface is larger than crosstalk effect at 80℃. This research validated the significance of thermal-aware UCIe-A interface design for chiplet systems.

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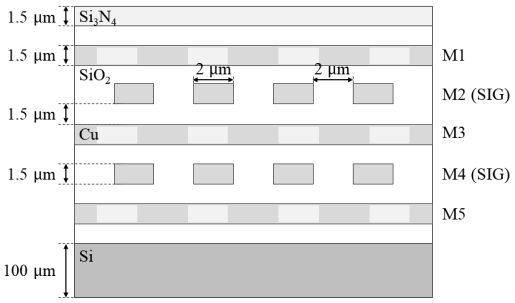

Fig. 2. Stack-up and physical dimensions of silicon interposer for UCIe-A.

II. Design and Thermal-Aware Signal Integrity Analysis of UCIe-A Channel

Fig. 2. shows the designed silicon interposer stack-up with physical dimensions for channel characteristic analysis. The channel was composed of 2 layers and width/space was set as 2 um/2 um considering the routability of UCIe-A interface. Also, the channel was designed by stripline topology for reducing the crosstalk effect to secure SI. The thickness of each layer of redistribution layer (RDL) was set as 1.5 um. The designed silicon interposer consisted of silicon, nitride, oxide, and copper. The temperature-dependent material properties, resistivity ρ and relative permittivity ε_r of each constituent were utilized based on [4].

Fig. 3. shows the simulated insertion loss and power sum far-end crosstalk (PSFEXT) of UCIe-A channels. We simulated the channel with 20℃, 50℃, and 80℃ conditions to analyze the thermal effects on channel characteristics. In terms of insertion loss, as temperature increases, the insertion loss is degraded along overall frequency range. At low frequency range, the increased temperature increases the DC resistance of channel. Therefore, it degrades the insertion loss. At high frequency range, AC resistance and channel self-capacitance are increased with increasing temperature.

Furthermore, we also analyzed the PSFEXT for analysis of the crosstalk effect that came from nearby aggressor channels. The simulation was implemented in 9 coupled channels, 1 victim and 8 aggressors. The PSFEXT also degraded with high temperature due to increased relative permittivity increases the mutual capacitance. However, the values at Nyquist frequency, 16 GHz, are similar in all temperature conditions. This is because the quarter wave resonance is shifted by changed temperature. Since the quarter wave resonance frequency is inversely proportional to relative permittivity, the quarter wave resonance frequency is shift to low frequency as temperature increases. The quarter wave resonance frequency is around 20 GHz which is close to the Nyquist frequency. Hence, the PSFEXT values at Nyquist frequency of each temperature are similar due to both shifted quarter wave resonance frequency and thermal effects on relative permittivity.

III. Thermal-Aware Signal Integrity Analysis of UCIe-A Interface

For SI analysis of UCIe-A interface, it requires channel characteristics, but also the I/O driver. The Tx driver is set as 25 ohm and 0.25 pF, and the Rx driver is set as 0.2 pF,

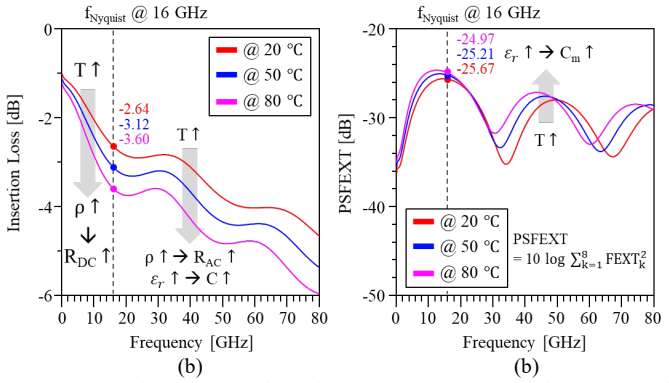

Fig. 3. Simulated temperature-dependent (a) insertion loss and (b) PSFEXT of UCIe-A channels consisting of 1 victim and 8 aggressor channels.

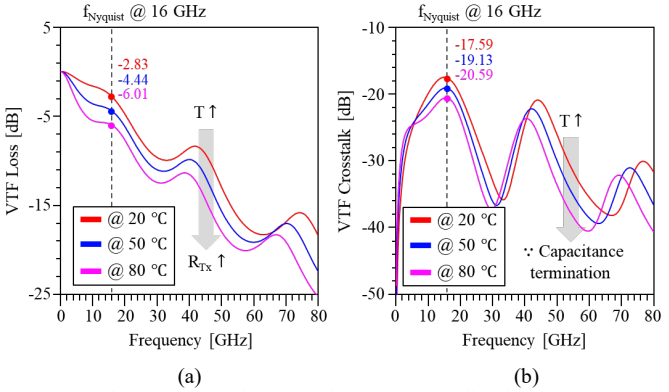

Fig. 4. Simulated (a) VTF loss and (b) VTF crosstalk of UCIe-A interface considering thermal effects on channel and driver.

respectively [1]. To analyze the thermal-aware SI, temperature-dependent I/O driver is required. The resistance of Tx driver is affected by temperature as follows [5]:

$$R_{\mathrm{Tx}}(T) = R_{\mathrm{Tx}}(T_{room})\left(\frac{T}{T_{room}}\right)^{2.3} \quad (1)$$

where R_{Tx} is the resistance of Tx driver, T_{room} is the room temperature, and the T is the temperature parameter in kelvin. In contrast, the capacitances of Tx and Rx drivers are identical with various temperature conditions [6].

Fig. 4. shows the simulated voltage transfer function (VTF)-based loss and crosstalk of UCIe-A interface considering thermal effect. As temperature increases, the VTF loss is degraded along the overall frequency range. It has same trend with insertion loss. Additionally, due to the increased resistance of Tx driver, the loss degradation is severe. Furthermore, the capacitance termination causes shift of quarter wave resonance frequency to higher frequency. This is because the phase changes by up to 90 degrees by capacitance termination. Hence, there is a noticeable difference in VTF values at Nyquist frequency. In terms of VTF crosstalk, it has opposite trends with PSFEXT at Nyquist frequency. This is because the VTF considers not only channel, but also driver. The drivers of UCIe-A interface are capacitance termination, while the standard package consists resistance termination.

Fig. 5. shows the temperature-dependent eye-diagram at various temperature conditions with and without crosstalk. The eye-diagram simulation was conducted at a datarate of 32 Gb/s

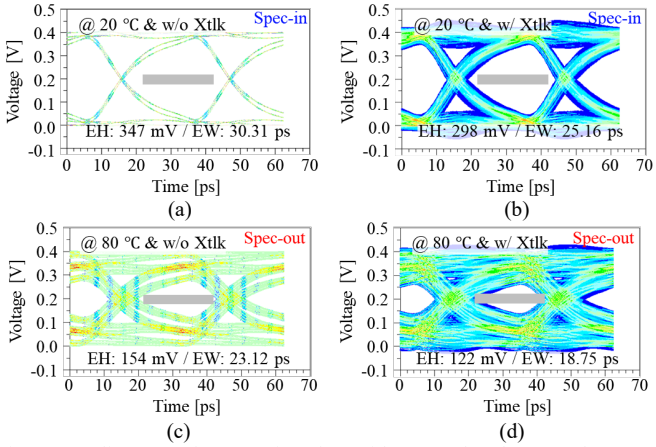

Fig. 5. Eye-diagrams of UCIe-A interface with gray-colored eye-mask (40 mV, 0.65 UI) on various conditions. (a) 20℃ and without crosstalk, (b) 20℃ and with crosstalk, (c) 80℃ and without crosstalk, and (d) 80℃ and with crosstalk.

with 0.4 V swing. Fig. 5(a) and (b) show the crosstalk effect of UCIe-A. The results show that the crosstalk effect is severe in UCIe-A due to its dense routing. In terms of thermal effects on SI of UCIe-A without crosstalk is illustrated in Fig 5(c). It shows the thermal effects on eye-diagram at 80℃. The thermal effect is larger than crosstalk effect compared with Fig. 5(b). Also, the eye-diagram considering both crosstalk and thermal effect is worst among the other conditions as shown in Fig. 5(d).

For a detailed analysis of crosstalk and thermal effects on UCIe-A interface, we conducted sensitive analysis about crosstalk and thermal effects on channel and it on driver. Fig. 6 (a) shows the normalized eye-height (EH) and eye-width (EW) of UCIe-A interface for thermal and crosstalk sensitive analysis. The thermal effect is more critical than crosstalk on EH and EW, at 50℃ and 80℃, respectively. The thermal effects on EH are stronger than the effect on EW. Also, the signal degradation due to the crosstalk worsens as temperature increases.

Fig. 6(b) shows the normalized EH and EW for thermal sensitive analysis. The thermal effects on channel degrade the EH, but its effect on EW is quite small. However, the thermal effects on driver degrades EH, but also EW. Increased temperature increases the resistance of Tx driver and it degrades the driver strength. Therefore, it critically affects the jitter. Also, the thermal effect on driver is more critical than its effect on channel at both EH and EW. The thermal effect on both channel and driver becomes worse than the summation of each effect, separately. Although the crosstalk is an important factor in SI, the thermal effect is more dominant compared to the crosstalk. Furthermore, it was also proved that high temperature induces more severe crosstalk. Therefore, this result shows that the thermal-aware SI design of the UCIe-A interface is inevitable.

IV. Discussion & Conclusion

In this paper, SI analysis of UCIe-A interface in terms of crosstalk and thermal effects was carried out. The crosstalk of UCIe-A channel is the dominant SI design issue. Furthermore, as the power consumption of chiplet increases, thermal effects on SI needs to be considered due to the high temperature degrades the SI. Hence, this research analyzed not only crosstalk, but also thermal effect on SI of the UCIe-A interface. Especially, channel characteristics such as insertion loss and PSFEXT, VTF,

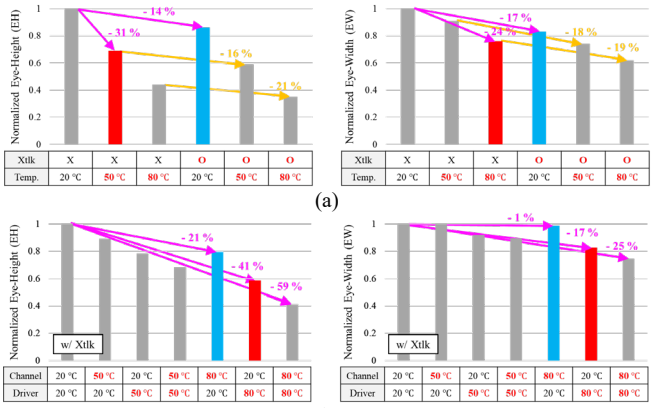

Fig. 6. (a) Normalized EH and EW of UCIe-A interface for thermal and crosstalk sensitive analysis. (b) Normalized EH and EW of UCIe-A interface for thermal sensitive analysis in channel and driver.

and even eye-diagrams are analyzed. The results show that the thermal effect on UCIe-A interface surpasses the crosstalk effect at 80℃. This research validated the significance of thermal-aware UCIe-A interface design for chiplet system. Later, the power consumption of chiplet system will increases, and temperature will increases, too. For securing SI, the thermal-aware SI design of UCIe-A interface is essential. In addition, it is obvious that close placement between chiplets degrades SI due to thermal effect. Nevertheless, the interconnect length will be smaller because it have a significant benefit in terms of SI. In conclusion, it shows that the electrical-thermal co-optimize for chiplet placement is required.

Acknowledgment

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