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Review Article

Chiplet Technology: Revolutionizing Semiconductor Design- A Review

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Abstract

This article explores the transformative journey of semiconductor design from monolithic structures to the cutting-edge era of chiplets. Chiplets, modular components offering specific functionalities, have emerged as a catalyst, reshaping the global semiconductor industry. Their capacity for tight interconnectivity, diverse applications, and cost-effective manufacturing marks a paradigm shift. The article delves into the historical context of Moore's Law, the rise of chiplets, and their impact on the semiconductor landscape. It further discusses key considerations in chiplet architecture, optimization algorithms, and future adoption in industries like data centers, mobile devices, AI, and automotive. Chiplet-based designs promise enhanced efficiency, collaboration, and innovation, heralding a new era in semiconductor evolution.

Keywords: Chiplets architecture, complex-function, manufacturing costs.

1. INTRODUCTION

The technological evolution in semiconductor design has witnessed a paradigm shift from traditional monolithic chip architectures to the innovative era of chiplets. Initially, single-chip designs were predominant, but the limitations posed by size constraints and manufacturing costs led to the emergence of chiplets. These modular components, featuring specific functionalities, enable a more flexible and scalable approach. Chiplets optimize performance, reduce costs, and facilitate customization by combining multiple smaller chips into a cohesive system. This evolution represents a transformative trend, shaping the future of semiconductor design, fostering collaboration, and unleashing new possibilities in diverse industries, from computing to IoT and beyond.

In a rapidly evolving technological landscape and its advancements, the advent of chiplets has become a transformative force, reshaping the global semiconductor industry, Chiplets, with their capacity to integrate small semiconductors into robust systems, have revolutionized the semiconductor landscape. chiplets have emerged as a catalyst, reshaping the global semiconductor industry [1].

Chiplets are individual semiconductor components that can be integrated together to form a complete system-on-a-chip (SoC) or a more complex semiconductor device. Chiplet technology creates smaller, specialized chiplets that can be interconnected to form a larger, more powerful chip. These chiplets can be manufactured separately and assembled onto a substrate or package [2].

Chiplets, or small chips, can be the size of a grain of sand or bigger than a thumbnail and are brought together in a process called advanced packaging [3]. The idea behind chiplets is to break apart the system on a chip into its composite functional blocks, or parts. Sub-elements of a complex-function chip could be made as chiplets, where these sub-elements might include separate computational processor or graphics unit, an AI accelerator, an I/O function, or a host of other chip functions [4]. Chiplets are individual semiconductor components or microchips that are manufactured and designed for specific tasks and are integrated into a larger circuit [5]. Chiplets, essentially are small semiconductors integrated into robust systems, have redefined the conventional norms of semiconductor design and manufacturing. Their capacity for tight interconnectivity has not only propelled performance to new heights but has also introduced a cost-effective paradigm to chip manufacturing. The ability to tightly interconnect chiplets boosts performance and offers a cost-effective approach to chip manufacturing. Bonding chiplets

tightly together can help make more powerful systems without shrinking the transistor size [3].

The technology of ongoing race to reduce transistor sizes, the global chip industry has increasingly embraced in recent years as chip manufacturing costs soar in the race to make transistors so small they are now measured in the number of atoms. The tightly bonded assembly of chiplets is a pivotal strategy for achieving more powerful systems without further reducing the size of individual transistors. This has become particularly crucial as the semiconductor landscape experiences a seismic shift in response to the escalating demand for more potent and energy-efficient electronic devices. In a panel discussion at CadenceLIVE Europe, experts from academia and industry converged to address the limitations posed by Moore's Law and traditional 2D chip architectures.

As the industry grapples with these challenges, the promises of 3D-IC chiplet integration have gained prominence. Chiplets, through decades of industry exploration, have evolved into indispensable components that offer a flexible and efficient solution for various compute subsystems. The potential to revolutionize the semiconductor industry became evident as chiplets opened doors to a whole new level of soft IP reuse, steering away from the monolithic design philosophy that encapsulates everything onto a single chip.

This evolution of monolithic design creates unprecedented opportunities for catering to dedicated needs in analog, radio frequency (RF), compute, and power domains. The modular nature of chiplets allows for the customization of semiconductor systems, optimizing performance for specific functions. Thus, chiplet technology has become a cornerstone in overcoming the limitations of traditional semiconductor designs, ushering in a new era of flexibility, efficiency, and innovation in the global semiconductor landscape. As the industry continues to explore and refine chiplet technologies, the future holds promising prospects for further advancements in semiconductor design and manufacturing.

2. Background and Evolution

In 1965, Gordon Moore, the Co-founder of Intel, made a groundbreaking prediction that has since become widely recognized as Moore's Law. This prediction posited that every two years, the number of transistors on a microchip would double at the same manufacturing cost per silicon area. The implication was a consistent acceleration in the power and capabilities of computers, accompanied by a steady reduction in costs for consumers. Gordon Moore's foresight held true for several decades, earning Moore's Law recognition as one of the most influential guiding principles in modern innovation. Over the years, this prediction materialized as demonstrated by the evolution of Intel's microchips. For instance, the Intel 4004 chip in 1971, with 2,250 transistors and a 10,000nm process, exemplified the doubling trend. Subsequently, the 1974 Intel 8080 chip, featuring 6,000 transistors and a 6,000nm process on a 20mm2 chip, continued this trajectory. This remarkable trend persisted until the early 2020s, with the exponential increase in transistor count contributing to the continuous enhancement of computer performance [6]. However, challenges emerge as the industry approaches physical limits and encounters economic constraints in maintaining Moore's Law as Moore’s Law shows signs of slowdown since 2000. The gap between predictions of Moore’s Law and the actual performance of chips grew by 15 times by 2008. Dennard scaling began to slow down significantly in 2007 and nearly lapsed in 2012 [7, 8]. Despite these challenges, the enduring legacy of Moore's Law has significantly shaped the trajectory of technological advancement, marking a pivotal era in the history of microchip evolution [6].

3. Modularity of Chiplets & Design

The modularity of chiplets, a revolutionary concept in semiconductor design, allows for the creation of highly customized systems by combining smaller, specialized components. This modular approach enhances flexibility, promotes cost-effectiveness, and facilitates the seamless integration of diverse functionalities, ushering in a new era of adaptable and efficient semiconductor architectures.

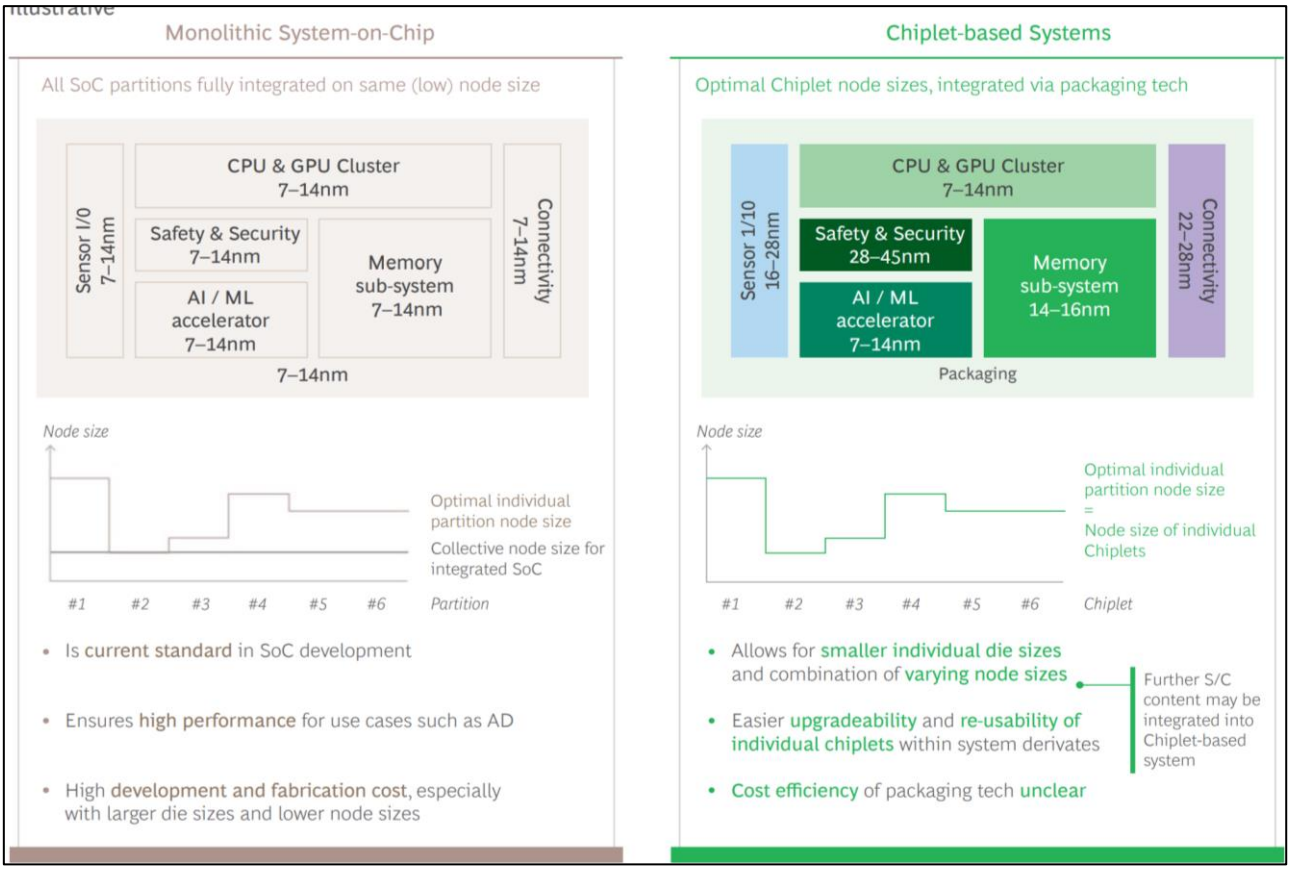
The inherent modularity of chiplets not only optimizes system performance but also offers scalability and ease of upgrades. By breaking down traditional monolithic designs, chiplets enable targeted enhancements in specific areas like processing power, memory, or specialized functions. This flexibility fosters innovation, cost-efficient manufacturing, and adaptability to evolving technological demands, marking a paradigm shift in semiconductor engineering.

Due to Moore framework, chiplet-based design technology addresses multiple challenges. Firstly, it integrates modular chips into a single package, efficiently solving scale, development cost, and period issues. Secondly, advanced packaging technologies like 2.5D and 3D enable high-performance multi-chip interconnection, enhancing system integration, performance, and power optimization. Lastly, modular integration accelerates development speed, lowers costs, and reduces thresholds, shifting the focus of chip research and development towards core technologies and algorithms, significantly boosting overall innovation capabilities [8]. Chiplets improve the optimization potentials on performance and power consumption by recombining multiple small chips. Thus, it supports the domain-specific customization and mitigating the effect from the slowdown of Moore’s law for developing diverse chips.

3.1 Chiplet Architecture and Design:

Compute performance has been increasing exponentially in the past three decades. For supercomputer, there has been 1.25 years per 2x performance increase in the past 30 years. For personal devices, there has been 2.2~3 years per 2x performance increase in the past 15 years. Computing performance boost synchs with transistor count has been increasing. The available power consumption (power wall) limits computing performance. Energy efficiency improvement drives computing performance boost [9].

Chiplet Systems revolutionize System-on-Chip (SoC) design by dividing it into smaller units, or Chiplets, rather than consolidating all partitions on a single die. Leveraging advanced packaging technologies like 2.5D packaging, this modular approach enhances flexibility, performance, and scalability in semiconductor design, marking a significant departure from traditional monolithic structures [15]. Exhibit 1. Chiplet Systems as an Alternative Alongside Monolithic SoC [15].



In chiplet design, critical considerations center around seamless interconnectivity, efficient power distribution, and effective thermal management. Interconnectivity is pivotal for the cohesive functioning of modular chips within a system, influencing performance and data transfer. Effective power distribution ensures that each chiplet receives the required power, optimizing energy usage. Thermal management is crucial to prevent overheating, as densely packed chiplets can generate substantial heat. Ensuring a balanced thermal environment enhances reliability and longevity. The synergy of these key design considerations is imperative, guaranteeing the successful implementation of chiplet technology, fostering optimal performance, energy efficiency, and reliability in semiconductor systems [10].

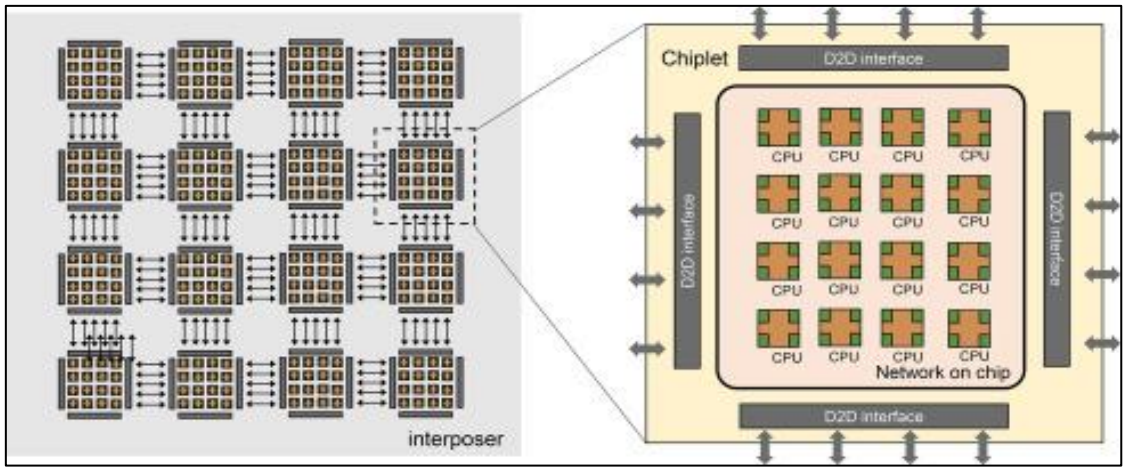
Wang *et al.*, [9] present a multi-objective optimization algorithm that simultaneously optimizes communication consumption and system temperature. By introducing communication and temperature-based heuristic information, a balance is achieved using the weight factor and algorithm, the peak temperature reduced by 8.34 K, and communication power consumption dropped by 232.13uJ compared to the initial layout. This flexibility makes their algorithm adaptable to varying design requirements, offering efficient control over the trade-off between communication power consumption and temperature optimization.

Graening *et al.*, 800mm2 design study seems to indicate that the best size for chiplets is somewhere between 50mm2 and 150mm2 for microprocessor logic and above 200mm2 for random logic they examined the case of a large design that could be built as a single monolithic system on chip (SoC) or as a system of chiplets and show that optimal chiplet size depends on a

wide range of parameters. Their analysis indicates that the smallest chiplet sizes that are viable cost-wise depends both on technology node and on type of logic. The optimal point appears to be 50-150mm2 in 40nm and 40-80mm2 in 7nm for microprocessor type logic [11].

For Zhen *et al*., [12] multi-package architecture was a popular alternative to optimize the reliability and cost for advanced packages to overcome the primary challenge of the multi-package co-design problem, which is the tradeoff between interconnection cost and reliability. Therefore, a co-design methodology was adopted to optimize multiple packages simultaneously to improve the quality of the whole system. To tackle this challenge, they adopted mathematical programming methods in the multi-package co-design problem regarding the nature of the synergistic optimization of multiple packages.

To improve performance, increasing the chip area to integrate more transistors has become an essential approach. However, due to restrictions such as the maximum reticle area, cost, and manufacturing yield, the chip's area cannot be continuously increased, and it encounters what is known as the "area-wall". In their paper Yinhe Han *et al*., [13] provided a detailed analysis of the area-wall and propose a practical solution, the Big Chip, as a novel chip form to continuously improve performance. The Zhejiang Big Chip adopts a scalable tile-based architecture, as illustrated in fig below. This processor consists of 16 chiplets, and it has the potential to scale up to 100 chiplets. In each chiplet, there are 16 CPU processors that are connected via a network-on-chip (NOC), and each tile is fully symmetrically interconnected to enable communication among multiple chiplets. The CPU processors are designed based on the RISC-V instruction set. Moreover, this processor adopts a unified memory system, which means any core on any tile can directly access the memory across the entire processor.



Zhuoping Yang *et al*., [14] first discussed the diversity and evolving demands of different AI workloads and how chiplet brings better cost efficiency and shorter time to market. The authors also discussed about heterogeneous chiplet architecture which is favored to keep scaling up and scaling out the system as well as to reduce the design complexity and the cost stemming from the traditional monolithic chip design.

In the proceedings of ISSCC 2009 [20], Intel presented a series of papers focusing on the Nehalem processor. The plenary session, led by Mark Bohr, underscored Intel's significant investment in advancing system-on-chip (SoC) technology. This commitment was evident in the design of the Core i7 Nehalem, which featured the integration of memory controllers and DDR3 I/Os onto a shared substrate with the CPU cores. Notably, Intel signaled a strategic shift during this period, expressing a vision that extended beyond the traditional PC market, particularly emphasizing interest in dynamic sectors such as mobile technology. Bohr encapsulated Intel's evolution, emphasizing that it was no longer a one-size-fits-all company.

4.Future Chiplet Adoption in Industry & Advantages

Chiplet development is still emerging, but it promises to transform the semiconductor industry and electronics. Here's a peek into the potential future:

***Diverse Specialized Chiplets*:** Expect more chiplets tailored for specific functions, seamlessly combining different capabilities. This will lead to highly efficient systems for tasks like edge computing and scientific research.

***Edge Computing and IoT*:** Chiplets are ideal for making IoT devices more power-efficient and responsive. In edge computing, chiplets enable real-time data processing, fueling smart cities, autonomous vehicles, and intelligent infrastructure.

***Quantum Computing*:** Chiplets could revolutionize quantum computing by offering accessible and scalable solutions. Quantum chiplets, assembling quantum processors, may enhance performance and reliability, pushing the boundaries of computation.

As chiplet technology evolves [19], it is expected to see chiplets being further utilized in some of the following industries prominently.

- **Data Centers:** Chiplets are revolutionizing data center architectures by enabling efficient and modular designs. They offer enhanced performance and energy efficiency while simplifying upgrades and maintenance.
- **Mobile Devices: I**n smartphones and tablets, chiplets can be customized to optimize power consumption, graphics, and AI processing, resulting in improved performance and longer battery life.
- **AI and Machine Learning:** Chiplet-based AI accelerators can be tailored for specific AI workloads, delivering faster inferencing and training capabilities.
- **Automotive:** Chiplets can enhance autonomous vehicles' processing power and safety.

Chiplet architectures are fundamental to the continued economic viable growth of power efficiency of AI, 5G and edge computing [21]. Due to the platform idea, the chiplet approach also allows scaling of computing power. If more power is needed to process AI algorithms, then several of these circuits can be installed on the chiplet system [22].

Chiplet-based designs promise robust growth, driven by following several key advantages [16, 17]:

1. Enhance Chip Production Efficiency:
   - Independent manufacturing of chip modules.
   - Utilizes diverse processes and latest manufacturing technologies.
   - Elevates production efficiency and cost-effectiveness.
   - Mitigates entire chip scrappage, enhancing reliability

2. Facilitate Industrial Collaboration and Innovation:
   - Fosters collaboration across diverse industries.
   - Enables different manufacturers to develop chip modules.
   - Strengthens cooperative ties, accelerating innovation.
   - Introduces a diverse array of product choices to the market.

3. Increased Yield:
   - Smaller chiplet sizes enhance wafer utilization.
   - Minimizes manufacturing defects, ensuring a higher yield.

4. Cost Efficiency:
   - Enables cost savings by combining dies from different nodes.
   - Reduces over-specification and improves purpose-specific fits.

5. Performance Optimization:
   - Task-specific chiplets deliver performance enhancements.
   - Integrated photonics in multi-die packages offer superior bandwidth density.

6. Expanded Chip Area:
   - Overcomes size limitations imposed by reticle size.
   - Allows for larger chip areas compared to monolithic designs.

7. Lower Power Consumption:
   - Reduces interconnection distance and minimizes power loss.
   - Contributes to lower power requirements in chiplet configurations.

8. Flexibility in Development:
   - Chiplet modularity facilitates swift adjustments to product portfolios.
   - Enables design reuse and de-risks system-on-chip development.
   - Shortens design time, promoting flexibility and adaptability.

Chiplets can provide many benefits in the context of processor design in a post Moore's Law world, but effective utilization of chiplets still requires careful engineering and optimization along many different and sometimes conflicting dimensions [18].

In nutshell, the accelerated growth in the advanced packaging market, driven by chiplet technology, presents a substantial opportunity for companies agile enough to embrace and leverage these advancements.

Annexure/s

Different Types of Chiplets for Computation

Types of Chiplets	**Description**
Compute Chiplets	Primary processing units with CPU and GPU cores for executing computational tasks.
Memory Chiplets	Dedicated memory modules like DRAM or HBM enhancing data access speeds and storage capacities.
I/O Chiplets	Interfaces enable communication between chiplets, the external world, and peripherals.
Fabric Chiplets	Facilitating high-speed data transfer and communication between chiplets within a package.
Ref: Cadence	

CONCLUSION

Over the past several years, chiplets have moved from a buzzword to a proven technology, enabling chip shipments in the millions of units per year. Lacking a mature ecosystem, however, chiplet-based design has been available to only large vendors. Now, the industry is poised for broader adoption once D2D interfaces are standardized and a wave of vendors adopt new chiplet-based business models. Customer demand is creating momentum behind this approach, with the ultimate goal of rapid chip design using mix-and-match third-party chiplets. The chiplet approach reduces the cost and time required to develop custom processors. By using an off-the-shelf compute die, customers can focus on developing the IP that differentiates their processor for a target application rather than duplicating a common block. Most of the I/O-hub functions are readily available as IP blocks, so the customer task is primarily integration. Using a compute chiplet also allows customers to use leading-edge process technology for that function, whereas many SoCs lack the volume to justify a monolithic design in that same node.

In summary, the shift from monolithic to chiplet-based semiconductor design represents a revolutionary change. Chiplets offer flexibility, scalability, and cost efficiency, addressing challenges posed by traditional architectures. Ongoing research and studies highlight benefits and challenges, contributing to the continuous refinement of chiplet technology.

The advantages of chiplet architectures, including enhanced production efficiency and increased yield, position them as key players in various industries. Future adoption in data centers, mobile devices, AI, and automotive sectors promises transformative outcomes. As chiplets move towards broader adoption, standardization of interfaces will be crucial, driven by customer demand for rapid and cost-effective chip design.

Thus, chiplet technology heralds a new era in semiconductor evolution, fostering innovation, adaptability, and efficiency in a rapidly advancing technological landscape.

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