Chiplet Communication Link: Bunch of Wires (BoW)

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Bunch of wires (BoW) is a new open die-to-die (D2D) interface that aims to gracefully tradeoff performance for design and packaging complexity across a wide range of process nodes. BoW performance can range from 320 Gb/s/mm with a simple design and packaging to 1+ Tb/s/mm with complex design and/or packaging. BoW directly enables heterogeneous integration, a primary advantage of chiplets. We discuss progress on BoW based on extensive design and performance studies by engineers from multiple companies. These studies aim to make BoW easy to use in a system. This open innovation project will deliver a low-complexity D2D interface with competitive power-performance metrics with the economies of scale for services and technologies associated with an open ecosystem.

Bunch of wires (BoW) is a new open D2D interface that aims to enables a graceful tradeoff of performance for design effort and/or packaging complexity.[1] Basic BoW uses CMOS IOs in a 16-bit source-synchronous DDR bus[2,3] and is designed to be easy to port to multiple process nodes. Basic BoW on an organic laminate with C4 bumps has a raw bandwidth of 80 Gb/s per slice. Slices can be stacked 4-deep to achieve a beachfront bandwidth of 320 Gb/s/mm. For bandwidth similar to 112-Gb/s SerDes, designers can realize 1+ Tb/s/mm of beachfront bandwidth with either more design an optional terminated mode with C4 bumps or more advanced packaging and microbumps. This article reviews results of studies that evaluated design options, implementation complexity, performance, and system integration for BoW: a) at mature (65 nm) and advanced (5 nm) process nodes; b) with regular-sized bumps on organic substrates and with microbumps on advanced packaging (Si interposers, EMIB, InFO, etc.). With this flexibility, BoW uniquely enables heterogeneous integration, a primary advantage of chiplets, across a wide range of process nodes and packaging technologies for products in a diverse price-performance range (high-performance accelerators, NICs, data converters, etc.). No other open interface offers this tradeoff. An open specification and corresponding collateral will enable economies of scale for services and technologies for BoW such as interface IP, packaging, and test, accelerating chiplet adoption.

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BOW DEFINITION

BoW has the following target attributes[4] (while an implementation may achieve higher performance):

- A set of backward-compatible D2D interfaces unencumbered by technology license costs.
- Inexpensive to implement with the flexibility to tradeoff throughput per wire for design, and packaging complexity.
- Portable across: a) process nodes ranging from 65 to 5 nm; b) Multiple bump pitches and packaging technology.

BoW has two modes of the operation BoW Basic and BoW Fast.[1] BoW Basic with optional termination can operate up to 8 Gb/s over 1-mm distance on silicon interposer. BoW Basic with source termination is defined for

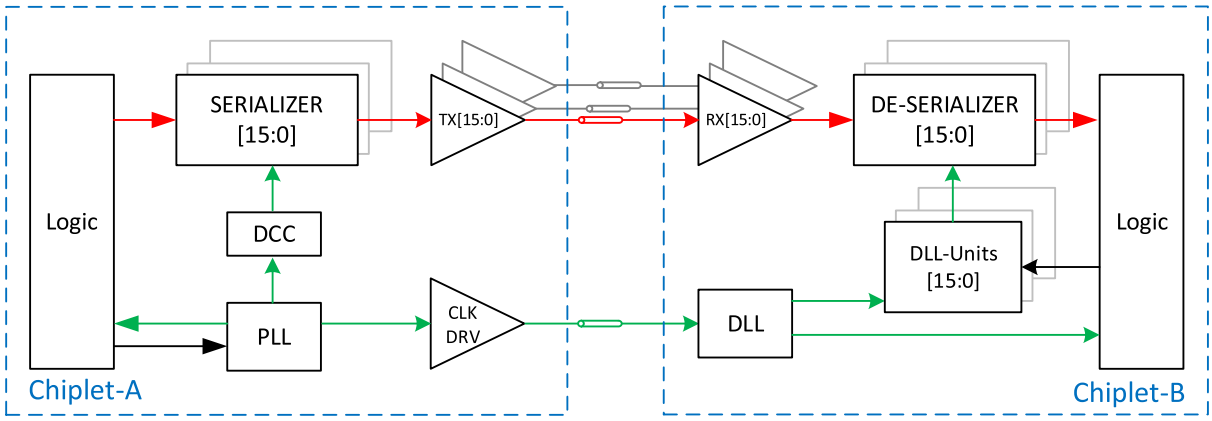

FIGURE 1. BoW reference design.

organic interposer with 5-mm reach at 8 Gb/s. BoW Fast, double terminated, archives 16 Gb/s with 50-mm reach A BoW link may be configured to operate at higher clock and data rates. Figure 1 shows an example implementation of a 16-bit slice. The sending slice (Chiplet-A) transmits clock and data signals. The receiving slice (Chiplet-B) receives both clock and data and phase alignment between clock and data is adjusted.

TO SUPPORT HETEROGENEOUS INTEGRATION, BoW MAY BE IMPLEMENTED USING ANY SUPPLY OR SIGNALING VOLTAGE, BUT MUST SUPPORT A MODE THAT SUPPORTS SIGNALING LEVELS CONSISTENT WITH A 0.75-V SUPPLY WITH A 5% TOLERANCE.

The basic BoW unit is a **slice**, with 18 or 20 signal bumps: 2 for the differential clock, 16 single-ended data, and optional signals FEC and AUX. Each slice is configured to be Tx or Rx and is paired with an Rx or Tx slice on the far end. BoW does not specify a bump map but does mandate a signal order—that Tx signal numbers increase clockwise around the die perimeter, and Rx signal numbers increase in the *counter*-clockwise direction. Figure 2 shows four reference maps on each die, with the mandated signal order between two pairs of connected slices. The *reference* bump maps in Figure 2 use hexagonal closest-packing bump patterns. Other arrangements are permitted if signal/wire ordering is maintained. Most alternatives will use more bump area to optimize other characteristics. The power and ground bumps may be reassigned or placed in two rows. The signal bumps may be placed in more than two rows to minimize wire pitch. The signal bumps may be square packed instead of hexagonal.

Multiple slices may be placed in a **stack**. A logical **link** from one chiplet to another is composed of one or more stacks placed along the chip edge.

DESIGN STUDIES

We review studies for key attributes. The studies focused on choosing options that made package and system integration in heterogeneous systems easier while preserving performance.

Operational Voltages

To support heterogeneous integration, BoW may be implemented using any supply or signaling voltage, but must support a mode that supports signaling levels consistent with a 0.75-V supply with a 5% toler-

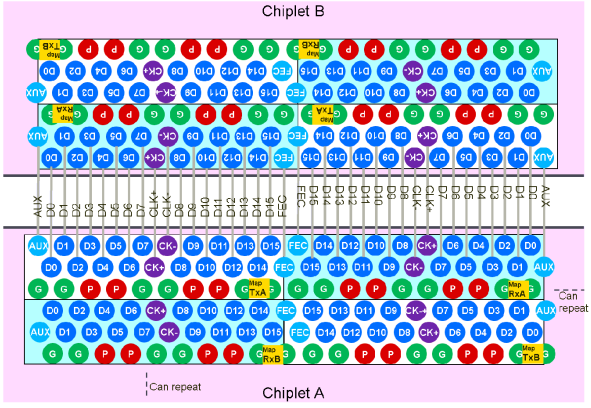

FIGURE 2. BoW Slice.

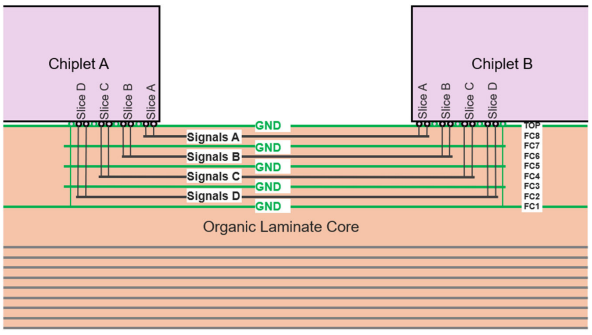

FIGURE 3. Routing a BoW Slice. Cross-section, not to scale.

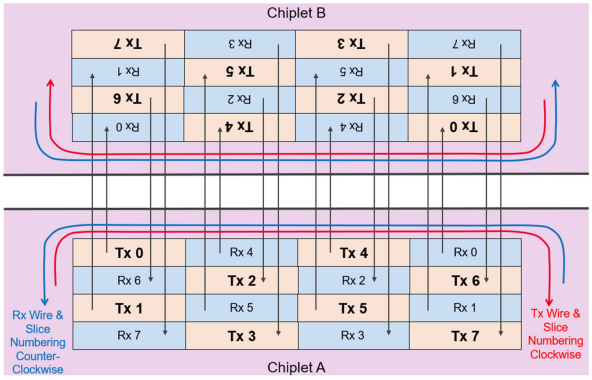

FIGURE 4. Slice number and routing in a multi-slice BoW link.

ance. This voltage is supported in a wide range of process nodes, consistent with the goal of enabling heterogeneous integration.

Package Integration

A basic BoW slice, configured as Tx or Rx, is wired to a corresponding Rx or Tx in the far end chiplet. In any technology, the slice at the edge on chiplet A must be connected to the edge slice on chiplet B (one must be configured for Tx and one for Rx). The next-to-edge slices are connected together, and so on. The mandated signal exit order for a slice is specified to simplify package circuit design. Wires must be short, no more than 10 mm to maintain low wire loss and wire-to-wire skew. Figure 3 shows how the wires for connected slices at the chip edge are routed in a package. The slice is oriented parallel to the chip edge in order to allow flexibility for different levels of packaging complexity.

In an organic package, signal layers should be alternated with ground layers to maintain a controlled impedance of 50 Ω. In interposer or other high-density packaging, the wires for one slice will typically occupy one signal routing layer, the next layer will be ground for signal integrity and the next slice in the stack will be on the next deeper signal layer. In organic laminate packages, a bump pitch of 130 μm and a wire pitch limit of 50 μm are common today. In BoW standard, only the wire order is specified, therefore chiplets with somewhat different bump pitches can be interconnected. Similarly, two slices with different bump patterns can also be interconnected.

Slices can be stacked to increase edge density. There is no specified limit to the number of slices in a stack. An organic package with a low layer count will allow use of just one or two slices in a stack, while a package with more layers supports use of more slices. The practical limit in 2020 is an 8-2-8 laminate, which supports four stacked slices. Layers on the bottom side of the package typically cannot be used for BoW signals due to low via density passing through the thick central core layer. With interposers,[5] InFO[6] and other advanced interconnect technologies that allow bump pitches of 50 μm or less and wire pitches below 10 μm, the wires for multiple slices might be interleaved on a single signal layer in the interconnect.

For a bidirectional link, the preferred arrangement of slices is in a checkerboard of Tx and Rx slices, as shown in Figure 4. In the slices aggregated in a link, the slices can be ordered so as to minimize package routing complexity for the entire link. The slice numbering follows the same direction as the wire numbering in a slice: Tx slices are numbered in ascending order clockwise along the edge of the chip; Rx slices are numbered in ascending order counterclockwise. Slice numbering restarts on a new link. In the checkerboard, the slices nearest the edge on the two chiplets are wired to each other; the stacked slices second-nearest to the edge are also wired to each other, and so on. The clockwise polarity allows interoperation of chiplets at any n*90° rotation without requiring wire order reversal hardware, a feature unique to BoW.

Slices may be assembled into asymmetric links or unidirectional links and the stack depth is an implementation choice (4 slices per stack may be a practical limit for organic substrates). Two chiplets with different stack depths may be connected by configuring the active slices at powerup.

A basic BoW slice that is configurable to operate as either Rx or Tx simplifies packaging and can be used for self-test. The additional circuit area is small compared to the bump array area. In a future extension, full-duplex slices may be supported.

System Logic Integration

A BoW interface instance will interface with the logic in a chiplet through a MAC or a controller. A transaction protocol controller for protocols such as PCIe, CXL, and CCIX will typically contain both the transaction and link layers.[1]

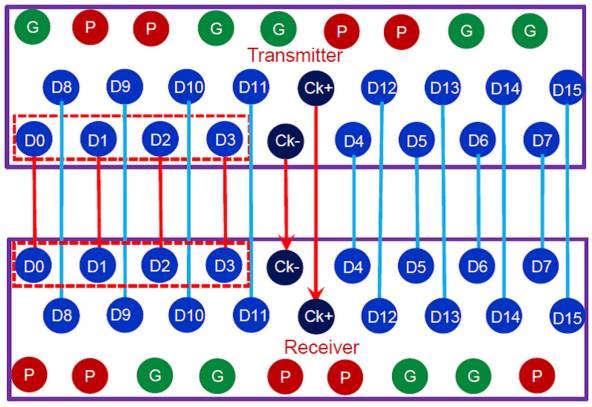

FIGURE 5. In-band initialization proposal for a BoW link.

Link/System Initialization

When powered on, all the BoW links in a system will need to be initialized, tested, and trained to operate. BoW is exploring two options to support initialization: a) virtual registers and b) in-band initialization. With virtual registers, the link relies on an external control mechanism such as I2C, SPI, or JTAG to exchange status information and update the status registers. Readers are referred to BoW GitHub report[4] for more detail.

The second approach to exchanging information is an optional in-band mechanism. This proposal requires at least four pads in the Transmitter and Receiver to have low-speed bidirectional capability. Once the two sides are reset, the Transmitter initiates this mode and inform the Receiver by sending the clock to Receiver and toggling its pads at low frequency D0-D3 (e.g., 1/N the nominal baud rate, with $N>8$) from "0" to "1" one at a time continuously with a "known pattern." When the Receiver detects the "known pattern" for more than M cycles ($M>1$), it also enters the link initialization mode. The receiver sends back an acknowledgement pattern on its pads D0-D3 once (at same low baud rate) and stays at last setting. Once the transmitter gets receiver's acknowledgment, both sides are in Startup/Training Mode, and any future values on the pads D0-D3 are to communicate to each other the startup/training states. The four pads provide 16 distinct states to be communicated to the other side, such as, duty-cycle-cal, DLL-lock, offset-cal, PCS-byte-alignment, MAC-ready, etc.

BoW Testing

A BoW interface will be used for loopback testing[8] in two use cases: a) at wafer-sort time for chiplet test; b) for full-system bring-up and debug validation. Wafer sort tests are currently only practical for the BoW interface with regular bump pitches (~130 μm), where automatic testing equipment (ATE) probe boards with matching pin pitches are available. Microbump probes will require additional effort.[9]

TABLE 1. AIB-BoW comparison.

Parameter	*AIB+*	*BoW Basic Laminate/Advanced*
Dataplane		
Voltage (V)	0.7-0.9	0.75
Bump Pitch (um)	≤55	≤150 / ≤55
Clock	1 GHz	1-2.5 GHz
Data Rate	DDR	DDR
Channel Length (mm)	4	10
I/Os	Unidirectional	Unidirectional
BW per bump (Gbps)	2	2-5
Basic unit	Channel	Slice
Bits/unit	20	16+2
Bump Map	Specified	Reference
Chip edge orientation	Perpendicular	Parallel
Substrate	Advanced	Laminate/Advanced
Clocking	Differential	Differential
Clock loopback Rx	Yes	Optional
DCC	Yes	Optional
Ck/Data Phase Adj	Yes (DLL)	Yes
Control plane		
Power on reset	Yes	Yes
NS_MAC_RDY	Yes	Yes
FS_MAC_RDY	Yes	Yes
Sideband control	Yes	Optional
Redundancy	Yes	No
Config done	Yes	Yes
Link training	No	TBD
BIST	No	Yes
Rx termination	No	Optional
Tx termination	No	Yes/Optional
FEC	No	Optional
DBI	No	Optional

Unidirectional links will need open-loop testing. In open-loop testing, a chiplet transmits to (receives from) a golden reference receiver (transmitted) through the ATE load board. With bidirectional links, loopback mode tests can be implemented. In the short loopback mode, data are looped back within the chip. The short loopback can be triggered by the ATE. In the long loopback mode, the PRBS pattern is generated by chiplet-A, sent over the channel and received by chiplet-B. The received pattern will be passed to a bit error rate tester (BERT) to analyze the performance of the link with off-chip data and clock wires.

Both loopback modes can potentially be used for in-field validation bring-up and test.[1] Cooperation across chiplets will be required to execute these tests in the field. Open-loop testing requires the use of a fixed test pattern recognized by both ends and is the only option for unidirectional links. Long loopback

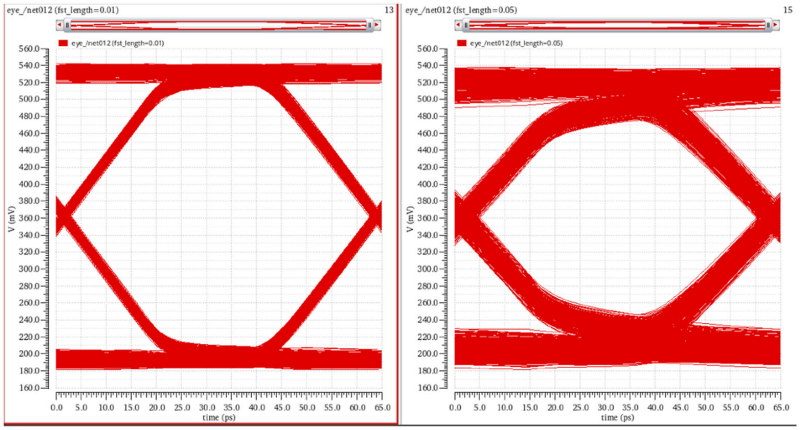

FIGURE 6. Eye-diagram 16 Gb/s (a) 10 mm. (b) 50 mm.

mode can be implemented on interposer or organic laminate for validation/verification purposes.[1]

Interoperation With Parallel D2D Interfaces

BoW Basic can potentially interoperate with parallel D2D interfaces such as AIB,[10] HBM,[11] and Open HBI,[3] that use advanced packaging for chiplet-based products. As an example, Table I compares AIB+ and BoW. As can be seen, BoW includes several features to scale across substrates. In the data plane, a BoW slice can be electrically connected with an AIB Channel with up to 18 signal wires.

Chiplets with BoW interfaces can connect to chiplets that support the AIB interface, such as the Stratix FPGA product line from Intel.

PERFORMANCE STUDIES

This section discusses design-performance and package-performance tradeoffs with BoW.

Scaling With Design

BoW Fast performance has been analyzed using a link test structure with a behavioral model of CMOS driver, same as the model used by Ardalan *et al.*[1] for BoW basic. The source termination and driver capacitive parasitics (e.g., ESD, bump) are modeled as simple R, C elements. The receiver is modeled as 40-Ω termination to half of the supply voltage, along with capacitive parasitics.

For package traces (in organic substrate), a 2-D field solver is used to extract the RLGC model of a 5-bit bus with typical trace width (25 μm) and spacing (25 μm) and height (18 μm) of above/below reference planes. The nominal impedance for this stripline configuration is $\sim$39 Ω, using GX92 dielectric material. The model includes crosstalk components for the bus. Each I/O is simultaneously stimulated with an independent PRBS source (n = 27-31): Bit period (UI) -62.5 ps; T_{rise} and T_{fall} –25 ps. Eye diagrams for two channel lengths are shown in Figure 6.

The 55-mm trace compares to 10-mm, has $\sim$5-ps eye-width and $\sim$60-mV eye-height degradation. In summary, a simple CMOS driver with source termination and far-end termination to half the supply can deliver 16 Gb/s over 50 mm with standard package materials and trace geometries.

Scaling With Packaging

The tradeoff between bandwidth density and IP complexity enabled by BoW is evident with further study across package technologies for key data rates (shown in Figure 7). For this comparison, bandwidth density per mm of chip edge and per 0.1 mm^2 of chip area (for better visualization) is evaluated for data rates of 5, 8, and 16 Gb/s. The increasing data rates represent increasing complexity of BoW implementation. Combinations that may require expensive implementation are included in the analysis but are grayed out, including 16 Gb/s/lane implementations at very fine bump pitches. One observation is that nearly equivalent bandwidth density per mm of chip edge is achievable by either implementing a lower data rate BoW (5 Gb/s) at a denser 40-μm bump pitch or a higher data rate BoW (16 Gb/s) with a less-dense 130-μm bump pitch, with the latter occupying less overall silicon area. BoW is unique as it enables a choice to invest in package technology or higher performance circuit design to achieve compelling bandwidth density metrics.

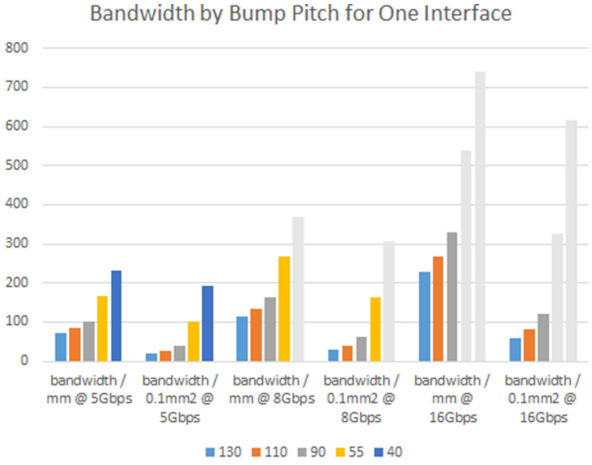

FIGURE 7. BoW performance comparison.

TABLE 2. BoW status summary.

Parameter	*Original Target*	*Current Status*
BoW Basic/Wire	4 Gbps, 10 mm Unterminated	5 Gbps, 10 mm with source termination
BoW Fast/Wire	16 Gbps, 50 mm Destination Term	16 Gbps, 10 mm with double termination
Process Nodes	28 nm to 5 nm	65 nm to 5 nm
Packaging	Basic/Advanced	Basic/Advanced
Physical Spec	Bump Map	Wire order
Control/Operation	Mode bit	Virtual wire
Testing	Not defined	Loopback testing
Txn protocol	Standard (e.g.PCIe), Custom protocols	PIPE/LPIF adapter MAC interface

THE OPEN INNOVATION MODEL FOR THE BOW INTERFACE HAS GROWN ACTIVE PARTICIPATION AND ENABLED A WIDE RANGE OF USE CASES TO BE CONSIDERED IN FURTHER DEVELOPING THE BOW. THE SHAREABLE COLLATERAL MADE POSSIBLE BY AN OPEN DEFINITION AND SCALABILITY OF THE INTERFACE WILL ENABLE ECONOMIES OF SCALE.

CONCLUSION

Table II summarizes progress on BoW attributes against targets set in the initial paper or subsequently.

The analyses show that it is possible to meet the objectives of creating a high-performance interface that enables: a) a performance-cost tradeoff; b) heterogeneous integration; c) multivendor integration. The ODSA also has a set of activities to develop collateral to make the interface easier to use including: a) a test chip and a packaging prototype; b) Interface adapters to carry off-package (PCIe, CXL, CCIX) and on-die (AXI, TileLink) protocols on D2D interfaces; c) A proposal to build a test probe card based on the reference bump pattern.

The open innovation model for the BoW interface has grown active participation and enabled a wide range of use cases to be considered in further developing the BoW. The shareable collateral made possible by an open definition and scalability of the interface will enable economies of scale. The performance, scalability, and economics of the BoW interface should make it a strong contender to meet the D2D requirements of a wide range of use cases.

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