Special Session Paper

Understanding Chiplets Today to Anticipate Future Integration Opportunities and Limits

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***Abstract*—Chiplet-based architectures have recently started attracting a lot of attention, and we are seeing real-world architectures utilizing chiplet technologies in high-volume commercial production in multiple mainstream markets. In this special session paper, we provide a technical overview of the current state of chiplet technology including its benefits and limitations. This provides background and grounding in the current state-of-the-art and also lays out a range of technical areas to consider for the remaining forward-looking papers in this special session. We discuss the benefits and costs of different approaches to splitting and modularizing a monolithic chip into chiplets. In particular, we cover supporting high bandwidth and low latency communication between the die, mixed integration of multiple process technology nodes, and silicon and IP reuse. We then explore future challenges for chiplet architectures looking into the next decade of innovation.**

***Keywords*—chiplets, integration, process technology**

I. Introduction

Over the past several years, the continued slowing down of Moore's Law combined with the end of Dennard Scaling has created a variety of potential headwinds for the continued improvements of processor designs. In response to these challenges, the industry is increasingly looking toward advanced integration and packaging technologies to help keep processor capabilities moving forward [1].

While the general idea is not new [2], recent advancements in certain technologies have made "chiplets" a viable and effective technology to help fight against the slowing of Moore's Law. Traditionally, microprocessors are implemented as a single monolithic die of silicon. The chiplet approach takes a system-on-chip (SoC) design and repartitions it across multiple smaller chiplets. Coupled with integration technologies that allow high-speed communications between chiplets, the functionality and performance of a monolithic SoC can potentially be realized in a more cost-effective and scalable module with multiple chiplets.

II. Current State of Chiplet Technology

A. Motivation

The historical rate of Moore's Law delivered a doubling in the number of transistors per unit area every 18 to 24 months. In turn, processor designers have continually used the additional device count to construct more powerful microprocessors. Figure 1 plots the peak performance of the world's fastest supercomputers over the past several decades. Even before the slowdown of Moore's Law, the peak performance of these machines was increasing faster than the

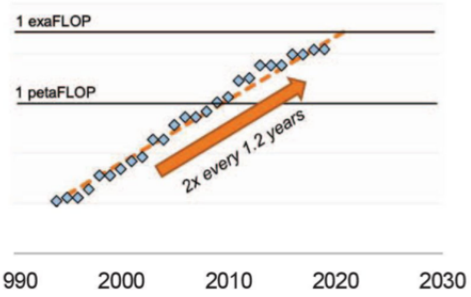

Figure 1. Peak performance of the world's fastest supercomputers.

rate of the corresponding device densities. This trend does not appear to be slowing down as several recent exascale-class supercomputers have been announced [3][4]. The challenge for the industry is finding ways to continue to deliver ever increasing performance and capabilities in a world where the underlying silicon no longer provides the same historical rate of density improvements.

B. Background

If the underlying silicon technology is not providing the increases in device density that one historically would expect, one possible path for increasing processor capability and

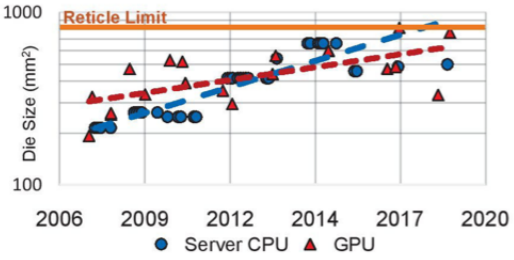

Figure 2. Microprocessor die sizes over time [1].

performance is to build larger chips. As a hypothetical example, if a new technology node only provides a 1.5× increase in device density, then building a chip that is 33% larger can still provide an overall increase in total device count

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