Design and Evaluation of Chiplet Interconnect Standards for Efficient System Integration

Project Overview:

This project aims to explore, compare, and implement chiplet interconnect standards to enable scalable and efficient communication between heterogeneous chiplets (e.g., CPUs, GPUs, AI accelerators, memory). By leveraging industry standards such as UCIe (Universal Chiplet Interconnect Express), BoW (Bunch of Wires), and OpenHBI (High Bandwidth Interconnect), the project will identify the most suitable protocol for high-performance, power-efficient chiplet-based systems.

The outcome of the project will include the design, simulation, and evaluation of interconnect solutions based on these standards, considering factors such as bandwidth, latency, power consumption, and compatibility with advanced packaging technologies like 2.5D interposers and 3D stacking.

Project Goals:

1. Research and Comparison of Chiplet Interconnect Standards:
   - Identify and study the key features, capabilities, and limitations of UCIe, BoW, and OpenHBI standards.
   - Analyze their performance (bandwidth, latency), power efficiency, and scalability for different applications (e.g., AI, high-performance computing).
2. Simulation and Design of Interconnect Fabric:
   - Design a prototype interconnect fabric using one or more of these standards.
   - Simulate the performance of the chosen interconnects in 2.5D and 3D stacked environments using industry-standard EDA tools.
   - Implement the interconnect in a virtual chiplet-based system (using tools like Gem5 or MATLAB/Simulink).

3. Evaluate Performance Metrics:
   - Measure and analyze the bandwidth, latency, and power consumption of each interconnect standard.
   - Assess the feasibility of integrating chiplets from different vendors, considering modularity and compatibility.
   - Simulate the thermal impact of the interconnect in advanced packaging environments (using tools like ANSYS or COMSOL).

4. Develop a Roadmap for Future Scalability:
   - Propose a scalability plan for the chosen interconnect standard(s), focusing on support for future chiplet generations (e.g., optical interconnects, 3nm/2nm nodes).
   - Ensure compatibility with evolving packaging technologies (e.g., optical interfaces, heterogeneous integration).

Key Deliverables:
- Research Report on the comparison of UCIe, BoW, and OpenHBI standards, highlighting strengths, weaknesses, and suitable use cases.
- Interconnect Fabric Design: Schematic and layout of an interconnect fabric based on one or more standards, optimized for chiplet integration in 2.5D or 3D packages.

Target Audience:
This project is designed for chip architects, hardware engineers, and system designers interested in developing scalable multi-chiplet systems using standardized interconnect protocols. It is especially relevant for industries developing AI processors, high-performance computing (HPC), and heterogeneous computing platforms.
standard into emerging packaging technologies.

This project will provide valuable insights into the next-generation of chiplet-based systems, offering a detailed understanding of how standardized interconnect protocols can be implemented in cutting-edge designs.