

LAB 4

Deliverable 2: Generate an 8Hz Clock

We need a value $CLOCK_DIVIDER_TC := 6.25 \times 10^6$, which requires 23 bits.

Deliverable 3: Testbench and Screenshots

Testing Plan

1. Wait off for a few clock cycles. All LEDs should be off.
2. Flip both switches to test hazard mode. All LEDs should blink on and off simultaneously.
3. Test right turn by setting the left_switch low. We should see the cascading R* LEDs.
4. Test the left turn by flipping the right switch off and switching the left switch on. Also test that the signal runs to completion by flipping right switch on mid turn signal.

Annotated Screenshot of Simulation



Figure 1: Annotated Simulation Screenshot

VHDL Testbench

On Canvas.

Deliverable 4: Constrain File

On canvas.

Deliverable 5: Program the FPGA

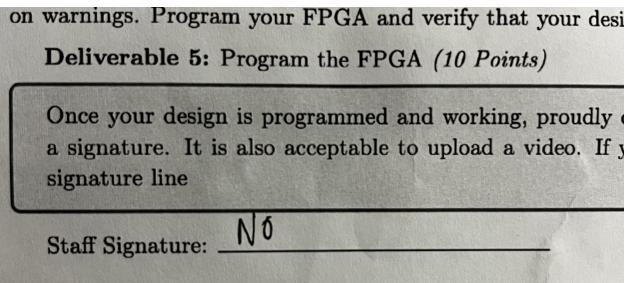


Figure 2: TA Signature

Deliverable 6: Final Design

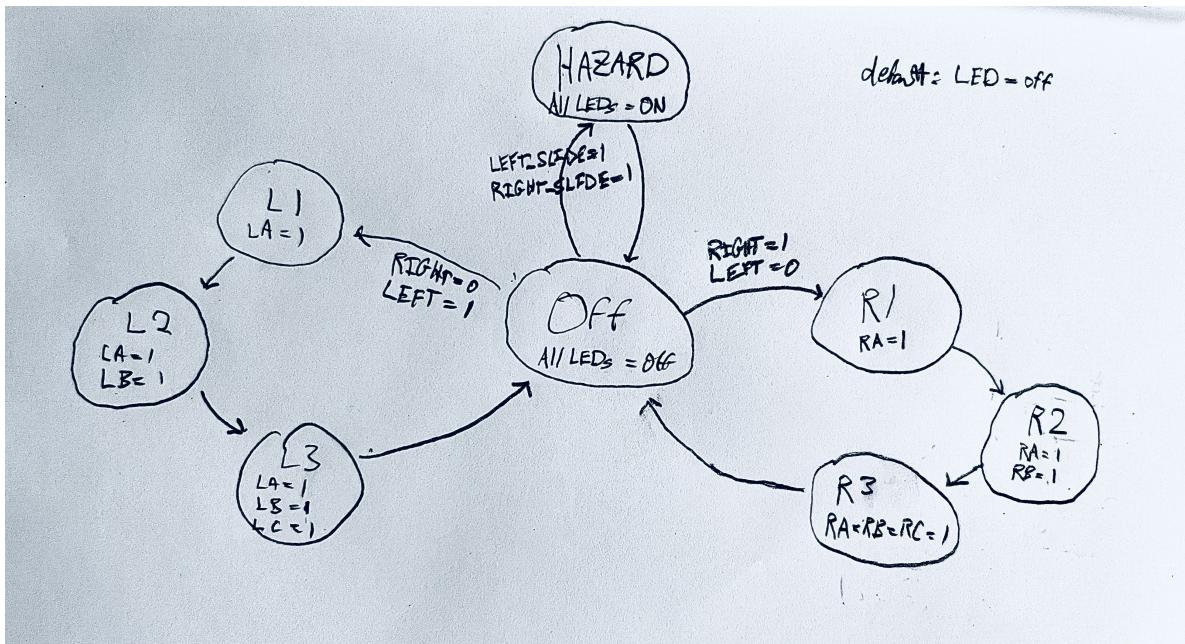


Figure 3: Final State Machine Diagram