

LAB 5

Deliverable 1: Block Diagram

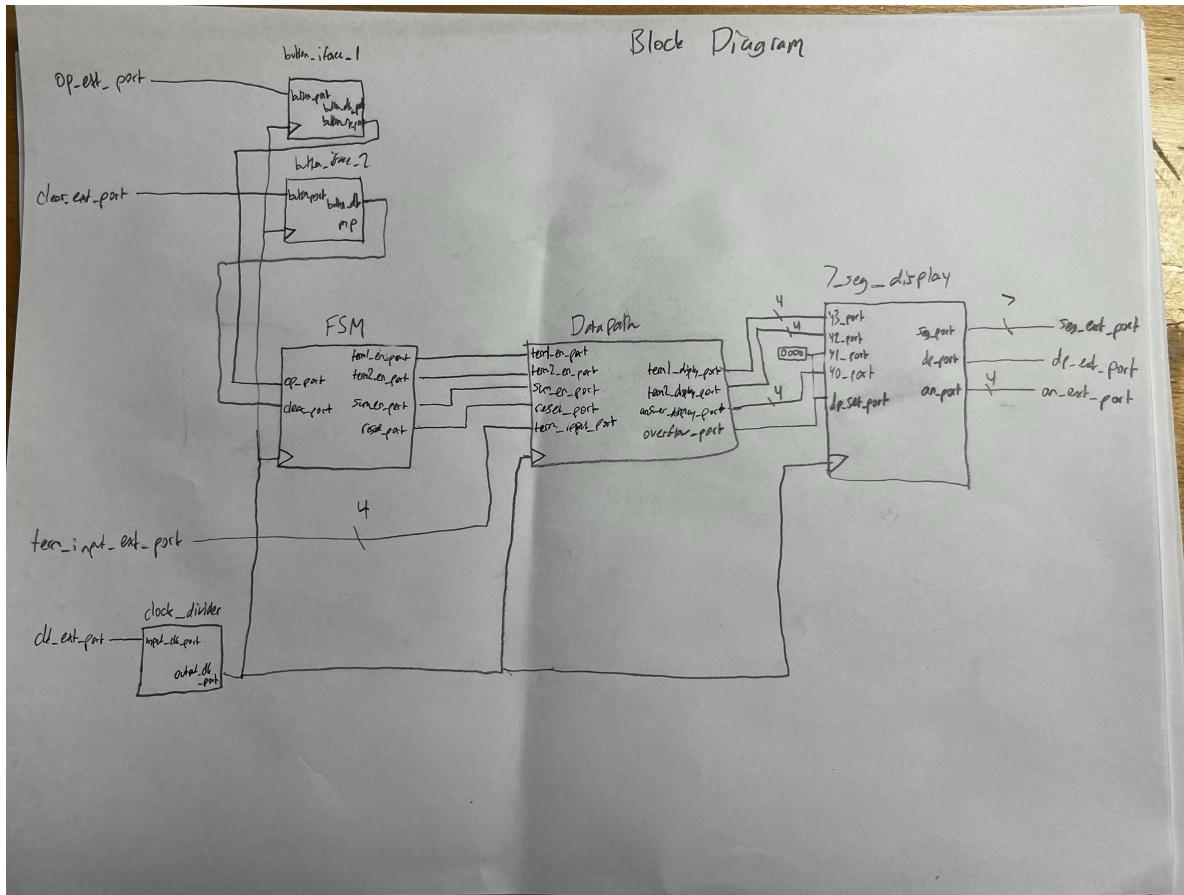


Figure 1: Block Diagram

Deliverable 2: Datapath RTL Model and VHDL

See VHDL file attached separately...

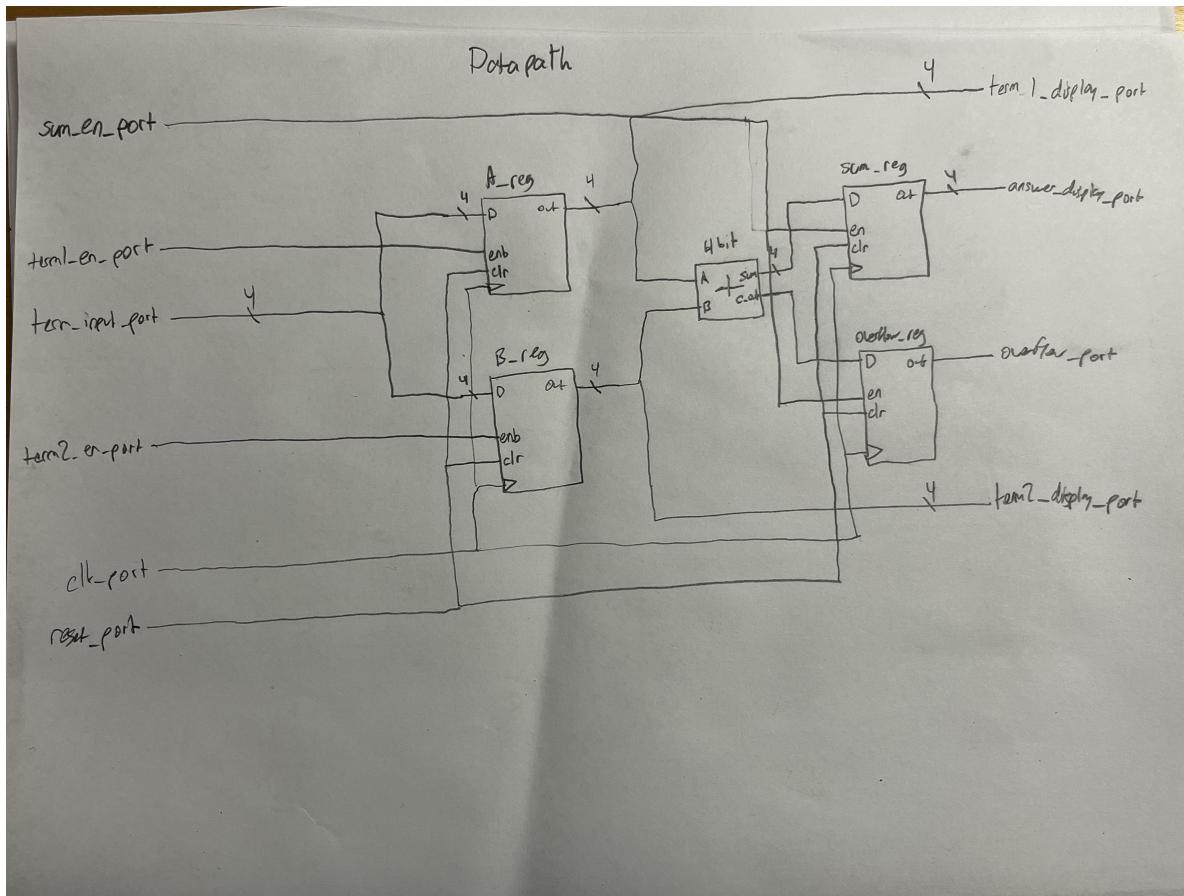


Figure 2: Datapath RTL Diagram

Deliverable 3: State Machine

See VHDL file attached separately...

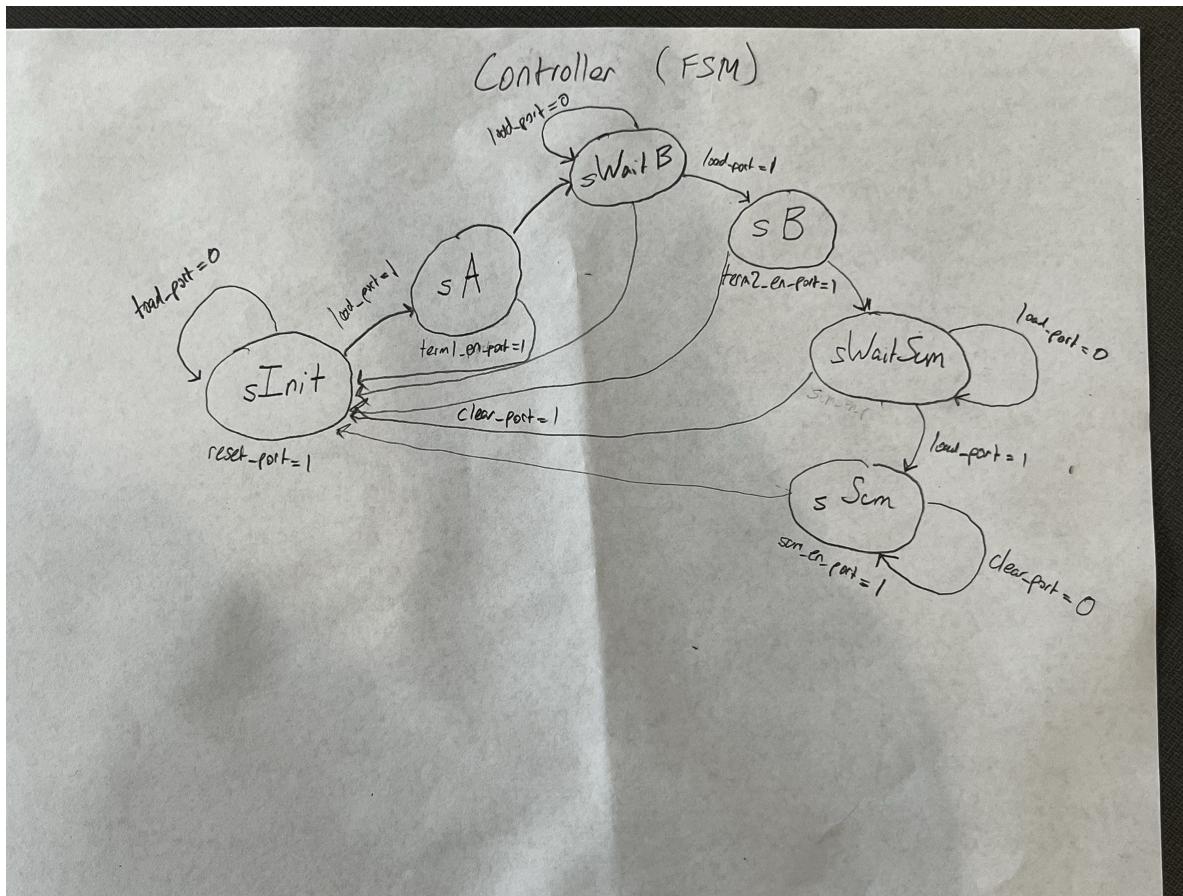


Figure 3: Finite State Machine for the Controller

Deliverable 4: Clock Divider

$$TC := 50$$

Deliverable 5: Controller Test Bench

0.0.1 Planned Tests

1. Normal Operation
2. Clear on sB state (premature clear)
3. Hold Clear and try to load number

0.0.2 Testbench Code

See VHDL file attached separately...

0.0.3 Annotated Testbench Waveform

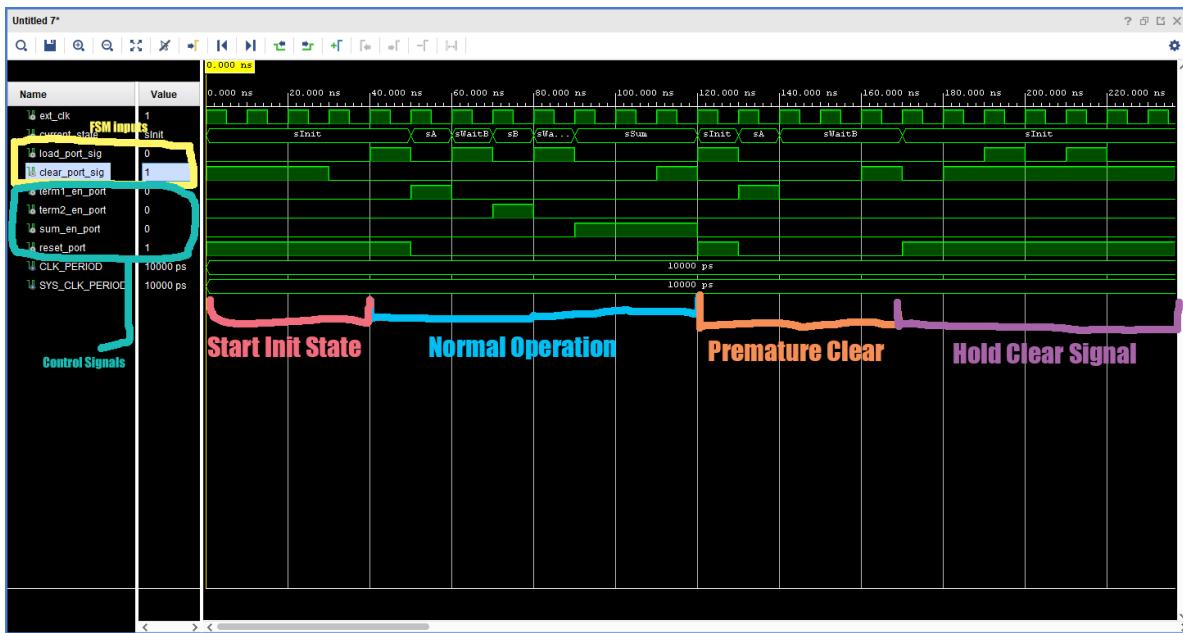


Figure 4: Annotated Controller Testbench Waveform, Annotated (Note How Control Signals Follow the FSM)

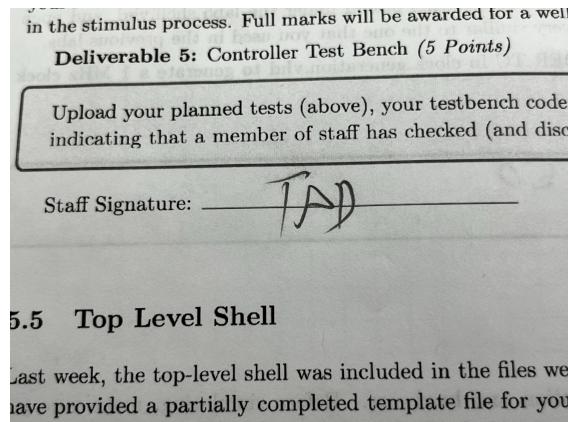


Figure 5: Staff Signature for Controller Test Bench

Deliverable 6: Elaborated Schematic

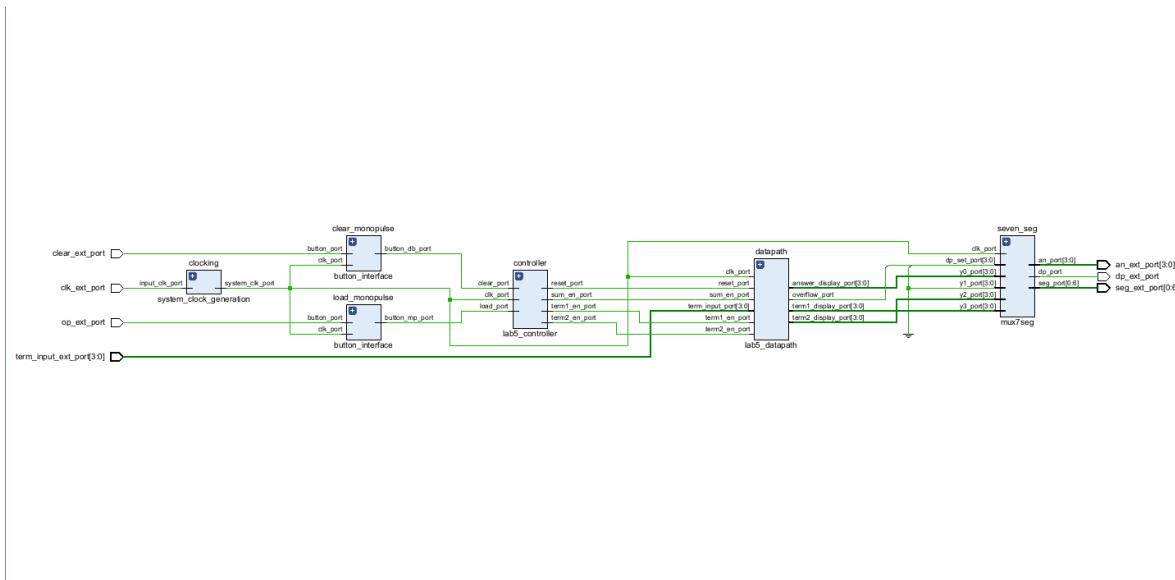


Figure 6: Full RTL Schematic

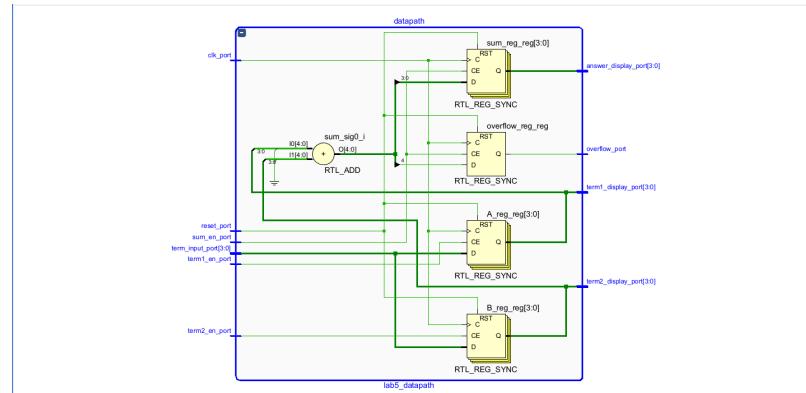


Figure 7: Datapath RTL Schematic

Deliverable 7: Top Level Testbench

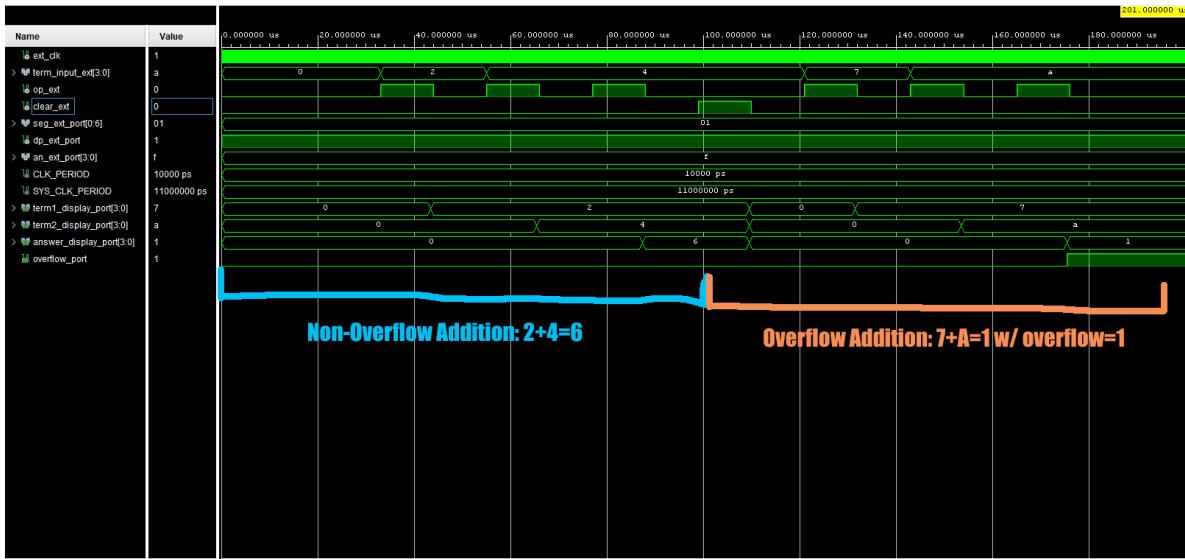


Figure 8: Top Level Simulation Waveform, Annotated

Deliverable 8: Program Your FPGA

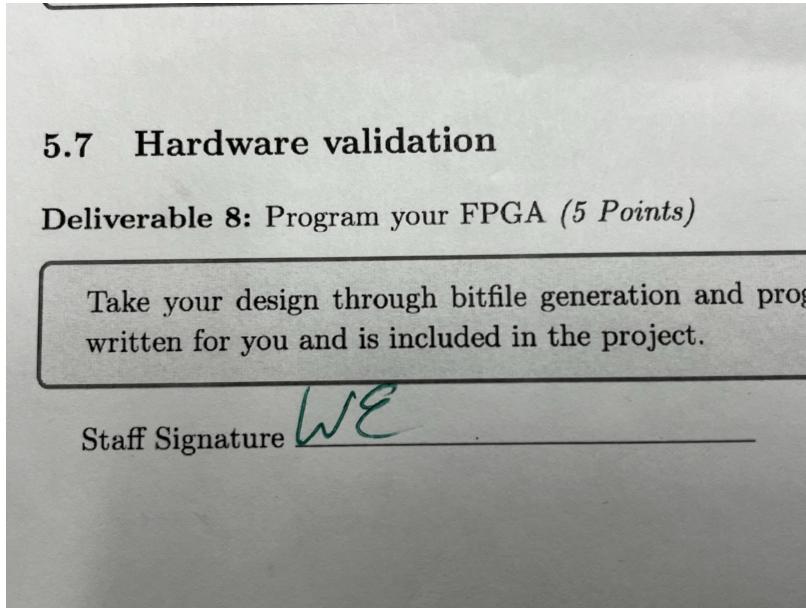


Figure 9: Staff Signature for Hardware

Deliverable 9: Reflections

For me, the most difficult steps of the process were designing the FSM and writing the timing logic for the testbenches.

For the FSM, I initially didn't include the waiting states between loading the numbers and displaying the sums which would not have been per spec. However, this ended up being a quick fix because I just had to add those intermediate

states. Another bug that I discovered was that I used the output pin, reset_signal, interchangeably with the input port, clear_port, since they had similar names. This slight error led to difficult to find errors in the elaboration step. The most difficult step was writing the testbench for the controller. Initially, I was not monopolising the button inputs which led to unexpected behavior with the FSM states. Once realizing this however, I had to make sure to sync these button presses with the clock period. Once writing the testbench for the full design, I also had to take in account the slower clock pulse from the clock divider, which in turn, complicated the timing.