

HOMEWORK 1

1. (a) BIN: 10101101
HEX: 0xAD
BCD: 0001 0111 0011

- (b) BIN: 0111111
HEX: 0x7F
BCD: 0001 0010 0111

- (c) BIN: 01000100
HEX: 0x44
BCD: 0110 1000

2. (a) HEX: 0x69
DEC: 105
BCD: 69

- (b) HEX: 0x48
DEC: 72
BCD: 48

- (c) HEX: 0x5E
DEC: 94
BCD: N/A

3. (a)

$$A = W'X'Y' + W'X'Y + W'XY' + WX'Y' + WX'Y + WXY'$$

$$B = W'X'Y + W'XY + WX'Y + WXY'$$

$$C = W'XY' + W'XY + WX'Y' + WX'Y$$

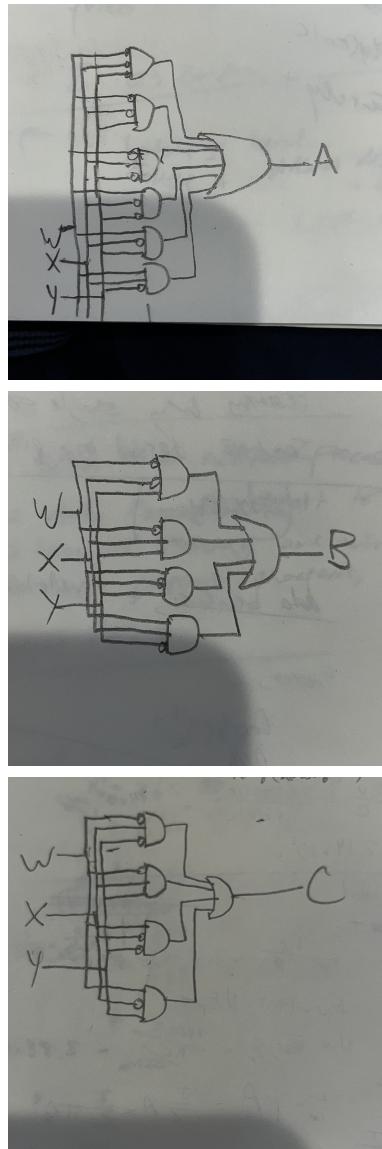


Figure 1: Unimplified Logic Circuits

(b)

$$\begin{aligned} A &= W'X'Y' + W'X'Y + W'XY' + WX'Y' + WX'Y + WXY' \\ &= (X'Y' + X'Y + XY')(W + W') \\ &= X'(Y' + Y) + XY' \\ &= X' + Y' \end{aligned}$$

$$\begin{aligned}
 B &= W'X'Y + W'XY + WX'Y + WXY' \\
 &= Y(W'X' + W'X + WX') + WXY' \\
 &= Y(W' + X') + WXY' \\
 &= W'Y + X'Y + WXY'
 \end{aligned}$$

$$\begin{aligned}
 C &= W'XY' + W'XY + WX'Y' + WX'Y \\
 &= W'(XY' + XY) + W(X'Y' + X'Y) \\
 &= W'X + WX'
 \end{aligned}$$

(c)

$$C = W \oplus X$$

4. .

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Figure 2: Truth Table

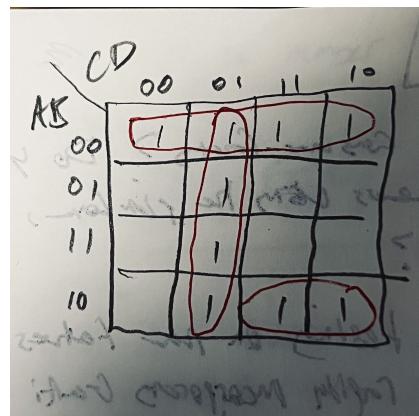


Figure 3: Karnaugh Map

Simplified logic equation:

$$X = A'B' + C'D + AB'C$$

Number of transistors:

- Before: 30 gates, 150 transistors (AND: 9x12; OR: 1x20; NOT: 20x2)
- After: 8 gates, 36 transistors (AND: 2x6+1x8; OR: 1x8; NOT: 4x2)